EXAR
...the analog plus company^{TM}

May 1996-4

EVALUATION KIT PARTS LIST

This kit contains the following:

- XRD6415AB Application Board (48 QFP or 28 SOIC)
- XRD6415 5V ADC or XRD64L15 3V ADC
- XRD6415AB Application Note
- XRD6415 or XRD64L15 Data Sheet

FEATURES

- Easy Evaluation of XRD6415, XRD64L15
- True 10-Bit Accurate Circuit & Board Layout
- Optimized Support Circuits
- User Friendly / Flexible Interface

INTRODUCTION

The XRD6415AB is a complete printed circuit test board designed to permit quick and accurate evaluation of EXAR's XRD6415 & XRD64L15, 10-bit 20 MSPS analog-to-digital converters.

This application board combines a proven PC Board layout with optimized analog and digital interface circuitry to satisfy the stringent requirements needed in evaluating high performance devices of this type.

The board contains the device being tested (XRD6415), operational amplifiers for input buffers, latches, numerous connectors, jumper options, and observation test points in commonly used locations.

Complete DC and AC performance of the part can be evaluated by interfacing external laboratory equipment to the flexible user interface.

PREVIEW OF COMMON TEST CONFIGURATIONS

The board is set up as a general A/D test circuit. *Figure 1.* shows this default test circuit. Circuit timing is demonstrated in *Figure 6.* There are many other circuit possibilities built into the universal test board, however, starting with the default circuit is recommended.

In addition to the default test circuit, two other test configurations are discussed: the cross plot test and the external reconstruction DAC test.

Options for analyzing the output results are discussed in detail below. The most effective of these is the use of a high speed data acquisition system and FFT software to compute the performance parameters.
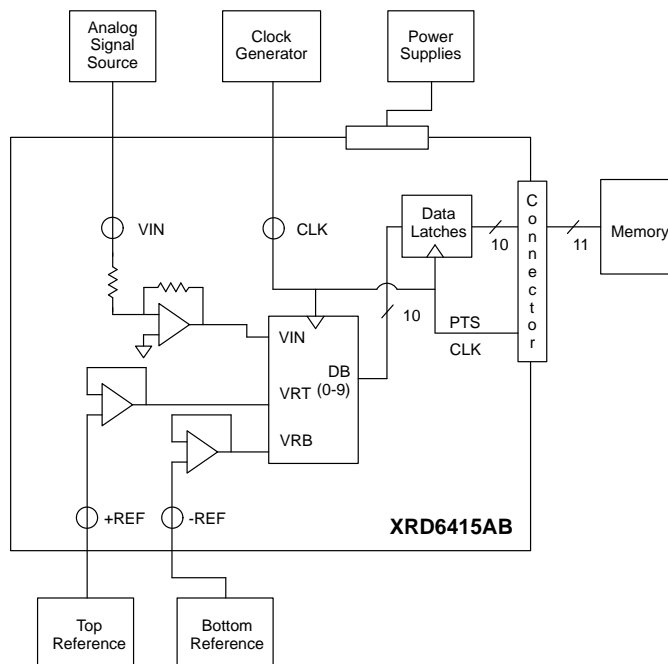

Figure 1. Default A/D Test Circuit

PCB CONSTRUCTION & LAYOUT

The XRD6415AB printed circuit board is a four layer board with two internal layers dedicated to power and ground. Top and bottom layers are used for the routing of circuitry. The internal power planes have a 5 mil separation that use the inherent board capacitance to aid power supply bypassing. The board's finished thickness is 100 mils. *Figures 12 through 23* at the back of this application note show each layer of the board.

SYSTEM CONFIGURATION - LAB SETUP

The evaluation block diagrams of the XRD6415AB with typical external test equipment are shown in *Figure 1., Figure 4.*, and *Figure 10.* The following is a more detailed description of the major on-board and external components used in these systems.

Application Board Circuitry

The application board support circuitry for the 48 pin QFP package is shown in *Figure 2. Figure 3.* is the circuitry for the 28 pin SOIC package.

The major components supporting the A/D under test are:

1. VREF BUFFERS - Op amps, U3 & U2, (AD843) can be used to isolate the externally supplied VRT and VRB from the device under test and provides a low source impedance. These buffers can be bypassed with onboard jumpers (JP1 and JP2). Holes for optional compensation and gain are provided.

2. ANALOG INPUT AMPLIFIER - An operational amplifier, U1, (AD847) is used to provide a low source impedance to the A/D. Provisions are made for summing a dither signal and/or offset voltage with the input. On-board jumper JP13 allows the referencing of analog input signals to the VRB reference voltage. Note that JP13 or JP9 must be in for the op amp to establish a pseudo-ground.

3. DATA LATCHES - The digital output of the A/D drive on-board latches U4 & U5 (74HC174) which buffer the device under test from the external test equipment.

4. RECONSTRUCTION DAC - A simple resistor implementation of a reconstruction DAC allows for a cross plot test at the test point labeled XPLOT. An analog waveform is generated from the four LSBs taken at the outputs of the data latches. See the Cross Plot Test section.

5. CLOCK DIVIDE CIRCUIT - The U6A (74HC74) latch divides the CLK frequency in half to synchronize slower external lab equipment. The XRD6415 still functions at the CLK frequency independent of the clock divide circuit output at the PTS CLK pin. Either half of the output data from the XRD6415 is discarded when using the clock divide circuit output or the output data can ping-pong between two different memories. The PTS CLK pin frequency is selected using JP4.

6. DIGITAL & ANALOG WORK AREAS - 100 mil spaced holes allow configuration of additional circuitry powered from either analog or digital planes.

External Equipment Required

The system block diagrams (*Figure 1., Figure 4.*, and *Figure 10.*) show the external test equipment required to perform all test and evaluation functions. These include:

1. POWER SUPPLIES - $\pm$15V and several +5V or +3V external power supplies are needed. Three separate ground planes are provided on the board. The AGND plane contains the XRD6415 GND pins. A separate plane, DUTGND, is connected to the DGND pin. The third plane labeled DGND is dedicated to grounding the logic components on the board. Decoupling circuits are provided on the application board, however, low noise, low output impedance supplies are necessary for best performance. A 100 mil spaced connector is provided for all power connections. Connect all grounds together at the power connector. For best results, twist the power supply cable pairs. This minimizes coupling to and from unrelated sections of the setup.

2. CLOCK GENERATOR - A clock signal is applied to the SMB connector labeled CLK. Select a low jitter clock with a 50% duty cycle for best spectral results. Note there is a 50 Ω termination resistor on the board for the CLK input.
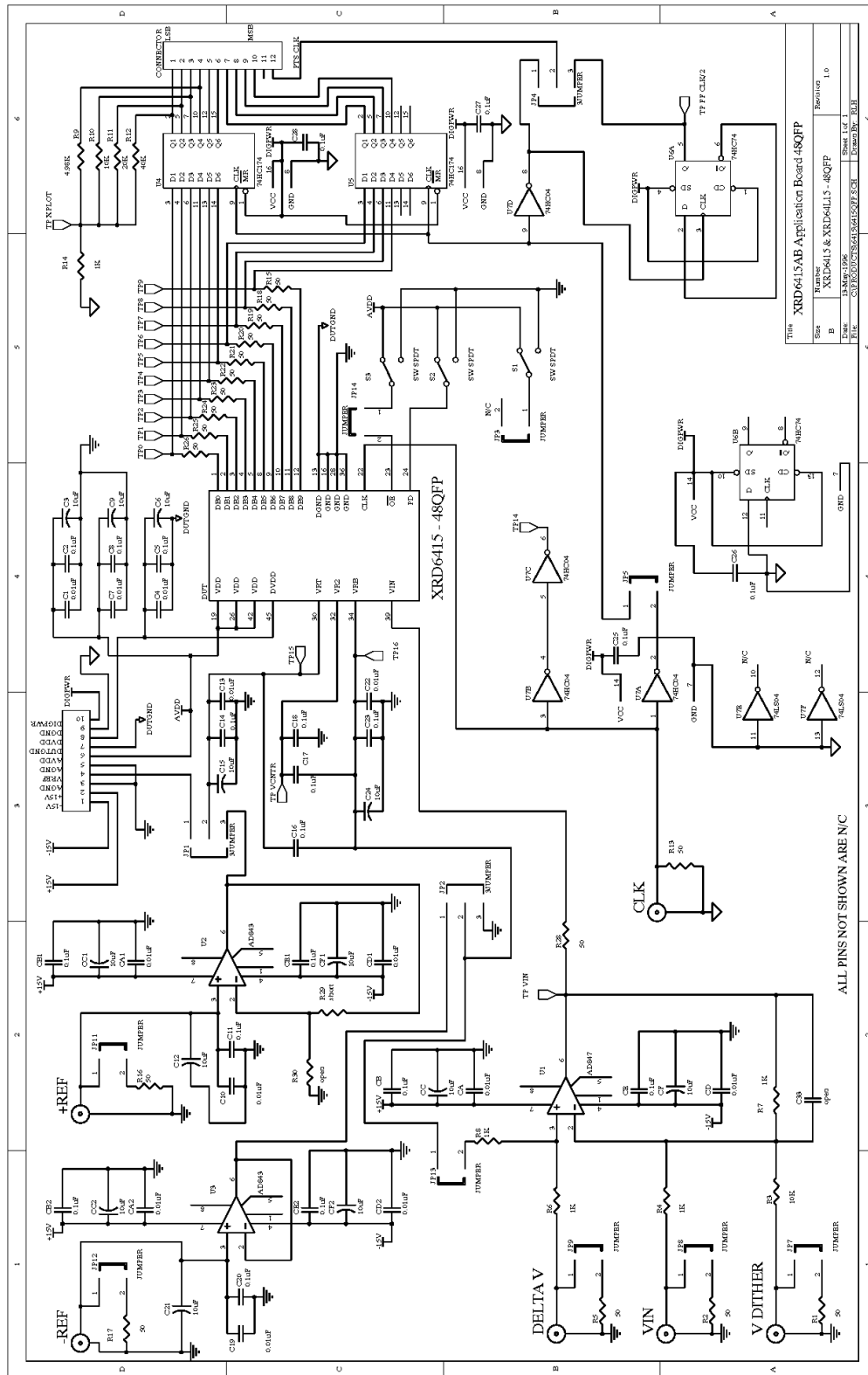
Figure 2. XRD6415AB 48 Pin QFP Schematic

Figure 3. XRD6415AB 28 Pin SOIC Schematic

3. REFERENCE SUPPLIES - A positive and negative reference voltage is connected through the SMB coax connectors labeled +REF and -REF (typically +5 and 0V respectively). The external reference voltages can be configured to go through the op amp buffers or go directly to the A/D from the power connection labeled VREF. Using JP1, the positive reference can be shorted to VREF at the power connector. Using JP2, the negative reference can be shorted to AGND. Note that +REF must be more positive than -REF, since the positive reference voltage must be greater than the negative reference voltage on-chip. Best results are achieved by using low noise voltage references as opposed to standard power supplies.

4. INPUT SIGNAL GENERATOR - A clean, low distortion sine wave generator is used as a signal source. A band pass or low pass filter is sometimes required to further reduce harmonics and band limit noise. The SMB coax connector labeled VIN accepts the analog input. An op amp U1 (AD847) is used to amplify this input and provide low source impedance to drive the A/D under test. U1 is used for single ended inputs or applying a DC offset for level shifting. The socket has a standard 741 type pin out which allows experimentation with alternative amplifiers.

5. DITHER INPUT SIGNAL GENERATOR - The cross plot test configuration (described later) requires a low noise triangle wave signal source. This signal is added through the SMB connector labeled V DITHER (an inverting input with a gain of 1/10).

6. OSCILLOSCOPE - The output of a reconstruction DAC, test point XPLOT, is used to drive the vertical input of the oscilloscope for manual linearity testing using the "cross plot" method. The reconstruction DAC is simply a 5 resistor implementation.

Optional Equipment

1. EXTERNAL PRECISION OUTPUT DAC - As an alternative to DSP, a high speed precision digital-to-analog converter can reconstruct the output in analog form. Analog measurements can be used to evaluate the A/D's performance using conventional analog instrumentation as shown in *Figure 4.*

2. DSP - Evaluation of dynamic and static performance is done by external processing devices that perform histogram and harmonic analysis to determine characteristics such as linearity, noise, harmonic distortion, intermodulation distortion, etc. The data is available at the 24 pin data connector. Each output pin is complemented by a ground pin. The external clock output is available on a pin labelled PTS CLK.
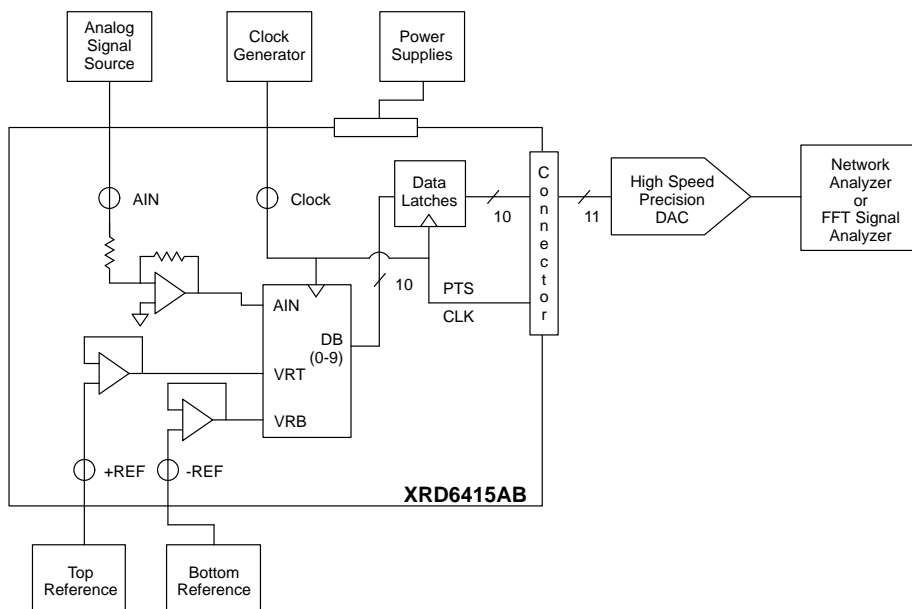

Figure 4. External Precision DAC Reconstruction Test

SYSTEM OPERATION

Reference Inputs

With the reference op amps in circuit, the ADC's reference pins (VRB and VRT) are driven in an offset and range mode:

$$VRB = (-REF), VRT = (+REF)$$

Hence -REF defines the offset and +REF defines the span.

DNL and INL performance is optimized when the VRB input of the XRD6415 is buffered. If VRB is connected to the PCB ground plane it is subject to the noise and ground bounce in that plane. For example VRB could be buffered by U3 to 50mV above ground and still have a wide reference voltage range set by connecting VRT to a voltage near VDD.

VIN Input

Either JP9 or JP13 must be connected for the op amp U1 to establish a pseudo ground. The input to the ADC (VIN) is determined by the circuit in *Figure 5.* If JP13 is connected, the pseudo ground of U1 tracks VRB of the XRD6415. R28 decouples the output of U1 from the switching input capacitance of the XRD6415.
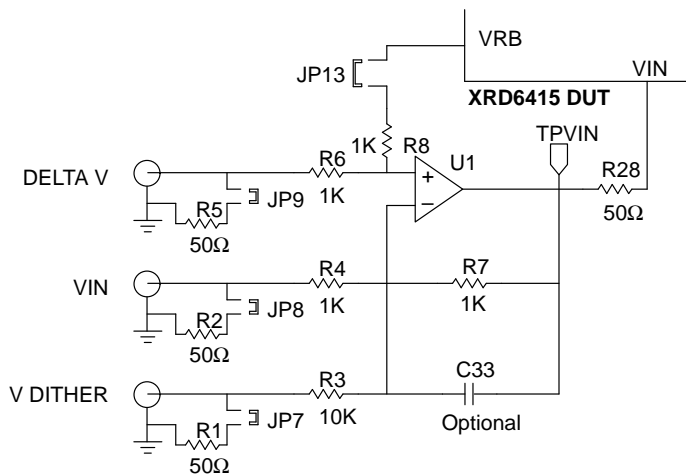

Figure 5. VIN Circuit

Timing

Figure 6. demonstrates the circuit timing of the XRD6415AB. The CLK is provided by the user as specified on the XRD6415 data sheet. The PTS CLK is an output that allows for synchronization of external lab equipment with the output data DB(0-9). DB(0-9) are valid after the rising edge of the PTS CLK.

The DC performance of the XRD6415 is optimized with rise and fall times of CLK edges limited to greater than or equal to 10ns. A resistor in series with the CLK input pin can combine with parasitic capacitance to limit rise and fall times. This is evident in both the cross plot and DNL tests. DC performance is not significantly degraded for duty cycles up to either 60% or 40%.
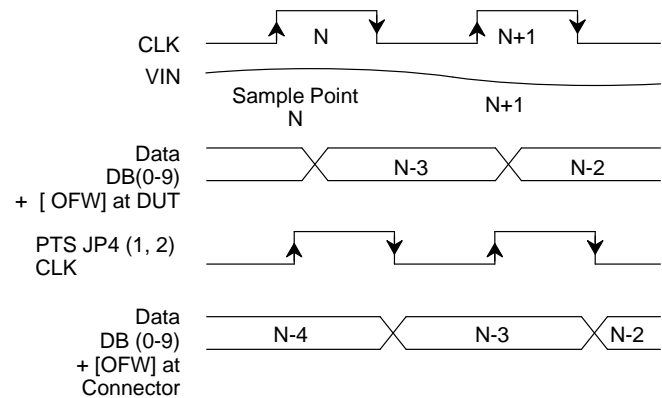

Figure 6. XRD6415AB Circuit Timing

XRD64L15AB 3.3V Operation

The XRD64L15 can be evaluated by simply lowering AVDD and DVDD to 3.3V. Note that the voltage at VRT, VRB and VIN must remain within the supply range of the XRD64L15. DIGPWR provides a separate supply voltage to the digital logic ICs (U4, U5, U6, U7) on the XRD6415AB board. Typically, the digital logic thresholds will work with the XRD64L15 operating at 3.3V when DIGPWR is lowered to 4.5V. If the output is intermittent, either adjust the DIGPWR supply voltage or use 3.3V logic. If 3.3V logic is used, swap out the digital logic ICs and lower DIGPWR to 3.3V.

XRD6415 5V with 3.3V Logic Output Interface

The DVDD pin of the XRD6415 is a separate power supply dedicated to the logic output drivers. DVDD is not connected internally with any of the other power supplies. This allows the XRD6415 to output 3.3V logic levels when DVDD is driven to 3.3V independent of the voltage at the other VDD pins. The XRD6415AB has a separate connector for the DVDD supply to test this function. Logic thresholds of the digital logic ICs (U4, U5, U6, U7) typically match when DIGPWR is lowered to 4.5V. *Figure 7.* illustrates the power supply circuity of the XRD6415.
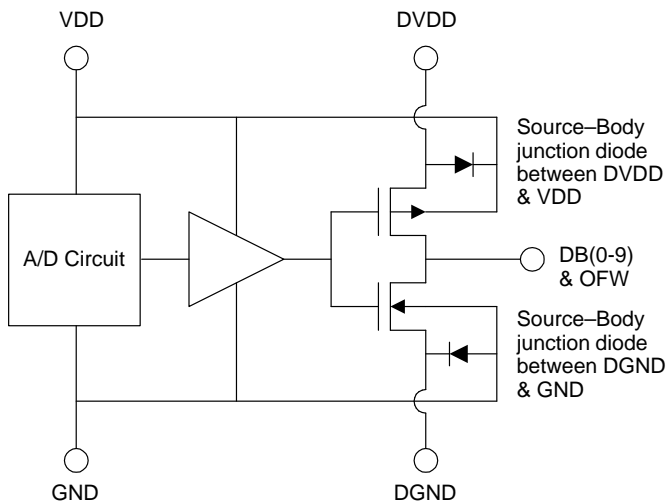
**Figure 7. XRD6415 ADC Power Supply
Circuit Allows Separate VDD & DVDD
and Separate GND & DGND**

Digital Inputs

The input logic thresholds of the XRD6415 ($\overline{OE}$, PD &
CLK) are set by the voltage at the VDD pins.

Digital Outputs

The digital output drive circuitry of the XRD6415 and
XRD64L15 was designed to operate separately from the
analog supplies. DVDD and DGND connect directly to the
digital logic power of the system isolating the analog and
digital power supplies and grounds. DGND is not
common to the XRD6415 substrate as shown in *Figure 7*.
The XRD6415 substrate is common only to the packages'
GND pins. The XRD6415AB has three separate ground
connections at the power header to allow
experimentation.

Use 50 or 100 Ω resistors to isolate the XRD6415 digital
output pins from a latch or bus connection. If the layout
requires a digital bus trace greater than 3 inches use a
latch or digital buffers as shown with U4 & U5 in the
schematic. This protects the output drivers and reduces
the effects of high speed switching logic signals from
degrading the ADC performance. Layout the latch or
digital buffers as close to the ADC as possible.

DIGITAL SIGNAL PROCESSING

A comprehensive dynamic performance evaluation is
most often done by using external hardware capable of
fast data acquisition and storage. The computation of
integral linearity, differential linearity, signal-to-noise and
distortion ratios, the effective number of bits, and other
useful figures of merit is performed using software having
histogram and FFT capability. The accuracy of the test
results depends upon the quality of the input sinewave. A
low distortion sinewave generator with a band pass or low
pass filter will be necessary.

The Tektronix PTS101 and other internally developed
proprietary systems are used by EXAR to acquire and
analyze the ADC data. The DNL graph in *Figure 8.* and
the INL graph in *Figure 9.* are examples of these
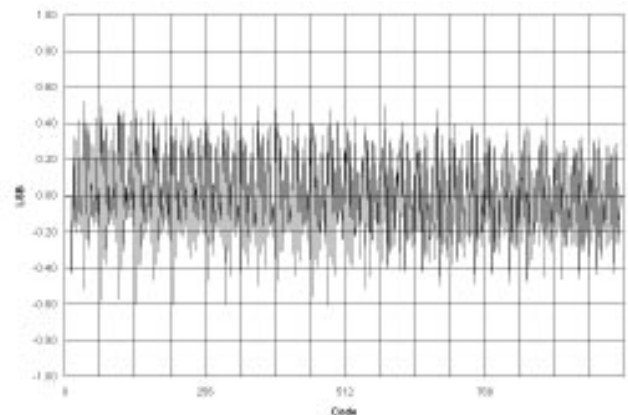techniques using the XRD6415AB.

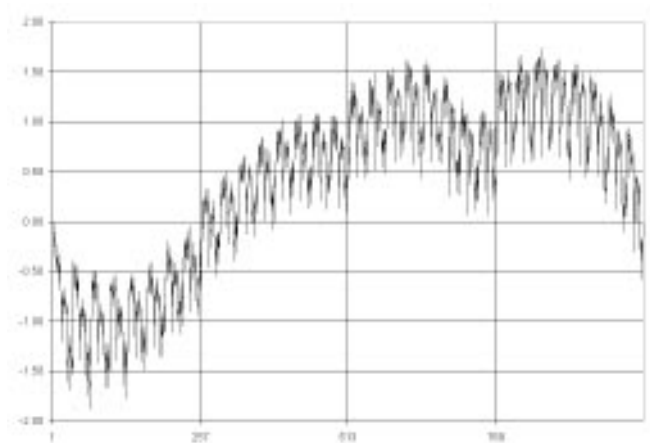**Figure 8. XRD64L15 DNL @ 15 MSPS,
VDD = 3V, VRT=2.5V, VRB = 0.5V**

**Figure 9. XRD64L15 INL @ 15 MSPS,
VRT – VRB = 2.5V, VDD = 3V**

ANALOG TESTING WITH EXTERNAL DAC

The logic output of the system can be converted back to analog by using a high performance digital-to-analog converter. Laboratory spectrum analyzers and oscilloscopes can be used to measure linearity, frequency response, harmonic distortion, noise, intermodulation distortion, etc. These measurements can be converted to the specifications commonly used in specifying A/D's dynamically. In addition to a high quality sinewave input, the output digital-to-analog converter must be significantly more accurate than the A/D under test.

Note that measurements taken with this method demonstrate the combined errors of all the circuitry involved.

CROSS PLOT

An evaluation of differential linearity can be simply done with an oscilloscope, a triangle wave or sinusoid generator and a low noise DC signal source. Input SMBs are provided on the board so this "cross plot" method can be conveniently implemented (See *Figure 10.*) The oscilloscope must be set in the X-Y display mode.

A triangle wave (500 Hz) with a peak-to-peak amplitude of approximately 100 LSBs is supplied to the "DITHER" input. This is attenuated by a factor of R7/R3 by the input amplifier. The triangle wave is also used to drive the x axis of the scope. The horizontal gain is set so that 16 divisions are swept. Look at Test Point (XPLOT) with the vertical input. Set the horizontal gain at about 2 LSB per division.
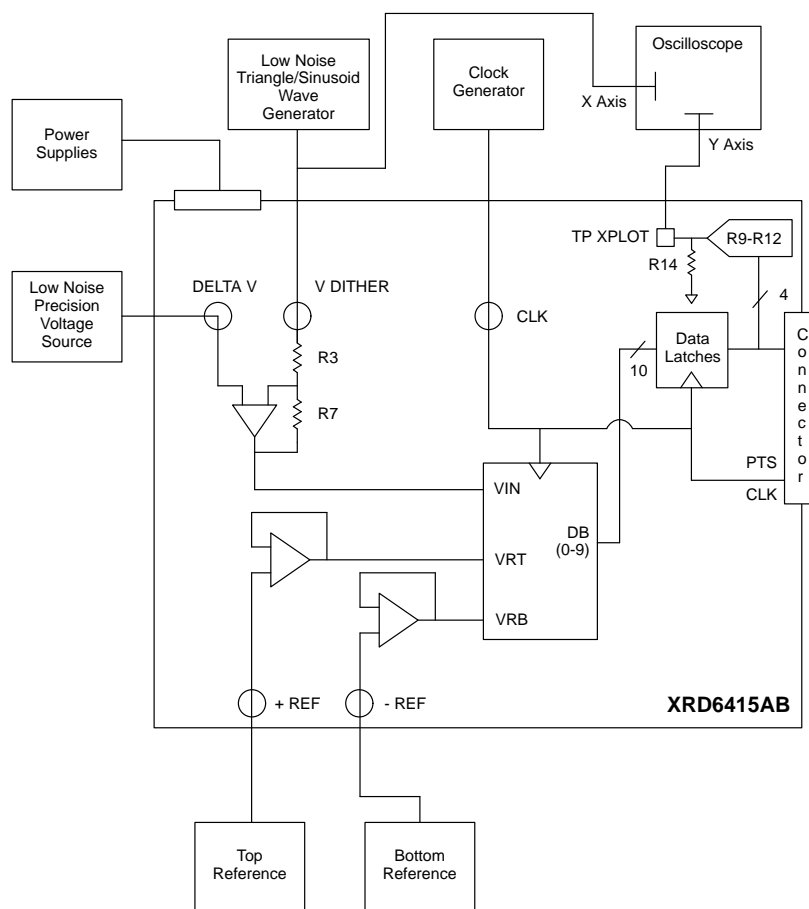

Figure 10. Crossplot Setup

A stair step waveform will result (See *Figure 11.*) By changing the DC input at DELTA V, sixteen code transitions can be observed about any DC input level. The horizontal distance between these transitions is the code width. Missing codes cause steps to be absent. By setting the end point thresholds to coincide with the scope grid lines, integral linearity errors are displayed as thresholds which are off-centered from these grid lines. A precision DC voltage source is necessary for the integral linearity measurement.

Since the conversion speed is much faster than the dither frequency, multiple readings are taken at each threshold. The horizontal variation of each threshold gives a qualitative measure of noise (in LSBs).

Using this "cross plot" method is a good way to prove out the lab setup prior to more sophisticated DSP test.
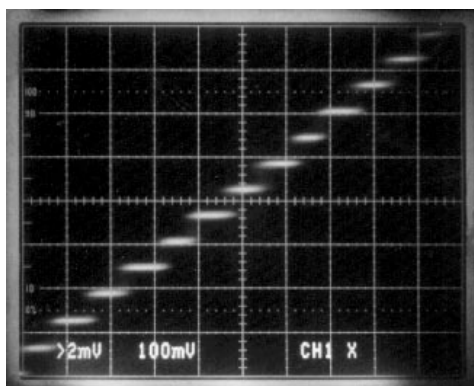

Figure 11. Crossplot Staircase Output
CLK = (15 MSPS, t_{rf} = 15 ns), VIN = 3V,
VREF = 2V

JUMPER OPTIONS

The XRD6415AB offers flexibility through configuration determining jumpers and switches. These options furnish choices for (1) input termination resistors, (2) bypassing of the reference input buffers, and (3) the selection of several logic and clock options. *Table 1.* shows the jumper functions along with the default configuration set-up prior to shipment. *Table 2.* plots the test points available. *Table 3.* demonstrates the switch functions.

Termination of Input Coax Cables		
Jumper	**Description**	**Default**
JP8	Connecting adds 50 Ω from VIN to AGND	IN
JP7	Connecting adds 50 Ω from V DITHER to AGND	OUT
JP9	Connecting adds 50Ω from DELTA V to AGND	IN
JP11	Connecting adds 50 Ω from +REF to AGND	OUT
JP12	Connecting adds 50 Ω from -REF to AGND	OUT
Reference Amplifier/Buffer Bypass (1)		
JP1 (1, 2)	Connecting shorts VREF in Power Connector to VRT pin of ADC	OUT
JP1 (2, 3)	Connecting Shorts Output of U2 to VRT Pin of ADC	IN
JP2 (2, 3)	Connecting shorts AGND to VRB pin of ADC	OUT
JP2 (1, 2)	Connecting Shorts Output of U3 to VRB Pin of ADC	IN
JP13	Connecting Biases U1 Relative to VRB Pin of ADC	OUT
Logic and Clock Jumpers (1)		
JP5	Connects CLK to U4, U5, and PTS CLK Output	IN
JP3	Connects S1 to N/C Pin on ADC, Always Leave Out	OUT
JP14	Connects S3 to $\overline{OE}$ of ADC	IN
JP4 (1, 2)	Connects CLK to PTS CLK	IN
JP4 (2, 3)	Connects CLK/2 to PTS CLK	OUT

Notes:
1. *Jx (a, b) means short pin a and pin b of jumper x.*

Table 1. Jumper Options

Test Point	Description
TP0-10	DB0-9 and OFW of ADC
TP14	CLK Output of U7C
TP15	VRT of ADC
TP16	VRB of ADC
TP VCNTR	VR2 of ADC
TP FF CLK/2	Output of CLK Divide Circuit
TP VIN	VIN of ADC
TP XPLOT	Crossplot Output

Table 2. Test Points

XRD6415AB

Switch		Function
S1	HI	AVDD to JP3
	Lo	AGND to JP3
S2	HI	AVDD to PD of ADC
	Lo	AGND to PD of ADC
S3	HI	AVDD to JP14 ($\overline{OE}$ of ADC)
	Lo	AGND to JP14 ($\overline{OE}$ of ADC)

Table 3. Switches

FINAL DESIGN CONSIDERATIONS

After the XRD6415AB has been used to demonstrate that the XRD6415, the clock timing, and the analog support circuits are acceptable, the design must be successfully transferred to the user's system. A close copy of the proven layout is recommended as is the use of identical support devices.

1. Be generous with analog and digital ground planes. Mirror the ground plane with the supply planes. Use a 5 mil power / ground plane separation if a four layer board can be used. The XRD6415 substrate is common to the packages' GND pins only. DGND and DVDD are separate supplies dedicated to the output logic drivers of the XRD6415. Connect DGND and DVDD to the power planes of the system's digital logic.

2. Keep high frequency decoupling capacitors very close to the A/D pins and minimize the loop area included so less flux will induce less noise. Use decoupling capacitors in the same locations as on the XRD6415AB.

3. Coupling between logic signals and analog circuitry can easily change a 10-bit system into an 8-bit system or worse. Completely separate them. Watch for coupling opportunities from other sources not im-

mediately associated with the A/D. Don't use switching power supplies in adjacent locations, for example.

4. The DC performance of the XRD6415 is optimized with rise and fall times of CLK edges limited to greater than or equal to 10ns. A resistor in series with the CLK input pin can combine with parasitic capacitance to limit rise and fall times. Select a low jitter clock with a 50% duty cycle for best spectral results.

5. Use support devices equivalent to those used on the evaluation board. Use the application board to verify these devices up front, i.e. use very linear passive components in the signal path.

6. Select a driving op amp whose noise, speed, and linearity fits the application. Use a resistor to decouple the output of the driving op amp from the switching input capacitance of the XRD6415.

7. DNL and INL performance is optimized when the VRB input of the XRD6415 is buffered. If VRB is connected to the PCB ground plane it is subject to the noise and ground bounce in that plane. For example VRB could be buffered by U3 to 50mV above ground and still have a wide reference voltage range set by connecting VRT to a voltage near VDD.

8. Use 50 or 100 Ω resistors to isolate the XRD6415 digital output pins from a latch or bus connection. This protects the output drivers and reduces the effects of high speed switching logic signals from degrading the ADC performance. Layout the latch or digital buffers as close to the ADC as possible to minimize trace length.

PCB LAYOUT

A set of drawings showing the details of the electrical circuit and board layout for both the 48 QFP and 28 Pin SOIC package options are shown in *Figures 12 through 23*.

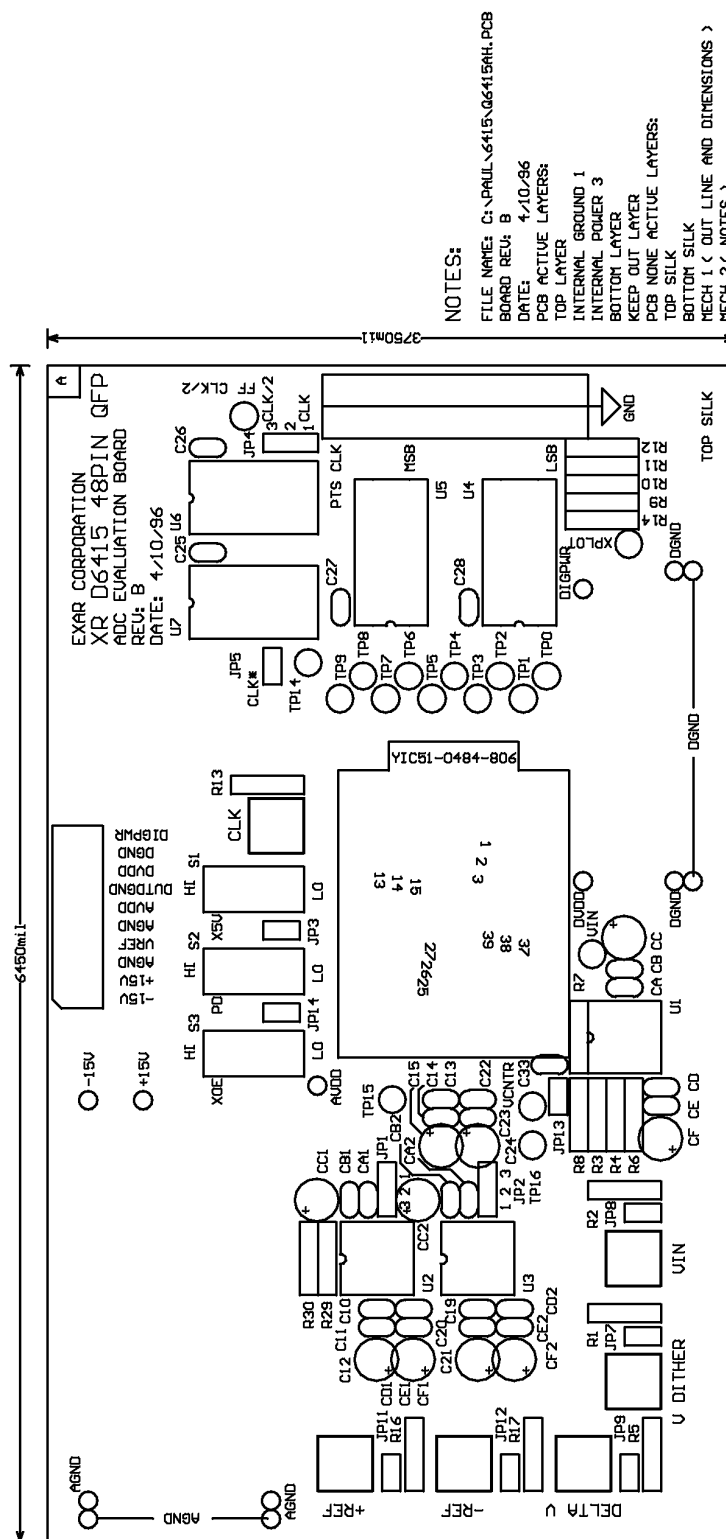| Qty	Value	Ref Designators
18	Test Point	TP0-9, TP10 (SOIC only), TP14, TP15, TP16, TP FF CLK/2, TP VCNTR, TP VIN, TP XPLOT
14	0.01µF	C1, C4, C7, C10, C13, C19, C22, C30 (SOIC only), CA, CA1, CA2, CD, CD1, CD2
21	0.1µF	C2, C5, C8, C11, C14, C16, C17, C18, C20, C23, C25, C26, C27, C28, C31 (SOIC only), CB, CB1, CB2, CE, CE1, CE2
14	10µF	C3, C6, C9, C12, C15, C21, C24, C32 (SOIC only), CC, CC1, CC2, CF, CF1, CF2
5	1KΩ	R4, R6, R7, R8, R14
1	4.98KΩ	R9
2	10KΩ	R3, R10
1	20KΩ	R11
1	40KΩ	R12
18	50Ω	R1, R2, R5, R13, R15, R16, R17, R18, R19, R20, R21, R22, R23, R24, R25, R26, R27 (SOIC only), R28
1	74HC04	U7
1	74HC74	U6
2	74HC174	U4, U5
2	AD843	U2, U3
1	AD847	U1
3	3JUMPER	JP1, JP2, JP4
9	JUMPER	JP3, JP5, JP7, JP8, JP9, JP11, JP12, JP13, JP14
3	SW SPDT	S1, S2, S3
1	XRD6415	DUT
1	Short	R29
2	Open	C33, R30
2	Header Connectors	Power, Data
6	SMB	-REF, +REF, DELTA V, VIN, V DITHER, CLK
1	DUT Socket	48 QFP or 28 SOIC
1	PCB	EXAR Corporation XRD6415 28 Pin or 48 QFP

Table 4. List of Components

XRD6415AB

EXAR

Figure 12. Top Silk - 48 QFP

Rev. 1.00

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NOTES:

FILE NAME: C:\PAUL\6415\Q6415AH.PCB
BOARD REV: B
DATE: 4/10/96
PCB ACTIVE LAYERS:
TOP LAYER
INTERNAL GROUND 1
INTERNAL POWER 3
BOTTOM LAYER
KEEP OUT LAYER
PCB NONE ACTIVE LAYERS:
TOP SILK
BOTTOM SILK
MECH 1 (OUT LINE AND DIMENSIONS)
MECH 2 (NOTES)

TOP

3750mil

6450mil
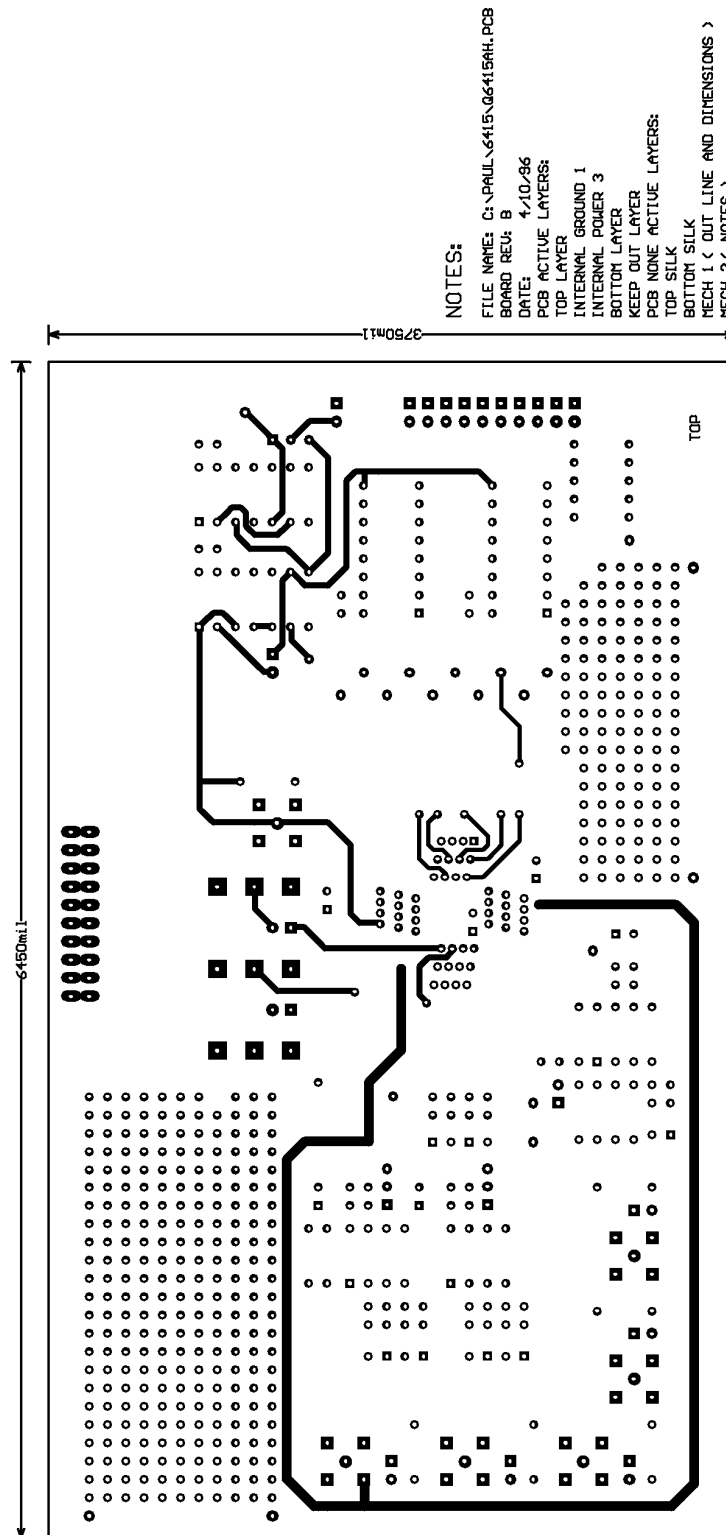
Figure 13. Top Trace - 48 QFP

NOTES:

FILE NAME: C:\PAUL\6415\Q6415AH.PCB
BOARD REV: B
DATE: 4/10/96
PCB ACTIVE LAYERS:
TOP LAYER
INTERNAL GROUND 1
INTERNAL POWER 3
BOTTOM LAYER
KEEP OUT LAYER
PCB NONE ACTIVE LAYERS:
TOP SILK
BOTTOM SILK
MECH 1 (OUT LINE AND DIMENSIONS)
MECH 2 (NOTES)

POWER

3750mil

6450mil
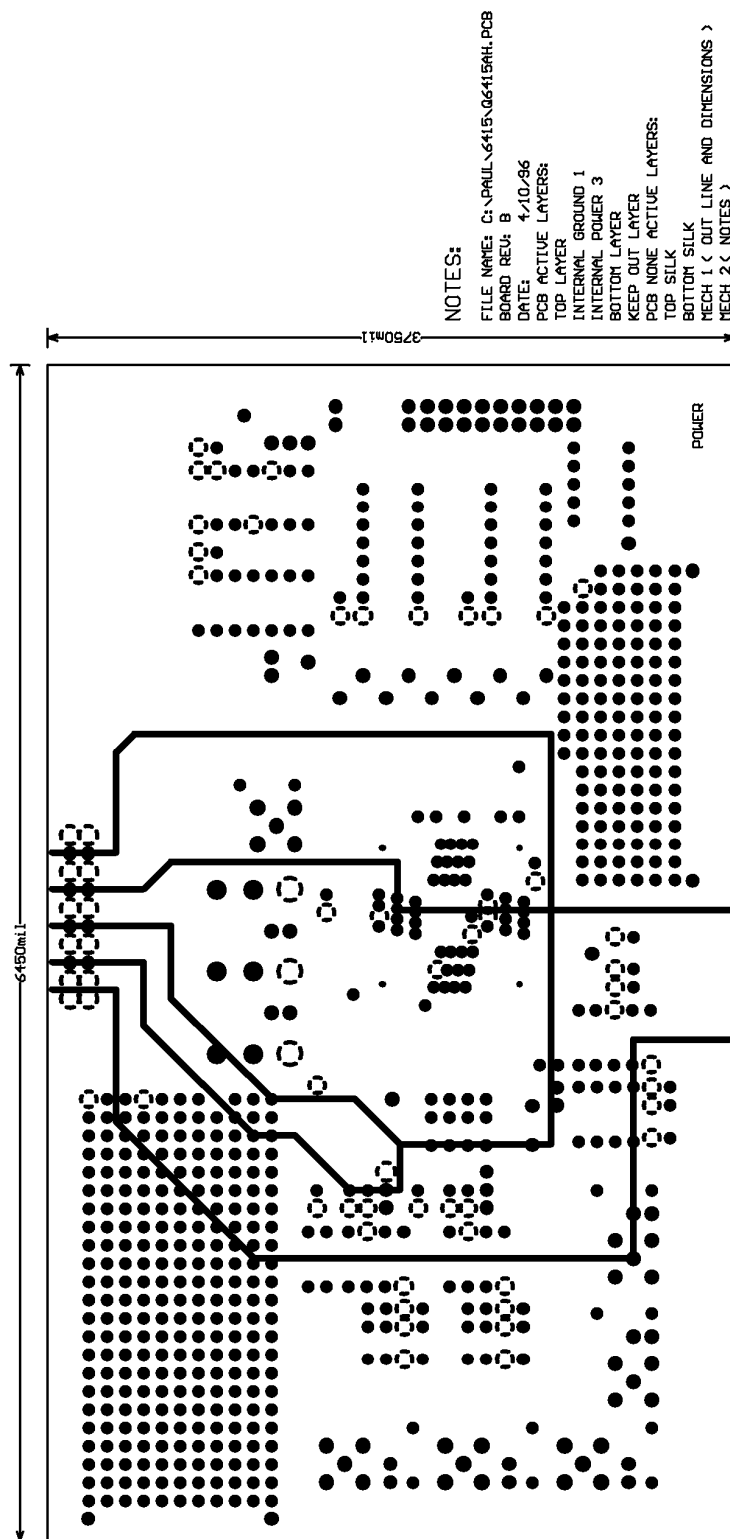
Figure 14. Power Plane - 48 QFP

NOTES:

FILE NAME: C:\PAUL\6415\G6415AH.PCB
BOARD REV: B
DATE: 4/10/96
PCB ACTIVE LAYERS:
TOP LAYER
INTERNAL GROUND 1
INTERNAL POWER 3
BOTTOM LAYER
KEEP OUT LAYER
PCB NONE ACTIVE LAYERS:
TOP SILK
BOTTOM SILK
MECH 1 (OUT LINE AND DIMENSIONS)
MECH 2 (NOTES)
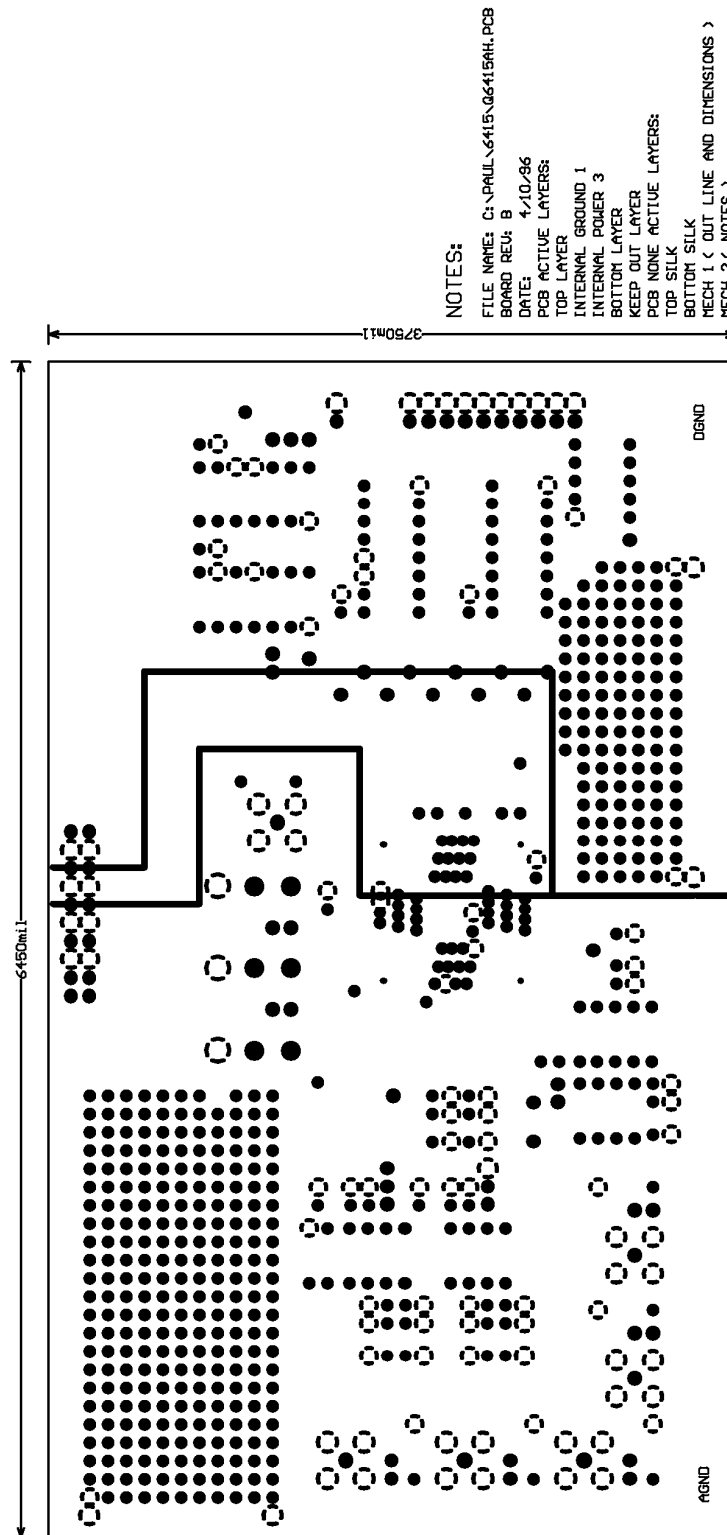
Figure 15. Ground Plane - 48 QFP
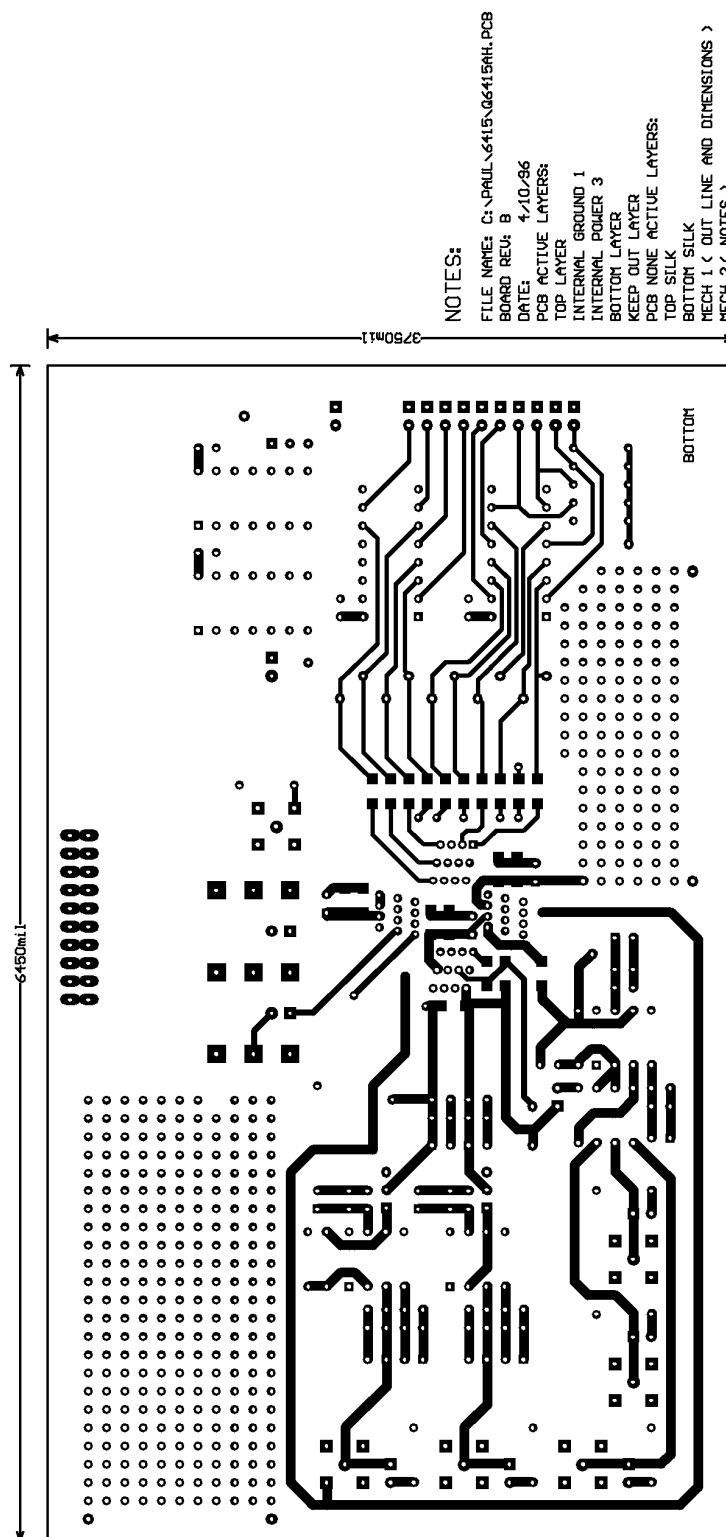
Figure 16. Bottom Trace - 48 QFP
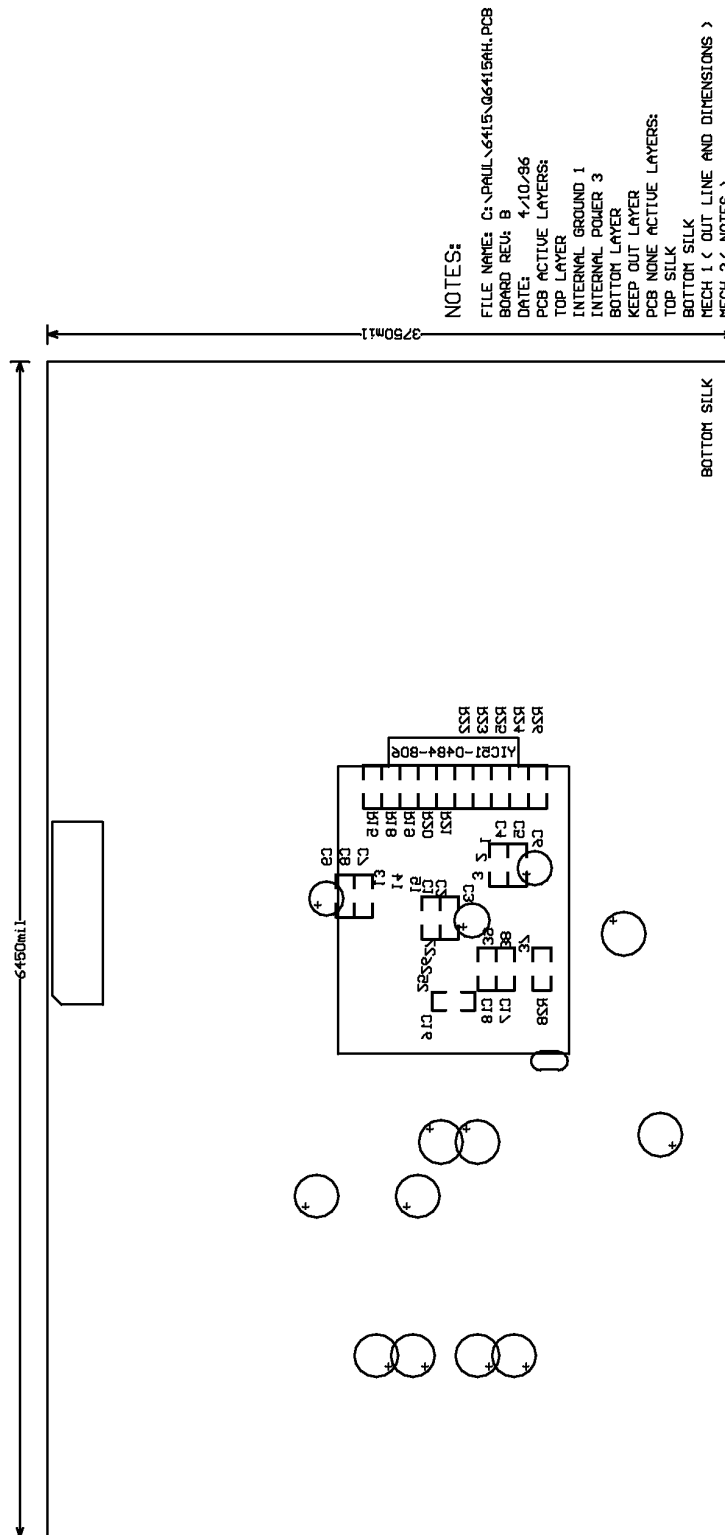
Figure 17. Bottom Silk - 48 QFP

Figure 18. Top Silk - 28 Pin SOIC

NOTES:

FILE NAME: C:\PAUL\6415\S6415SE.PCB
BOARD REV: B
DATE: 4/10/96
PCB ACTIVE LAYERS:
TOP LAYER
INTERNAL GROUND 1
INTERNAL POWER 3
BOTTOM LAYER
KEEP OUT LAYER
PCB NONE ACTIVE LAYERS:
TOP SILK
BOTTOM SILK
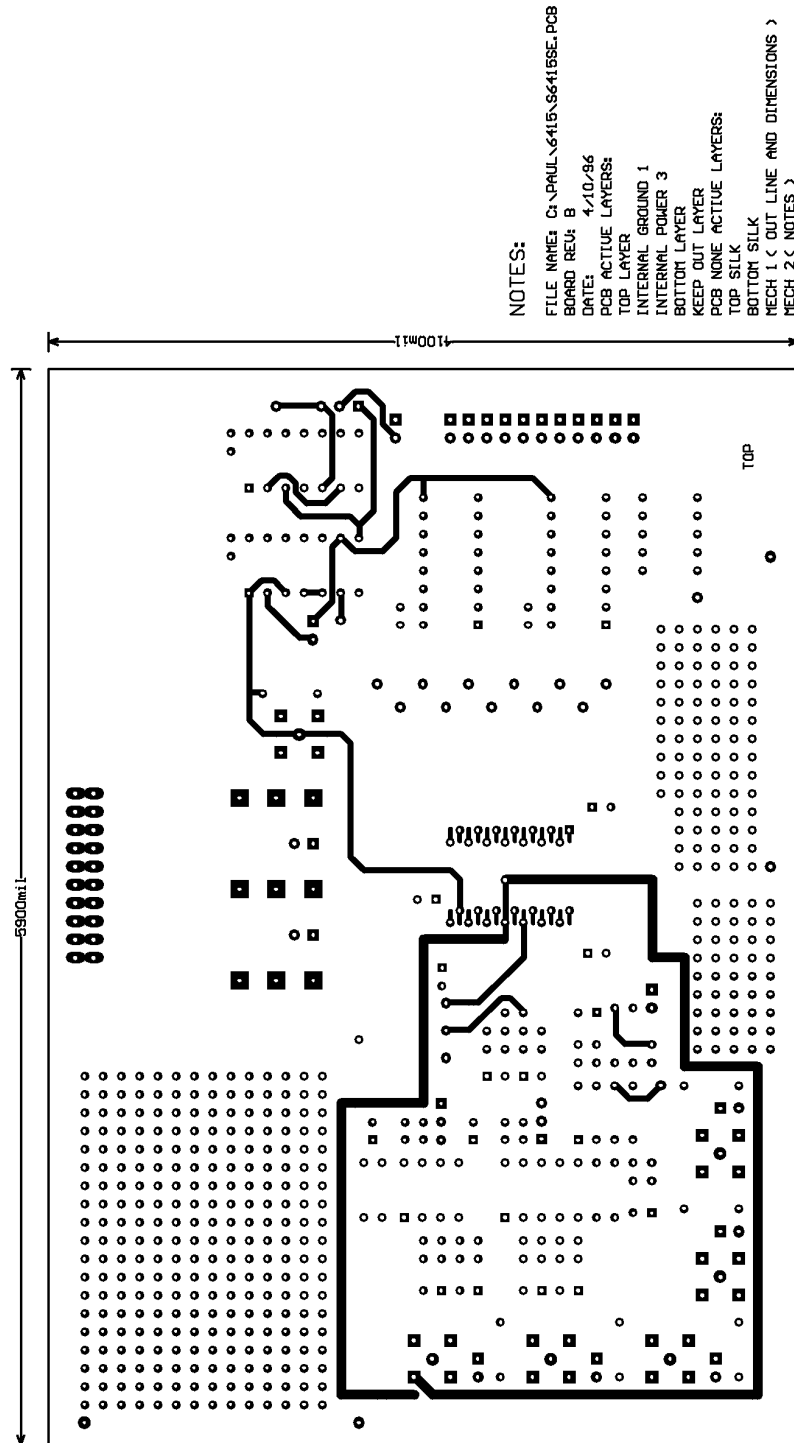MECH 1 (OUT LINE AND DIMENSIONS)
MECH 2 (NOTES)

TOP

1100mil

5900mil

Figure 19. Top Trace - 28 Pin SOIC

NOTES:

FILE NAME: C:\PAUL\6415\S6415SE.PCB
BOARD REV: B
DATE: 4/10/96
PCB ACTIVE LAYERS:
TOP LAYER
INTERNAL GROUND 1
INTERNAL POWER 3
BOTTOM LAYER
KEEP OUT LAYER
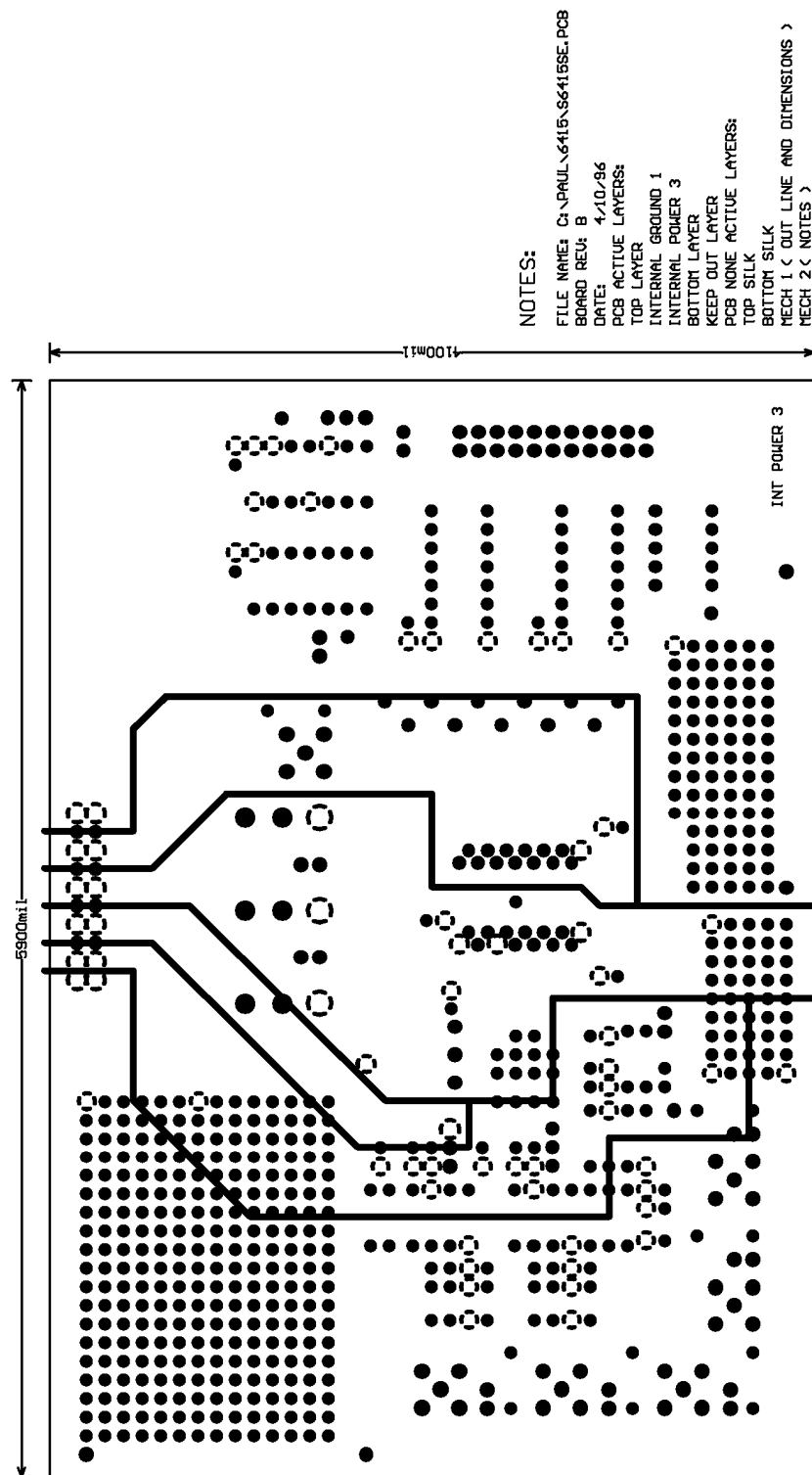PCB NONE ACTIVE LAYERS:
TOP SILK
BOTTOM SILK
MECH 1 (OUT LINE AND DIMENSIONS)
MECH 2(NOTES)

INT POWER 3

Figure 20. Power Plane - 28 Pin SOIC

NOTES:

FILE NAME: C:\PAUL\6415\S6415SE.PCB
BOARD REV: B
DATE: 4/10/96
PCB ACTIVE LAYERS:
TOP LAYER
INTERNAL GROUND 1
INTERNAL POWER 3
BOTTOM LAYER
KEEP OUT LAYER
PCB NONE ACTIVE LAYERS:
TOP SILK
BOTTOM SILK
MECH 1 (OUT LINE AND DIMENSIONS)
MECH 2 (NOTES)
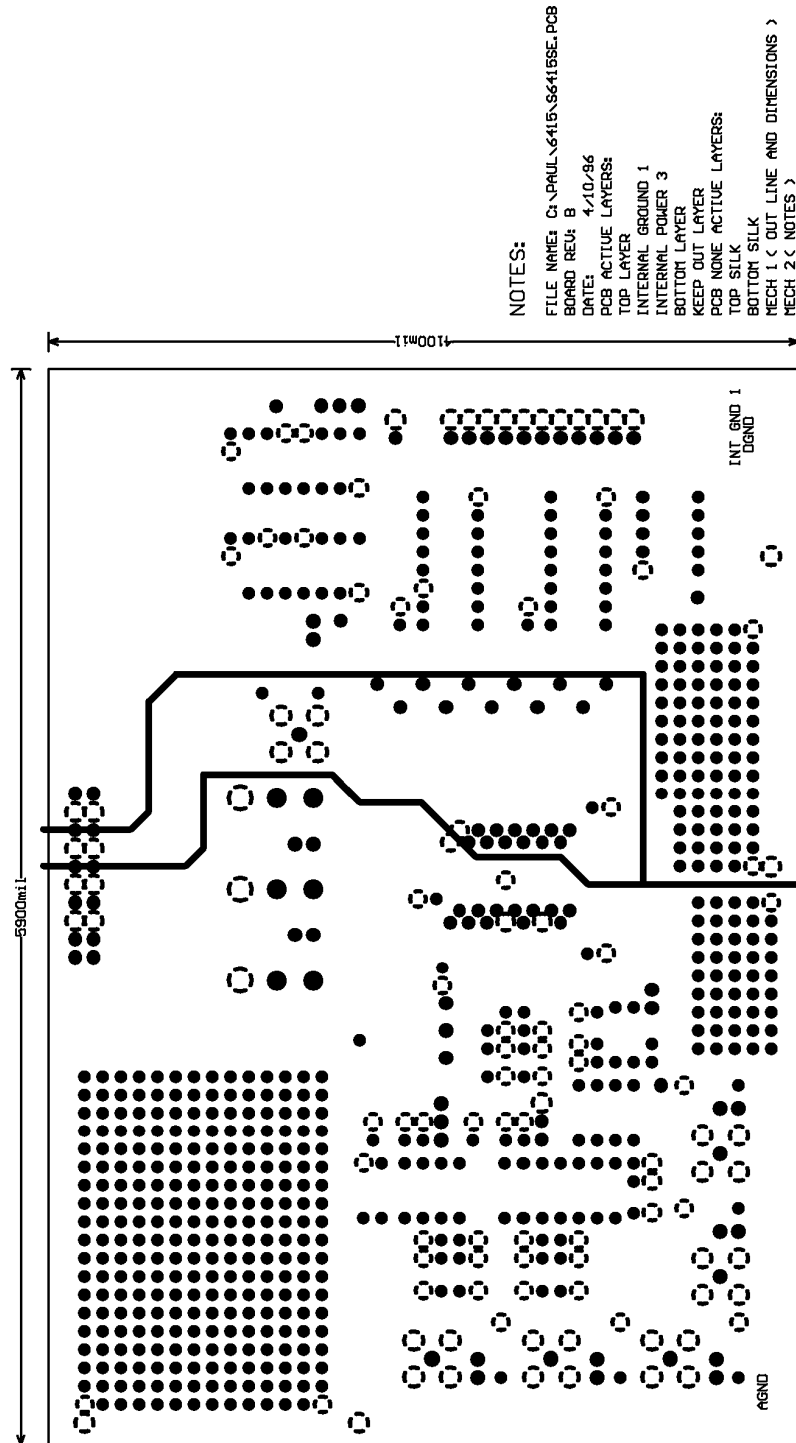
Figure 21. Ground Plane - 28 Pin SOIC

NOTES:

FILE NAME: C:\PAUL\6415\S6415SE.PCB
BOARD REV: B
DATE: 4/10/96
PCB ACTIVE LAYERS:
TOP LAYER
INTERNAL GROUND 1
INTERNAL POWER 3
BOTTOM LAYER
KEEP OUT LAYER
PCB NONE ACTIVE LAYERS:
TOP SILK
BOTTOM SILK
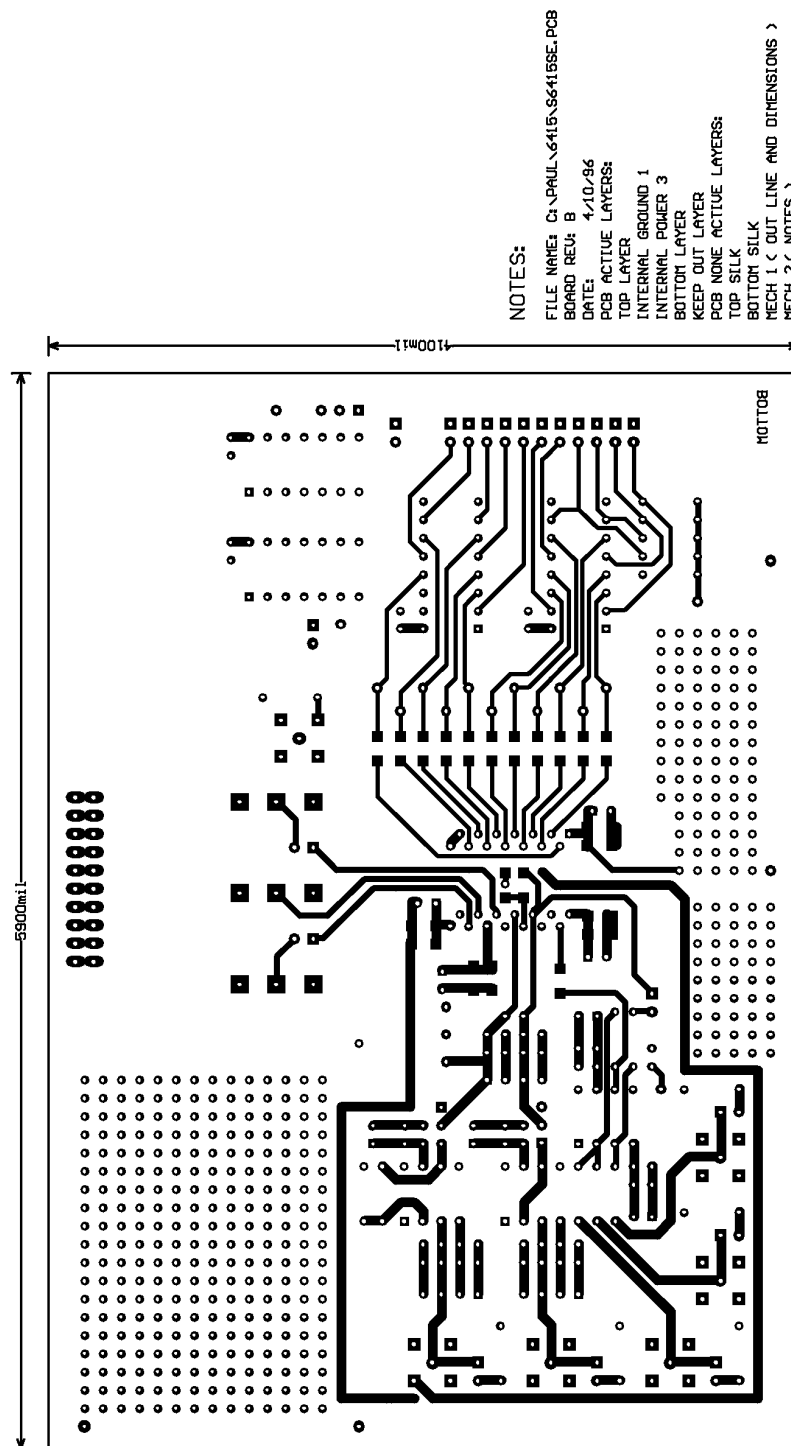MECH 1 (OUT LINE AND DIMENSIONS)
MECH 2 (NOTES)
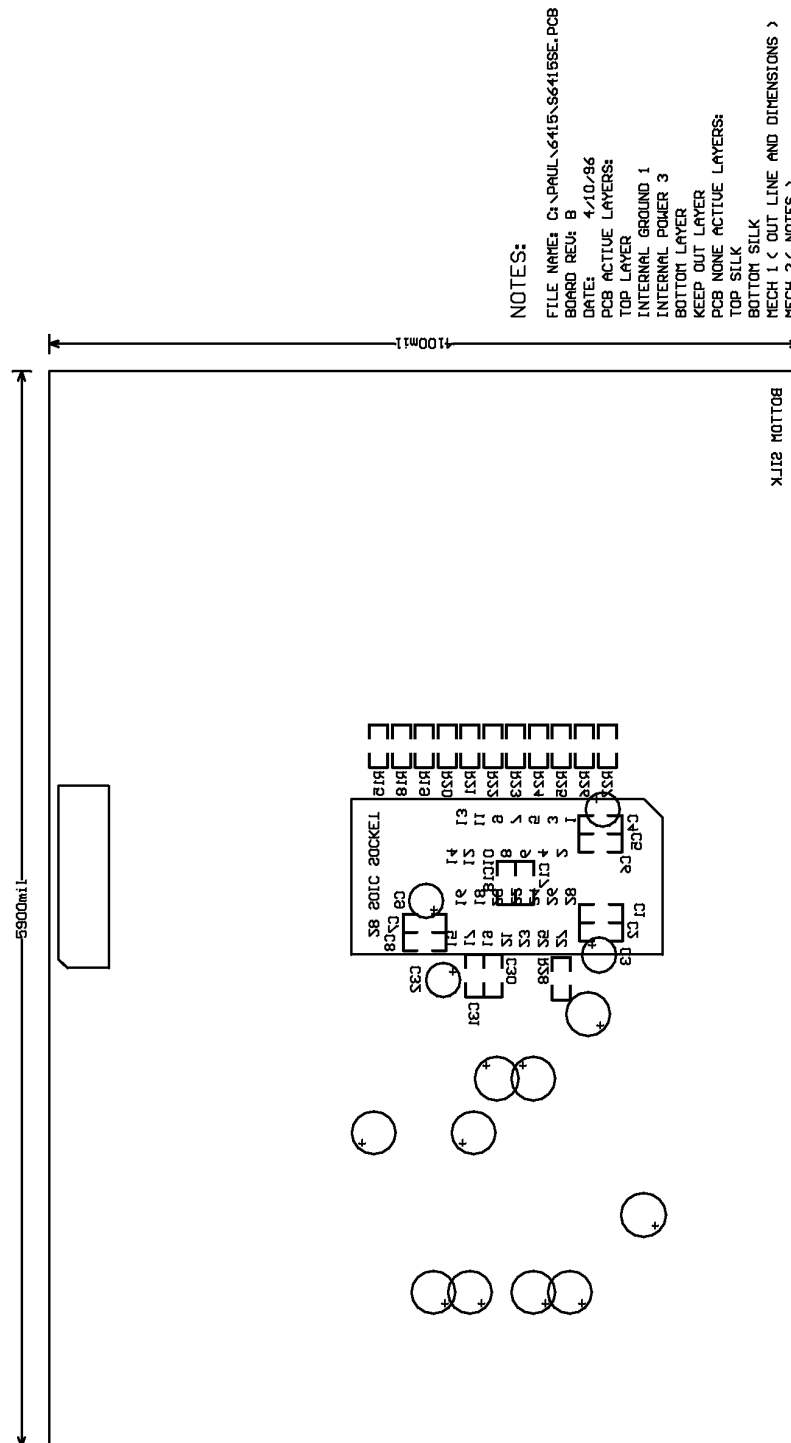
Figure 22. Bottom Trace - 28 Pin SOIC

Figure 23. Bottom Silk - 28 Pin SOIC

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