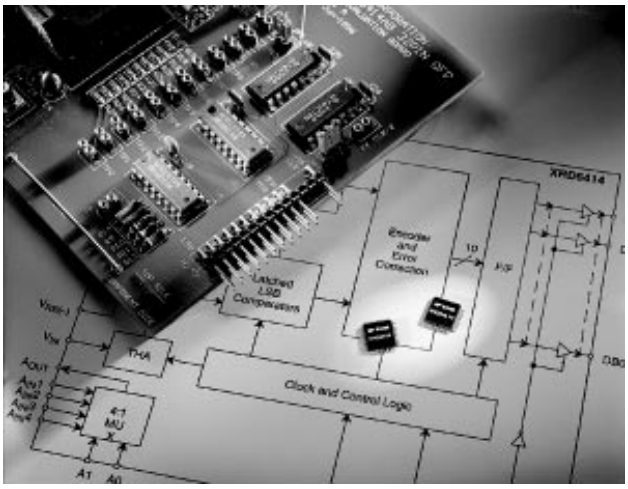
October 1996-1

XRD6414AB
APPLICATION BOARD



Application Note
Rev. 1.00

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User Manual October 1996

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EVALUATION KIT PARTS LIST

This kit contains the following:

- XRD6414AB Application Board (32 QFP)
- XRD6414 5V ADC, XRD64L14 3V ADC, XRD6415 5V ADC or XRD64L15 3V ADC
- XRD6414AB Application Note
- XRD6414, XRD64L14, XRD6415 or XRD64L15 Data Sheets

FEATURES

- Easy Evaluation of XRD6414, XRD64L14, XRD6415, and XRD64L15 in the 32 pin QFP Package
- True 10-Bit Accurate Circuit & Board Layout
- Optimized Support Circuits
- User Friendly / Flexible Interface

INTRODUCTION

The XRD6414AB is a complete printed circuit test board designed to permit quick and accurate evaluation of EXAR's XRD6414 & XRD64L14, 10-bit 20 MSPS analog-to-digital converters with 4:1 MUX. The XRD6415 and XRD64L15 in the 32 pin QFP package can also be evaluated using this board.

This application board combines a proven PC Board layout with optimized analog and digital interface circuitry to satisfy the stringent requirements needed in evaluating high performance devices of this type.

The board contains the device being tested, operational amplifiers for input buffers, latches, numerous connectors, jumper options, and observation test points in commonly used locations.

Complete DC and AC performance of the part can be evaluated by interfacing external laboratory equipment to the flexible user interface.

PREVIEW OF COMMON TEST CONFIGURATIONS

The board is set up as a general A/D test circuit. *Figure 1.* shows this default test circuit. Circuit timing is demonstrated in *Figure 12.* There are many other circuit possibilities built into the universal test board, however, starting with the default circuit is recommended.

In addition to the default test circuit, two other test configurations are discussed: the cross plot test and the external reconstruction DAC test.

Options for analyzing the output results are discussed in detail below. The most effective of these is the use of a high speed data acquisition system and FFT software to compute the performance parameters.

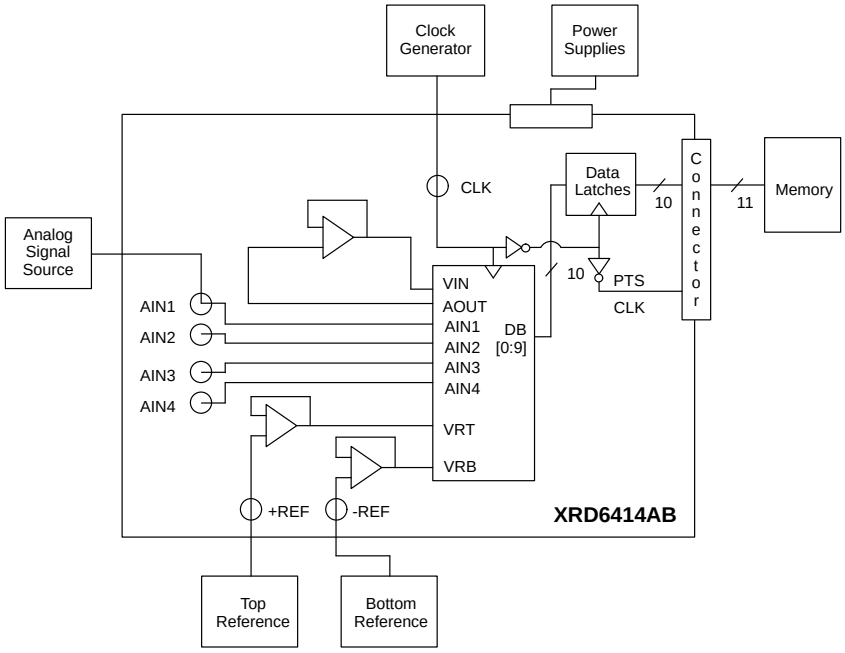

Figure 1. Default A/D Test Circuit

PCB CONSTRUCTION & LAYOUT

The XRD6414AB printed circuit board is a four layer board with two internal layers dedicated to power and ground. Top and bottom layers are used for the routing of circuitry. The internal power planes have a 5 mil separation that use the inherent board capacitance to aid power supply bypassing. The board's finished thickness is 100 mils. *Figures 31 through 36* at the back of this application note show each layer of the board.

SYSTEM CONFIGURATION - LAB SETUP

The evaluation block diagrams of the XRD6414AB with typical external test equipment are shown in *Figure 1., Figure 28.*, and *Figure 29.* The following is a more detailed description of the major on-board and external components used in these systems.

Application Board Circuitry

The application board support circuitry for the XRD6414 and XRD64L14 is shown in *Figure 2. Figure 3.* is the circuitry for the XRD6415 and XRD64L15 in the 32 pin QFP package.

The major components supporting the A/D under test are:

1. VREF BUFFERS - Op amps, U3 & U2, (AD843) can be used to isolate the externally supplied VRT and VRB from the device under test and provides a low source impedance. Holes for optional compensation and gain are provided.

2. ANALOG INPUT AMPLIFIER - An operational amplifier, U1, (AD847) is used to provide a low source impedance to the A/D. Provisions are made for summing a dither signal and/or offset voltage with the input. On-board jumper JP13 allows the referencing of analog input signals to the VRB reference voltage. Note that JP13 or JP9 must be in for the op amp to establish a virtual ground.

3. ANALOG MUX INPUTS – Four SMB input connectors labeled AIN1 to AIN4 are selected using digital inputs A0 and A1.

4. DATA LATCHES - The digital output of the A/D drive on-board latches U4 & U5 (74HC174) which buffer the device under test from the external test equipment.

5. RECONSTRUCTION DAC - A simple resistor implementation of a reconstruction DAC allows for a cross plot test at the test point labeled XPLOT. An analog waveform is generated from the four LSBs taken at the outputs of the data latches. See the Cross Plot Test section.

6. CLOCK DIVIDE CIRCUIT - The U6A (74HC74) latch divides the CLK frequency in half to synchronize slower external lab equipment. The XRD6414 still functions at the CLK frequency independent of the clock divide circuit output at the PTS CLK pin. Either half of the output data from the XRD6414 is discarded when using the clock divide circuit output or the output data can ping-pong between two different memories. The PTS CLK pin frequency is selected using JP4.

7. DIGITAL & ANALOG WORK AREAS - 100 mil spaced holes allow configuration of additional circuitry powered from the analog plane.

External Equipment Required

The system block diagrams (*Figure 1., Figure 28.*, and *Figure 29.*) show the external test equipment required to perform all test and evaluation functions. These include:

1. POWER SUPPLIES - ±15V and several +5V or +3V external power supplies are needed. Refer to the Power Supply Sequencing section before applying power to the board. Two separate ground planes are provided on the board. The AGND plane contains the XRD6414 GND pins. A separate plane, DGND, is connected to the XRD6414 DGND pin and the logic components on the board. Decoupling circuits are provided on the application board, however, low noise, low output impedance supplies are necessary for best performance. A 100 mil spaced connector is provided for all power connections. For best results, twist the power supply cable pairs. This minimizes coupling to and from unrelated sections of the setup.

2. CLOCK GENERATOR - A clock signal is applied to the SMB connector labeled CLK. Select a low jitter clock with a 50% duty cycle for best spectral results. Note there is a 50 Ω termination resistor on the board for the CLK input.

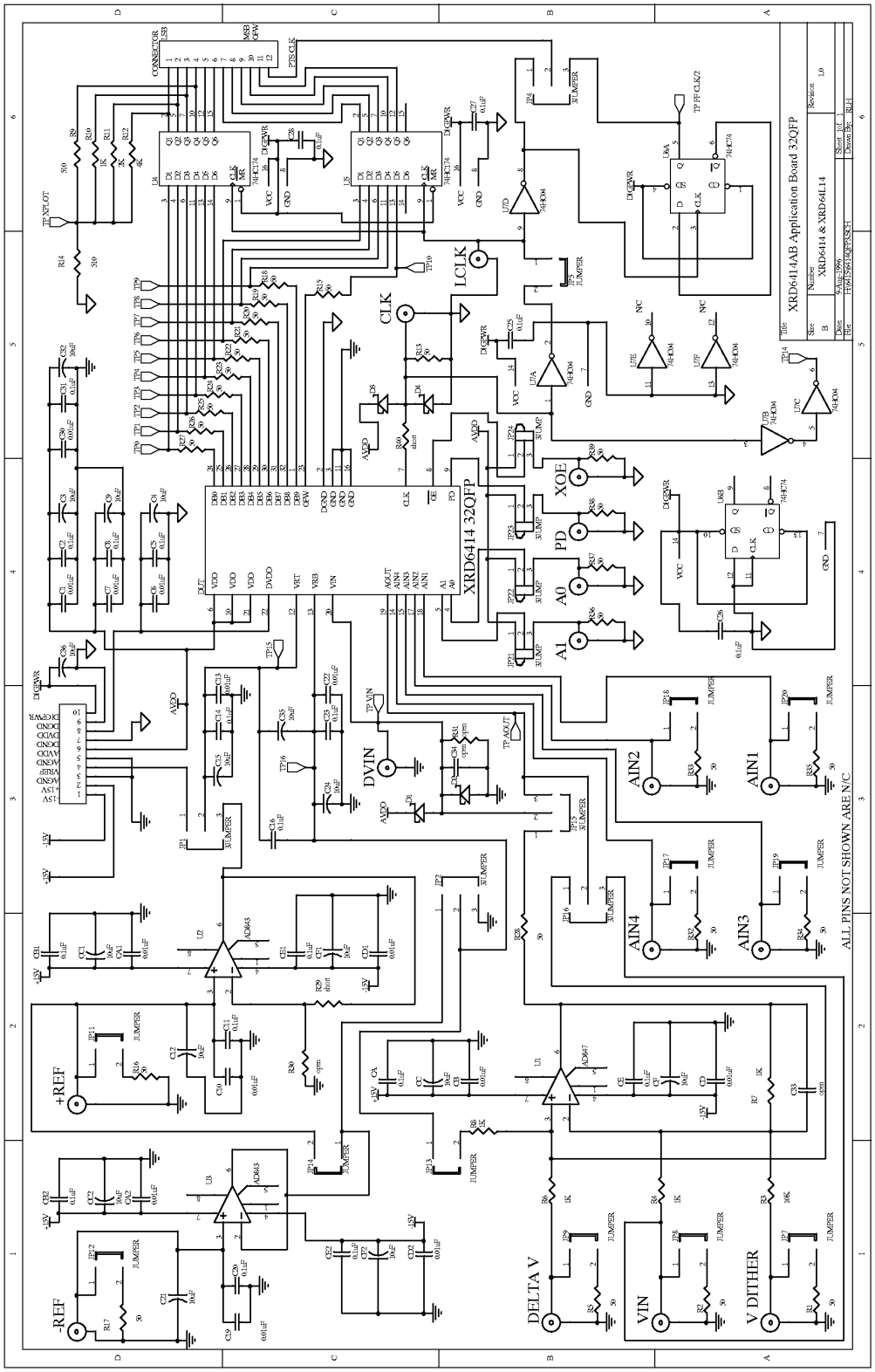

Figure 2. XRD6414AB Schematic

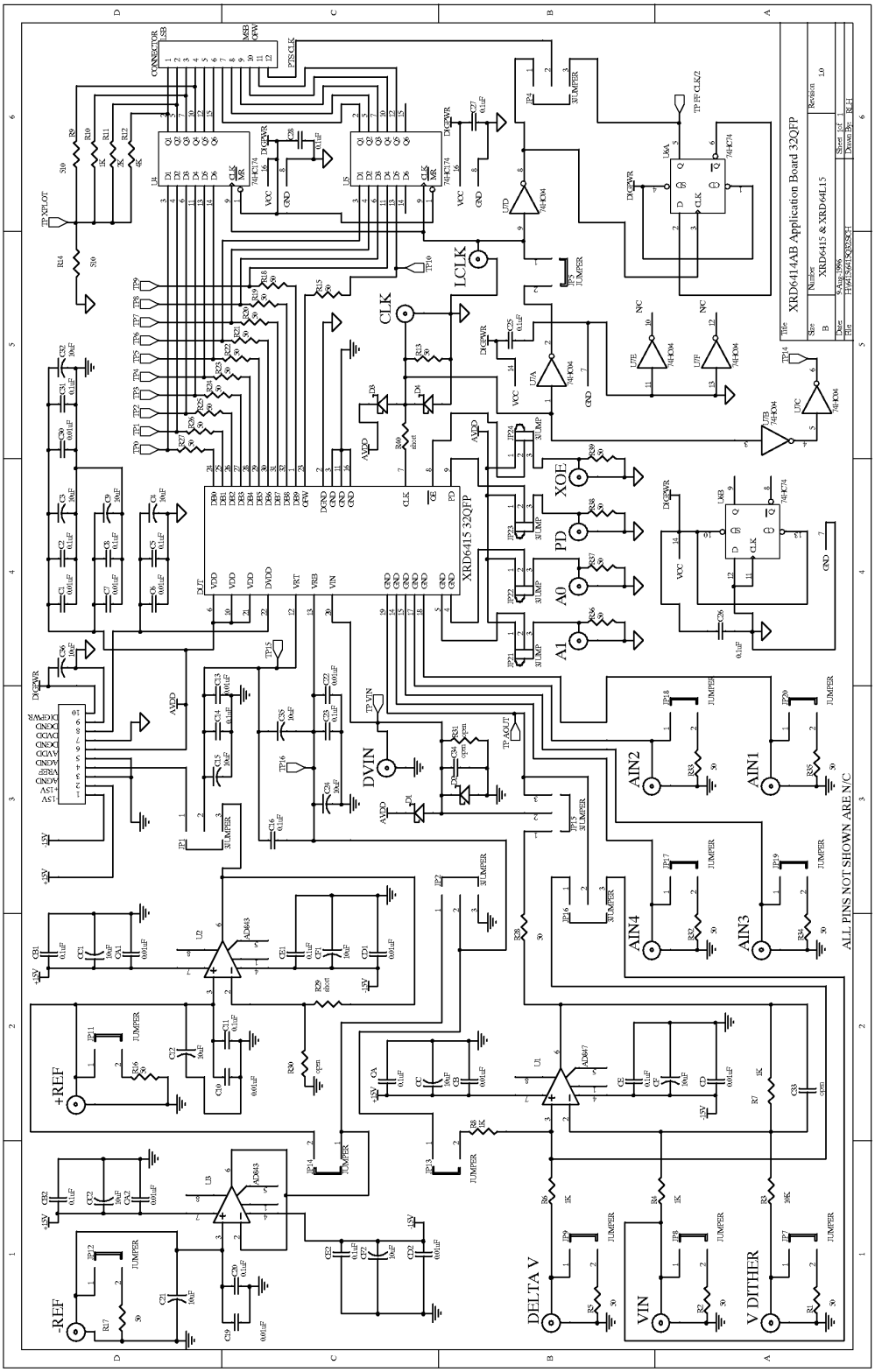

Figure 3. XRD6414AB Schematic with XRD6415 32 Pin QFP

3. REFERENCE SUPPLIES - A positive and negative reference voltage is connected through the SMB coax connectors labeled +REF and -REF (typically +5 and 0V respectively). Best results are achieved by using low noise voltage references as opposed to standard power supplies.

4. INPUT SIGNAL GENERATOR - A clean, low distortion sine wave generator is used as a signal source. A band pass or low pass filter is sometimes required to further reduce harmonics and band limit noise. The SMB coax connectors labeled VIN, V DITHER, DELTA V, AIN4, AIN3, AIN2 and AIN1 accept the analog inputs. An op amp U1 (AD847) is used to amplify this input and provide low source impedance to drive the A/D under test. The socket has a standard 741 type pin out which allows experimentation with alternative amplifiers.

5. DITHER INPUT SIGNAL GENERATOR - The cross plot test configuration (described later) requires a low noise triangle wave signal source. This signal is added through the SMB connector labeled V DITHER (an inverting input with a gain of 1/10).

6. OSCILLOSCOPE - The output of a reconstruction DAC, test point XPLOT, is used to drive the vertical input of the oscilloscope for manual linearity testing using the "cross plot" method. The reconstruction DAC is simply a 5 resistor implementation.

Optional Equipment

1. EXTERNAL PRECISION OUTPUT DAC - As an alternative to DSP, a high speed precision digital-to-analog converter can reconstruct the output in analog form. Analog measurements can be used to evaluate the A/D's performance using conventional analog instrumentation.

2. DSP - Evaluation of dynamic and static performance is done by external processing devices that perform time and frequency analysis to determine characteristics such as linearity, noise, harmonic distortion, intermodulation distortion, etc. The data is available at the 24 pin data connector. Each output pin is complemented by a ground pin. The external clock output is available on a pin labelled PTS CLK.

SYSTEM OPERATION

Reference Inputs

With the reference op amps in circuit, the ADC's reference pins (VRB and VRT) are driven in an offset and range mode:

VRB = (-REF), VRT = (+REF)

Hence -REF defines the offset and (+REF – –REF) defines the span.

The external reference voltages can be configured to go through the op amp buffers or go directly to the A/D from the power connection labeled VREF. Using JP1, the positive reference can be shorted to VREF at the power connector. Using JP2, the negative reference can be shorted to AGND. Note that +REF must be more positive than -REF, since the positive reference voltage must be greater than the negative reference voltage on-chip.

A single voltage reference design is shown in *Figure 4.* The +REF voltage is derived by applying gain with U2 to the –REF voltage connected at JP14.

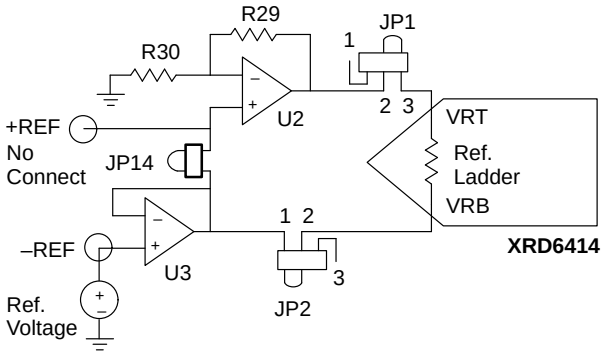

Figure 4. Single Voltage Reference Design

The single voltage reference approach can reduce system cost because only one fixed voltage reference is required as opposed to using two.

DNL and INL performance is optimized when the VRB input of the XRD6414 is buffered. If VRB is connected to the PCB ground plane it is subject to the noise and ground bounce in that plane.

VIN Input

The input to the ADC (VIN) is determined by the circuit in *Figure 5.* Either JP9 or JP13 must be connected for the op amp U1 to establish a pseudo ground. If JP13 is connected, the virtual ground of U1 tracks VRB of the XRD6414. R28 decouples the output of U1 from the

switching input capacitance of the XRD6414. Alternatively, all input circuitry can be bypassed by placing the input signal directly into DVIN. ADC performance is optimized with a capacitor at the input such as C34 = 100pF.

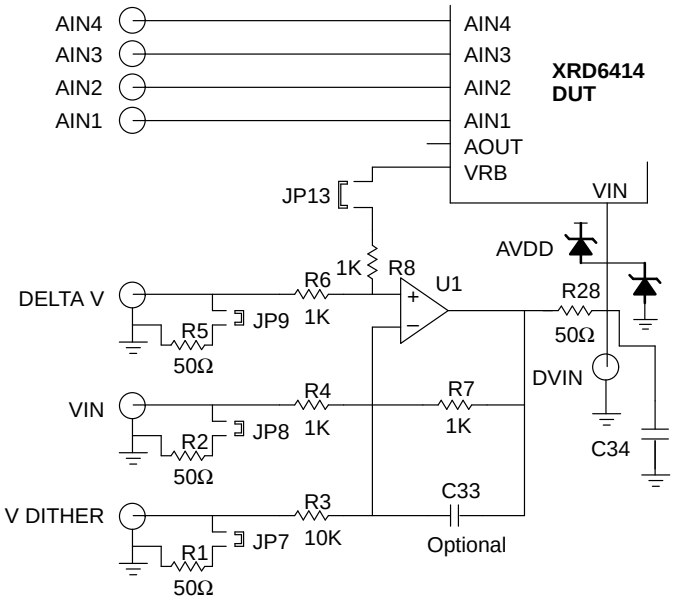

Figure 5. VIN Circuit

Analog MUX Input

The four channel analog MUX is controlled by two digital logic signals at A1 and A0. The analog MUX output is configured with jumpers JP15 and JP16 to connect directly with VIN or the inputs of U1.

Placing a capacitor (such as C34 $\geq$ 15pF) on the output of the MUX will cause a degradation in SNR and SNDR due to the phase shift induced by the varying R_{ON} of the MUX. When using the MUX, make the terminating resistance at the output of the MUX (such as R31 or the high impedance input of an opamp) >> R_{ON} of the MUX. If this condition is not maintained, then R_{ON} will vary to a greater degree.

The R_{ON} as a function of input voltage is shown in *Figure 6.* Note the degradation in SNDR shown in *Figure 25., Figure 26.* and *Figure 27.* due to the analog MUX. Typical worst case channel-to-channel matching is within ±10% of R_{ON} for VDD = 5V and ±6% for VDD = 3V.

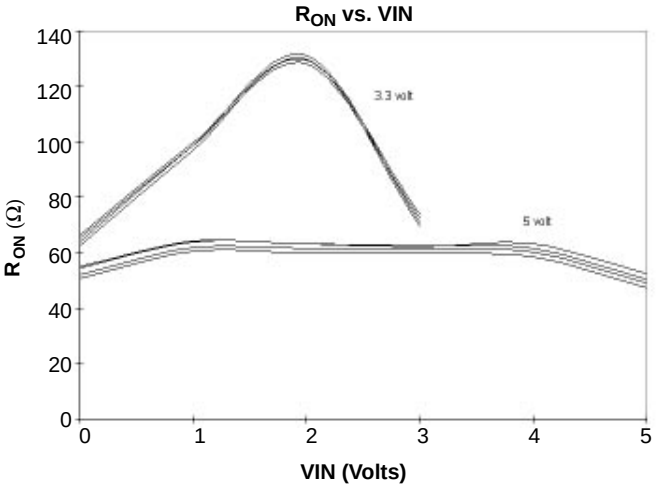

Figure 6. Analog MUX R_{ON} vs. Input Voltage

The MUX switching time is shown in *Figure 7.* and *Figure 8.* The test circuit for *Figure 7.* and *Figure 8.* is illustrated in *Figure 9.*

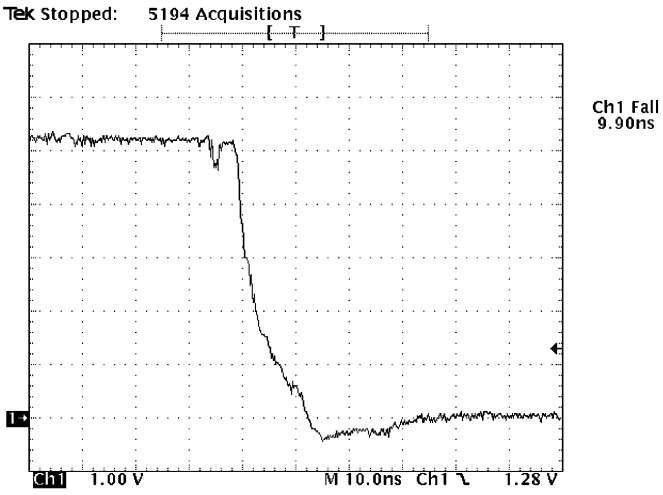

Figure 7. MUX Switching Time 5V Waveform, VDD = 5 V

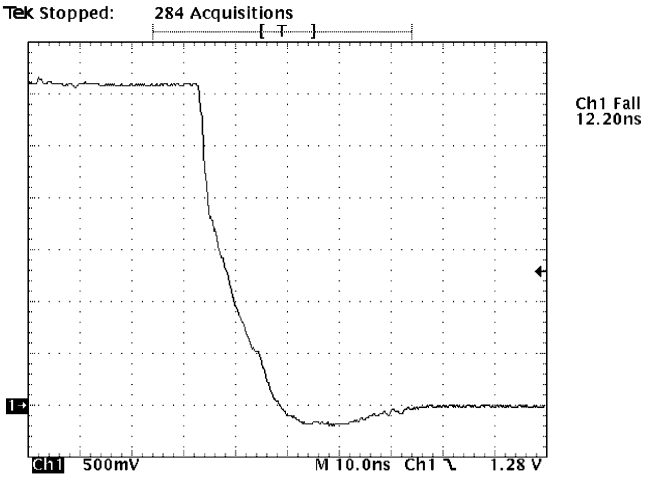

Figure 8. MUX Switching Time 3V Waveform VDD = 3 V

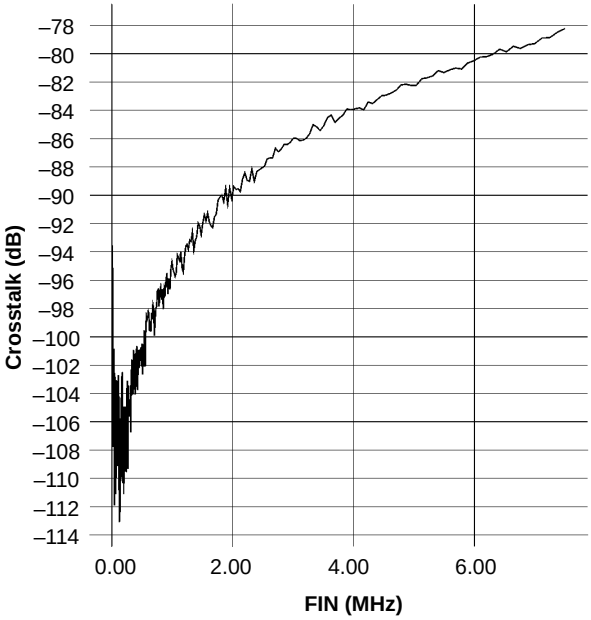

Figure 10. XRD6414 Crosstalk, VDD = 3 V and VIN = 8dBm

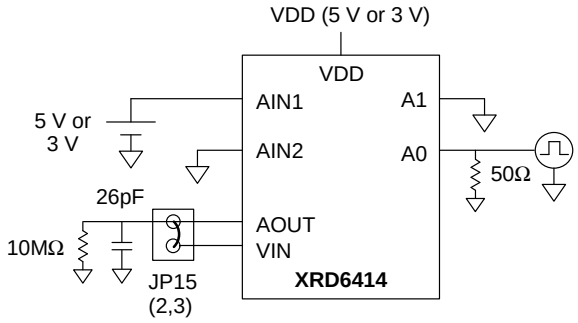

Figure 9. MUX Switching Time Test Circuit

The crosstalk from AIN1 to AIN3 on the XRD6414AB is shown in *Figure 10.* for an 8 dbm source voltage with VDD=3V.

Crosstalk is measured by the following equation:

$$Crosstalk\ (dB)\ =\ 20\ \log\frac{V_{OUT}}{V_{IN}}$$

The crosstalk test circuit is shown in *Figure 11.*

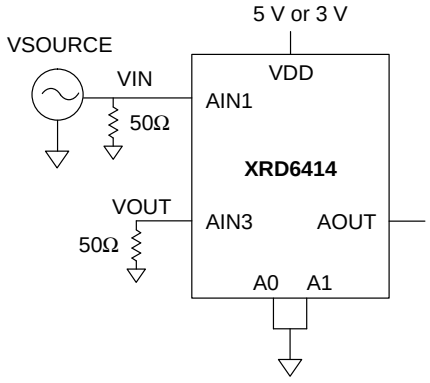

Figure 11. Crosstalk Test Circuit

Timing

Figure 12. demonstrates the circuit timing of the XRD6414AB. The CLK is provided by the user as specified on the XRD6414 data sheet. The PTS CLK is an output that allows for synchronization of external lab equipment with the output data DB[0:9]. DB[0:9] are valid after the rising edge of the PTS CLK.

The DC performance of the XRD6414 is optimized with rise and fall times of CLK edges limited to greater than or equal to 7ns. A resistor in series with the CLK input pin can combine with parasitic capacitance to limit rise and fall times. This is evident in both the cross plot, DNL, and SNR tests. DC performance is not significantly degraded for duty cycles up to either 60% or 40%.

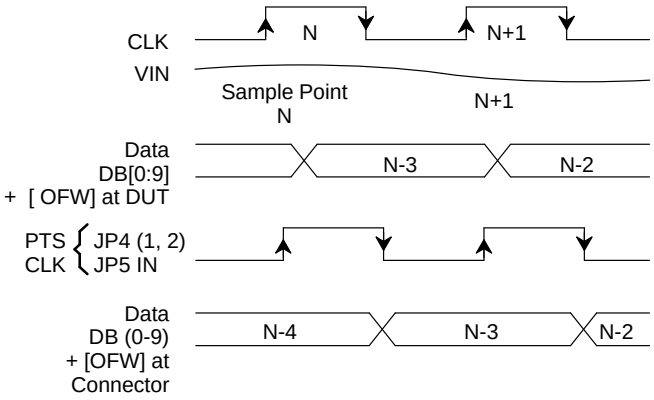

Figure 12. XRD6414AB Circuit Timing

An alternative to using the on-board timing circuitry is to externally drive LCLK. If LCLK is driven by an external clock source, JP5 should be removed. LCLK provides the clocking for latches U4 and U5. The inversion of LCLK is available at the PTSCLK output header for synchronization of lab equipment. The frequency of PTSCLK is equal to LCLK if JP4 is connected at (1, 2) or half of LCLK if JP4 is at (2, 3).

XRD6414AB 3.3 V Operation

The XRD64L14 and XRD64L15 can be evaluated by simply lowering AVDD and DVDD to 3.3V. Note that the voltage at VRT, VRB and VIN must remain within the supply range of the XRD64L14 and XRD64L15. DIGPWR provides a separate supply voltage to the digital logic ICs (U4, U5, U6, U7) on the XRD6414AB board. Typically, the digital logic thresholds will work with the XRD64L14 or XRD64L15 operating at 3.3V when DIGPWR is lowered to 4.5V. If the output is intermittent, either adjust the DIGPWR supply voltage or use 3.3V logic. If 3.3V logic is used, swap out the digital logic ICs and lower DIGPWR to 3.3V.

5 V Operation of XRD6414 and XRD6415 with 3.3 V Logic Output Interface

The DVDD pin of the XRD6414 or XRD6415 is a separate power supply dedicated to the logic output drivers. DVDD is not connected internally with any of the other power supplies. This allows the XRD6414 to output 3.3V logic levels when DVDD is driven to 3.3V independent of the voltage at the other VDD pins. The XRD6414AB has a separate connector for the DVDD supply to test this function. Logic thresholds of the digital logic ICs (U4, U5, U6, U7) typically match when DIGPWR is lowered to 3.3V. *Figure 13.* illustrates the power supply circuity of the XRD6414. Best parametric results are obtained when DVDD = 3.3V instead of 5V.

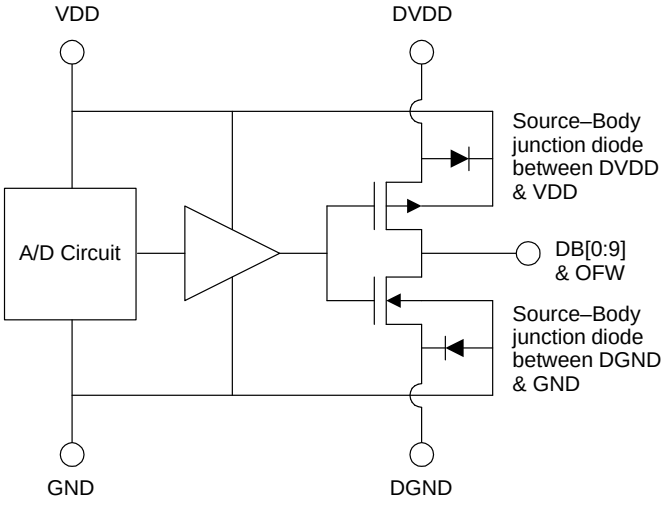

Figure 13. XRD6414 and XRD6415 ADC Power Supply Circuit Allows Separate VDD & DVDD and Separate GND & DGND

Power Supply Sequencing

There are no power supply sequencing issues if DVDD and VDD of the XRD6414 are driven from the same supply. Best parametric results, however, are obtained when DVDD and VDD are driven from separate supplies. When DVDD and VDD are driven separately, VDD must come up at the same time or before DVDD, and go down at the same time or after DVDD. If the power supply sequencing in this case is not followed, then damage may occur to the product due to current flow through the source-body junction diodes between DVDD and VDD. A low threshold schottky diode placed locally between DVDD and VDD can prevent damage to the XRD6414.

Digital Outputs

The digital output drive circuitry of the XRD6414, XRD64L14, XRD6415, and XRD64L15 was designed to operate separately from the analog supplies. DVDD and DGND connect directly to the digital logic power of the system isolating the analog and digital power supplies and grounds. DGND is not common to the XRD6414 or XRD6415 substrate as shown in *Figure 13.* The substrate is common only to the packages' GND pins. The XRD6414AB has two separate ground connections at the power header to allow experimentation.

Use 50 or 100 Ω resistors to isolate the XRD6414 digital output pins from a latch or bus connection. If the layout requires a digital bus trace greater than 3 inches use a latch or digital buffers as shown with U4 & U5 in the schematic. This protects the output drivers and reduces the effects of high speed switching logic signals from degrading the ADC performance. Layout the latch or digital buffers as close to the ADC as possible.

Digital Inputs

The input logic thresholds of the XRD6414 and XRD6415 ($\overline{OE}$, PD, A1, A0 & CLK) are set by the voltage at the VDD pins.

DIGITAL SIGNAL PROCESSING

A comprehensive dynamic performance evaluation is most often done by using external hardware capable of fast data acquisition and storage. The computation of integral linearity, differential linearity, signal-to-noise and distortion ratios, the effective number of bits, and other useful figures of merit is performed using software having histogram and FFT capability. The accuracy of the test results depends upon the quality of the input sinewave and clock source.

The Tektronix PTS101 and other internally developed proprietary systems are used by EXAR to acquire and analyze the ADC data. The DNL graph in *Figure 14.* and the INL graph in *Figure 15.* are examples of these techniques using the XRD6414AB.

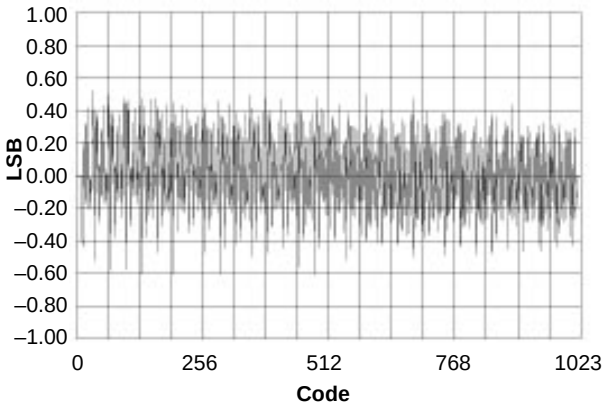

Figure 14. XRD64L14 DNL @ 15 MSPS, VDD = 3V, VRT=2.5V, VRB = 0.5V

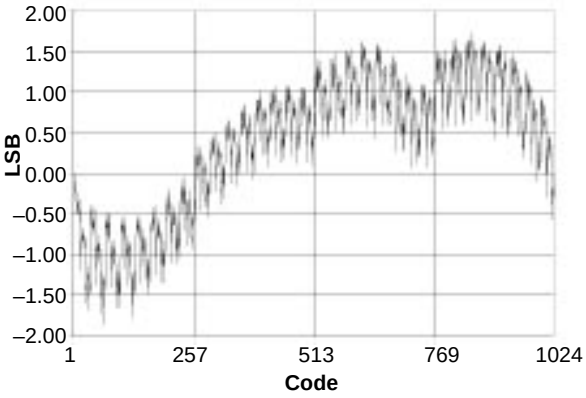

Figure 15. XRD64L14 INL @ 15 MSPS, VRT – VRB = 2.5V, VDD = 3V

Figures 16 through 27 demonstrate the typical dynamic performance of the ADC with and without the analog MUX.

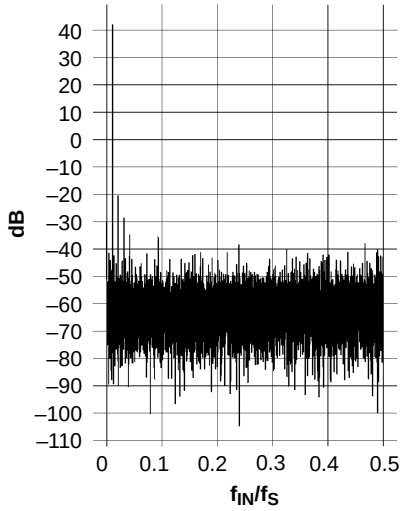

Figure 16. XRD6414 FFT VREF = VDD = 5V, DVDD = 3.3V, FIN = 100 kHz, 10 MSPS, C34 = 100pF

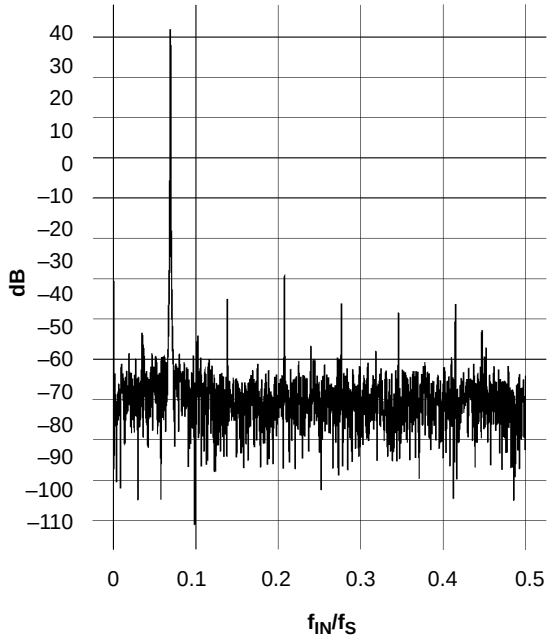

Figure 17. XRD64L14 FFT VREF = VDD = 3.3V, DVDD = 3.3V, FIN = 1 MHz, 15 MSPS, C34 = 100pF

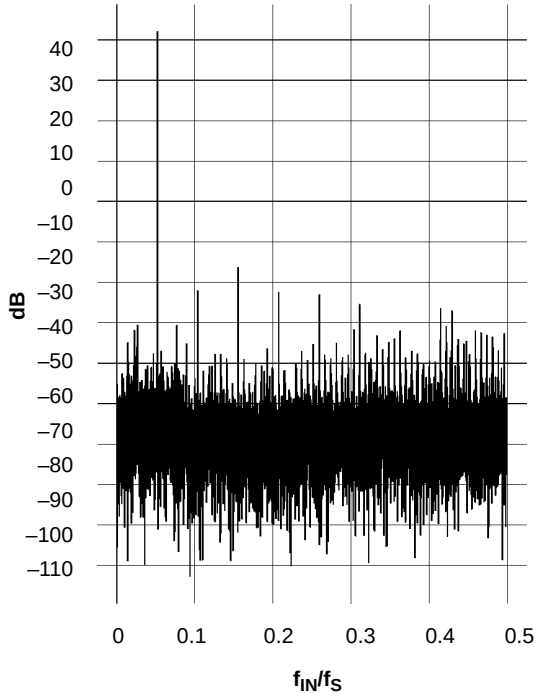

Figure 18. XRD64L14 FFT VREF = VDD = 3.3V, DVDD = 3.3V, FIN = 1 MHz, 20 MSPS, C34 = 100pF

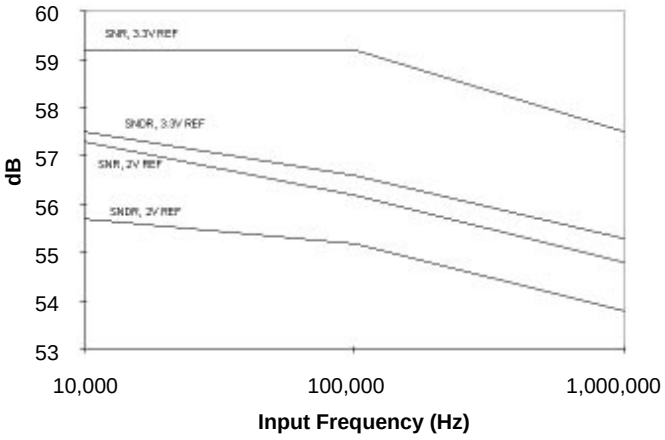

Figure 19. XRD64L14 SNR & SNDR vs. FIN, VDD = 3.3V, DVDD = 3.3V, VREF = 3.3V & 2V, 10 MSPS, C34 = 100pF

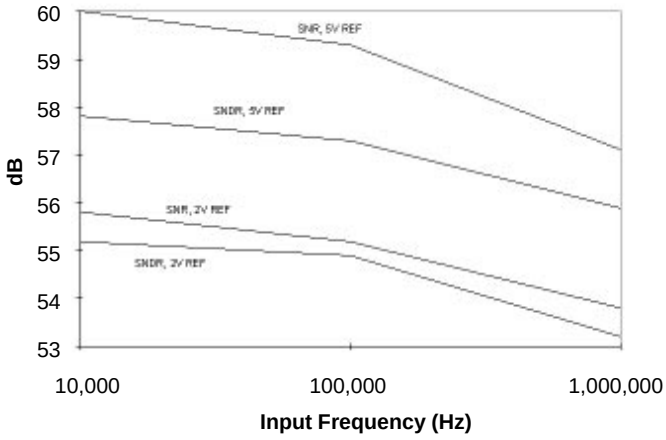

Figure 20. XRD6414 SNR & SNDR vs. FIN, VDD = 5V, DVDD = 3.3V, VREF = 5V & 2V, 10 MSPS, C34 = 100pF

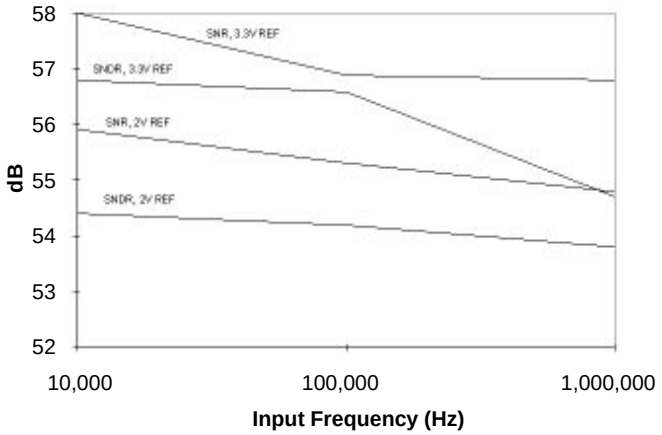

Figure 21. XRD64L14 SNR & SNDR vs. FIN, VDD = 3.3V, DVDD = 3.3V, VREF = 3.3V & 2V, 15 MSPS, C34 = 100pF

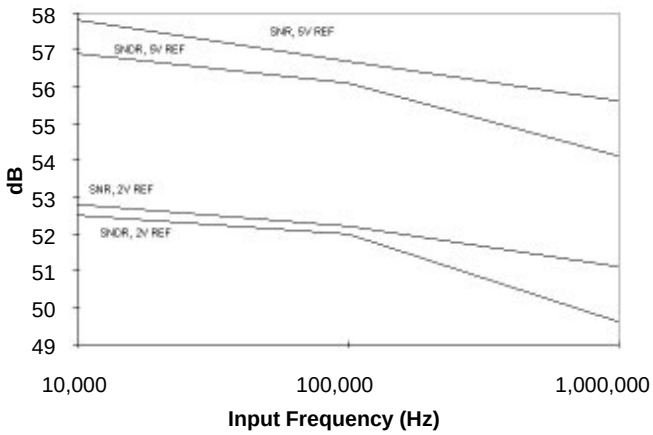

Figure 22. XRD6414 SNR & SNDR vs. FIN, VDD = 5V, DVDD = 3.3V, VREF = 5V & 2V, 15 MSPS, C34 = 100pF

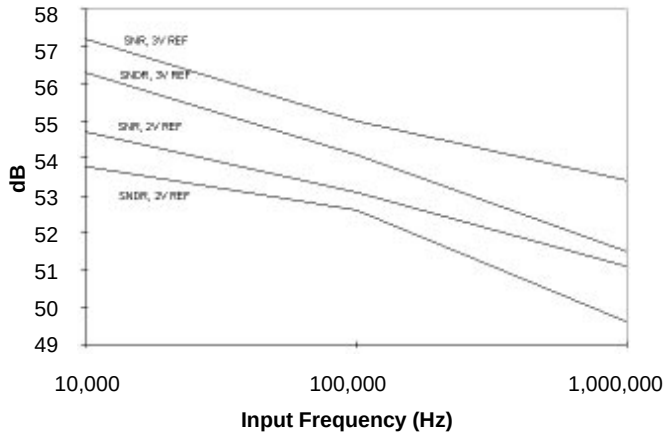

Figure 23. XRD64L14 SNR & SNDR vs. FIN, VDD = 3.3V, DVDD = 3.3V, VREF = 3.3V & 2V, 20 MSPS, C34 = 100pF

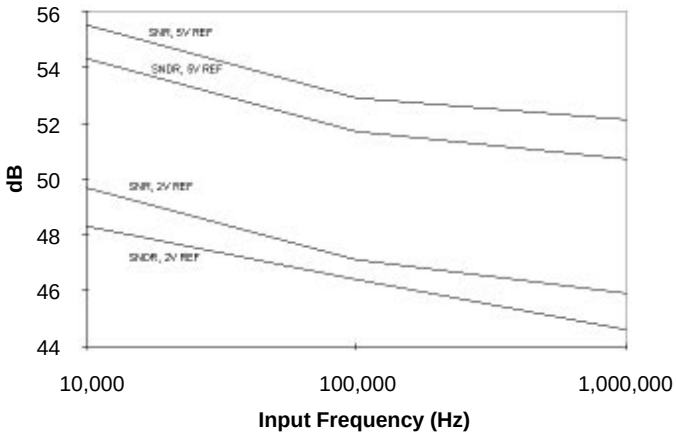

Figure 24. XRD6414 SNR & SNDR vs. FIN, VDD = 5V, DVDD = 3.3V, VREF = 5V & 2V, 20 MSPS, C34 = 100pF

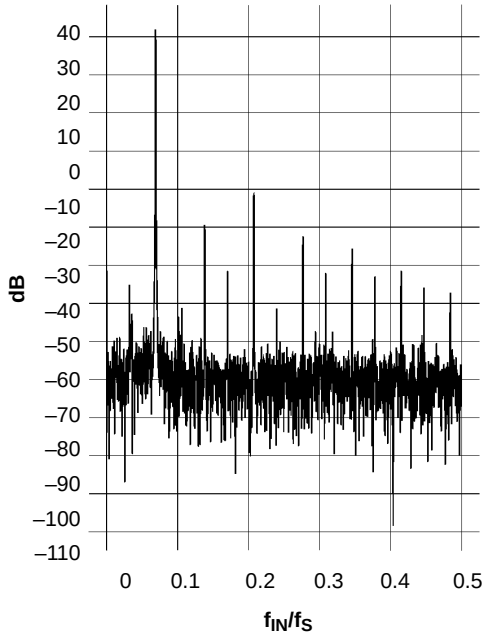

Figure 25. XRD64L14 FFT Through Analog MUX, VREF = VDD = 3.3V, DVDD = 3.3V, FIN = 1 MHz, 15 MSPS, C34 = Open

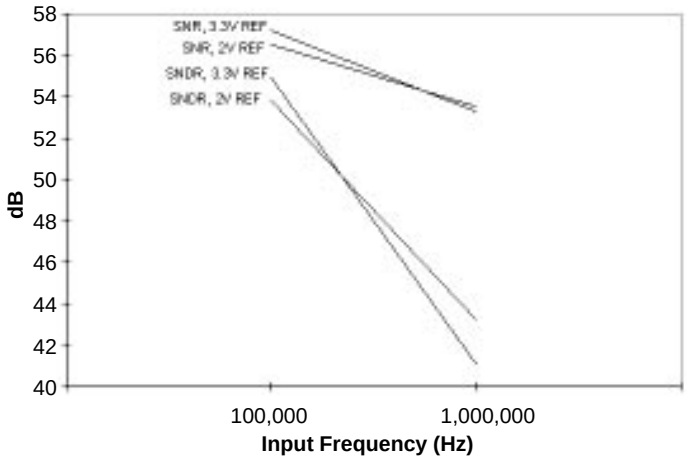

Figure 26. XRD64L14 SNR & SNDR vs. FIN through Analog MUX, VDD = 3.3V, DVDD = 3.3V, VREF = 3.3V & 2V, 15 MSPS, C34 = Open

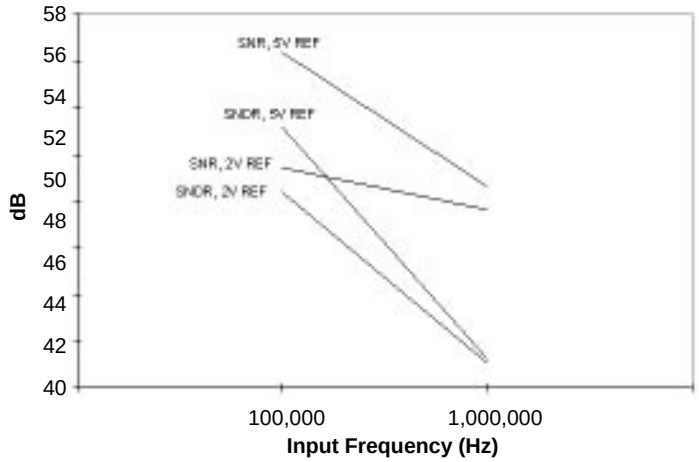

Figure 27. XRD6414 SNR & SNDR vs. FIN through Analog MUX, VDD = 5V, DVDD = 3.3V, VREF = 5V & 2V, 15 MSPS, C34 = Open

ANALOG TESTING WITH EXTERNAL DAC

The logic output of the system can be converted back to analog by using a high performance digital-to-analog converter. Laboratory spectrum analyzers and oscilloscopes can be used to measure linearity, frequency response, harmonic distortion, noise, intermodulation distortion, etc. These measurements can be converted to the specifications commonly used in specifying A/D's dynamically. In addition to a high quality sinewave input, the output digital-to-analog converter must be significantly more accurate than the A/D under test as shown in *Figure 28.*

Note that measurements taken with this method demonstrate the combined errors of all the circuitry involved.

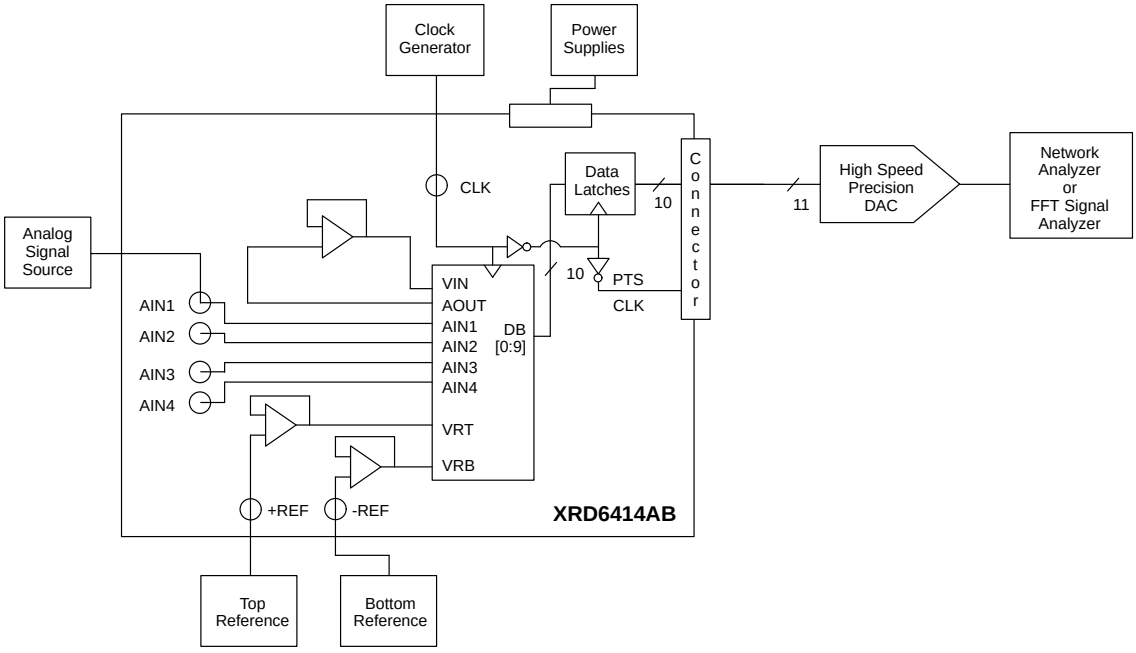

Figure 28. External Precision DAC Reconstruction Test

CROSS PLOT

An evaluation of differential linearity can be simply done with an oscilloscope, a triangle wave or sinusoid generator and a low noise DC signal source. Input SMBs are provided on the board so this "cross plot" method can be conveniently implemented (See *Figure 29.*) The oscilloscope must be set in the X-Y display mode.

A triangle wave (500 Hz) with a peak-to-peak amplitude of approximately 100 LSBs is supplied to the "VDITHER" input. This is attenuated by a factor of R7/R3 by the input amplifier. The triangle wave is also used to drive the x axis of the scope. The horizontal gain is set so that 16 divisions are swept. Look at Test Point (XPLOT) with the vertical input. Set the horizontal gain at about 2 LSB per division.

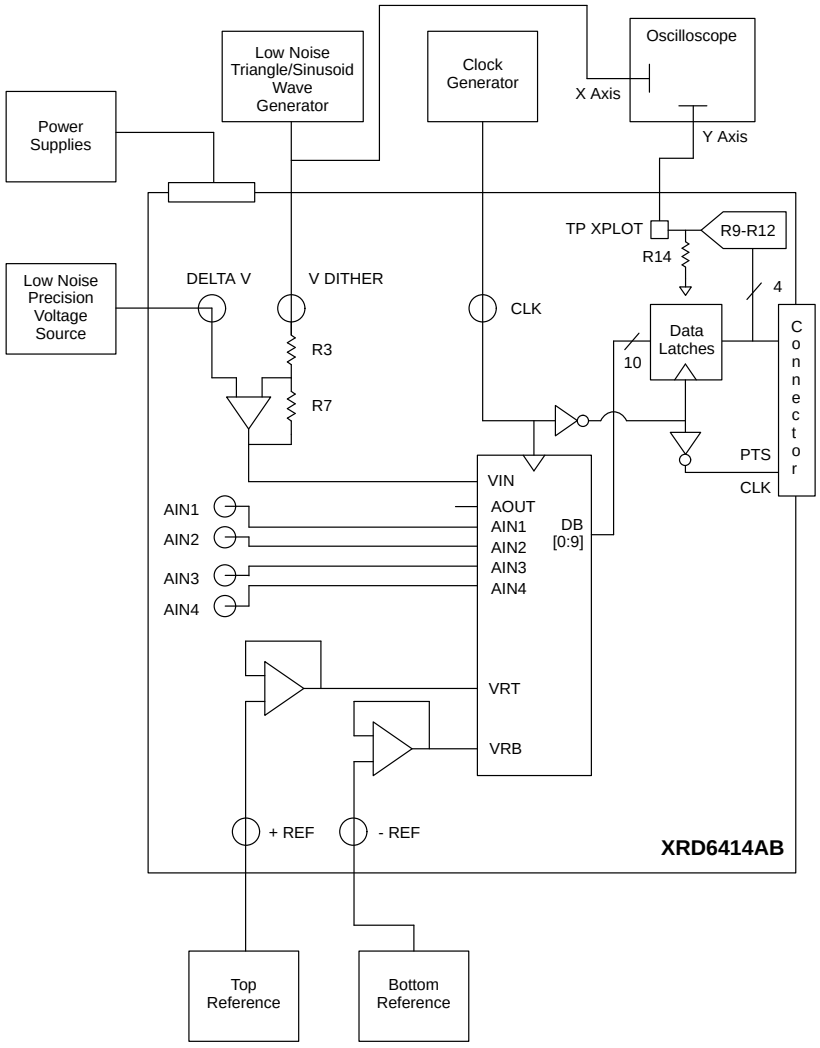

Figure 29. Crossplot Setup

A stair step waveform will result (See *Figure 30.*) By changing the DC input at DELTA V, sixteen code transitions can be observed about any DC input level. The horizontal distance between these transitions is the code width. Missing codes cause steps to be absent. By setting the end point thresholds to coincide with the scope grid lines, integral linearity errors are displayed as thresholds which are off-centered from these grid lines. A precision DC voltage source is necessary for the integral linearity measurement.

Since the conversion speed is much faster than the dither frequency, multiple readings are taken at each threshold. The horizontal variation of each threshold gives a qualitative measure of noise (in LSBs).

Using this “cross plot” method is a good way to prove out the lab setup prior to more sophisticated DSP test.

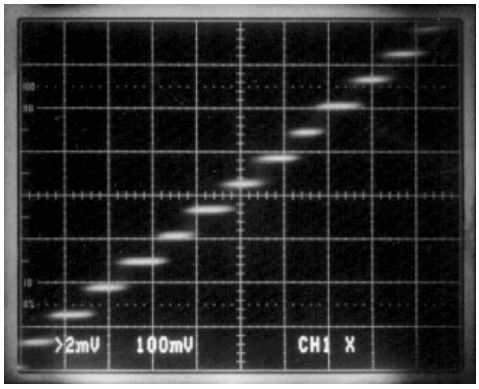

Figure 30. Crossplot Staircase Output CLK = (15 MSPS, t_{rf} = 15 ns), VIN = 3V, VREF = 2V

JUMPER OPTIONS

The XRD6414AB offers flexibility through configuration determining jumpers and switches. These options furnish choices for (1) input termination resistors, (2) bypassing of the reference input buffers, and (3) the selection of several logic and clock options. *Table 1.* shows the jumper functions along with the default configuration set-up prior to shipment. *Table 2.* plots the test points available.

Termination of Input Coax Cables		
Jumper	**Description**	**Default**
JP8	Connecting adds 50Ω from VIN to AGND	IN
JP7	Connecting adds 50Ω from V DITHER to AGND	OUT
JP9	Connecting adds 50Ω from DELTA V to AGND	IN
JP11	Connecting adds 50Ω from +REF to AGND	OUT
JP12	Connecting adds 50Ω from -REF to AGND	OUT
JP17, 18, 19, 20	Connecting adds 50Ω from one of AIN1-4 to AGND	OUT
Reference Amplifier/Buffer Bypass (1)		
JP1 (1, 2)	Connecting shorts VREF in Power Connector to VRT pin of ADC	OUT
JP1 (2, 3)	Connecting Shorts Output of U2 to VRT Pin of ADC	IN
JP2 (2, 3)	Connecting shorts AGND to VRB pin of ADC	OUT
JP2 (1, 2)	Connecting Shorts Output of U3 to VRB Pin of ADC	IN
JP13	Connecting Biases U1 Relative to VRB Pin of ADC	OUT
JP14	Connects –REF to Input of U2	OUT
JP15	Selects VIN from AOUT or U1	(1, 2)
JP16	Feeds AOUT to U1 Non-Inverting or Inverting Input	OUT
Logic and Clock Jumpers (1)		
JP5	Connects CLK to U4, U5, and PTS CLK Output	IN
JP4 (1, 2)	Connects CLK to PTS CLK	IN
JP4 (2, 3)	Connects CLK/2 to PTS CLK	OUT
JP21, 22	Sets Logic Levels of A1, A0	(2, 3)
JP23	Sets PD of ADC	(2, 3)
JP24	Sets $\overline{OE}$ of ADC	(2, 3)

Notes:
1. Jx (a, b) means short pin a and pin b of jumper x.

Table 1. Jumper Options

Test Point	Description
TP0-10	DB0-9 and OFW of ADC
TP14	CLK Output of U7C
TP15	VRT of ADC
TP16	VRB of ADC
TP FF CLK/2	Output of CLK Divide Circuit
TP VIN	VIN of ADC
TP XPLOT	Crossplot Output
TP AOUT	AOUT of ADC

Table 2. Test Points

FINAL DESIGN CONSIDERATIONS

After the XRD6414AB has been used to demonstrate that the XRD6414 or XRD6415, the clock timing, and the analog support circuits are acceptable, the design must be successfully transferred to the user's system. A close copy of the proven layout is recommended as is the use of identical support devices.

1. Be generous with analog and digital ground planes. Mirror the ground plane with the supply planes. Use a 5 mil power / ground plane separation if a four layer board can be used. The XRD6414 substrate is common to the packages' GND pins only. DGND and DVDD are separate supplies dedicated to the output logic drivers of the XRD6414. Connect DGND and DVDD to the power planes of the system's digital logic. Best results are obtained by completely separating DGND and GND planes and separating DVDD and VDD. A low threshold schottky diode placed locally between DVDD and VDD can prevent damage to the XRD6414 when DVDD and VDD are separate supplies.

2. Keep high frequency decoupling capacitors very close to the A/D pins and minimize the loop area included so less flux will induce less noise. Use decoupling capacitors in the same locations as on the XRD6414AB.

3. Coupling between logic signals and analog circuitry can easily change a 10-bit system into an 8-bit system or worse. Completely separate them. Watch for coupling opportunities from other sources not immediately associated with the A/D. Don't use switching power supplies in adjacent locations, for example.

4. The DC and AC performance of the XRD6414 is optimized with rise and fall times of CLK edges limited to greater than or equal to 7ns. A resistor in series with the CLK input pin can combine with parasitic capacitance to limit rise and fall times. Select a low jitter clock with a 50% duty cycle for best spectral results.

5. Use support devices equivalent to those used on the evaluation board. Use the application board to verify these devices up front, i.e. use very linear passive components in the signal path.

6. Select a driving op amp whose noise, speed, and linearity fits the application. Use a resistor to decouple the output of the driving op amp from the switching input capacitance of the XRD6414.

7. DNL and INL performance is optimized when the VRB input of the XRD6414 is buffered. If VRB is connected to the PCB ground plane it is subject to the noise and ground bounce in that plane.

8. Use 50 or 100 Ω resistors to isolate the XRD6414 digital output pins from a latch or bus connection. This protects the output drivers and reduces the effects of high speed switching logic signals from degrading the ADC performance. Layout the latch or digital buffers as close to the ADC as possible to minimize trace length.

9. Placing a capacitor (such as C34 $\geq$ 15pF) on the output of the MUX will cause a degradation in SNR and SNDR due to the phase shift induced by the varying R_{ON} of the MUX. When using the MUX, make the terminating resistance at the output of the MUX >> R_{ON} (such as R31 or the high impedance input of an opamp) of the MUX. If this condition is not maintained, then R_{ON} will vary to a greater degree.

10. When the MUX is not directly driving the ADC input, the SNR and SNDR of the ADC are optimized with a capacitor at the ADC input such as C34 = 100pF. SNR and DNL are optimized by setting DVDD = 3.3V using a separate power supply whether VDD = 5V or 3.3V.

PCB LAYOUT

A set of drawings showing the details of the electrical circuit and board layout for the 32 QFP package is shown in *Figures 31 through 36.*

Qty	Value	Ref Designators
19	Test Point	TP0-9, TP10, TP14, TP15, TP16, TP FF CLK/2, TP VIN, TP XPLOT, TP AOUT
14	0.01µF	C1, C7, C10, C13, C19, C22, C30, CA1, CA2, CD, CD1, CD2, CB, C6
19	0.1µF	C2, C5, C8, C11, C14, C16, C20, C23, C25, C26, C27, C28, C31, CA, CB1, CB2, CE, CE1, CE2
16	10µF	C3, C9, C12, C15, C21, C24, C32, CC, CC1, CC2, CF, CF1, CF2, C36, C35, C4
5	1KΩ	R4, R6, R7, R8, R10
1	510Ω	R9, R14
2	10KΩ	R3
1	2KΩ	R11
1	4KΩ	R12
26	50Ω	R1, R2, R5, R13, R15, R16, R17, R18, R19, R20, R21, R22, R23, R24, R25, R26, R27, R28, R36, R37, R38, R39, R32, R33, R34, R35
1	74HC04	U7
1	74HC74	U6
2	74HC174	U4, U5
2	AD843	U2, U3
1	AD847	U1
9	3JUMPER	JP1, JP2, JP4, JP21, JP22, JP23, JP24, JP15, JP16
13	JUMPER	JP5, JP7, JP8, JP9, JP11, JP12, JP13, JP14, JP17, JP18, JP19, JP20
4	Schottky Diodes	D1, D2, D3, D4
1	XRD6414 or XRD6415	DUT
2	Short	R29, R40
4	Open	C33, R30, R31, C34
2	Header Connectors	Power, Data
16	SMB	-REF, +REF, DELTA V, VIN, V DITHER, CLK, LCLK, AIN4, AIN3, AIN2 AIN1, DVIN, A1, A0, PD, XOE
1	DUT Socket	32 QFP
1	PCB	EXAR Corporation XRD6414 32 QFP

Table 3. List of Components

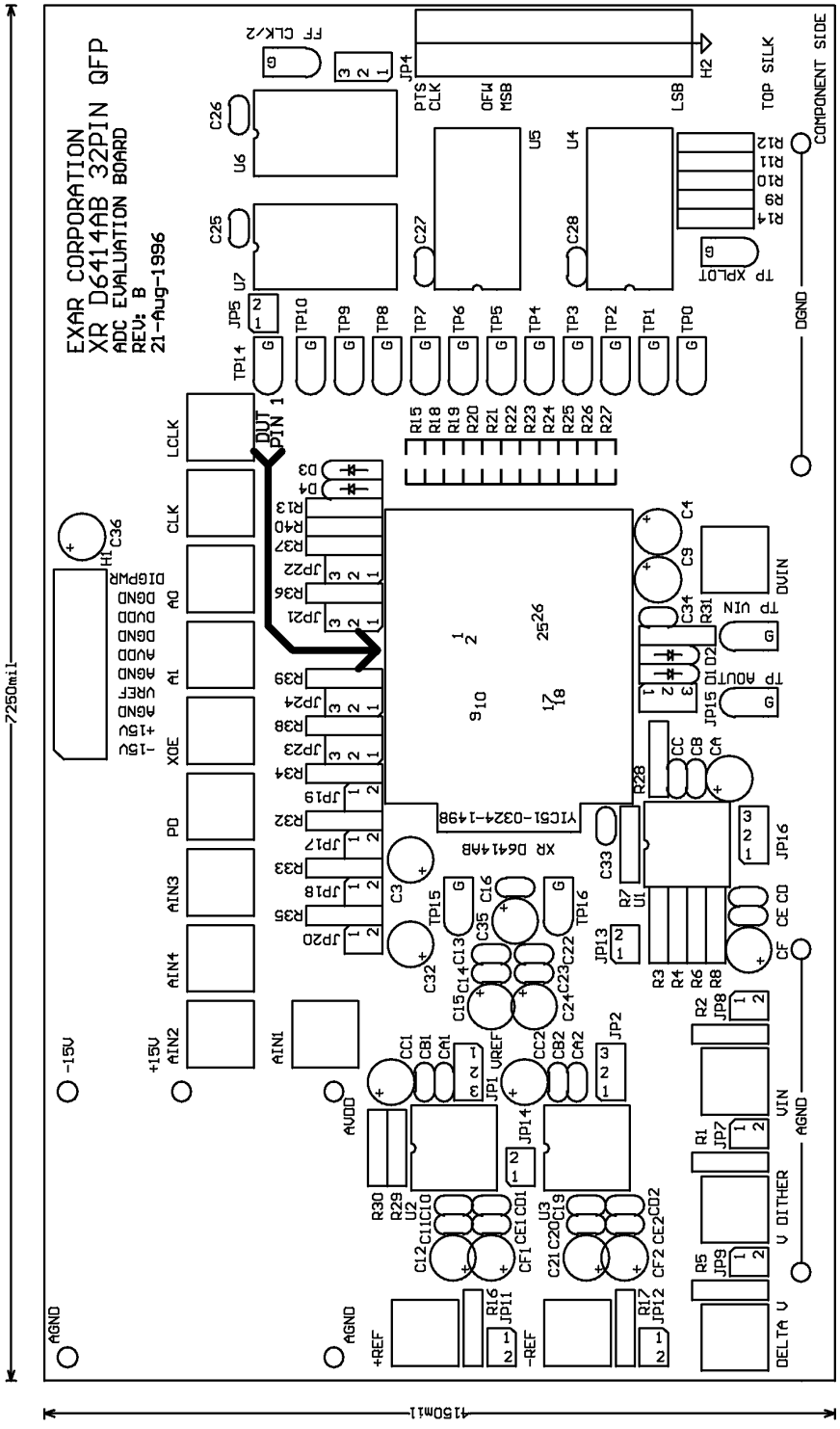

Figure 31. Top Silk

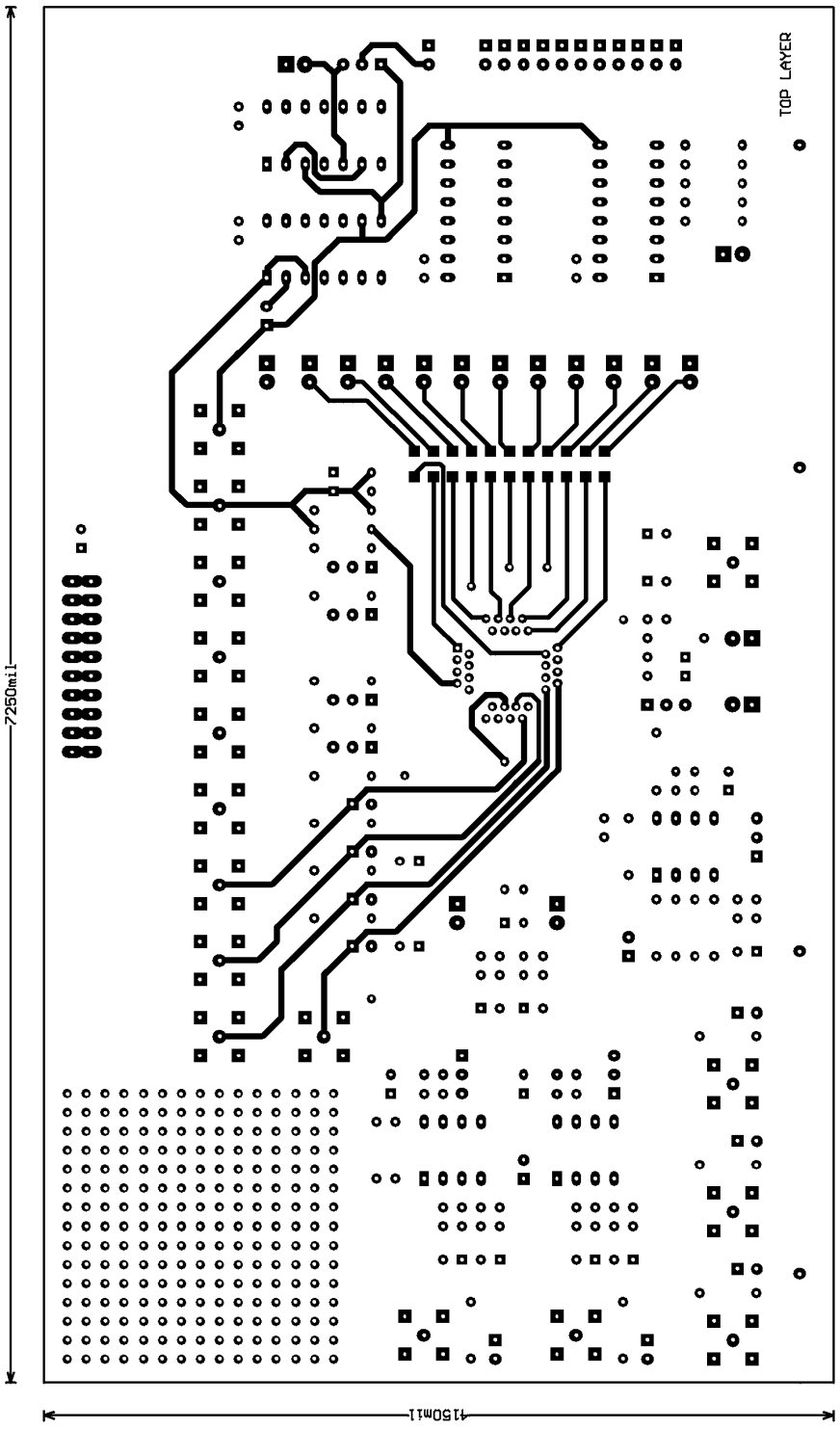

Figure 32. Top Trace

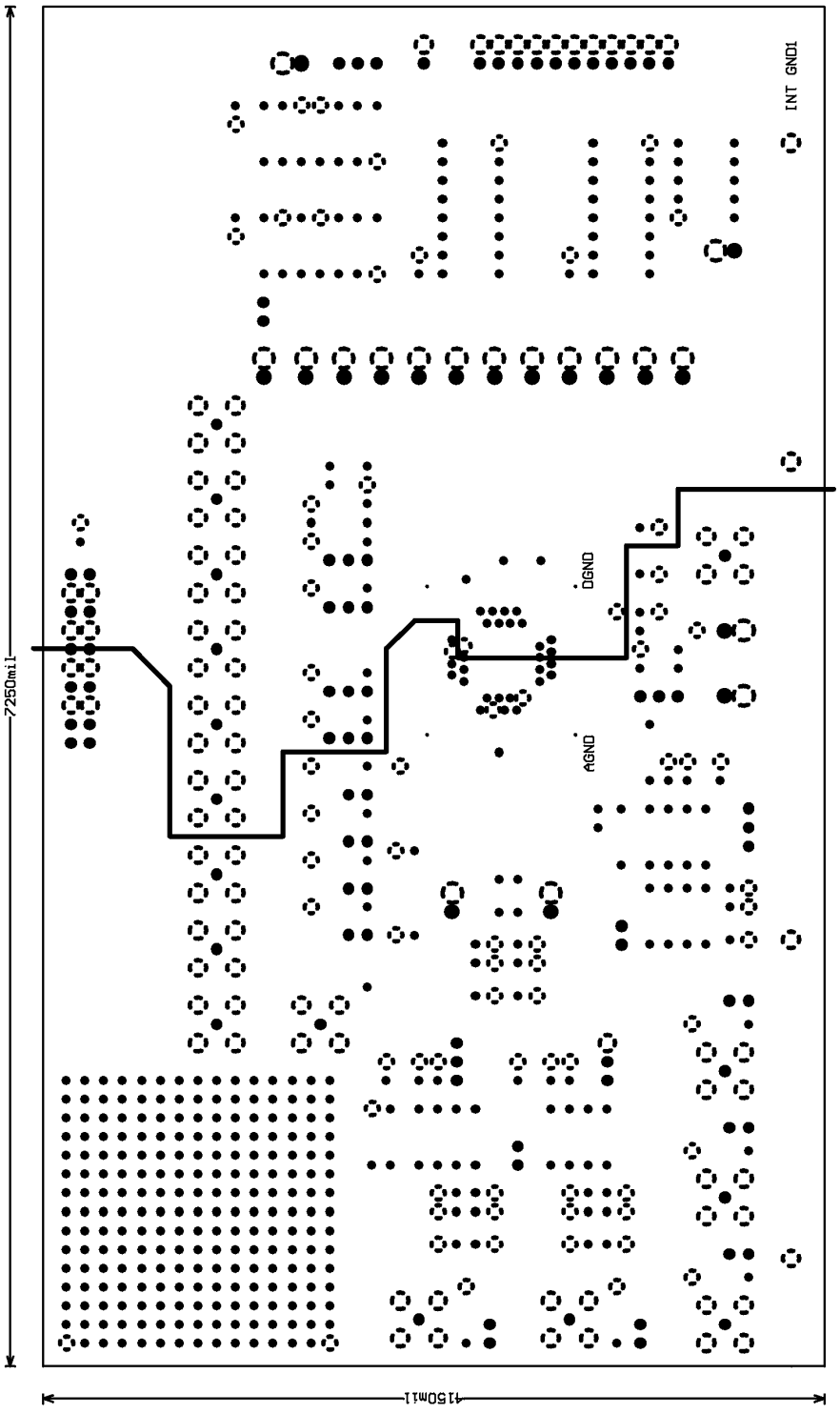

Figure 33. Ground Plane

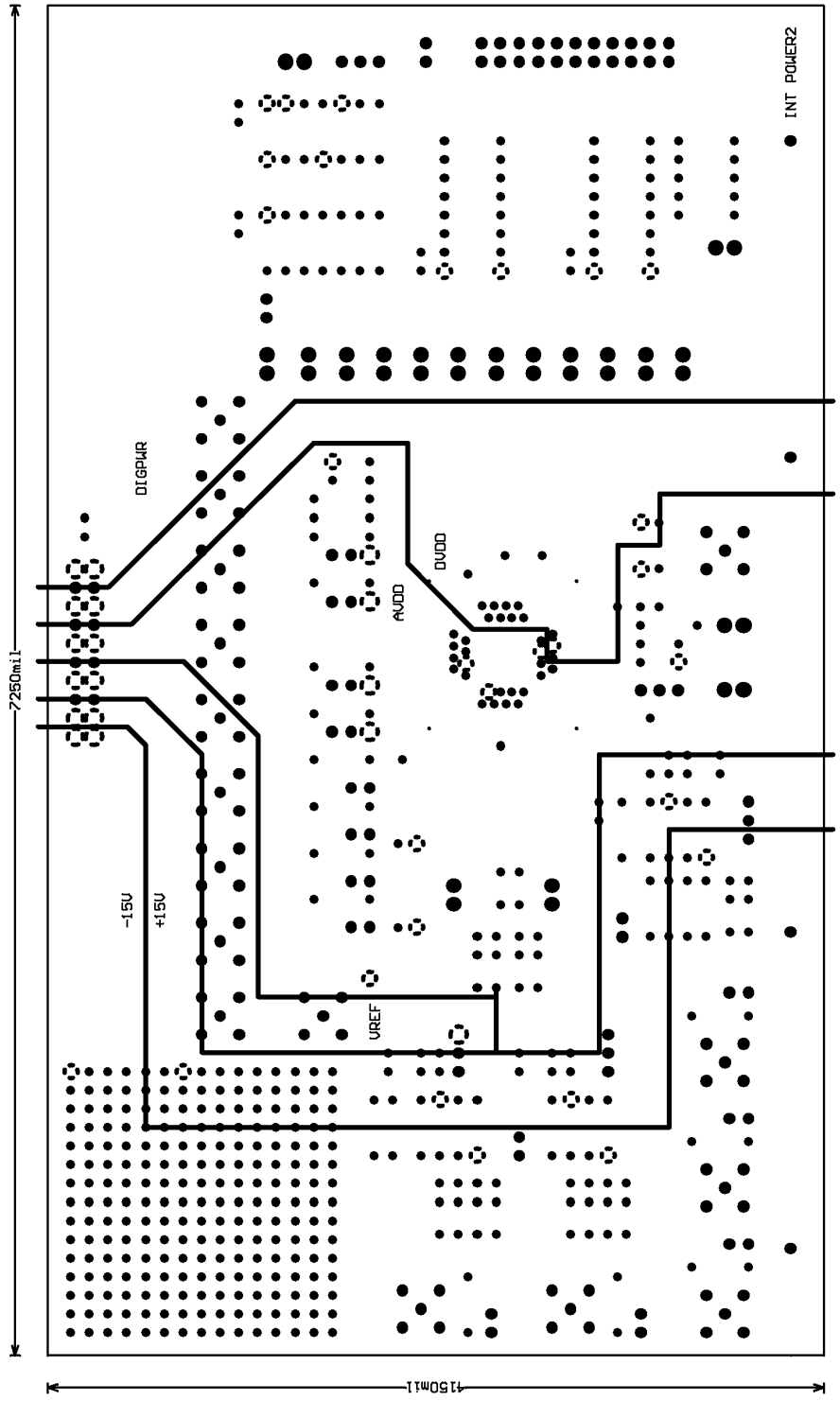

Figure 34. Power Plane

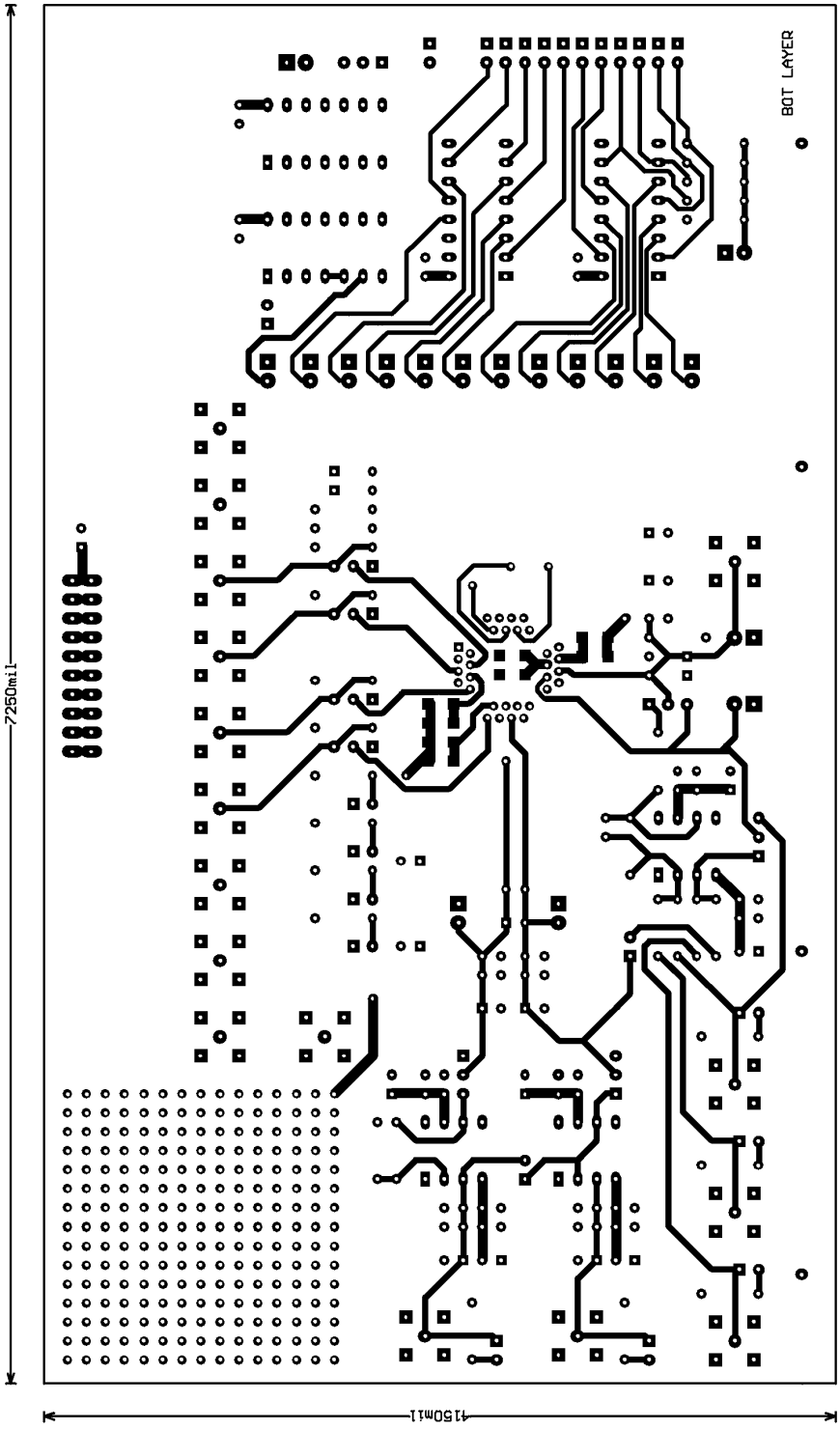

Figure 35. Bottom Trace

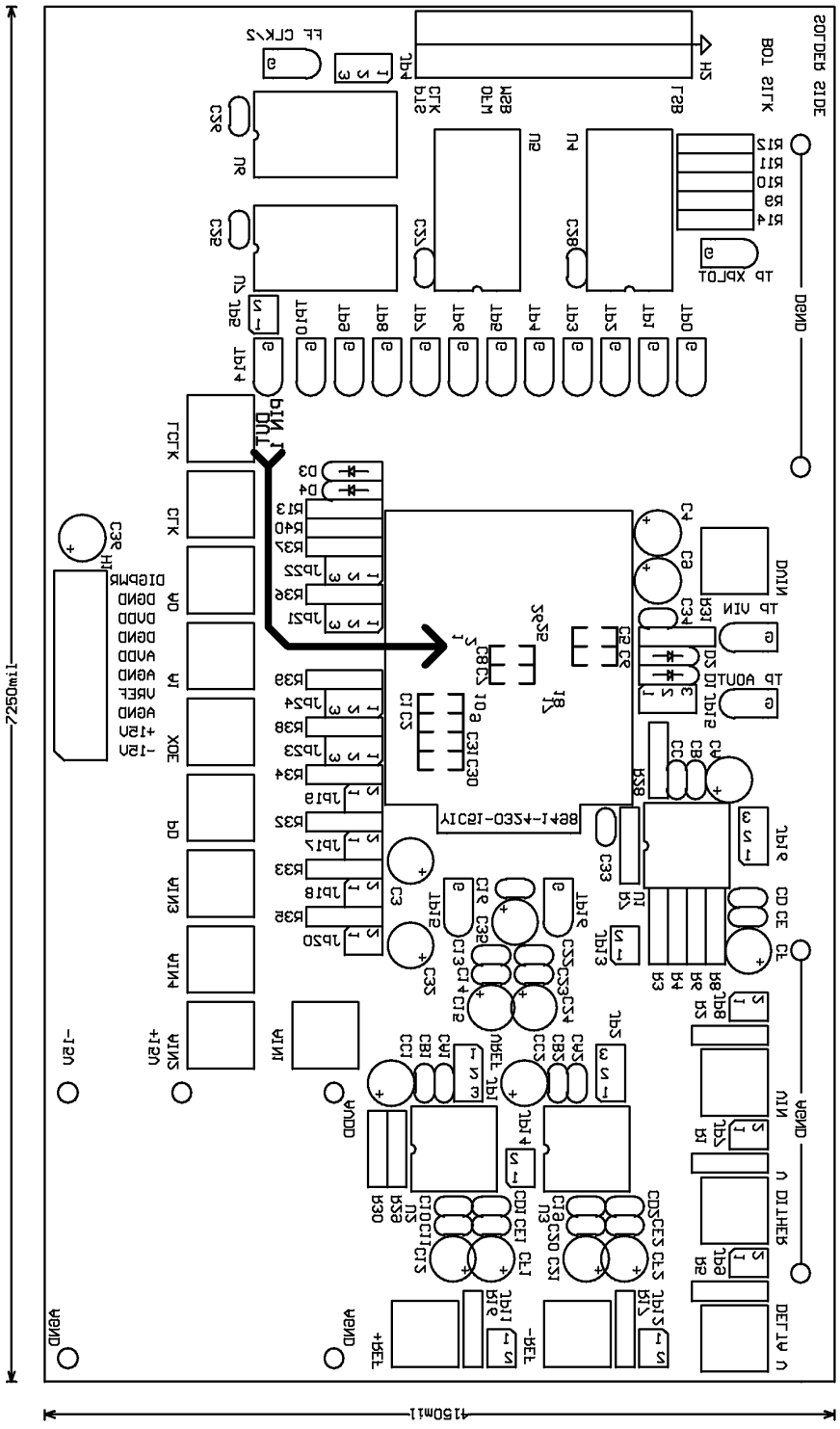

Figure 36. Bottom Silk

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