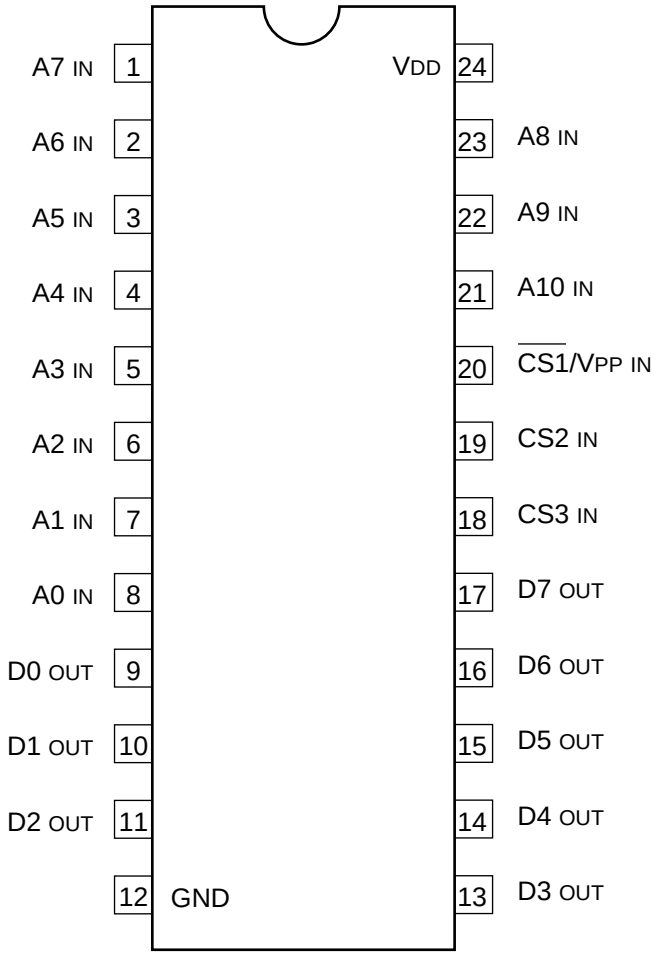
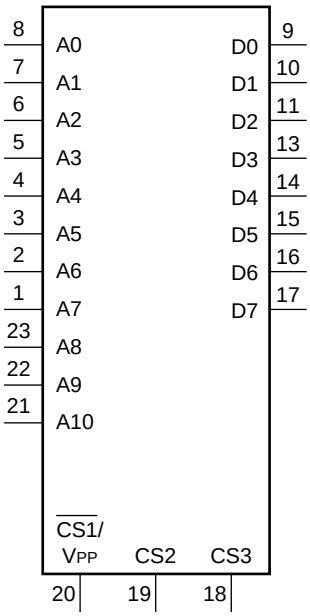
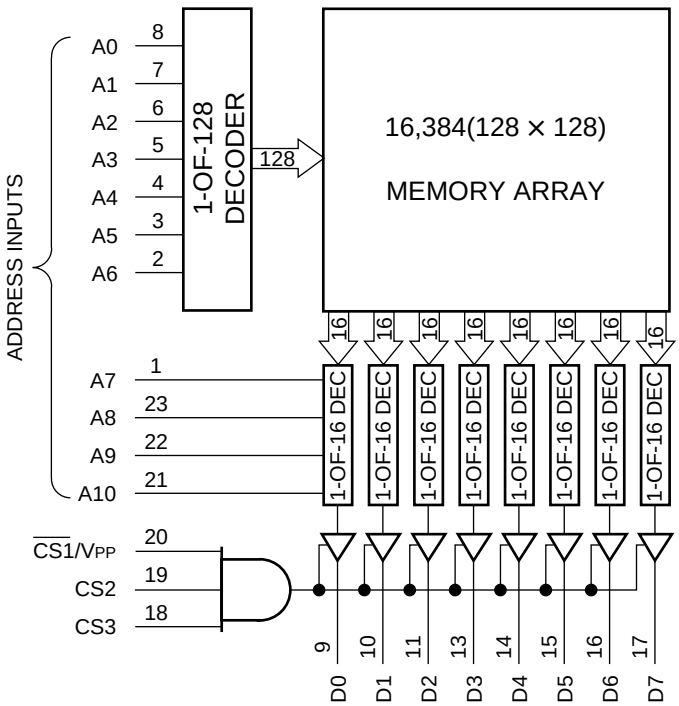
C-MOS 16 K-BIT (2,048 × 8) HIGH SPEED ERASABLE P-ROM

—TOP VIEW—





A0 - A12 ; ADDRESS INPUTS
D0 - D7 ; DATA OUTPUTS
$\overline{CS1}$ - CS3 ; CHIP SELECT INPUT
VPP ; PROGRAM POWER SUPPLY



CHIP SEL			OUTPUT
$\overline{CS1}$/VPP	CS2	CS3	
0	1	1	ENABLE
1	0	×	HI-IMPEDANCE
1	×	0	

0 ; LOW LEVEL
1 ; HIGH LEVEL
× ; DON'T CARE