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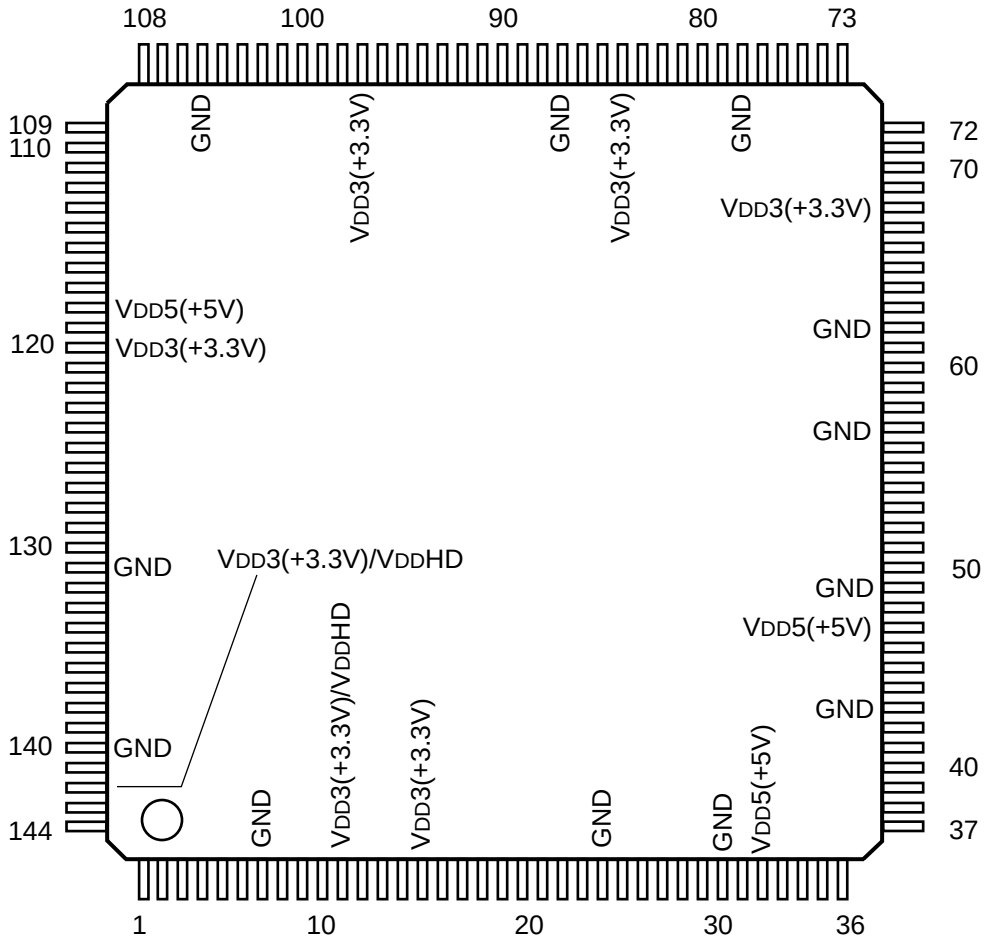
IL16

C-MOS ADDRESS,DATA,HARD DISK BUFFERS AND POWER MANAGEMENT DEVICE

-TOP VIEW-



ADDRESS BUFFER FUNCTION, MIXED MODE APPLICATION

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	O	PMCR8	37	I/O	SA11	73	I	$\overline{\text{XRSMRQ1}}$	109	I/O	A21
2	O	PMCR10	38	I/O	SA12	74	I	$\overline{\text{XRSMRQ2}}$	110	I/O	A22
3	O	PMCR11	39	I/O	SA13	75	I	$\overline{\text{XRSMRQ3}}$	111	I/O	A23
4	O	PMCR14	40	I/O	SA14	76	I	$\overline{\text{RSTSW}}$	112	I/O	$\overline{\text{BHE}}$
5	I	ALE	41	I/O	SA15	77	I	$\overline{\text{READY}}$	113	I/O	MS120
6	I	WE	42	I/O	SA16	78	-	GND	114	I	$\overline{\text{SUSPBLK}}$
7	-	GND	43	-	GND	79	I	$\overline{\text{SUSPSW}}$	115	I	$\overline{\text{RSMBLK}}$
8	O	$\overline{\text{LCDEN}}$	44	O	SA17	80	I	$\overline{\text{RSMSW}}$	116	I	$\overline{\text{MINISUS}}$
9	O	BLEN	45	O	SA18	81	I	MXCTL0	117	I	P5VPGD
10	O	LCL ACK/	46	O	SA19	82	I	MXCTL1	118	-	$V_{DD}5$
11	-	$V_{DD}3$	47	-	$V_{DD}5$	83	I	MXCTL2	119	I	RAD0
12	O	PMCR9	48	I/O	$\overline{\text{SBHE}}$	84	-	$V_{DD}3$	120	-	$V_{DD}3$
13	O	IDEON/PMCR12	49	-	GND	85	I	DACKEN	121	I	RAD1
14	O	$\overline{\text{RSTIDE}}$	50	O	RESET	86	O	RESIN	122	I	RAD2
15	-	$V_{DD}3$	51	I/O	LA17	87	-	GND	123	I	RAD3
16	O	$\overline{\text{WE0}}$	52	I/O	LA18	88	I/O	A1	124	I	RAD4
17	O	$\overline{\text{WE1}}$	53	I/O	LA19	89	I/O	A2	125	I	RAD5
18	O	$\overline{\text{WE2}}$	54	I/O	LA21	90	I/O	A3	126	I	RAD6
19	O	$\overline{\text{WE3}}$	55	I/O	LA22	91	I/O	A4	127	I	RAD7
20	O	PMCR13	56	I/O	LA23	92	I/O	A5	128	I	PCUW0
21	O	PMCR15	57	-	GND	93	I/O	A6	129	I	PCUW1
22	O	PROCPDN	58	I	SA0	94	I/O	A7	130	I	$\overline{\text{TURBO}}$
23	O	$\overline{\text{RESIN}}$	59	I	$\overline{\text{MASTER}}$	95	I/O	A8	131	-	GND
24	-	GND	60	I	AEN	96	I/O	A9	132	I	PROCPGD
25	I/O	SA1	61	I	$\overline{\text{REFRESH}}$	97	-	$V_{DD}3$	133	I	LCL REQ
26	I/O	SA2	62	-	GND	98	I/O	A10	134	I	PMCIN4
27	I/O	SA3	63	I/O	SA2LV	99	I/O	A11	135	I	PMCIN6
28	I/O	SA4	64	I	$\overline{\text{LOWPREQ}}$	100	I/O	A12	136	I	PMCIN7
29	I/O	SA5	65	O	PMCINMX	101	I/O	A13	137	I	LOWPWR
30	-	GND	66	O	$\overline{\text{CSPORTZ}}$	102	I/O	A14	138	O	$\overline{\text{RESUME}}$
31	I/O	SA6	67	I/O	$\overline{\text{CSBASE}}$	103	I/O	A15	139	O	$\overline{\text{FIXCS}}$
32	-	$V_{DD}5$	68	-	$V_{DD}3$	104	I/O	A16	140	-	GND
33	I/O	SA7	69	I	BATPWR	105	-	GND	141	I	$\overline{\text{FSAD}}$
34	I/O	SA8	70	I	$\overline{\text{BATLO2}}$	106	I/O	A17	142	-	$V_{DD}3$
35	I/O	SA9	71	O	FULLPDN	107	I/O	A18	143	O	PMCR4
36	I/O	SA10	72	I	$\overline{\text{XSUSPRQ}}$	108	I/O	A19	144	O	PMCR6

DATA BUFFER FUNCTION, MIXED MODE APPLICATION

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	I/O	HD3	37	I/O	SD10	73	I	$\overline{DEN0}$	109	I/O	PA3
2	I/O	HD4	38	I/O	SD11	74	I	$\overline{DEN1}$	110	I/O	PA4
3	I/O	HD5	39	I/O	SD12	75	I	$\overline{SDEN}$	111	I/O	PA5
4	I/O	HD6	40	I/O	SD13	76	I	$\overline{RESIN}$	112	I/O	PA6
5	I/O	HD8	41	I/O	SD14	77	I	SDTR	113	I/O	PA7
6	I/O	HD9	42	I/O	SD15	78	-	GND	114	I	PZ0
7	-	GND	43	-	GND	79	I	$\overline{IDEDENL}$	115	I	PZ1
8	I/O	HD10	44	O	$\overline{DACK1}$	80	I	$\overline{IDEDENH}$	116	I	PZ2
9	I/O	HD11	45	O	$\overline{DACK2}$	81	I	MXCTL0	117	I	PZ3
10	I/O	HD12	46	O	$\overline{DACK3}$	82	I	MXCTL1	118	-	$V_{DD}5$
11	-	$V_{DD}HD$	47	-	$V_{DD}5$	83	I	MXCTL2	119	I/O	PB0
12	I/O	HD13	48	I	DRQ3	84	-	$V_{DD}3$	120	-	$V_{DD}3$
13	I/O	HD14	49	-	GND	85	I	DACKEN	121	I/O	PB1
14	I/O	HD15	50	O	$\overline{SMEMW}$	86	I	DTR	122	I/O	PB2
15	-	$V_{DD}5$	51	I	DRQ0	87	-	GND	123	I/O	PB3
16	O	$\overline{DACK0}$	52	I	DRQ1	88	I/O	D0	124	I/O	PB4
17	O	$\overline{DACK5}$	53	I	DRQ2	89	I/O	D1	125	I/O	PB5
18	O	$\overline{DACK6}$	54	I	DRQ5	90	I/O	D2	126	I/O	PB6
19	O	$\overline{DACK7}$	55	I	DRQ6	91	I/O	D3	127	I/O	PB7
20	I	SA0	56	I	DRQ7	92	I/O	D4	128	I/O	PC0
21	I	SA1	57	-	GND	93	I/O	D5	129	I/O	PC1
22	I	SA2	58	I	$\overline{IOR}$	94	I/O	D6	130	I/O	PC2
23	O	$\overline{SMEMR}$	59	I	$\overline{IOW}$	95	I/O	D7	131	-	GND
24	-	GND	60	I	$\overline{MEMR}$	96	I/O	D8	132	I/O	PC3
25	I/O	SD0	61	I	$\overline{MEMW}$	97	-	$V_{DD}3$	133	I/O	PC4
26	I/O	SD1	62	-	GND	98	I/O	D9	134	I/O	PC5
27	I/O	SD2	63	I/O	$\overline{IORLV}$	99	I/O	D10	135	I/O	PC6
28	I/O	SD3	64	O	$\overline{IOWLV}$	100	I/O	D11	136	I/O	PC7
29	I/O	SD4	65	O	DRQIN	101	I/O	D12	137	I/O	PY0
30	-	GND	66	I	$\overline{CSPORTZ}$	102	I/O	D13	138	I	$\overline{IDEON}$
31	I/O	SD5	67	I	$\overline{CSBASE}$	103	I/O	D14	139	I	PROCPDN
32	-	$V_{DD}5$	68	-	$V_{DD}3$	104	I/O	D15	140	-	GND
33	I/O	SD6	69	O	SDLV2	105	-	GND	141	I/O	HD0
34	I/O	SD7	70	I/O	SDLV3	106	I/O	PA0	142	-	$V_{DD}HD$
35	I/O	SD8	71	I	FULLPDN	107	I/O	PA1	143	I/O	HD1
36	I/O	SD9	72	I	$\overline{LOWMEG}$	108	I/O	PA2	144	I/O	HD2

ADDRESS BUFFER FUNCTION, MIXED MODE APPLICATION

INPUT

AEN	; ADDRESS ENABLE
ALE	; ADDRESS LATCH ENABLE
$\overline{\text{BATLO2}}$	; BATTERY POWER LOW
BATPWR	; BATTERY POWER
DACKEN	; DACK ENABLE
$\overline{\text{FSAD}}$	; FULL STRENGTH ADDRESS BUFFER CONTROL
LCL REQ	; LOCAL ACCESS REQUEST
$\overline{\text{LOWPREQ}}$	; LOW POWER REQUEST
LOWPWR	; LOW POWER
$\overline{\text{MASTER}}$	; MASTER
$\overline{\text{MINISUS}}$	; MINI SUSPEND
MXCTL0-MXCTL2	; MULTIPLEXER CONTROL 0 - 2
P5VPGD	; POWER TO 5V POWER GOOD
PCUW0, PCUW1	; POWER CONTROL UNIT WRITE STROBE 0, 1
PMCIN4, PMCIN6, PMCIN7	; POWER MANAGEMENT CONTROL INPUTS 4, 6, 7
PROCPGD	; PROCESSOR POWER GOOD
RAD0-PAD7	; RAM ADDRESS BUS
$\overline{\text{READY}}$	; READY
$\overline{\text{REFRESH}}$	; REFRESH
$\overline{\text{RSMBLK}}$	; RESUME REQUEST CIRCUIT BLOCK
$\overline{\text{RSMSW}}$	; RESUME SWITCH
$\overline{\text{RSTSW}}$	; RESET SWITCH
SA0	; SYSTEM ADDRESS 0
$\overline{\text{SUSPBLK}}$	; SUSPEND REQUEST CIRCUIT BLOCK
$\overline{\text{SUSPSW}}$	; SUSPEND SWITCH
$\overline{\text{TURBO}}$	; TURBO
WE	; WRITE ENABLE
$\overline{\text{XSUSPRQ}}$	; EXTERNAL SUSPEND REQUEST
$\overline{\text{XRSMRQ1}}$-$\overline{\text{XRSMRQ3}}$	; EXTERNAL RESUME REQUEST 1 - 3

INPUT/OUTPUT

A1-A19, A21-A23	; CPU ADDRESS
$\overline{\text{BHE}}$	; BUS HIGH ENABLE
$\overline{\text{CSBASE}}$	; CHIP SELECT BASE
LA17-LA19, LA21-LA23	; EARLY ADDRESS
MS120	; 120 MILLISECOND WATCHDOG TIMER STROBE
SA1-SA16	; SYSTEM ADDRESS
SA2LV	; SYSTEM ADDRESS 2 LOW VOLTAGE
$\overline{\text{SBHE}}$	; SYSTEM BUS HIGH ENABLE

ADDRESS BUFFER FUNCTION, MIXED MODE APPLICATION

OUTPUT

BLEN	; POWER MANAGEMENT CONTROL REGISTER
$\overline{\text{CSPORTZ}}$	; CHIP SELECT PORT Z
$\overline{\text{FIXCS}}$	; EXTERNAL CHIP SELECT
FULLPDN	; POWER MANAGEMENT CONTROL REGISTER
IDEON/	; POWER MANAGEMENT CONTROL REGISTER
$\overline{\text{LCDEN}}$	; POWER MANAGEMENT CONTROL REGISTER
LCL ACK/	; POWER MANAGEMENT CONTROL REGISTER
PMCINMX	; POWER MANAGEMENT CONTROL INPUT MULTIPLEXED
PMCR4,6,8-15	; POWER MANAGEMENT CONTROL REGISTER
PROCPDN	; POWER MANAGEMENT CONTROL REGISTER
RESET	; RESET DRIVE
$\overline{\text{RESIN}}$, RESIN	; SYSTEM RESET
$\overline{\text{RESUME}}$	; RESUME
$\overline{\text{RSTIDE}}$	; RESET IDE
SA17-19	; SYSTEM ADDRESS
$\overline{\text{WE0}}$-$\overline{\text{WE3}}$	; WRITE ENABLE

DATA BUFFER FUNCTION, MIXED MODE APPLICATION

INPUT

$\overline{\text{CSPORTZ}}$; CHIP SELECT PORT Z
$\overline{\text{CSBASE}}$; CHIP SELECT BASE
DACKEN ; DACK ENABLE
$\overline{\text{DEN0, 1}}$; DATA BUS ENABLE
DRQ0-3, 5-7 ; DMA REQUESTS
DTR ; DIRECTION CONTROL
$\overline{\text{FULLPDN}}$; FULL POWER DOWN
$\overline{\text{IDEDENH}}$; IDE HIGH BYTE ENABLE
$\overline{\text{IDEDENL}}$; IDE LOW BYTE ENABLE
$\overline{\text{IDEON}}$; IDE POWER ON
$\overline{\text{IOR}}$; I/O READ
$\overline{\text{IOW}}$; I/O WRITE
$\overline{\text{LOWMEG}}$; FIRST MEGABYTE
$\overline{\text{MEMR}}$; MEMORY READ
$\overline{\text{MEMW}}$; MEMORY WRITE
MXCTL0-2 ; MULTIPLEXER CONTROL
PROCPDN ; PROCESSOR POWER DOWN
PZ0-3 ; REGISTER Z
$\overline{\text{RESIN}}$; RESET INPUT
SA0-2 ; SYSTEM ADDRESS
$\overline{\text{SDEN}}$; SWAP DATA ENABLE
SDTR ; SWAP DIRECTION

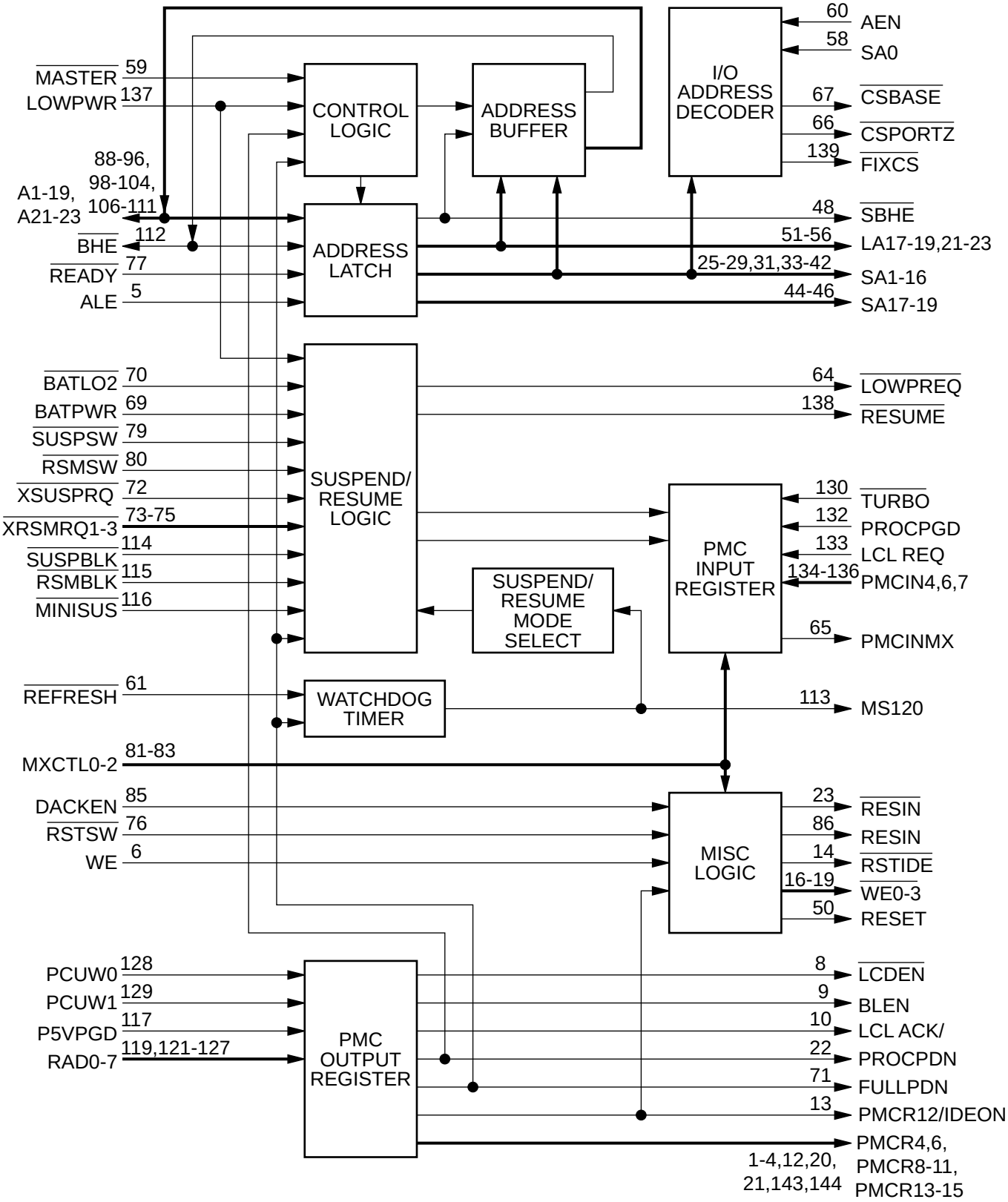
INPUT/OUTPUT

D0-15 ; DATA BUS
$\overline{\text{IORLV}}$; I/O READ LOW VOLTAGE
HD0-6, 8-15 ; HARD DISK DATA BUS
PA0-7 ; GENERAL PURPOSE PORT A
PB0-7 ; GENERAL PURPOSE PORT B
PC0-7 ; GENERAL PURPOSE PORT C
PY0 ; REGISTER Y0
SD0-15 ; SYSTEM DATA BUS
SDLV3 ; LOW VOLTAGE SD3

OUTPUT

$\overline{\text{DACK0-3, 5-7}}$; DACK
DRQIN ; MULTIPLEXED DRQ
$\overline{\text{IOWLV}}$; I/O WRITE LOW VOLTAGE
SDLV2 ; LOW VOLTAGE SD2
$\overline{\text{SMEMR}}$; SYSTEM MEMORY READ
$\overline{\text{SMEMW}}$; SYSTEM MEMORY WRITE

ADDRESS BUFFER FUNCTION, MIXED MODE APPLICATION



DATA BUFFER FUNCTION, MIXED MODE APPLICATION