12.0 SPECIFICATIONS

12.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage	-0.5 to 7.0	V
Input Voltage	-0.5 to V_{DD}+0.5	V
Battery Voltage V_{BAT}	4.0 to 1.8	V
Operating Temperature	0 to +70	° C
Storage Temperature	-55 to +150	° C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

12.2 DC CHARACTERISTICS

(Ta = 0° C to 70° C, V_{DD} = 5V ± 10%, V_{SS} = 0V)

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Battery Quiescent Current	I_{BAT}			2.4	uA	V_{BAT} = 2.5 V
Stand-by Power Supply Quiescent Current	I_{BAT}			2.0	mA	V_{SB} = 5.0 V, All ACPI pins are not connected.
I/O_{8t} - TTL level bi-directional pin with source-sink capability of 8 mA						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = - 8 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = V_{DD}
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/O_{6t} - TTL level bi-directional pin with source-sink capability of 6 mA						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 6 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = - 6 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = V_{DD}
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V

12.2 DC CHARACTERISTICS, continued

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I/O_8 - CMOS level bi-directional pin with source-sink capability of 8 mA						
Input Low Voltage	V_{IL}			0.3 x V_{DD}	V	
Input High Voltage	V_{IH}	0.7 x V_{DD}			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	3.5			V	I_{OH} = -8 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = V_{DD}
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/O_{12} - CMOS level bi-directional pin with source-sink capability of 12 mA						
Input Low Voltage	V_{IL}			0.3 x V_{DD}	V	
Input High Voltage	V_{IH}	0.7 x V_{DD}			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	3.5			V	I_{OH} = -12 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = V_{DD}
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/O_{16u} - CMOS level bi-directional pin with source-sink capability of 16 mA, with internal pull-up resistor						
Input Low Voltage	V_{IL}			0.3 x V_{DD}	V	
Input High Voltage	V_{IH}	0.7 x V_{DD}			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 16 mA
Output High Voltage	V_{OH}	3.5			V	I_{OH} = -16 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = V_{DD}
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/OD_{16u} - CMOS level Open-Drain pin with source-sink capability of 16 mA, with internal pull-up resistor						
Input Low Voltage	V_{IL}			0.3xV_{DD}	V	
Input High Voltage	V_{IH}	0.7xV_{DD}			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 16 mA
Output High Voltage	V_{OH}	3.5			V	I_{OH} = -16 mA
Input High Leakage	I_{LIH}			+ 10	µA	V_{IN} = V_{DD}
Input Low Leakage	I_{LIL}			- 10	µA	V_{IN} = 0V

12.2 DC CHARACTERISTICS, continued

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I/O_{12t} - TTL level bi-directional pin with source-sink capability of 12 mA						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = V_{DD}
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/O_{24t} - TTL level bi-directional pin with source-sink capability of 24 mA						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = - 24 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = V_{DD}
Input Low Leakage	I_{LIL}			- 10	µA	V_{IN} = 0V
OUT_{8t} - TTL level output pin with source-sink capability of 8 mA						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -8 mA
OUT_{12t} - TTL level output pin with source-sink capability of 12 mA						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
OD_{12} - Open-drain output pin with sink capability of 12 mA						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
OD_{24} - Open-drain output pin with sink capability of 24 mA						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
IN_t - TTL level input pin						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = V_{DD}
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V

12.2 DC CHARACTERISTICS, continued

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
IN_C - CMOS level input pin						
Input Low Voltage	V_{IL}			$0.3 \times V_{DD}$	V	
Input High Voltage	V_{IH}	$0.7 \times V_{DD}$			V	
Input High Leakage	I_{LIH}			+10	μA	$V_{IN} = V_{DD}$
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{CS} - CMOS level Schmitt-triggered input pin						
Input Low Threshold Voltage	V_{t-}	1.3	1.5	1.7	V	V_{DD} = 5 V
Input High Threshold Voltage	V_{t+}	3.2	3.5	3.8	V	V_{DD} = 5 V
Hystersis	V_{TH}	1.5	2		V	V_{DD} = 5 V
Input High Leakage	I_{LIH}			+10	μA	$V_{IN} = V_{DD}$
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{CU} - CMOS level input pin with internal pull-up resistor						
Input Low Voltage	V_{IL}			0.7 x V_{DD}	V	
Input High Voltage	V_{IH}	0.7 x V_{DD}			V	
Input High Leakage	I_{LIH}			+10	μA	$V_{IN} = V_{DD}$
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{TS} - TTL level Schmitt-triggered input pin						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{DD} = 5 V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{DD} = 5 V
Hystersis	V_{TH}	0.5	1.2		V	V_{DD} = 5 V
Input High Leakage	I_{LIH}			+10	μA	$V_{IN} = V_{DD}$
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{TSU} - TTL level Schmitt-triggered input pin with internal pull-up resistor						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{DD} = 5 V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{DD} = 5 V
Hystersis	V_{TH}	0.5	1.2		V	V_{DD} = 5 V
Input High Leakage	I_{LIH}			+10	μA	$V_{IN} = V_{DD}$
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V

12.3 AC Characteristics

12.3.1 FDC: Data rate = 1 MB, 500 KB, 300 KB, 250 KB/sec.

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP. (NOTE 1)	MAX.	UNIT
SA9-SA0, AEN, $\overline{DACK}$, $\overline{CS}$, setup time to $\overline{IOR}$ ¡õ	TAR		25			nS
SA9-SA0, AEN, $\overline{DACK}$, hold time for $\overline{IOR}$ ¡ô	TAR		0			nS
$\overline{IOR}$ width	TRR		80			nS
Data access time from $\overline{IOR}$ ¡õ	TFD	CL = 100 pf			80	nS
Data hold from $\overline{IOR}$ ¡õ	TDH	CL = 100 pf	10			nS
SD to from $\overline{IOR}$ ¡ô	TDF	CL = 100 pf	10		50	nS
IRQ delay from $\overline{IOR}$ ¡ô	TRI				360/570 /675	nS
SA9-SA0, AEN, $\overline{DACK}$, setup time to $\overline{IOW}$ ¡õ	TAW		25			nS
SA9-SA0, AEN, $\overline{DACK}$, hold time for $\overline{IOW}$ ¡ô	TWA		0			nS
$\overline{IOW}$ width	TWW		60			nS
Data setup time to $\overline{IOW}$ ¡ô	TDW		60			nS
Data hold time from $\overline{IOW}$ ¡ô	TWD		0			nS
IRQ delay from $\overline{IOW}$ ¡ô	TWI				360/570 /675	nS
DRQ cycle time	TMCY		27			µS
DRQ delay time $\overline{DACK}$ ¡õ	TAM				50	nS
DRQ to $\overline{DACK}$ delay	TMA		0			nS
$\overline{DACK}$ width	TAA		260/430 /510			nS
$\overline{IOR}$ delay from $\overline{DRQ}$	TMR		0			nS
$\overline{IOW}$ delay from $\overline{DRQ}$	TMW		0			nS

12.3.1 AC Characteristics, FDC continued

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP. (NOTE 1)	MAX.	UNIT
$\overline{IOW}$ or $\overline{IOR}$ response time from DRQ	TMRW			6/12 /20/24		µS
TC width	TTC		135/220 /260			nS
RESET width	TRST		1.8/3/3. 5			µS
$\overline{INDEX}$ width	TIDX		0.5/0.9 /1.0			µS
$\overline{DIR}$ setup time to $\overline{STEP}$	TDST		1.0/1.6 /2.0			µS
$\overline{DIR}$ hold time from $\overline{STEP}$	TSTD		24/40/48			µS
$\overline{STEP}$ pulse width	TSTP		6.8/11.5 /13.8	7/11.7 /14	7.2/11.9 /14.2	µS
$\overline{STEP}$ cycle width	TSC		Note 2	Note 2	Note 2	µS
$\overline{WD}$ pulse width	TWDD		100/185 /225	125/210 /250	150/235 /275	µS
Write precompensation	TWPC		100/138 /225	125/210 /250	150/235 /275	µS

Notes:

1. Typical values for T = 25° C and normal supply voltage.

2. Programmable from 2 mS through 32 mS in 2 mS increments.

12.3.2 UART/Parallel Port

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
Delay from Stop to Set Interrupt	TSINT		9/16		Baud Rate
Delay from $\overline{IOR}$ Reset Interrupt	TRINT	100 pf Loading		1	µS
Delay from Initial IRQ Reset to Transmit Start	TIRS		1/16	8/16	Baud Rate
Delay from $\overline{IOW}$ to Reset interrupt	THR	100 pf Loading		175	nS
Delay from Initial $\overline{IOW}$ to interrupt	TSI		9/16	16/16	Baud Rate
Delay from Stop to Set Interrupt	TSTI			1/2	Baud Rate
Delay from $\overline{IOR}$ to Reset Interrupt	TIR	100 pF Loading		250	nS
Delay from $\overline{IOR}$ to Output	TMWO	100 pF Loading		200	nS
Set Interrupt Delay from Modem Input	TSIM			250	nS
Reset Interrupt Delay from $\overline{IOR}$	TRIM			250	nS
Interrupt Active Delay	TIAD	100 pF Loading		25	nS
Interrupt Inactive Delay	TIID	100 pF Loading		30	nS
Baud Divisor	N	100 pF Loading		2^{16}-1	

12.3.3 Parallel Port Mode Parameters

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT
PD0-7, $\overline{INDEX}$, $\overline{STROBE}$, $\overline{AUTOFD}$ Delay from $\overline{IOW}$	t1			100	nS
IRQ Delay from $\overline{ACK}$, nFAULT	t2			60	nS
IRQ Delay from $\overline{IOW}$	t3			105	nS
IRQ Active Low in ECP and EPP Modes	t4	200		300	nS
$\overline{ERROR}$ Active to IRQ Active	t5			105	nS

12.3.4 EPP Data or Address Read Cycle Timing Parameters

PARAMETER	SYM.	MIN.	MAX.	UNIT
Ax Valid to $\overline{IOR}$ Asserted	t1	40		nS
IOCHRDY Deasserted to $\overline{IOR}$ Deasserted	t2	0		nS
$\overline{IOR}$ Deasserted to Ax Valid	t3	10	10	nS
$\overline{IOR}$ Deasserted to $\overline{IOW}$ or $\overline{IOR}$ Asserted	t4	40		
$\overline{IOR}$ Asserted to IOCHRDY Asserted	t5	0	24	nS
PD Valid to SD Valid	t6	0	75	nS
$\overline{IOR}$ Deasserted to SD Hi-Z (Hold Time)	t7	0	40	µS
SD Valid to IOCHRDY Deasserted	t8	0	85	nS
$\overline{WAIT}$ Deasserted to IOCHRDY Deasserted	t9	60	160	nS
PD Hi-Z to PDBIR Set	t10	0		nS
$\overline{WRITE}$ Deasserted to $\overline{IOR}$ Asserted	t13	0		nS
$\overline{WAIT}$ Asserted to $\overline{WRITE}$ Deasserted	t14	0	185	nS
Deasserted to $\overline{WRITE}$ Modified	t15	60	190	nS
$\overline{IOR}$ Asserted to PD Hi-Z	t16	0	50	nS
$\overline{WAIT}$ Asserted to PD Hi-Z	t17	60	180	nS
Command Asserted to PD Valid	t18	0		nS
Command Deasserted to PD Hi-Z	t19	0		nS
$\overline{WAIT}$ Deasserted to PD Drive	t20	60	190	nS
$\overline{WRITE}$ Deasserted to Command	t21	1		nS
PBDIR Set to Command	t22	0	20	nS
PD Hi-Z to Command Asserted	t23	0	30	nS
Asserted to Command Asserted	t24	0	195	nS
$\overline{WAIT}$ Deasserted to Command Deasserted	t25	60	180	nS
Time out	t26	10	12	nS
PD Valid to $\overline{WAIT}$ Deasserted	t27	0		nS
PD Hi-Z to $\overline{WAIT}$ Deasserted	t28	0		µS

12.3.5 EPP Data or Address Write Cycle Timing Parameters

PARAMETER	SYM.	MIN.	MAX.	UNIT
Ax Valid to $\overline{IOW}$ Asserted	t1	40		nS
SD Valid to Asserted	t2	10		nS
$\overline{IOW}$ Deasserted to Ax Invalid	t3	10		nS
$\overline{WAIT}$ Deasserted to IOCHRDY Deasserted	t4	0		nS
Command Asserted to $\overline{WAIT}$ Deasserted	t5	10		nS
$\overline{IOW}$ Deasserted to $\overline{IOW}$ or $\overline{IOR}$ Asserted	t6	40		nS
IOCHRDY Deasserted to $\overline{IOW}$ Deasserted	t7	0	24	nS
$\overline{WAIT}$ Asserted to Command Asserted	t8	60	160	nS
$\overline{IOW}$ Asserted to $\overline{WAIT}$ Asserted	t9	0	70	nS
PBDIR Low to $\overline{WRITE}$ Asserted	t10	0		nS
$\overline{WAIT}$ Asserted to $\overline{WRITE}$ Asserted	t11	60	185	nS
$\overline{WAIT}$ Asserted to $\overline{WRITE}$ Change	t12	60	185	nS
$\overline{IOW}$ Asserted to PD Valid	t13	0	50	nS
$\overline{WAIT}$ Asserted to PD Invalid	t14	0		nS
PD Invalid to Command Asserted	t15	10		nS
$\overline{IOW}$ to Command Asserted	t16	5	35	nS
$\overline{WAIT}$ Asserted to Command Asserted	t17	60	210	nS
$\overline{WAIT}$ Deasserted to Command Deasserted	t18	60	190	nS
Command Asserted to $\overline{WAIT}$ Deasserted	t19	0	10	µS
Time out	t20	10	12	µS
Command Deasserted to $\overline{WAIT}$ Asserted	t21	0		nS
$\overline{IOW}$ Deasserted to $\overline{WRITE}$ Deasserted and PD invalid	t22	0		nS

12.3.6 Parallel Port FIFO Timing Parameters

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
DATA Valid to nSTROBE Active	t1	600		nS
nSTROBE Active Pulse Width	t2	600		nS
DATA Hold from nSTROBE Inactive	t3	450		nS
BUSY Inactive to PD Inactive	t4	80		nS
BUSY Inactive to nSTROBE Active	t5	680		nS
nSTROBE Active to BUSY Active	t6		500	nS

12.3.7 ECP Parallel Port Forward Timing Parameters

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
nAUTOFD Valid to nSTROBE Asserted	t1	0	60	nS
PD Valid to nSTROBE Asserted	t2	0	60	nS
BUSY Deasserted to nAUTOFD Changed	t3	80	180	nS
BUSY Deasserted to PD Changed	t4	80	180	nS
nSTROBE Deasserted to BUSY Deasserted	t5	0		nS
BUSY Deasserted to nSTROBE Asserted	t6	80	200	nS
nSTROBE Asserted to BUSY Asserted	t7	0		nS
BUSY Asserted to nSTROBE Deasserted	t8	80	180	nS

12.3.8 ECP Parallel Port Reverse Timing Parameters

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
PD Valid to nACK Asserted	t1	0		nS
nAUTOFD Deasserted to PD Changed	t2	0		nS
nAUTOFD Asserted to nACK Asserted	t3	0		nS
nAUTOFD Deasserted to nACK Deasserted	t4	0		nS
nACK Deasserted to nAUTOFD Asserted	t5	80	200	nS
PD Changed to nAUTOFD Deasserted	t6	80	200	nS

12.3.9 KBC Timing Parameters

NO.	DESCRIPTION	MIN.	MAX.	UNIT
T1	Address Setup Time from WRB	0		nS
T2	Address Setup Time from RDB	0		nS
T3	WRB Strobe Width	20		nS
T4	RDB Strobe Width	20		nS
T5	Address Hold Time from WRB	0		nS
T6	Address Hold Time from RDB	0		nS
T7	Data Setup Time	50		nS
T8	Data Hold Time	0		nS
T9	Gate Delay Time from WRB	10	30	nS
T10	RDB to Drive Data Delay		40	nS
T11	RDB to Floating Data Delay	0	20	nS
T12	Data Valid After Clock Falling (SEND)		4	µS
T13	K/B Clock Period	20		µS
T14	K/B Clock Pulse Width	10		µS
T15	Data Valid Before Clock Falling (RECEIVE)	4		µS
T16	K/B ACK After Finish Receiving	20		µS
T17	RC Fast Reset Pulse Delay (8 Mhz)	2	3	µS
T18	RC Pulse Width (8 Mhz)	6		µS
T19	Transmit Timeout		2	mS
T20	Data Valid Hold Time	0		µS
T21	Input Clock Period (6–12 Mhz)	83	167	nS
T22	Duration of CLK inactive	30	50	µS
T23	Duration of CLK active	30	50	µS
T24	Time from inactive CLK transition, used to time when the auxiliary device sample DATA	5	25	µS
T25	Time of inhibit mode	100	300	µS
T26	Time from rising edge of CLK to DATA transition	5	T28-5	µS
T27	Duration of CLK inactive	30	50	µS
T28	Duration of CLK active	30	50	µS
T29	Time from DATA transition to falling edge of CLK	5	25	µS

12.3.10 GPIO Timing Parameters

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{WGO}	Write data to GPIO update		300 (Note 1)	nS

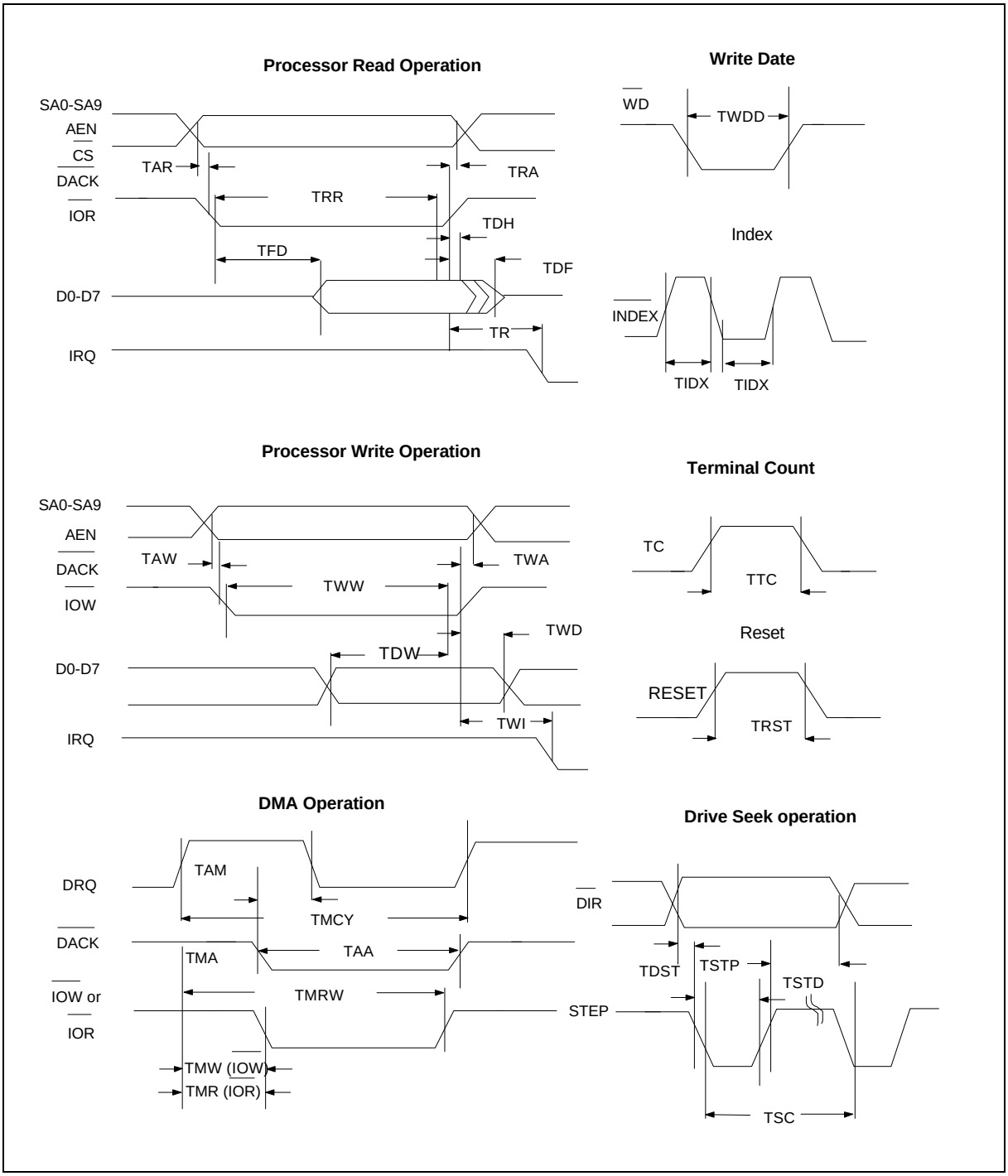
Note : Refer to Microprocessor Interface Timing for Read Timing.

12.3.11 Keyboard/Mouse Timing Parameters

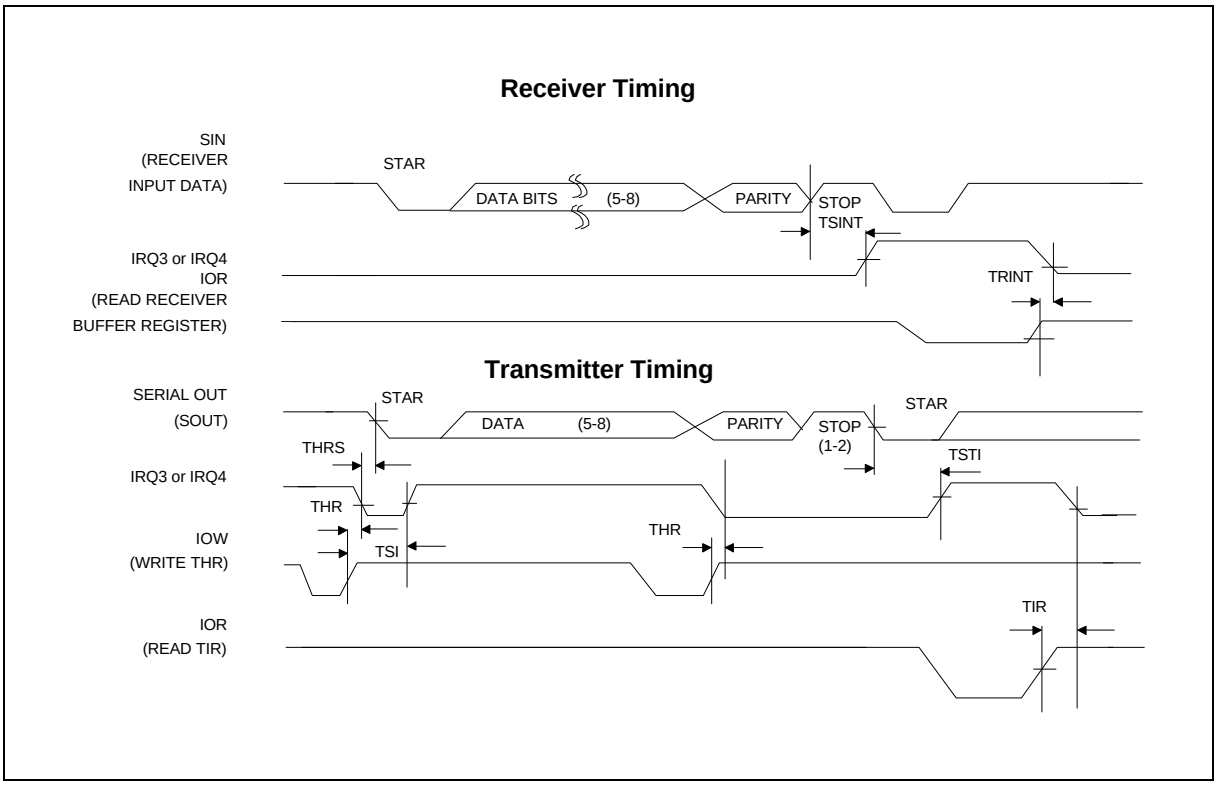
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{SWL}	$\overline{\text{PANSWIN}}$ falling edge to $\overline{\text{PANSWOUT}}$ falling edge		20	nS
t_{SWH}	$\overline{\text{PANSWIN}}$ falling edge to $\overline{\text{PANSWOUT}}$ Hi-Z		50	nS
t_{WKUPD}	KCLK/MCLK falling edge to $\overline{\text{PANSWOUT}}$ falling edge delay		200	nS
t_{WKUPW}	$\overline{\text{PANSWOUT}}$ active pulse width	0.5	1	sec

13.0 TIMING WAVEFORMS

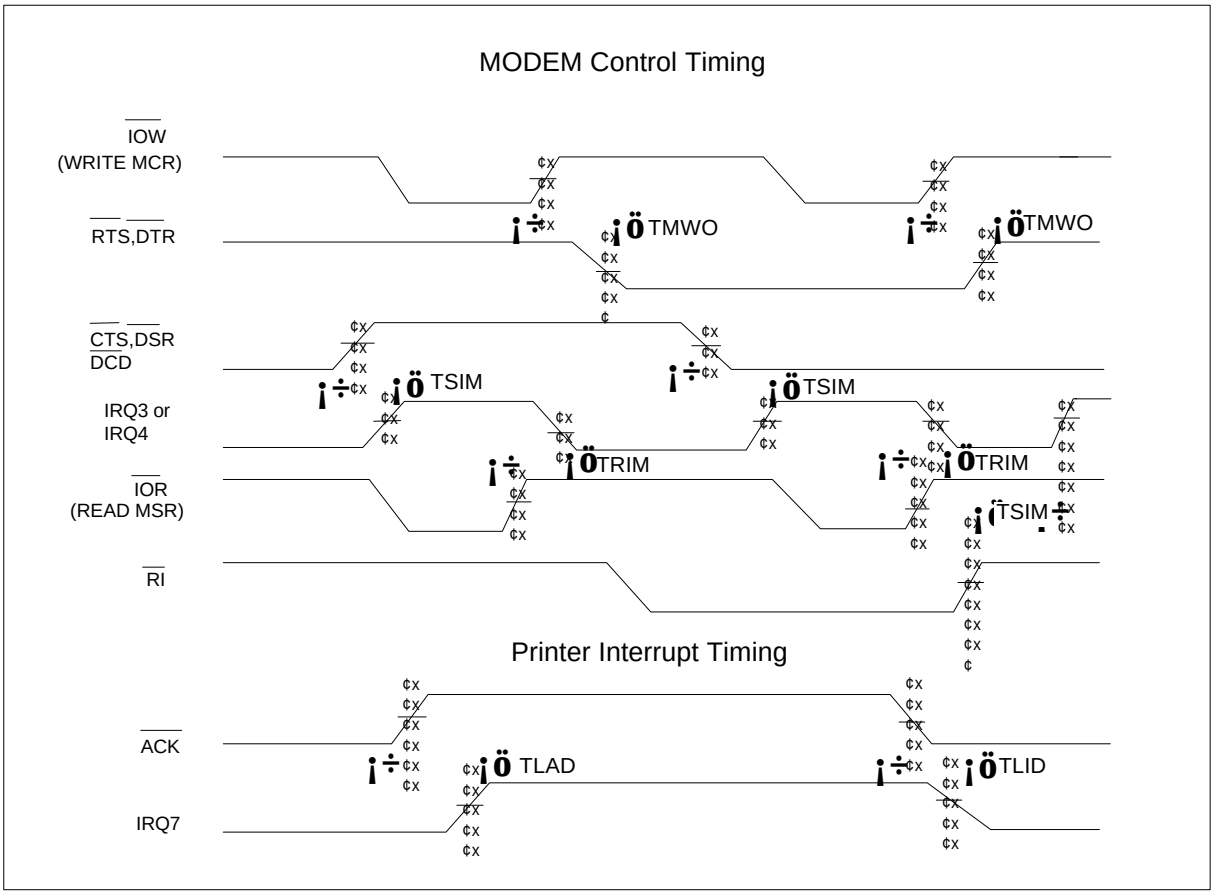
13.1 FDC



13.2 UART/Parallel

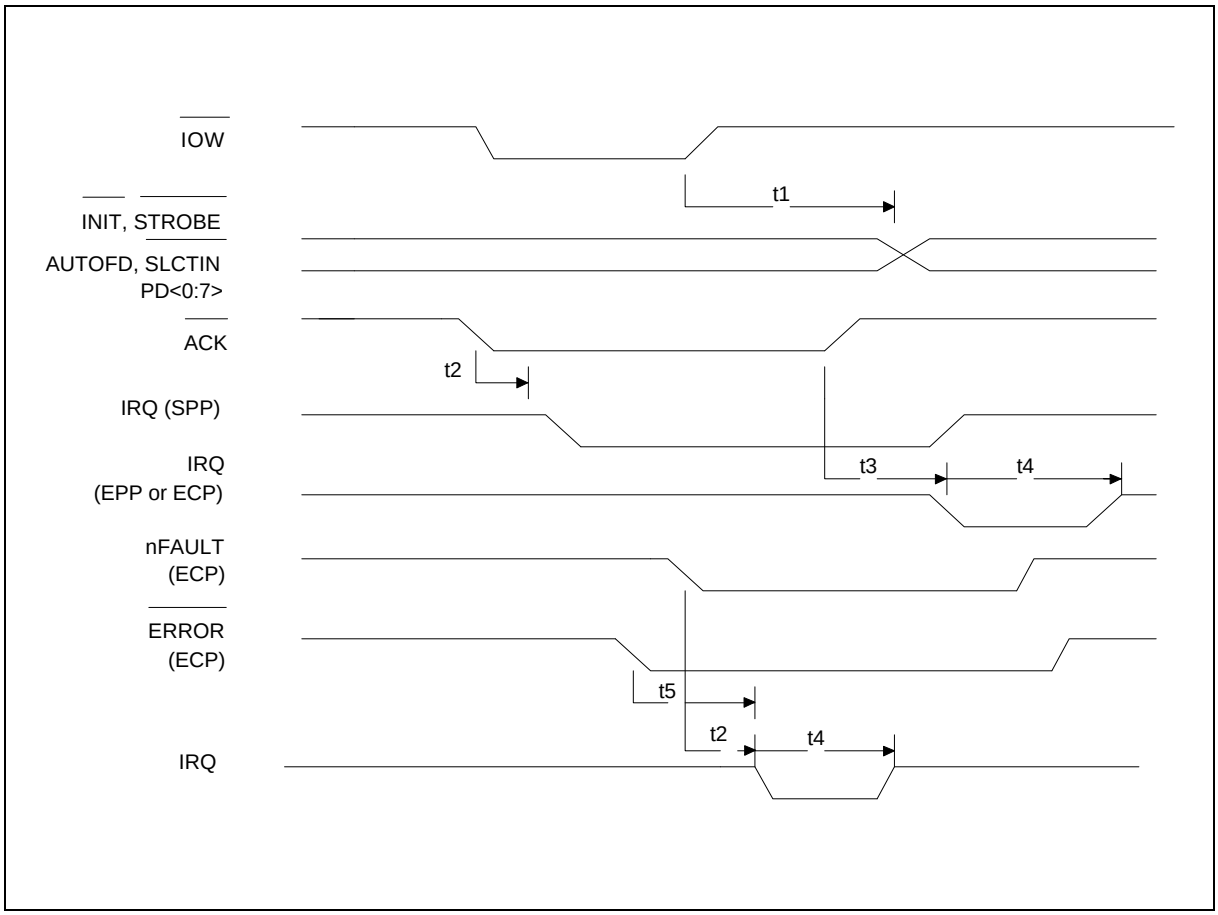


13.2.1 Modem Control Timing

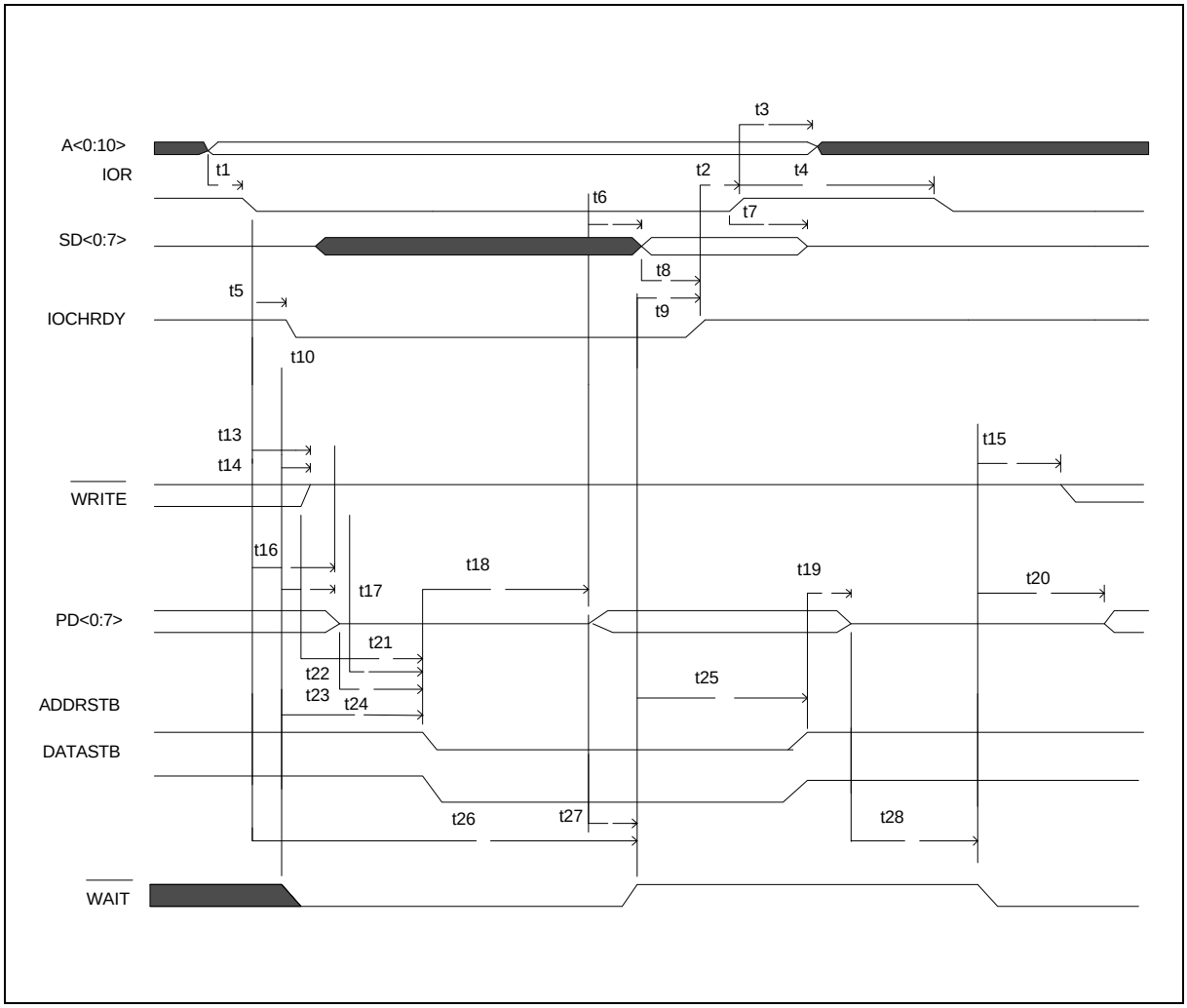


13.3 Parallel Port

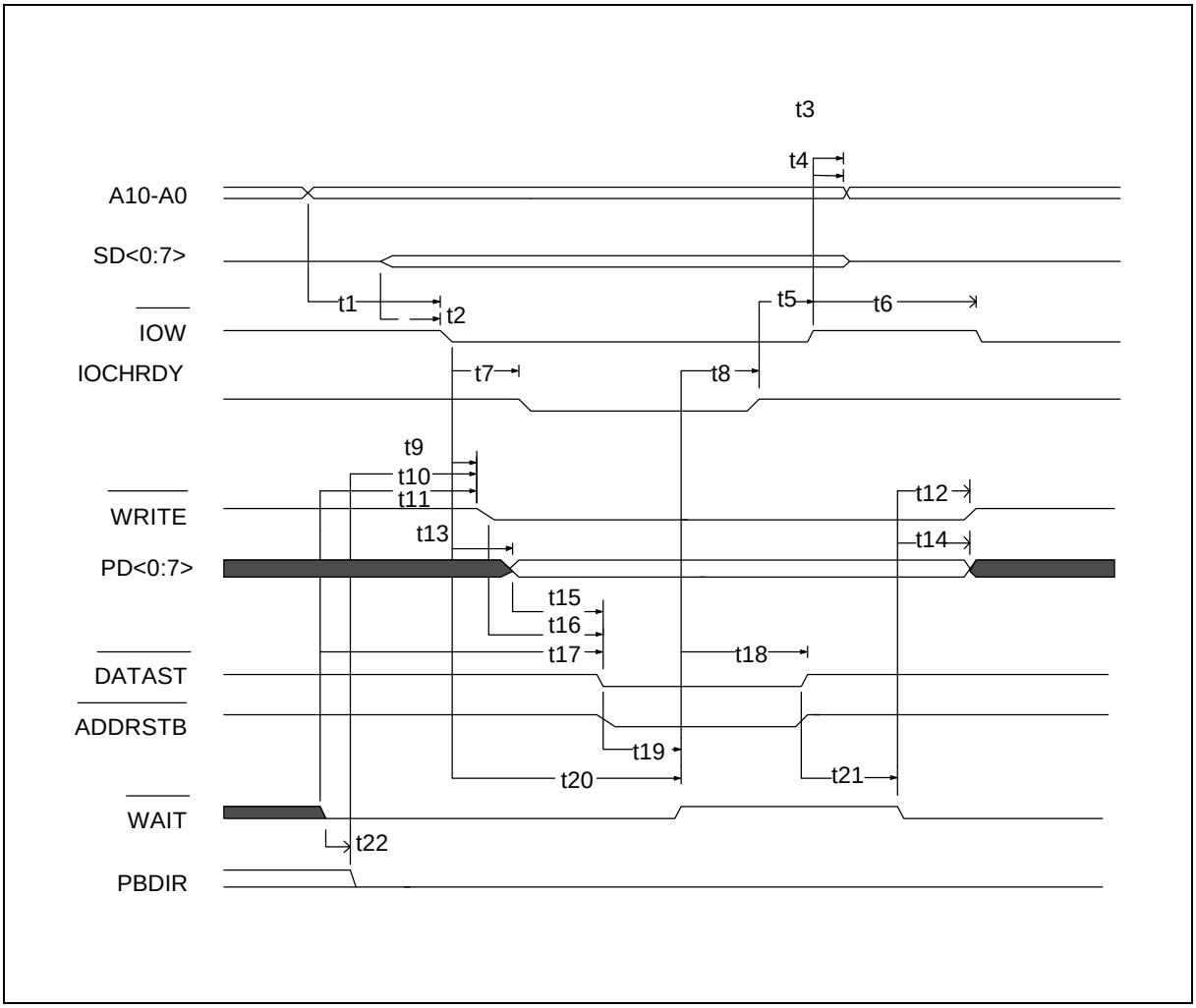
13.3.1 Parallel Port Timing



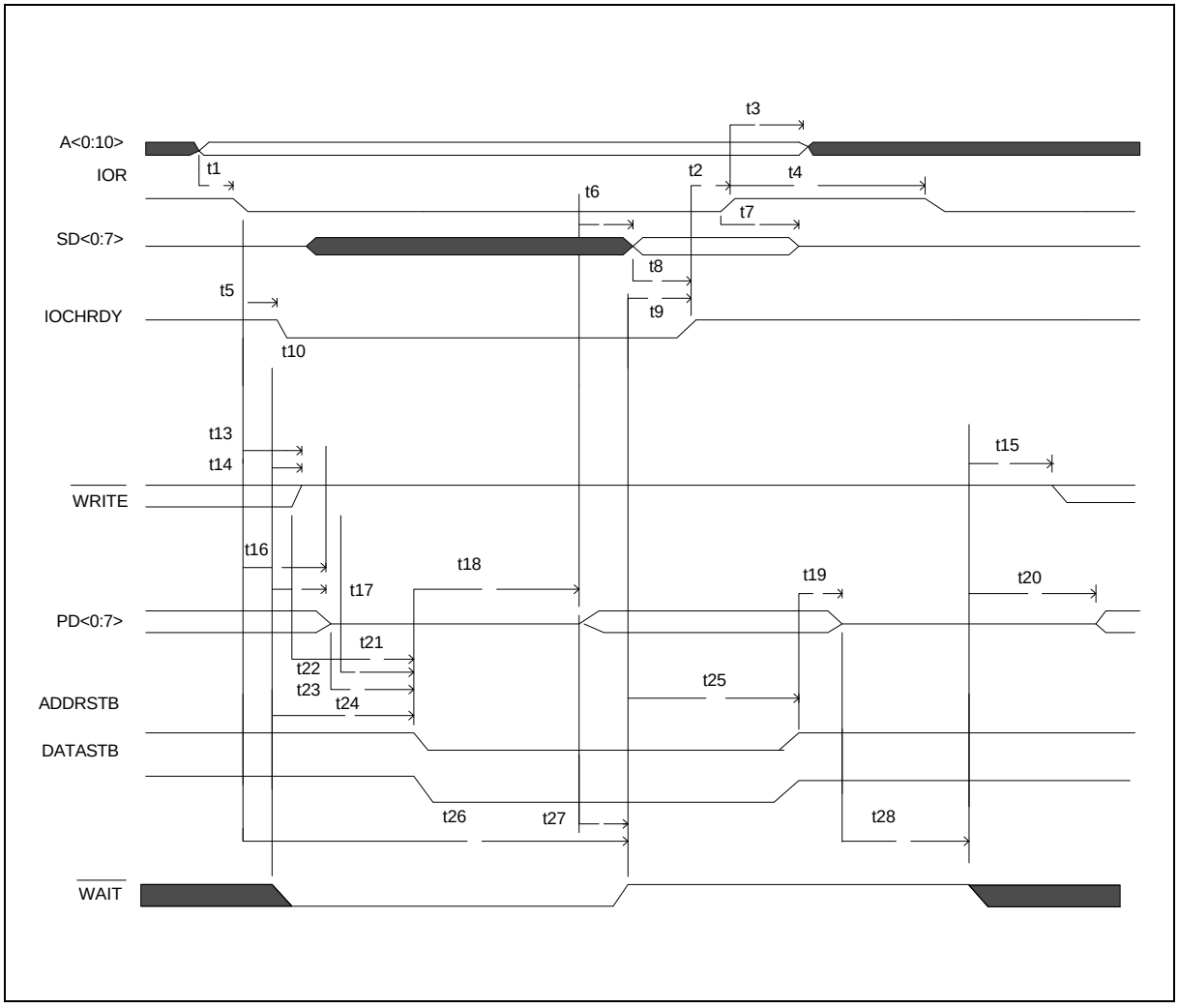
13.3.2 EPP Data or Address Read Cycle (EPP Version 1.9)



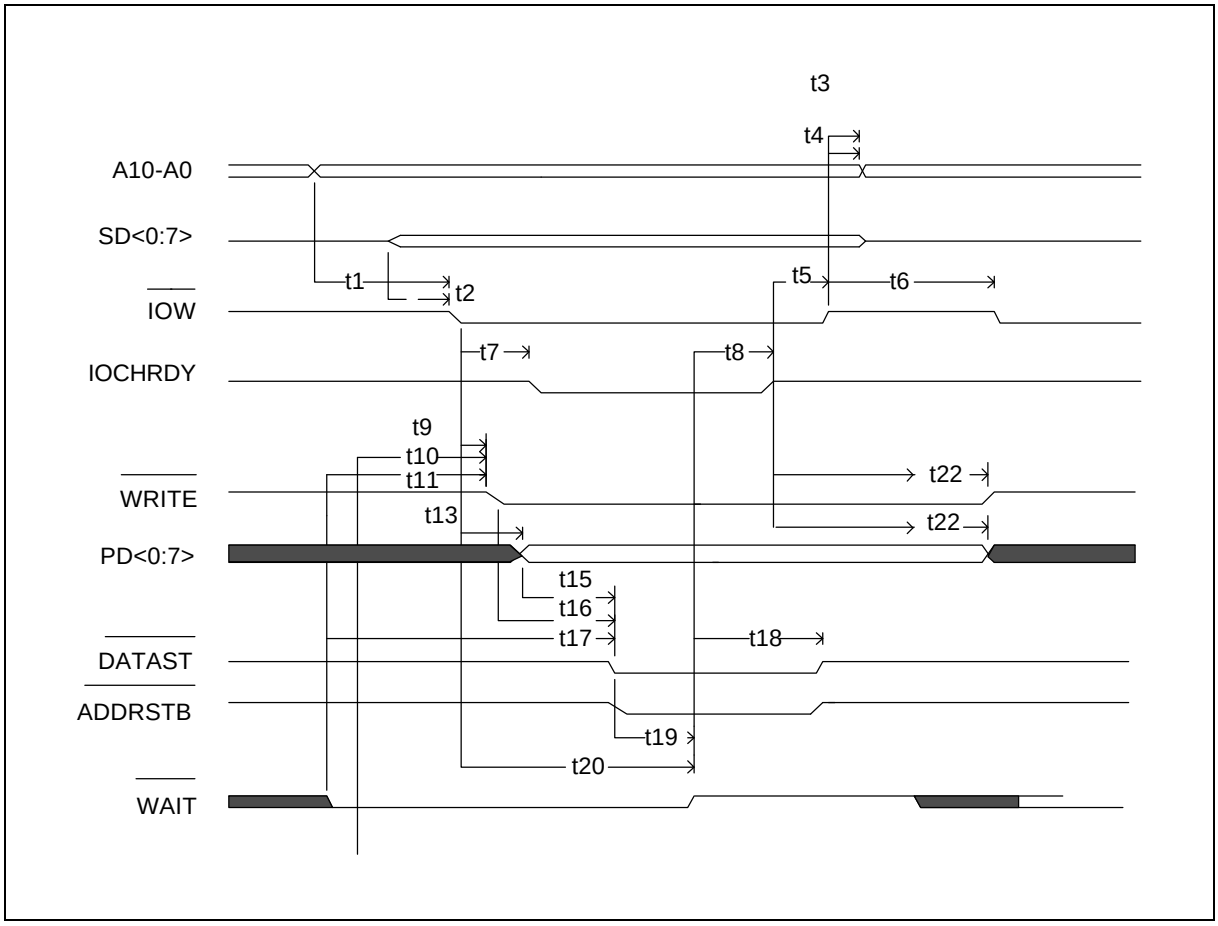
13.3.3 EPP Data or Address Write Cycle (EPP Version 1.9)



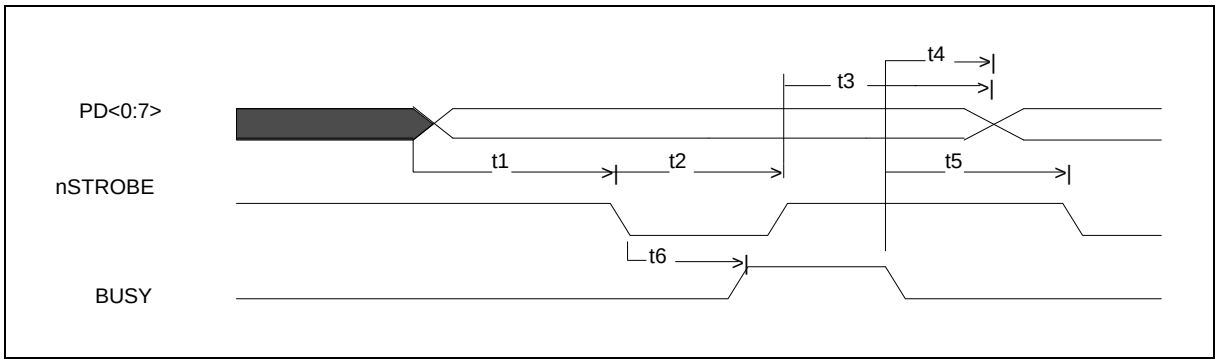
13.3.4 EPP Data or Address Read Cycle (EPP Version 1.7)



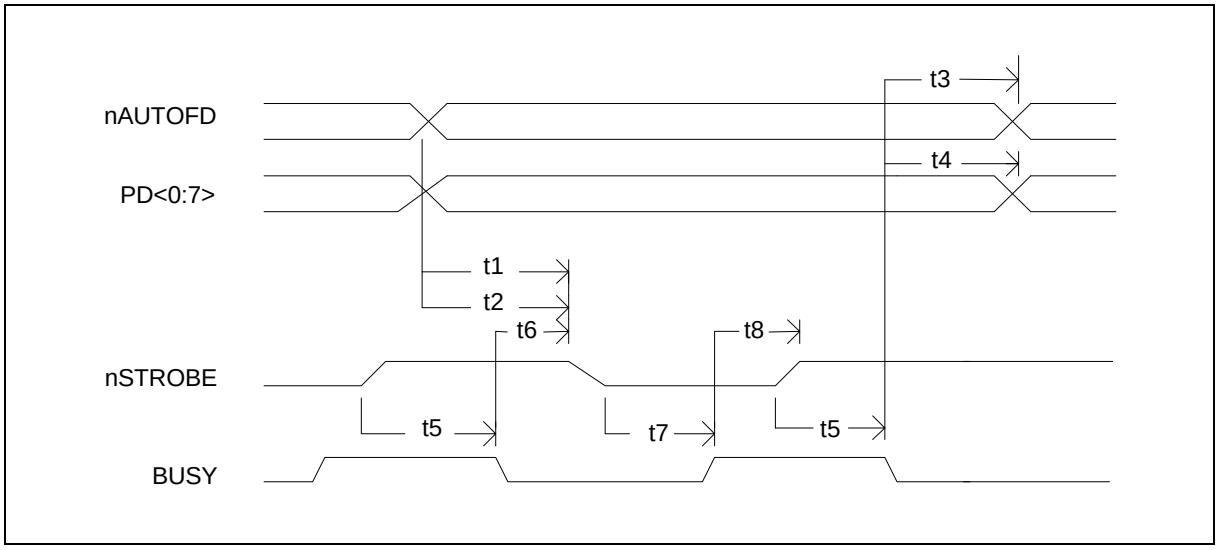
13.3.5 EPP Data or Address Write Cycle (EPP Version 1.7)



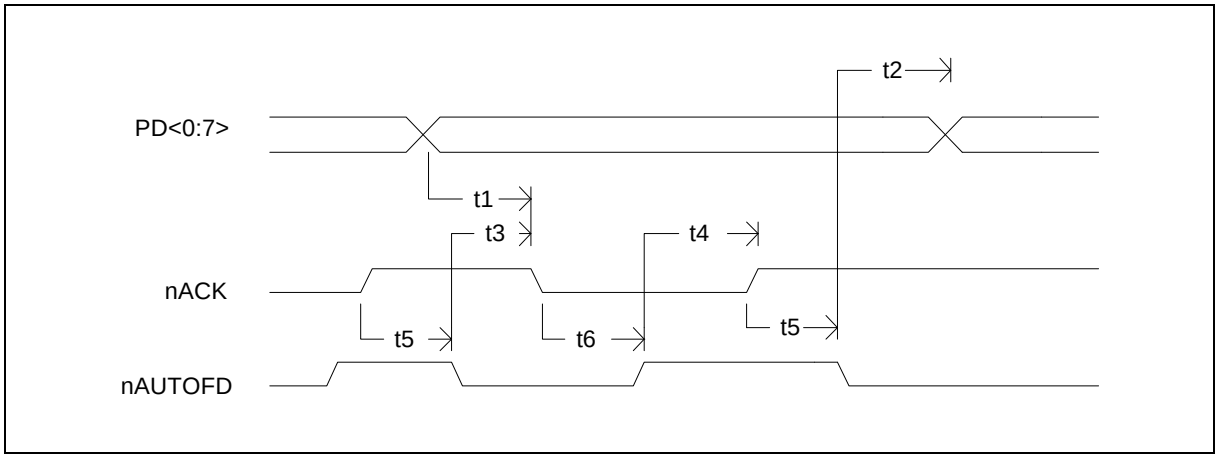
13.3.6 Parallel Port FIFO Timing



13.3.7 ECP Parallel Port Forward Timing

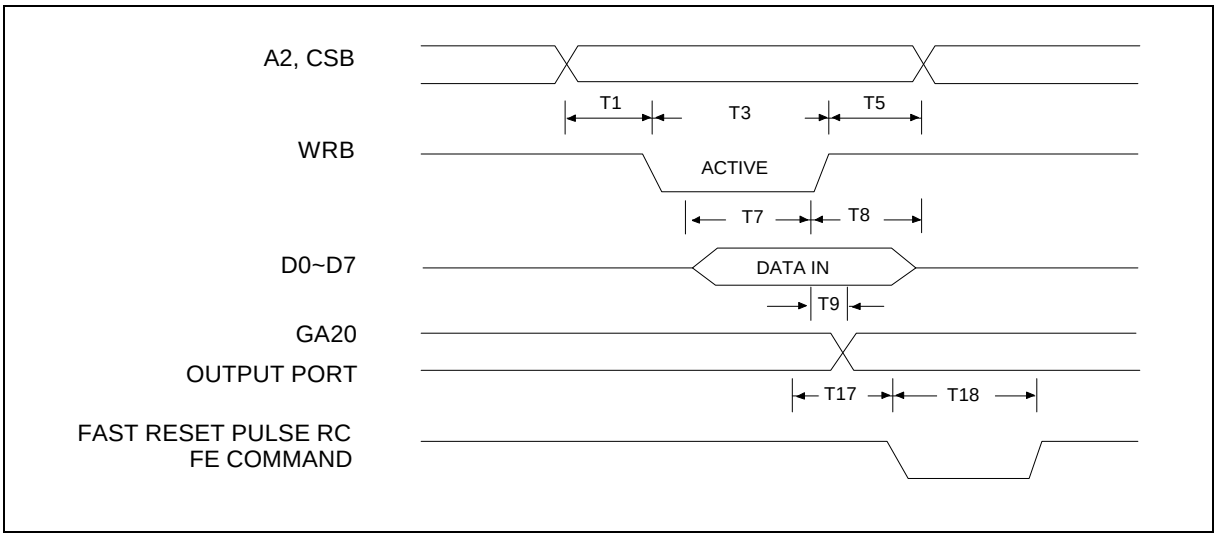


13.3.8 ECP Parallel Port Reverse Timing

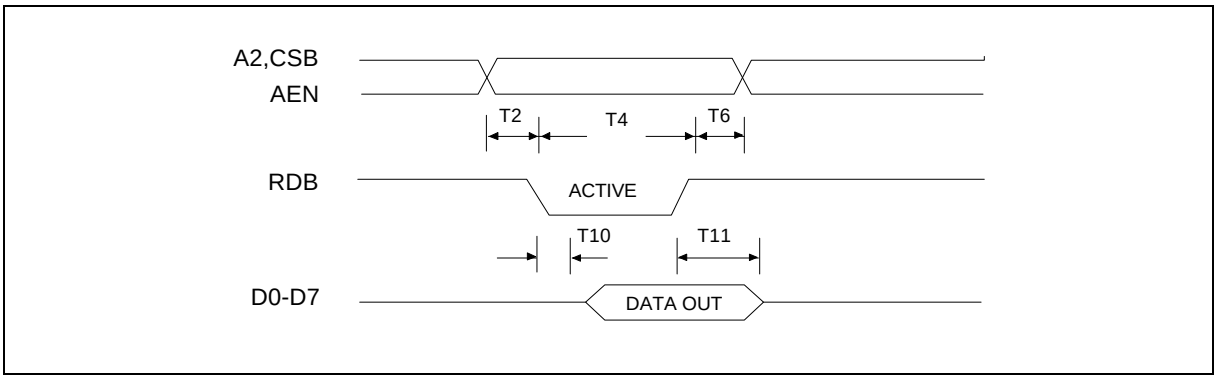


13.4 KBC

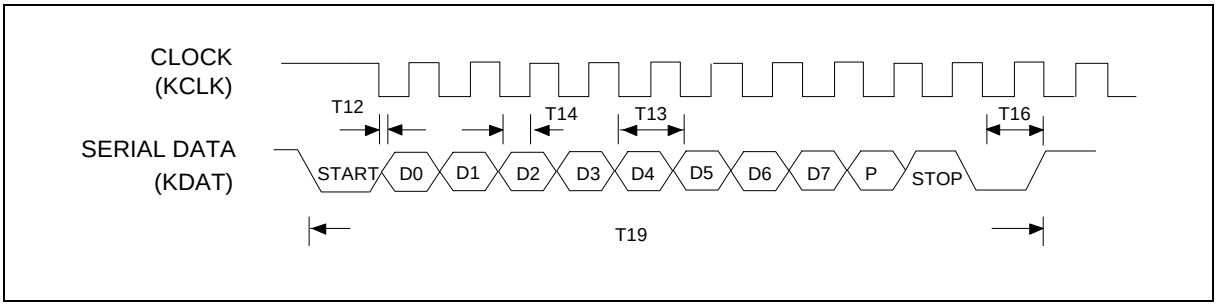
13.4.1 Write Cycle Timing



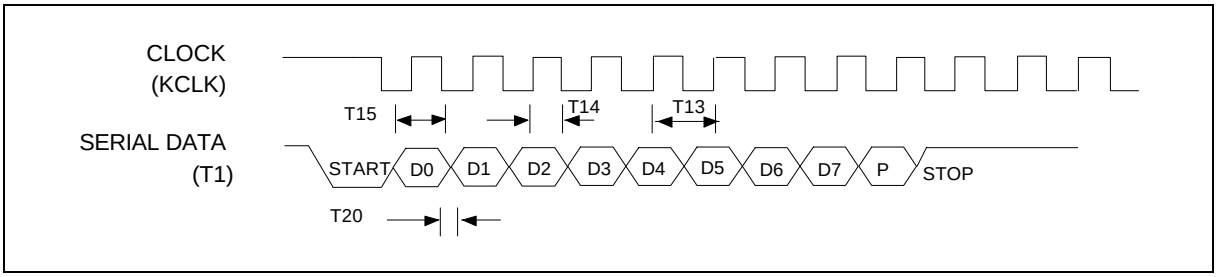
13.4.2 Read Cycle Timing



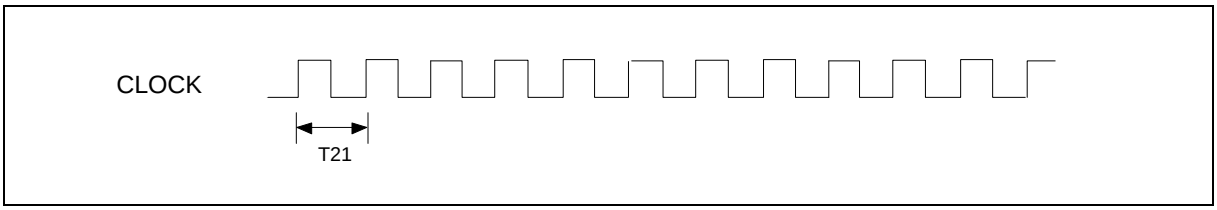
13.4.3 Send Data to K/B



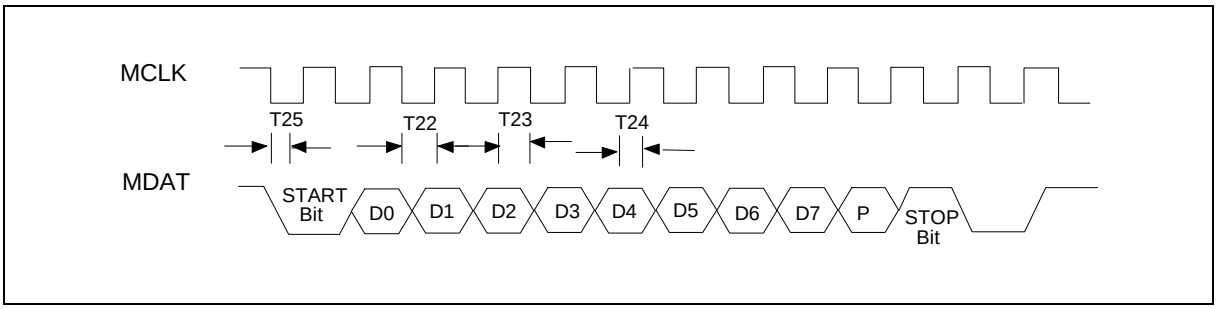
13.4.4 Receive Data from K/B



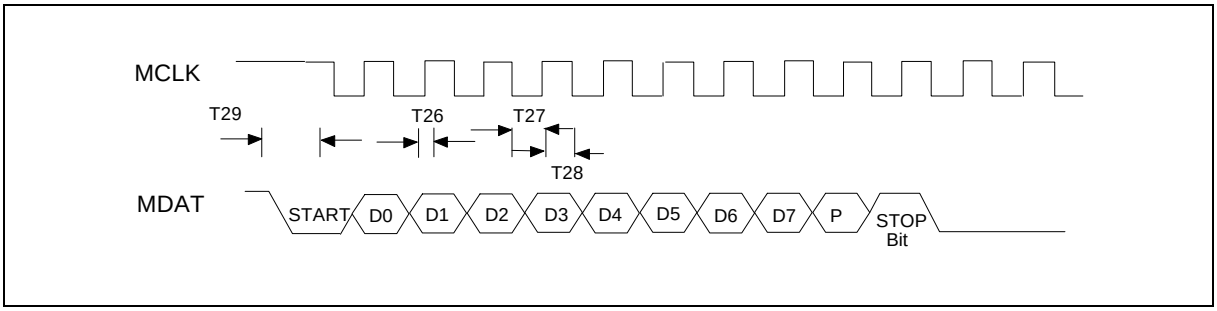
13.4.5 Input Clock



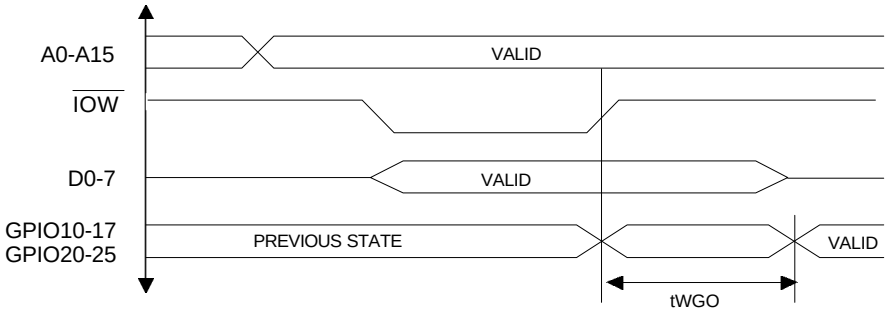
13.4.6 Send Data to Mouse



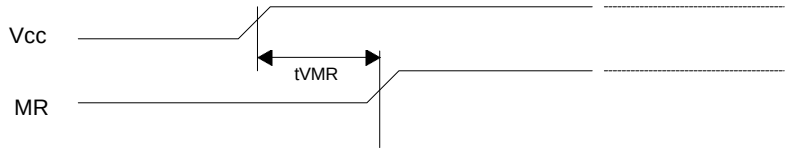
13.4.7 Receive Data from Mouse



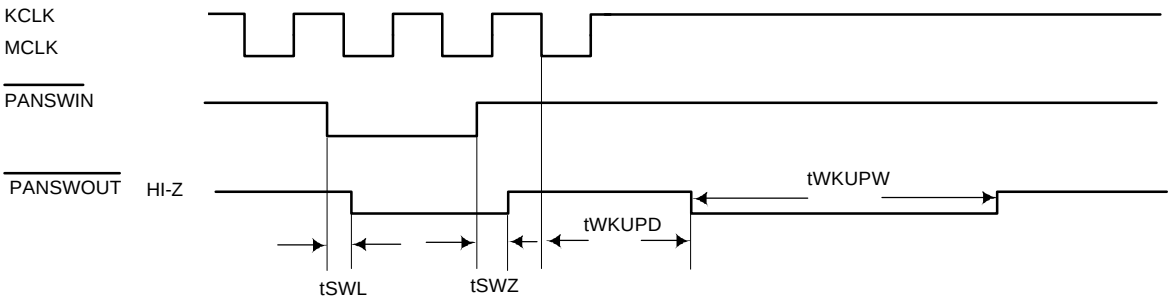
13.5 GPIO Write Timing Diagram



13.6 Master Reset (MR) Timing

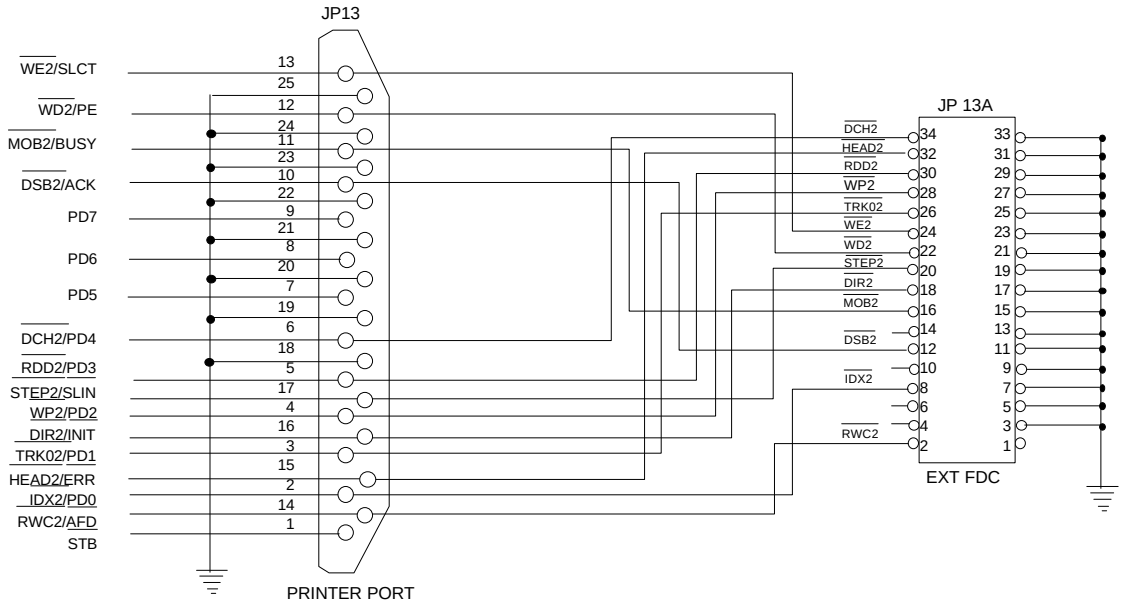


13.7 Keyboard/Mouse Wake-up Timing



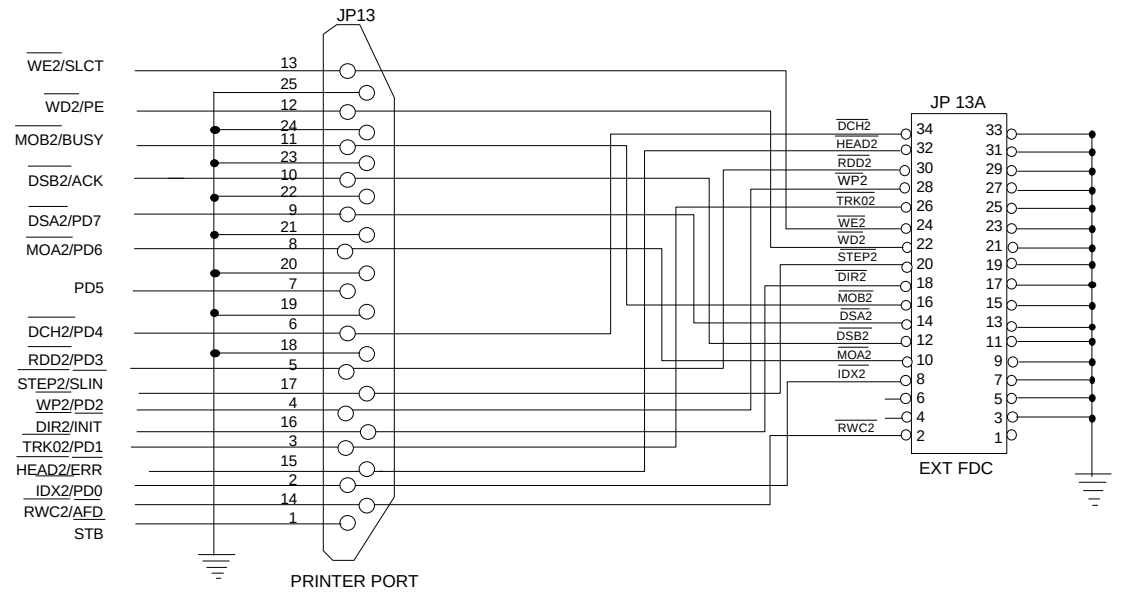
14.0 APPLICATION CIRCUITS

14.1 Parallel Port Extension FDD



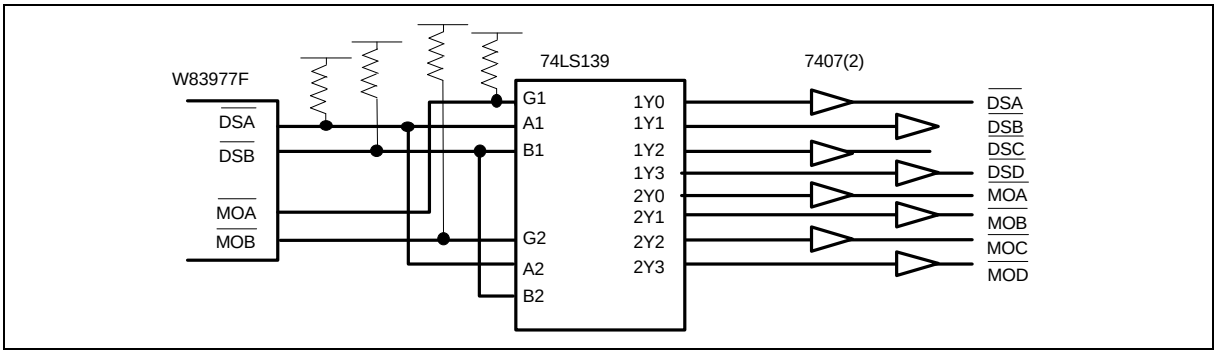
Parallel Port Extension FDD Mode Connection Diagram

14.2 Parallel Port Extension 2FDD



Parallel Port Extension 2FDD Connection Diagram

14.3 Four FDD Mode

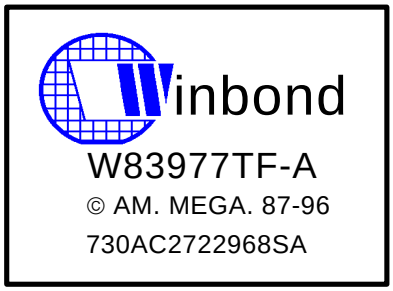


15.0 ORDERING INFORMATION

PART NO.	KBC FIRMWARE	REMARKS
W83977TF-P	Phoenix MultiKey/42™	
W83977TF-A	AMIKEY™-2	
W83977TF-PW	Phoenix MultiKey/42™	with OnNow / security keyboard wake-up
W83977TF-AW	AMIKEY™-2	with OnNow / security keyboard wake-up

16.0 HOW TO READ THE TOP MARKING

Example: The top marking of W83977TF-A



1st line: Winbond logo

2nd line: the type number: W83977TF-A

3rd line: the source of KBC F/W -- American Megatrends Incorporated™

4th line: the tracking code 730 A C 2 722968 SA

730: packages made in '97, week 30

A: assembly house ID; A means ASE, S means SPIL.... etc.

C: IC revision; B means version B, C means version C

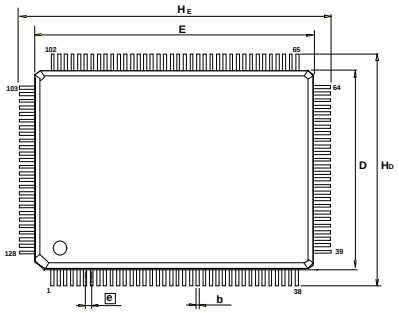
2: wafers manufactured in Winbond FAB 2

722968: wafer production series lot number

SA: if made by 0.5-um process: SA; otherwise by 0.6-um process: blank

17.0 PACKAGE DIMENSIONS

(128-pin PQFP)



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A_1	0.25	0.35	0.45	0.010	0.014	0.018
A_2	2.57	2.72	2.87	0.101	0.107	0.113
b	0.10	0.20	0.30	0.004	0.008	0.012
c	0.10	0.15	0.20	0.004	0.006	0.008
D	13.90	14.00	14.10	0.547	0.551	0.555
E	19.90	20.00	20.10	0.783	0.787	0.791
e	——	0.50	——	—	0.020	—
H_D	17.00	17.20	17.40	0.669	0.677	0.685
H_E	23.00	23.20	23.40	0.905	0.913	0.921
L	0.65	0.80	0.95	0.025	0.031	0.037
L_1	——	1.60	——	—	0.063	—
y	——	——	0.08	—	—	0.003
θ	0	——	7	0	—	7

Note:
1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion .
3. Controlling dimension : Millimeter
4. General appearance spec. should be based on final visual inspection spec.
5. PCB layout please use the "mm".

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