11. CONFIGURATION REGISTER

11.1 Chip (Global) Control Register

CR02 (Default 0x00)

Bit 7 - 1: Reserved.
Bit 0: SWRST --> Soft Reset.

CR07

Bit 7 - 0: LDNB7 - LDNB0 --> Logical Device Number Bit 7 - 0

CR20

Bit 7 - 0: DEVIDB7 - DEBIDB0 --> Device ID Bit 7 - Bit 0 = 0x97 (read only).

CR21

Bit 7 - 0: DEVREVB7 - DEBREVB0 --> Device Rev Bit 7 - Bit 0 = 0x73 (read only).

CR22 (Default 0xff)

Bit 7 - 6: Reserved.
Bit 5: URBPWD
= 0 Power down
= 1 No Power down
Bit 4: URAPWD
= 0 Power down
= 1 No Power down
Bit 3: PRTPWD
= 0 Power down
= 1 No Power down
Bit 2, 1: Reserved.
Bit 0: FDCPWD
= 0 Power down
= 1 No Power down

CR23 (Default 0xFE)

Bit 7 - 1: Reserved.
Bit 0: IPD (Immediate Power Down). When set to 1, it will put the whole chip into power down mode immediately.

CR24 (Default 0b1s000s0s)

Bit 7: EN16SA
= 0 12 bit Address Qualification
= 1 16 bit Address Qualification
Bit 6: EN48
= 0 The clock input on Pin 1 should be 24 Mhz.
= 1 The clock input on Pin 1 should be 48 Mhz.
The corresponding power-on setting pin is SOUTB (pin 53).

Bit 5 - 3: Reserved.

Bit 2: ENKBC

= 0 KBC is disabled after hardware reset.

= 1 KBC is enabled after hardware reset.

This bit is read only, and set/reset by power-on setting pin. The corresponding power-on setting pin is SOUTA (pin 46).

Bit 1: Reserved

Bit 0: $\overline{\text{PNPCSV}}$

= 0 The Compatible PnP address select registers have default values.

= 1 The Compatible PnP address select registers have no default value.

When trying to make a change to this bit, new value of $\overline{\text{PNPCSV}}$ must be complementary to the old one to make an effective change. For example, the user must set $\overline{\text{PNPCSV}}$ to 0 first and then reset it to 1 to reset these PnP registers if the present value of $\overline{\text{PNPCSV}}$ is 1. The corresponding power-on setting pin is NDTRA (pin 44).

CR25 (Default 0x00)

Bit 7 - 6: Reserved

Bit 5: URBTRI

Bit 4: URATRI

Bit 3: PRTTRI

Bit 2 - 1 : Reserved

Bit 0: FDCTRI.

CR26 (Default 0b0s000000)

Bit 7: SEL4FDD

= 0 Select two FDD mode.

= 1 Select four FDD mode.

Bit 6: HEFRAS

These two bits define how to enable Configuration mode. The corresponding power-on setting pin is NRTSA (pin 43).

HEFRAS Address and Value

= 0 Write 87h to the location 3F0h twice.

= 1 Write 87h to the location 370h twice.

Bit 5: LOCKREG

= 0 Enable R/W Configuration Registers.

= 1 Disable R/W Configuration Registers.

Bit 4: Reserved.

Bit 3: DSFDLGRQ

= 0 Enable FDC legacy mode on IRQ and DRQ selection, then DO register bit 3 is effective on selecting IRQ

= 1 Disable FDC legacy mode on IRQ and DRQ selection, then DO register bit 3 is not effective on selecting IRQ

Bit 2: DSPRLGRQ
= 0 Enable PRT legacy mode on IRQ and DRQ selection, then DCR bit 4 is effective on selecting IRQ
= 1 Disable PRT legacy mode on IRQ and DRQ selection, then DCR bit 4 is not effective on selecting IRQ

Bit 1: DSUALGRQ
= 0 Enable UART A legacy mode IRQ selecting, then MCR bit 3 is effective on selecting IRQ
= 1 Disable UART A legacy mode IRQ selecting, then MCR bit 3 is not effective on selecting IRQ

Bit 0: DSUBLGRQ
= 0 Enable UART B legacy mode IRQ selecting, then MCR bit 3 is effective on selecting IRQ
= 1 Disable UART B legacy mode IRQ selecting, then MCR bit 3 is not effective on selecting IRQ

CR28 (Default 0x00)

Bit 7 - 5: Reserved.
Bit 4: IRQ Sharing selection.
= 0 Disable IRQ Sharing
= 1 Enable IRQ Sharing
Bit 3:Reserved
Bit 2 - 0: PRTMODS2 - PRTMODS0
= 0xx Parallel Port Mode
= 100 Reserved
= 101 External FDC Mode
= 110 Reserved
= 111 External two FDC Mode

CR2A (Default 0x00)

Bit 7: PIN57S
= 0 KBRST
= 1 GP12
Bit 6: PIN56S
= 0 GA20
= 1 GP11
Bit 5 - 4: PIN40S1, PIN40S0
= 00 Reserved
= 01 GP24
= 10 8042 P13
= 11 Reserved
Bit 3 - 2: Reserved.
Bit 1 - 0: PIN3S1, PIN3S0
= 00 DRVDEN1
= 01 GP10
= 10 8042 P12
= 11 $\overline{SCI}$

CR2B (Default 0x00)

Bit 7 - 6: PIN73S1, PIN73S0

= 00 $\overline{\text{PANSWIN}}$
= 01 GP23
= 10 Reserved
= 11 Reserved

Bit 5: PIN72S

= 0 $\overline{\text{PANSWOUT}}$
= 1 GP22

Bit 4 - 3: PIN70S1, PIN70S0

= 00 $\overline{\quad}$

= 10 8042 P16
= 11 Reserved

Bit 0: PIN58S

= 1 GP13

Bit 7 - 6: PIN121S1, PIN121S0

= 01 GP17
= 10 8042 P14
$\overline{\text{SCI}}$

Bit 5 - 4: PIN119S1, PIN119S0

= 01 GP16
= 10 8042 P15
Reserved

Bit 3 - 2: PIN104S1, PIN104S0

= 00 IRQ15

= 10 WDTO
= 11 Reserved

= 00 IRQ14
= 01 GP14

= 11

CR2D (Default 0x00)

Test Modes: Reserved for Winbond.

Test Modes: Reserved for Winbond.

CR2F (Default 0x00)

11.2 Logical Device 0 (FDC)

CR30 (Default 0x01 if $\overline{\text{PNPCSV}}$ = 0 during POR, default 0x00 otherwise)

Bit 7 - 1: Reserved.

= 1 Activates the logical device.

= 0 Logical device is inactive.

$\overline{\text{PNPCSV}}$ = 0 during POR, default 0x00, 0x00 otherwise)

These two registers select FDC I/O base address [0x100:0xFF8] on 8 byte boundary.

CR70 (Default 0x06 if $\overline{\text{PNPCSV}}$ = 0 during POR, default 0x00 otherwise)

Bit 7 - 4: Reserved.

CR74 (Default 0x02 if $\overline{\text{PNPCSV}}$ = 0 during POR, default 0x04 otherwise)

Bit 2 - 0: These bits select DRQ resource for FDC.

= 0x00 DM

= 0x01 DMA1

= 0x02 DMA2

= 0x04 - 0x07 No DMA active

CRF0 (Default 0x0E)

Bit 7: FIPURDWN

This bit controls the internal pull-up resistors of the FDC input pins RDATA, INDEX, TRAK0,

= 0 The internal pull-up resistors of FDC are turned on.(Default)

= 1 The internal pull-up resistors of FDC are turned off.

This bit determines the polarity of all FDD interface signals.

= 0 FDD interface signals are active low.

= 1 FDD interface signals are active high.

Bit 5: DRV2EN (PS2 mode only)

register A.

Bit 4: Swap Drive 0, 1 Mode

= 1 Drive and Motor sel 0 and 1 are swapped.

Bit 3 - 2 Interface Mode

= 10 (Reserved)

= 01 PS/2

Bit 1: FDC DMA Mode

bled

Bit 0: Floppy Mode

= 1 Enhanced 3-mode FDD

Bit 7 - 6: Boot Floppy

= 01 FDD B
= 10 FDD C

Bit 5, 4: Media ID1, Media ID0. These bits will be reflected on FDC's Tape Drive Register bit 7, 6.
Bit 3 - 2: Density Select

= 01 Normal
= 10 1 (Forced to logic 1)
= 11 0 (Forced to logic 0)

Bit 1: DISFDDWR
= 0 Enable FDD write.

Bit 0: SWWP
= 0 Normal, use WP to determine whether the FDD is write protected or not.

CRF2 (Default 0xFF)

Bit 7 - 6: FDD D Drive Type

Bit 3 - 2: FDD B Drive Type
Bit 1:0: FDD A Drive Type

of CRF4 and CRF5 as follows.

DTYPE1		DRATE1	DRATE0	
0	0		1	1
	0	0		1
0		0	1	
0	0		0	0
	1	X		0
1		X	X	
1	1		1	0

Note: X means don't care.

CRF4 (Default 0x00)

FDD0 Selection:

Bit 7: Reserved.

Bit 6: Precomp. Disable.

= 1 Disable FDC Precompensation.

= 0 Enable FDC Precompensation.

Bit 5: Reserved.

Bit 4 - 3: DRTS1, DRTS0: Data Rate Table select (Refer to TABLE A).

= 00 Select Regular drives and 2.88 format

= 01 Specifical application

= 10 2 Meg Tape

= 11 Reserved

Bit 2: Reserved.

Bit 1:0: DMOD0, DMOD1 : Drive Model select (Refer to TABLE B).

CRF5 (Default 0x00)

FDD1 Selection: Same as FDD0 of CRF4.

TABLE A

DRIVE RATE TABLE SELECT		DATA RATE		SELECTED DATA RATE		SELDEN
DRTS1	DRTS0	DRATE1	DRATE0	MFM	FM	CRF0 bit 0 = 0
0	0	1	1	1Meg	---	1
		0	0	500K	250K	1
		0	1	300K	150K	0
		1	0	250K	125K	0
0	1	1	1	1Meg	---	1
		0	0	500K	250K	1
		0	1	500K	250K	0
		1	0	250K	125K	0
1	0	1	1	1Meg	---	1
		0	0	500K	250K	1
		0	1	2Meg	---	0
		1	0	250K	125K	0

Note:Refer to CRF2 for SELDEN value in the cases when CRF0, bit0=1.

TABLE B

DMOD0	DMOD1	DRVDEN0 (PIN 2)	DRVDEN1 (PIN 3)	DRIVE TYPE
0	0	SELDEN	DRATE0	4/2/1 MB 3.5″″ 2/1 MB 5.25” 2/1.6/1 MB 3.5″ (3-MODE)
0	1	DRATE1	DRATE0	
1	0	$\overline{\text{SELDEN}}$	DRATE0	
1	1	DRATE0	DRATE1	

11.3 Logical Device 1 (Parallel Port)

CR30 (Default 0x01 if $\overline{\text{PNPCSV}}$ = 0 during POR, default 0x00 otherwise)

Bit 7 - 1: Reserved.

Bit 0:

= 1 Activates the logical device.

= 0 Logical device is inactive.

CR60, CR 61 (Default 0x03, 0x78 if $\overline{\text{PNPCSV}}$ = 0 during POR, default 0x00, 0x00 otherwise)

These two registers select Parallel Port I/O base address.

[0x100:0xFFC] on 4 byte boundary (EPP not supported) or

[0x100:0xFF8] on 8 byte boundary (all modes supported, EPP is only available when the base address is on 8 byte boundary).

CR70 (Default 0x07 if $\overline{\text{PNPCSV}}$ = 0 during POR, default 0x00 otherwise)

Bit 7 - 4: Reserved.

Bit [3:0]: These bits select IRQ resource for Parallel Port.

CR74 (Default 0x04)

Bit 7 - 3: Reserved.

Bit 2 - 0: These bits select DRQ resource for Parallel Port.

0x00=DMA0

0x01=DMA1

0x02=DMA2

0x03=DMA3

0x04 - 0x07= No DMA active

CRF0 (Default 0x3F)

Bit 7: PP Interrupt Type:

Not valid when the parallel port is in the printer Mode (100) or the standard & Bi-directional Mode (000).

= 1 Pulsed Low, released to high-Z .

= 0 IRQ follows nACK when parallel port in EPP Mode or [Printer, SPP, EPP] under ECP.

Bit [6:3]: ECP FIFO Threshold.

Bit 2 - 0 Parallel Port Mode

= 100 Printer Mode (Default)

= 000 Standard and Bi-direction (SPP) mode

= 001 EPP - 1.9 and SPP mode

= 101 EPP - 1.7 and SPP mode

= 010 ECP mode

= 011 ECP and EPP - 1.9 mode

= 111 ECP and EPP - 1.7 mode.

11.4 Logical Device 2 (UART A)¢)

CR30 (Default 0x01 if $\overline{\text{PNPCSV}}$ = 0 during POR, default 0x00 otherwise)

Bit 7 - 1: Reserved.

Bit 0:

= 1 Activates the logical device.

= 0 Logical device is inactive.

CR60, CR 61 (Default 0x03, 0xF8 if $\overline{\text{PNPCSV}}$ = 0 during POR, default 0x00, 0x00 otherwise)

These two registers select Serial Port 1 I/O base address [0x100:0xFF8] on 8 byte boundary.

CR70 (Default 0x04 if $\overline{\text{PNPCSV}}$ = 0 during POR, default 0x00 otherwise)

Bit 7 - 4: Reserved.

Bit 3 - 0: These bits select IRQ resource for Serial Port 1.

CRF0 (Default 0x00)

Bit 7 - 2: Reserved.

Bit 1 - 0: SUACLKB1, SUACLKB0

= 00 UART A clock source is 1.8462 MHz (24 MHz/13)

= 01 UART A clock source is 2 MHz (24 MHz/12)

= 10 UART A clock source is 24 MHz (24 MHz/1)

= 11 UART A clock source is 14.769 MHz (24 MHz/1.625)

11.5 Logical Device 3 (UART B)

CR30 (Default 0x01 if $\overline{\text{PNPCSV}}$ = 0 during POR, default 0x00 otherwise)

Bit 7 - 1: Reserved.

Bit 0:

= 1 Activates the logical device.

= 0 Logical device is inactive.

CR60, CR 61 (Default 0x02, 0xF8 if $\overline{\text{PNPCSV}}$ = 0 during POR, default 0x00, 0x00 otherwise)

These two registers select Serial Port 2 I/O base address [0x100:0xFF8] on 8 byte boundary.

CR70 (Default 0x03 if $\overline{\text{PNPCSV}}$ = 0 during POR, default 0x00 otherwise)

Bit 7 - 4: Reserved.

Bit [3:0]: These bits select IRQ resource for Serial Port 2.

CRF0 (Default 0x00)

Bit 7 - 4: Reserved.

Bit 3: RXW4C

= 0 No reception delay when SIR is changed from TX mode to RX mode.

= 1 Reception delays 4 characters-time (40 bit-time) when SIR is changed from TX mode to RX mode.

Bit 2: TXW4C

= 0 No transmission delay when SIR is changed from RX mode to TX mode.

= 1 Transmission delays 4 characters-time (40 bit-time) when SIR is changed from RX mode to TX mode.

Bit 1 - 0: SUBCLKB1, SUBCLKB0

= 00 UART B clock source is 1.8462 Mhz (24MHz/13)

= 01 UART B clock source is 2 Mhz (24MHz/12)

= 10 UART B clock source is 24 Mhz (24MHz/1)

= 11 UART B clock source is 14.769 Mhz (24MHz/1.625)

CRF1 (Default 0x00)

Bit 7: Reserved.

Bit 6: IRLOCSEL. IR I/O pins' location select.

= 0 Through SINB/SOUTB.

= 1 Through IRRX/IRTX.

Bit 5: IRMODE2. IR function mode selection bit 2.

Bit 4: IRMODE1. IR function mode selection bit 1.

Bit 3: IRMODE0. IR function mode selection bit 0.

IR MODE	IR FUNCTION	IRTX	IRRX
00X	Disable	tri-state	high
010*	IrDA	Active pulse 1.6 μS	Demodulation into SINB/IRRX
011*	IrDA	Active pulse 3/16 bit time	Demodulation into SINB/IRRX
100	ASK-IR	Inverting IRTX/SOUTB pin	routed to SINB/IRRX
101	ASK-IR	Inverting IRTX/SOUTB & 500 KHZ clock	routed to SINB/IRRX
110	ASK-IR	Inverting IRTX/SOUTB	Demodulation into SINB/IRRX
111*	ASK-IR	Inverting IRTX/SOUTB & 500 KHZ clock	Demodulation into SINB/IRRX

Note: The notation is normal mode in the IR function.

Bit 2: HDUPLX. IR half/full duplex function select.

= 0 The IR function is Full Duplex.

= 1 The IR function is Half Duplex.

Bit 1: TX2INV.

= 0 the SOUTB pin of UART B function or IRTX pin of IR function in normal condition.

= 1 inverse the SOUTB pin of UART B function or IRTX pin of IR function.

Bit 0: RX2INV.

= 0 the SINB pin of UART B function or IRRX pin of IR function in normal condition.

= 1 inverse the SINB pin of UART B function or IRRX pin of IR function

11.6 Logical Device 5 (KBC)

CR30 (Default 0x01 if PENKBC= 1 during POR, default 0x00 otherwise)

Bit 7 - 1: Reserved.

Bit 0:

= 1 Activates the logical device.

= 0 Logical device is inactive.

CR60, CR 61 (Default 0x00, 0x60 if PENKBC= 1 during POR, default 0x00 otherwise)

These two registers select the first KBC I/O base address [0x100:0xFFF] on 1 byte boundary.

CR62, CR 63 (Default 0x00, 0x64 if PENKBC= 1 during POR, default 0x00 otherwise)

These two registers select the second KBC I/O base address [0x100:0xFFF] on 1 byte boundary.

CR70 (Default 0x01 if PENKBC= 1 during POR, default 0x00 otherwise)

Bit 7 - 4: Reserved.

Bit [3:0]: These bits select IRQ resource for KINT (keyboard).

CR72 (Default 0x0C if PENKBC= 1 during POR, default 0x00 otherwise)

Bit 7 - 4: Reserved.

Bit [3:0]: These bits select IRQ resource for MINT (PS2 Mouse)

CRF0 (Default 0x83)

Bit 7 - 6: KBC clock rate selection

= 00 Select 6MHz as KBC clock input.

= 01 Select 8MHz as KBC clock input.

= 10 Select 12Mhz as KBC clock input.

= 11 Select 16Mhz as KBC clock input.

Bit 5 - 3: Reserved.

Bit 2: = 0 Port 92 disable.

= 1 Port 92 enable.

Bit 1: = 0 Gate20 software control.

= 1 Gate20 hardware speed up.

Bit 0: = 0 KBRST software control.

= 1 KBRST hardware speed up.

11.7 Logical Device 7 (GP I/O Port I)

CR30 (Default 0x00)

Bit 7 - 1: Reserved.

Bit 0: = 1 Activates the logical device.

= 0 Logical device is inactive.

CR60, CR 61 (Default 0x00, 0x00)

These two registers select GP1 I/O base address [0x100:0xFFF] on 1 byte boundary.

CR62, CR 63 (Default 0x00, 0x00)

These two registers select GP14 alternate function Primary I/O base address [0x100:0xFFE] on 2 byte boundary; They are available as you setting GP14 to be an alternate function (General Purpose Address Decode).

CR64, CR 65 (Default 0x00, 0x00)

These two registers select GP15 alternate function Primary I/O base address [0x100:0xFFF] on 1 byte boundary; They are available as you setting GP15 to be an alternate function (General Purpose Write Decode).

CR70 (Default 0x00)

Bit 7 - 4: Reserved.

Bit 3 - 0: These bits select IRQ resource for GP10 as you setting GP10 to be an alternate function (Interrupt Steering).

CR72 (Default 0x00)

Bit 7 - 4: Reserved.

Bit 3 - 0: These bits select IRQ resource for GP11 as you setting GP11 to be an alternate function (Interrupt Steering).

CRE0 (GP10, Default 0x01)

Bit 7 - 5: Reserved.

Bit 4: IRQ Filter Select

= 1 Debounce Filter Enabled

= 0 Debounce Filter Bypassed

Bit 3: Select Function.

= 1 Select Alternate Function: Interrupt Steering.

= 0 Select Basic I/O Function.

Bit 2: Reserved.

Bit 1: Polarity.

= 1 Invert.

= 0 No Invert.

Bit 0: In/Out selection.
= 1 Input.
= 0 Output.

CRE1 (GP11, Default 0x01)

Bit 7 - 5: Reserved.
Bit 4: IRQ Filter Select
= 1 Debounce Filter Enabled
= 0 Debounce Filter Bypassed
Bit 3: Select Function.
= 1 Select Alternate Function: Interrupt Steering.
= 0 Select Basic I/O Function.
Bit 2: Reserved.
Bit 1: Polarity.
= 1 Invert.
= 0 No Invert.
Bit 0: In/Out selection.
= 1 Input.
= 0 Output.

CRE2 (GP12, Default 0x01)

Bit 7 - 5: Reserved.
Bit 4 - 3: Select Function.
= 00 Select Basic I/O function.
= 01 Select 1st alternate function: Watch Dog Timer Output.
= 10 Reserved
= 11 Reserved
Bit 2: Reserved.
Bit 1: Polarity: 1: Invert, 0: No Invert
Bit 0: In/Out: 1: Input, 0: Output

CRE3 (GP13, Default 0x01)

Bit 7 - 5: Reserved.
Bit 4 - 3: Select Function.
= 00 Select Basic I/O function.
= 01 Select 1st alternate function: Power LED output.
= 10 Reserved
= 11 Reserved
Bit 2: Reserved.
Bit 1: Polarity: 1: Invert, 0: No Invert
Bit 0: In/Out: 1: Input, 0: Output

CRE4 (GP14, Default 0x01)

Bit 7 - 5: Reserved.
Bit 4 - 3: Select Function.
= 00 Select Basic I/O function.
= 01 Select 1st alternate function: General Purpose Address Decoder(Active Low when Bit 1 = 0, Decode two byte address).
= 10 Select 2nd alternate function: Keyboard Inhibit(P17).
= 11 Reserved
Bit 2: Reserved.
Bit 1: Polarity: 1: Invert, 0: No Invert
Bit 0: In/Out: 1: Input, 0: Output

CRE5 (GP15, Default 0x01)

Bit 7 - 5: Reserved.
Bit 4 - 3: Select Function.
= 00 Select Basic I/O function.
= 01 General Purpose Write Strobe(Active Low when Bit 1 = 0).
= 10 8042 P12.
= 11 Reserved
Bit 2: Reserved.
Bit 1: Polarity: 1: Invert, 0: No Invert
Bit 0: In/Out: 1: Input, 0: Output

CRE6 (GP16, Default 0x01)

Bit 7 - 5: Reserved.
Bit 4 - 3: Select Function.
= 00 Select Basic I/O function.
= 01 Select 1st alternate function: Watch Dog Timer Output.
= 1x Reserved
Bit 2: Reserved.
Bit 1: Polarity: 1: Invert, 0: No Invert
Bit 0: In/Out: 1: Input, 0: Output

CRE7 (GP17, Default 0x01)

Bit 7 - 4: Reserved.
Bit 4 - 3: Select Function.
= 00 Select Basic I/O function.
= 01 Select 1st alternate function: Power LED output. Please refer to TABLE C
= 1x Reserved
Bit 2: Reserved.
Bit 1: Polarity: 1: Invert, 0: No Invert
Bit 0: In/Out: 1: Input, 0: Output

TABLE C

WDT_CTRL1* BIT[1]*	WDT_CTRL0* BIT[3]	WDT_CTRL1 BIT[0]	POWER LED STATE
1	X	X	1 Hertz Toggle pulse
0	0	X	Continuous high or low*
0	1	0	Continuous high or low*
0	1	1	1 Hertz Toggle pulse

*Note: 1). Regarding to the contents of WDT_CTR1 and WDT_CTRL0, please refer to CRF3 and CRF4 in Logic Device 8.

2). Continuous high or low depends on the polarity bit of GP13 or GP17 configure registers.

CRF1 (Default 0x00)

General Purpose Read/Write Enable*

Bit 7 - 2: Reserved

Bit 1:

= 1 Enable General Purpose Write Strobe

= 0 Disable General Purpose Write Strobe

Bit 0:

= 1 Enable General Purpose Address Decode

= 0 Disable General Purpose Address Decode

*Note: If the logical device's activate bit is not set then bit 0 and 1 have no effect.

11.8 Logical Device 8 (GP I/O Port II)

CR30 (Default 0x00)

Bit 7 - 1: Reserved.

Bit 0: = 1 Activates the logical device.

= 0 Logical device is inactive.

CR60, CR 61 (Default 0x00, 0x00)

These two registers select GP2 & Watch Dog I/O base address [0x100:0xFFE] on 2 byte boundary. I/O base address + 1: Watch Dog I/O base address.

CR70 (Default 0x00)

Bit 7 - 4: Reserved.

Bit 3 - 0: These bits select IRQ resource for Common IRQ of GP20~GP26 at Logic Device 8.

CR72 (Default 0x00)

Bit 7 - 4: Reserved.

Bit 3 - 0: These bits select IRQ resource for Watch Dog.

CRE8 (GP20, Default 0x01)

Bit 7 - 5: Reserved.

Bit 4 - 3: Select Function.

= 00 Select basic I/O function

= 01 Reserved

= 10 Select alternate function: Keyboard Reset (connected to KBC P20)

= 11 Reserved

Bit 2: Int En

= 1 Enable Common IRQ

= 0 Disable Common IRQ

Bit 1: Polarity: 1: Invert, 0: No Invert

Bit 0: In/Out: 1: Input, 0: Output

CRE9 (GP21, Default 0x01)

Bit 7 - 5: Reserved

Bit 4 - 3: Select Function.

= 00 Select Basic I/O function

= 01 Reserved

= 10 Select 2nd alternate function: Keyboard P13 I/O

= 11 Reserved

Bit 2: Int En

= 1 Enable Common IRQ

= 0 Disable Common IRQ

Bit 1: Polarity: 1: Invert, 0: No Invert

Bit 0: In/Out: 1: Input, 0: Output

CREA (GP22, Default 0x01)

Bit 7 - 5: Reserved.

Bit 4 - 3: Select Function.

= 00 Select Basic I/O function.

= 01 Reserved

= 10 Select 2nd alternate function: Keyboard P14 I/O.

= 11 Reserved

Bit 2: Int En

= 1 Enable Common IRQ

= 0 Disable Common IRQ

Bit 1: Polarity: 1: Invert, 0: No Invert

Bit 0: In/Out: 1: Input, 0: Output¡@¡@

CREB (GP23, Default 0x01)

Bit 7 - 5: Reserved.

Bit 4 - 3: Select Function.

= 00 Select Basic I/O function

= 01 Reserved

= 10 Select 2nd alternate function: Keyboard P15 I/O

= 11 Reserved

Bit 2: Int En

= 1 Enable Common IRQ

= 0 Disable Common IRQ

Bit 1: Polarity: 1: Invert, 0: No Invert

Bit 0: In/Out: 1: Input, 0: Output¡@

CREC (GP24, Default 0x01)

Bit 7 - 5: Reserved.

Bit 4 - 3: Select Function.

= 00 Select Basic I/O function

= 01 Reserved

= 10 Select 2nd alternate function: Keyboard P16 I/O

= 11 Reserved

Bit 2: Int En

= 1 Enable Common IRQ

= 0 Disable Common IRQ

Bit 1: Polarity: 1: Invert, 0: No Invert

Bit 0: In/Out: 1: Input, 0: Output

CRED (GP25, Default 0x01)

Bit 7 - 4: Reserved.

Bit 3: Select Function.

= 1 Select alternate function: GATE A20(Connect to KBC P21).

= 0 Select basic I/O function

Bit 2: Int En

= 1 Enable Common IRQ

= 0 Disable Common IRQ

Bit 1: Polarity: 1: Invert, 0: No Invert

Bit 0: In/Out: 1: Input, 0: Output

CREE (GP26, Default 0x01)

Bit 7 - 3: Reserved.

Bit 2: Int En

= 1 Enable Common IRQ

= 0 Disable Common IRQ

Bit 1: Polarity: 1: Invert, 0: No Invert

Bit 0: In/Out: 1: Input, 0: Output

CRF0 (Default 0x00)

Debounce Filter Enable or Disable for General Purpose I/O Combined Interrupt. The Debounce Filter can reject a pulse with 1ms width or less.

Bit 7 - 4: Reserved

Bit 3: GP Common IRQ Filter Select

= 1 Debounce Filter Enabled

= 0 Debounce Filter Bypassed

Bit 2 - 0: Reserved

CRF1 (Reserved)

CRF2 (Default 0x00)

Watch Dog Timer Time-out value. Writing a non-zero value to this register causes the counter to load the value to Watch Dog Counter and start to count down. If the Bit2 and Bit 1 are set, any Mouse Interrupt or Keyboard Interrupt happen will also cause to reload the non-zero value to Watch Dog Counter and count down. Read this register can not access Watch Dog Timer Time-out value, but can access the current value in Watch Dog Counter.

Bit 7 - 0:

= 0x00 Time-out Disable

= 0x01 Time-out occurs after 1 minute

= 0x02 Time-out occurs after 2 minutes

= 0x03 Time-out occurs after 3 minutes

.....

= 0xFF Time-out occurs after 255 minutes

CRF3 (WDT_CTRL0, Default 0x00)

Watch Dog Timer Control Register #0

Bit 7 - 4: Reserved

Bit 3: When Time-out occurs, Enable or Disable Power LED with 1 Hz and 50% duty cycle output.

= 1 Enable

= 0 Disable

Bit 2: Mouse interrupt reset Enable or Disable

= 1 Watch Dog Timer is reset upon a Mouse interrupt

= 0 Watch Dog Timer is not affected by Mouse interrupt

Bit 1: Keyboard interrupt reset Enable or Disable

= 1 Watch Dog Timer is reset upon a Keyboard interrupt

= 0 Watch Dog Timer is not affected by Keyboard interrupt

Bit 0: Reserved.

CRF4 (WDT_CTRL1, Default 0x00)

Watch Dog Timer Control Register #1

Bit 7 - 4: Reserved

Bit 3: Enable the rising edge of Keyboard Reset(P20) to force Time-out event, R/W*

= 1 Enable

= 0 Disable

Bit 2: Force Watch Dog Timer Time-out, Write only*

= 1 Force Watch Dog Timer time-out event; this bit is self-clearing.

Bit 1: Enable Power LED 1Hz rate toggle pulse with 50% duty cycle , R/W

= 1 Enable

= 0 Disable

Bit 0: Watch Dog Timer Status, R/W

= 1 Watch Dog Timer time-out occurred.

= 0 Watch Dog Timer counting

*Note: 1). Internal logic provides an 1us Debounce Filter to reject the width of P20 pulse less than 1us.

2). The P20 signal that coming from Debounce Filter is ORed with the signal generated by the Force Time-out bit and then connect to set the Bit 0(Watch Dog Timer Status). The ORed signal is self-clearing.

11.9 Logical Device 9 (GP I/O Port III)

CR30 (Default 0x00)

Bit 7 - 1: Reserved.

Bit 0: = 1 Activates the logical device.

= 0 Logical device is inactive.

CR60, CR 61 (Default 0x00, 0x00)

These two registers select GP3 I/O base address [0x100:0xFFF] on 1 byte boundary.

CR62, CR 63 (Default 0x00, 0x00)

These two registers select GP32 alternate function Primary I/O base address [0x100:0xFFE] on 2-byte boundary; They are available as you setting GP32 to be an alternate function (General Purpose Address Decode).

CR64, CR 65 (Default 0x00, 0x00)

These two registers select GP33 alternate function Primary I/O base address [0x100:0xFFF] on 2-byte boundary; They are available as you setting GP33 to be an alternate function (General Purpose Address Decode).

CR70 (Default 0x00)

Bit 7 - 4: Reserved.

Bit 3 - 0: These bits select IRQ resource for GP30 as you setting GP30 to be an alternate function (Interrupt Steering).

CR72 (Default 0x00)

Bit 7 - 4: Reserved.

Bit 3 - 0: These bits select IRQ resource for GP31 as you setting GP31 to be an alternate function (Interrupt Steering).

CRE0 (GP30, Default 0x01)

Bit 7 - 5: Reserved.

Bit 4: IRQ Filter Select

= 1 Debounce Filter Enabled.

= 0 Debounce Filter Bypassed.

Bit 3: Select Function.

= 1 Select Alternate Function: Interrupt Steering.

= 0 Select Basic I/O Function.

Bit 2: Reserved.

Bit 1: Polarity.

= 1 Invert.

= 0 No Invert.

Bit 0: In/Out selection.

= 1 Input.

= 0 Output.

CRE1 (GP31, Default 0x01)

Bit 7 - 5: Reserved.

Bit 4: IRQ Filter Select

= 1 Debounce Filter Enabled

= 0 Debounce Filter Bypassed

Bit 3: Select Function.

= 1 Select Alternate Function: Interrupt Steering.

= 0 Select Basic I/O Function.

Bit 2: Reserved.

Bit 1: Polarity.

= 1 Invert.

= 0 No Invert.

Bit 0: In/Out selection.

= 1 Input.

= 0 Output.

CRE2 (GP32, Default 0x01)

Bit 7 - 4: Reserved.

Bit 3: Select Function.

= 1 Select Alternate Function: General Purpose Address Decode.

= 0 Select Basic I/O Function.

Bit 2: Reserved.

Bit 1: Polarity: 1: Invert, 0: No Invert

Bit 0: In/Out: 1: Input, 0: Output

CRE3 (GP33, Default 0x01)

Bit 7 - 4: Reserved.

Bit 3: Select Function.

= 1 Select Alternate Function: General Purpose Address Decode.

= 0 Select Basic I/O Function.

Bit 2: Reserved.
Bit 1: Polarity: 1: Invert, 0: No Invert
Bit 0: In/Out: 1: Input, 0: Output

CRE4 (GP34, Default 0x01)

Bit 7 - 4: Reserved.
Bit 3: Select Function.
= 1 Select Alternate Function: Watch Dog Timer output.
= 0 Select Basic I/O Function.
Bit 2: Reserved.
Bit 1: Polarity: 1: Invert, 0: No Invert
Bit 0: In/Out: 1: Input, 0: Output

CRE5 (GP35, Default 0x01)

Bit 7 - 2: Reserved.
Bit 1: Polarity: 1: Invert, 0: No Invert
Bit 0: In/Out: 1: Input, 0: Output

CRE6 (GP36, Default 0x01)

Bit 7 - 2: Reserved.
Bit 1: Polarity: 1: Invert, 0: No Invert
Bit 0: In/Out: 1: Input, 0: Output

CRE7 (GP37, Default 0x01)

Bit 7 - 2: Reserved.
Bit 1: Polarity: 1: Invert, 0: No Invert
Bit 0: In/Out: 1: Input, 0: Output

CRF1 (Default 0x00)

Bit 7 - 3: Reserved
Bit 2: SERIRQ
= 0 The IRQ system is in normal mode.
= 1 The IRQ system is in serial IRQ mode.
Bit 1:
= 1 Enable GP33 General Purpose Address Decode.
= 0 Disable GP33 General Purpose Address Decode.
Bit 0:
= 1 Enable GP32 General Purpose Address Decode.
= 0 Disable GP32 General Purpose Address Decode.

*Note: If the logical device's activate bit is not set then bit 0 and 1 have no effect.

11.10 Logical Device A (ACPI)

CR30 (Default 0x00)

Bit 7 - 1: Reserved.

Bit 0: = 1 Activates the logical device.

= 0 Logical device is inactive.

CR60, CR 61 (Default 0x00, 0x00)

These two registers select PM1 register block base address [0x100:0xFF0] on 16-byte boundary.

CR62, CR 63 (Default 0x00, 0x00)

These two registers select GPE0 register block base address [0x100:0xFFC] on 4-byte boundary.

CR64, CR 65 (Default 0x00, 0x00)

These two registers select GPE1 register block base address [0x100:0xFFC] on 4-byte boundary.

CR70 (Default 0x00)

Bit 7 - 4: Reserved.

Bit 3 - 0: These bits select IRQ resource for $\overline{SCI}$.

CRE0 (Default 0x00)

Bit 7: DIS-PANSWIN. Disable panel switch input to turn system power supply on.

= 0 $\overline{PANSWIN}$ is wire-ANDed and connected to $\overline{PANSWOUT}$.

= 1 $\overline{PANSWIN}$ is blocked and can not affect $\overline{PANSWOUT}$.

Bit 6: ENKBWAKEUP. Enable Keyboard to wake-up system via $\overline{PANSWOUT}$.

= 0 Disable Keyboard wake-up function.

= 1 Enable Keyboard wake-up function.

Bit 5: ENMSWAKEUP. Enable Mouse to wake-up system via $\overline{PANSWOUT}$.

= 0 Disable Mouse wake-up function.

= 1 Enable Mouse wake-up function.

Bit 4: MSRKEY. Select Mouse Left/Right Botton to wake-up system via $\overline{PANSWOUT}$.

= 0 Select click on Mouse Left-botton twice to wake the system up.

= 1 Select click on Mouse right-botton twice to wake the system up.

Bit 3: Reserved.

Bit 2: KB/MS Swap. Enable Keyboard/Mouse port-swap.

= 0 Keyboard/Mouse ports are not swapped.

= 1 Keyboard/Mouse ports are swapped.

Bit 1: MSXKEY. Enable any character received from Mouse to wake-up the system.

= 0 Just clicking Mouse left/right-botton twice can wake the system up.

= 1 Any character received from Mouse can wake the system up (the setting of Bit 4 is ignored).

Bit 0: KBXKEY. Enable any character received from Keyboard to wake-up the system.

= 0 Only predetermined specific key combination can wake up the system.

= 1 Any character received from Keyboard can wake up the system.

CRE1 (Default 0x00) Keyboard Wake-up Index Register

This register is used to indicate which Keyboard Wake-up Shift register or Predetermined key Register is to be read/written via CRE2.

CRE2 Keyboard Wake-up Data Register

CRE3 (Read only) Keyboard/Mouse Wake-up Status Register

Bit 7-3: Reserved.

Bit 2: PANSW_STS. The Panel switch event is caused by $\overline{\text{PANSWIN}}$. This bit is cleared by reading this register.

Bit 1: Mouse_STS. The Panel switch event is caused by Mouse wake-up event. This bit is cleared by reading this register.

Bit 0: Keyboard_STS. The Panel switch event is caused by Keyboard wake-up event. This bit is cleared by reading this register.

CRE4 This Register is reserved for test.

CRF0 (Default 0x00)

Bit 7: CHIPPME. Chip level power management enable.

= 0 disable the ACPI/Legacy and the auto power management functions

= 1 enable the ACPI/Legacy and the auto power management functions.

Bit 6 - 4: Reserved. Return zero when read.

Bit 3: PRTPME. Printer port power management enable.

= 0 disable the auto power management functions.

= 1 enable the auto power management functions provided CRF0.bit7 (CHIPPME) is also set to 1.

Bit 2: FDCPME. FDC power management enable.

= 0 disable the auto power management functions.

= 1 enable the auto power management functions provided CRF0.bit7 (CHIPPME) is also set to 1.

Bit 1: URAPME. UART A power management enable.

= 0 disable the auto power management functions.

= 1 enable the auto power management functions provided CRF0.bit7 (CHIPPME) is also set to 1.

Bit 0: URBPME. UART B power management enable.

= 0 disable the auto power management functions.

= 1 enable the auto power management functions provided CRF0.bit7 (CHIPPME) is also set to 1.

CRF1 (Default 0x00)

Bit 7 - 4: Reserved. Return zero when read.

Bit 3 - 0: Devices' idle status.

These bits indicate that the individual device's idle timer expires due to no I/O access, no IRQ, and no external input to the device. These 4 bits are controlled by the printer port, FDC, UART A, and UART B power down machines individually. Writing a 1 clears this bit, and writing a 0 has no effect. Note that: the user is not supposed to change the status while the power management function is enabled.

Bit 3: PRTIDLSTS. Printer port idle status.

= 0 printer port is now in the working state.

= 1 printer port is now in the sleeping state due to no printer port access, no IRQ, no DMA acknowledge, and no transition on BUSY, $\overline{ACK}$, PE, SLCT, and $\overline{ERR}$ pins in a preset expiry time period.

Bit 2: FDCIDLSTS. FDC idle status.

= 0 FDC is now in the working state.

= 1 FDC is now in the sleeping state due to no FDC access, no IRQ, no DMA acknowledge, and no enabling of the motor enable bits in the DOR register in a preset expiry time period.

Bit 1: URAIDLSTS. UART A idle status.

= 0 UART A is now in the working state.

= 1 UART A is now in the sleeping state due to no UART A access, no IRQ, the receiver is now waiting for a start bit, the transmitter shift register is now empty, and no transition on MODEM control input lines in a preset expiry time period.

Bit 0: URBIDLSTS. UART B idle status.

= 0 UART B is now in the working state.

= 1 UART B is now in the sleeping state due to no UART A access, no IRQ, the receiver is now waiting for a start bit, the transmitter shift register is now empty, and no transition on MODEM control input lines in a preset expiry time period.

CRF2 (Default 0x00)

Bit 7 - 4: Reserved. Return zero when read.

Bit 3 - 0: Devices' trap status.

These bits indicate that the individual device wakes up due to any I/O access, IRQ, and external input to the device. The device's idle timer reloads the preset expiry depending on which device wakes up. These 4 bits are controlled by the printer port, FDC, UART A, and UART B power down machines respectively. Writing a 1 clears this bit, and writing a 0 has no effect. Note that: the user is not supposed to change the status while power management function is enabled.

Bit 3: PRTTRAPSTS. Printer port trap status.

= 0 the printer port is now in the sleeping state.

= 1 the printer port is now in the working state due to any printer port access, any IRQ, any DMA acknowledge, and any transition on BUSY, $\overline{ACK}$, PE, SLCT, and $\overline{ERR}$ pins.

Bit 2: FDCTRAPSTS. FDC trap status.

= 0 FDC is now in the sleeping state.

= 1 FDC is now in the working state due to any FDC access, any IRQ, any DMA acknowledge, and any enabling of the motor enable bits in the DOR register.

Bit 1: URATRAPSTS. UART A trap status.

= 0 UART A is now in the sleeping state.

= 1 UART A is now in the working state due to any UART A access, any IRQ, the receiver begins receiving a start bit, the transmitter shift register begins transmitting a start bit, and any transition on MODEM control input lines.

Bit 0: URBTRAPSTS. UART B trap status.

= 0 UART B is now in the sleeping state.

= 1 UART B is now in the working state due to any UART B access, any IRQ, the receiver begins receiving a start bit, the transmitter shift register begins transmitting a start bit, and any transition on MODEM control input lines.

CRF3 (Default 0x00)

Bit 7 - 6: Reserved. Return zero when read.

Bit 5 - 0: Device's IRQ status.

These bits indicate the IRQ status of the individual device. The device's IRQ status bit is set by their source device and is cleared by writing a 1. Writing a 0 has no effect.

Bit 5: MOUIRQSTS. MOUSE IRQ status.

Bit 4: KBCIRQSTS. KBC IRQ status.

Bit 3: PRTIRQSTS. printer port IRQ status.

Bit 2: FDCIRQSTS. FDC IRQ status.

Bit 1: URAIRQSTS. UART A IRQ status.

Bit 0: URBIRQSTS. UART B IRQ status.

CRF4 (Default 0x00)

Bit 7 - 4: Reserved. Return zero when read.

Bit 3 - 0: Enable bits of the $\overline{\text{SMI}}$ generation due to the device's idleness.

These bits enable the generation of an $\overline{\text{SMI}}$ interrupt due to the expiration of the device's idle timer. These 4 bits control the printer port, FDC, UART A, and UART B $\overline{\text{SMI}}$ logics respectively.

Bit 3: PRTIDLEN.

= 0 disable the generation of an $\overline{\text{SMI}}$ interrupt due to printer port's idleness.

= 1 enable the generation of an $\overline{\text{SMI}}$ interrupt due to printer port's idleness.

Bit 2: FDCIDLEN.

= 0 disable the generation of an $\overline{\text{SMI}}$ interrupt due to FDC's idleness.

= 1 enable the generation of an $\overline{\text{SMI}}$ interrupt due to FDC's idleness.

Bit 1: URAIDLEN.

= 0 disable the generation of an $\overline{SMI}$ interrupt due to UART A's idleness.

= 1 enable the generation of an $\overline{SMI}$ interrupt due to UART A's idleness.

Bit 0: URBIDLEN.

= 0 disable the generation of an $\overline{SMI}$ interrupt due to UART B's idleness.

= 1 enable the generation of an $\overline{SMI}$ interrupt due to UART B's idleness.

CRF5 (Default 0x00)

Bit 7 - 4: Reserved. Return zero when read.

Bit 3 - 0: Enable bits of the $\overline{SMI}$ generation due to device's trap.

These bits enable the generation of an $\overline{SMI}$ interrupt due to any I/O access, IRQ, and external input to the device. These 4 bits control the printer port, FDC, UART A, and UART B SMI logics respectively.

Bit 3: PRTTRAPEN.

= 0 disable the generation of an $\overline{SMI}$ interrupt due to printer port's trap.

= 1 enable the generation of an $\overline{SMI}$ interrupt due to printer port's trap.

Bit 2: FDCTRAPEN.

= 0 disable the generation of an $\overline{SMI}$ interrupt due to FDC's trap.

= 1 enable the generation of an $\overline{SMI}$ interrupt due to FDC's trap.

Bit 1: URATRAPEN.

= 0 disable the generation of an $\overline{SMI}$ interrupt due to UART A's trap.

= 1 enable the generation of an $\overline{SMI}$ interrupt due to UART A's trap.

Bit 0: URBTRAPEN.

= 0 disable the generation of an $\overline{SMI}$ interrupt due to UART B's trap.

= 1 enable the generation of an $\overline{SMI}$ interrupt due to UART B's trap.

CRF6 (Default 0x00)

Bit 7 - 6: Reserved. Return zero when read.

Bit 5 - 0: Enable bits of the $\overline{SMI}$ generation due to the device's IRQ.

These bits enable the generation of an $\overline{SMI}$ interrupt due to any IRQ of the devices. These 4 bits control the printer port, FDC, UART A, and UART B $\overline{SMI}$ logics respectively. The $\overline{SMI}$ logic output for the IRQs is as follows:

$\overline{SMI}$ logic output = (URBIRQEN and URBIRQSTS) or (URAIRQEN and URAIRQSTS) or
(FDCIRQEN and FDCIRQSTS) or (PRTIRQEN and PRTIRQSTS)
(KBCIRQEN and KBCIRQSTS) or (MOUIRQEN and MOUIRQSTS)

Bit 5: MOUIRQEN.

= 0 disable the generation of an $\overline{SMI}$ interrupt due to MOUSE's IRQ.

= 1 enable the generation of an $\overline{SMI}$ interrupt due to MOUSE's IRQ.

Bit 4: KBCIRQEN.

= 0 disable the generation of an $\overline{SMI}$ interrupt due to KBC's IRQ.

= 1 enable the generation of an $\overline{SMI}$ interrupt due to KBC's IRQ.

Bit 3: PRTIRQEN.

= 0 disable the generation of an $\overline{SMI}$ interrupt due to printer port's IRQ.

= 1 enable the generation of an $\overline{SMI}$ interrupt due to printer port's IRQ.

Bit 2: FDCIRQEN.

= 0 disable the generation of an $\overline{SMI}$ interrupt due to FDC's IRQ.

= 1 enable the generation of an $\overline{SMI}$ interrupt due to FDC's IRQ.

Bit 1: URAIRQEN.

= 0 disable the generation of an $\overline{SMI}$ interrupt due to UART A's IRQ.

= 1 enable the generation of an $\overline{SMI}$ interrupt due to UART A's IRQ.

Bit 0: URBIRQEN.

= 0 disable the generation of an $\overline{SMI}$ interrupt due to UART B's IRQ.

= 1 enable the generation of an $\overline{SMI}$ interrupt due to UART B's IRQ.

CRF7 (Default 0x00)

Bit 7 - 1: Reserved. Return zero when read.

Bit 0: SMI_EN.

This bit is the $\overline{SMI}$ output pin enable bit. When an $\overline{SMI}$ event is raised on the output of the $\overline{SMI}$ logic, setting this bit enables the $\overline{SMI}$ interrupt to be generated on the pin $\overline{SMI}$. If this bit is cleared, only the IRQ status bit in CRF3 is set, and no SMI interrupt is generated on the pin $\overline{SMI}$.

= 0 Disable $\overline{SMI}$

= 1 Enable $\overline{SMI}$

CRFE, FF (Default 0x00)

Reserved for Winbond test.