7. GENERAL PURPOSE I/O

W83977TF provides 23 Input/Output ports that can be individually configured to perform a simple basic I/O function or a pre-defined alternate function. Those 23 GP I/O ports are divided into three groups, the first group contains 8 ports, the second group contains only 7 ports, and the third group contains 8 ports. Each port in first group corresponds to a configuration register in logical device 7, the second group in logical device 8, and the third group in logical device 9. Users can select those I/O ports functions by independently programming those configuration registers. Figure 7.1, 7.2, and 7.3 respectively show the GP I/O port's structure of logical device 7, 8, and 9. Right after Power-on reset, those ports default to perform basic I/O functions.

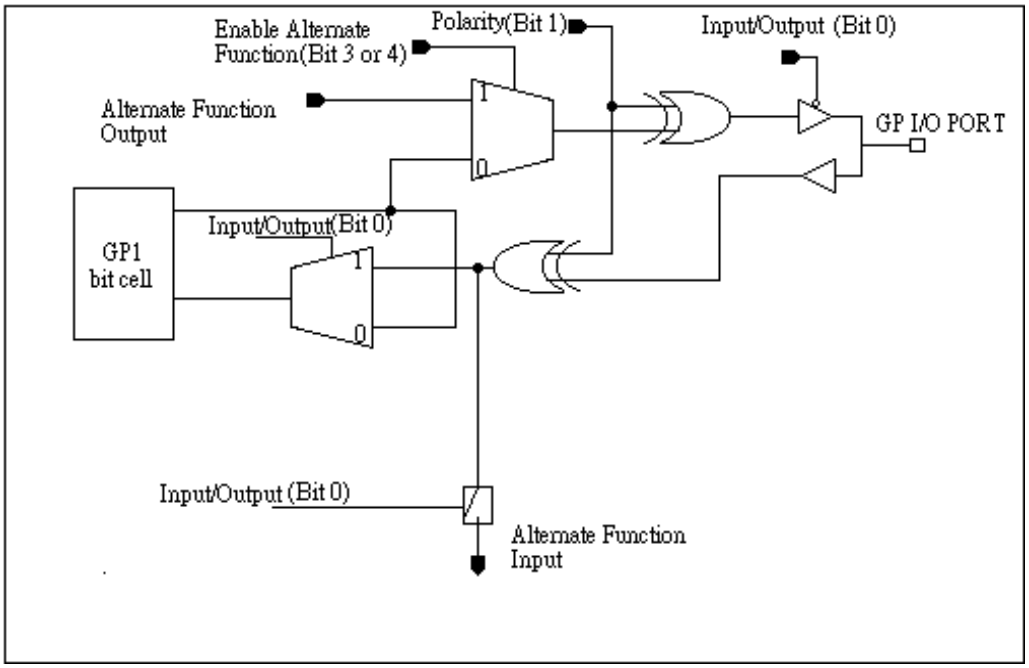


Figure 7.1

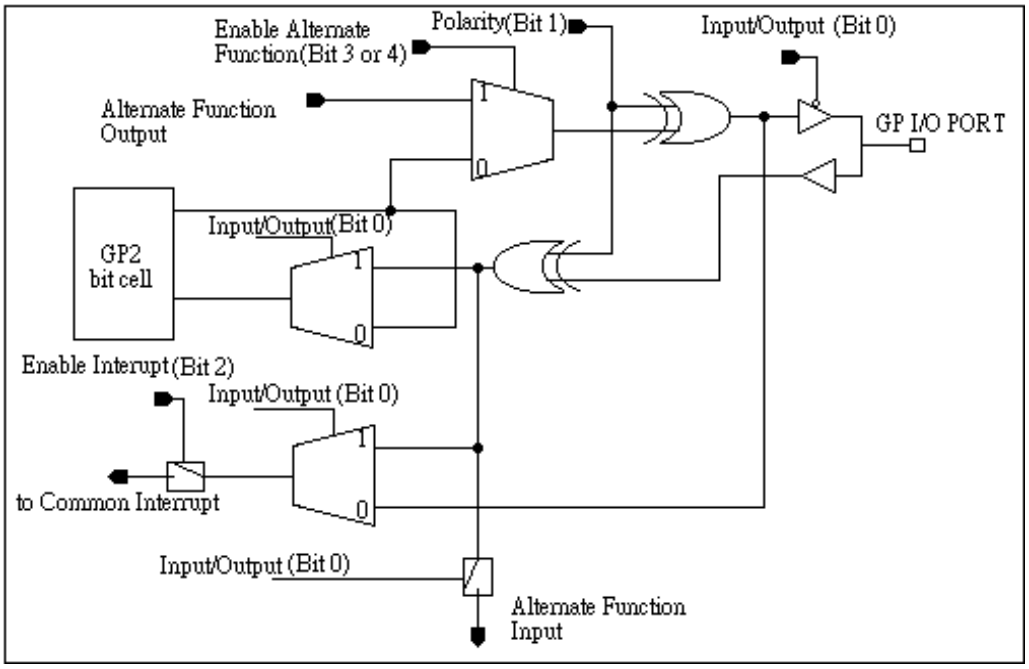


Figure 7.2

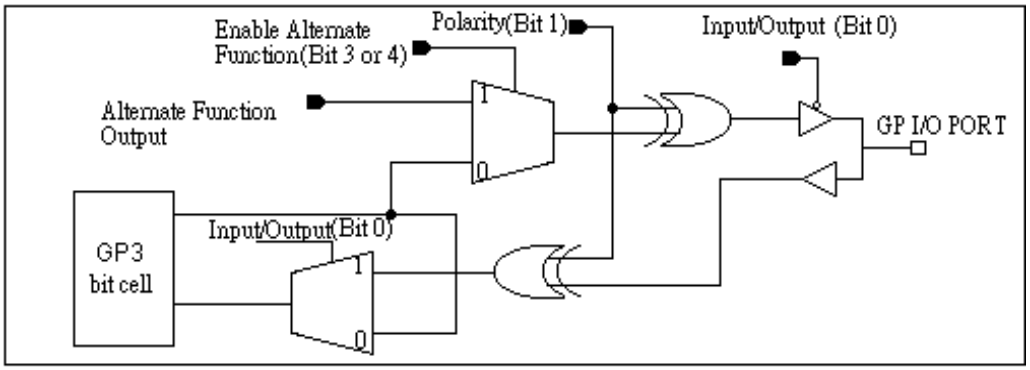


Figure 7.3

7.1 Basic I/O functions

The Basic I/O functions of W83977TF provide several I/O operations including driving a logic value to output port, latching a logic value from input port, inverting the input/output logic value, and steering Common Interrupt (only available in the second group of the GP I/O port). Common Interrupt is the ORed function of all interrupt channels in the second group of the GP I/O ports, and it also connects to a 1mS debounce filter which can reject a noise of 1 mS pulse width or less. There are three 8-bit registers (GP1, GP2, and GP3) which are directly connected to those GP I/O ports. Each GP I/O port is represented as a bit in one of three 8-bit registers. Only 6 bits of GP2 are implemented. Table 7.1.1 shows their combinations of Basic I/O functions, and Table 7.1.2 shows the register bit assignments of GP1, GP2, and GP3.

Table 7.1.1

I/O BIT 0 = OUTPUT 1 = INPUT	ENABLE INT BIT 0 = DISABLE 1 = ENABLE	POLARITY BIT 0 = NON INVERT 1 = INVERT	BASIC I/O OPERATIONS
0	0	0	Basic non-inverting output
0	0	1	Basic inverting output
0	1	0	Non-inverted output bit value of GP2 drive to Common Interrupt
0	1	1	Inverted output bit value of GP2 drive to Common Interrupt
1	0	0	Basic non-inverting input
1	0	1	Basic inverting input
1	1	0	Non-inverted input drive to Common Interrupt
1	1	1	Inverted input drive to Common Interrupt

Table 7.1.2

GP I/O PORT ACCESSED REGISTER	REGISTER BIT ASSIGNMENT	GP I/O PORT
GP1	BIT 0	GP10
	BIT 1	GP11
	BIT 2	GP12
	BIT 3	GP13
	BIT 4	GP14
	BIT 5	GP15
	BIT 6	GP16
	BIT 7	GP17
GP2	BIT 0	GP20
	BIT 1	GP21
	BIT 2	GP22
	BIT 3	GP23
	BIT 4	GP24
	BIT 5	GP25
	BIT 6	GP26
GP3	BIT 0	GP30
	BIT 1	GP31
	BIT 2	GP32
	BIT 3	GP33
	BIT 4	GP34
	BIT 5	GP35
	BIT 6	GP36
	BIT 7	GP37

7.2 Alternate I/O Functions

W83977TF provides several alternate functions which are scattered among the GP I/O ports. Table 7.2.1 shows their assignments. Polarity bit can also be set to alter their polarity.

Table 7.2.1

GP I/O PORT	ALTERNATE FUNCTION
GP10	Interrupt Steering
GP11	Interrupt Steering
GP12	Watch Dog Timer Output/IRRX input
GP13	Power LED output/IRTX output
GP14	General Purpose Address Decoder/Keyboard Inhibit(P17)
GP15	General Purpose Write Strobe/ 8042 P12
GP16	Watch Dog Timer Output
GP17	Power LED output
GP20	Keyboard Reset (8042 P20)
GP21	8042 P13
GP22	8042 P14
GP23	8042 P15
GP24	8042 P16
GP25	GATE A20 (8042 P21)
GP30	Interrupt Steering
GP31	Interrupt Steering
GP32	General Purpose Address Decoder
GP33	General Purpose Address Decoder
GP34	Watch Dog Timer Output

7.2.1 Interrupt Steering

GP10, GP11, GP30, and GP31 can be programmed to map their own interrupt channels. The selection of IRQ channel can be done in configuration registers CR70 and CR72 of logical device 7 and logical device 9. Each interrupt channel also has its own 1 mS debounce filter that is used to reject any noise whose width is equal to or less than 1 mS.

7.2.2 Watch Dog Timer Output

Watch Dog Timer contains a one minute resolution down counter, CRF2 of Logical Device 8, and two watch Dog control registers, WDT_CTRL0 and WDT_CTRL1 of Logical Device 8. The down counter can be programmed within the range from 1 to 255 minutes. Writing any new non-zero value to CRF2 or reset signal coming from a Mouse interrupt or Keyboard interrupt (CRF2 also contains non-zero value) will cause the Watch Dog Timer to reload and start to count down from the new value. As the counter reaches zero, (1) Watch Dog Timer time-out occurs and the bit 0 of WDT_CTRL1 will be set to logic 1; (2) Watch Dog interrupt output is asserted if the interrupt is enable in CR72 of logical device 8; and (3) Power LED starts to toggle output if the bit 3 of WDT_CTRL0 is enabled. WDT_CTRL1 also can be accessed through GP2 I/O base address + 1.

7.2.3 Power LED

The Power LED function provides 1 Hertz rate toggle pulse output with 50 percent duty cycle. Table 7.2.2 shows how to enable Power LED.

Table 7.2.2

WDT_CTRL1 BIT[1]	WDT_CTRL0 BIT[3]	WDT_CTRL1 BIT[0]	POWER LED STATE
1	X	X	1 Hertz Toggle pulse
0	0	X	Continuous high or low *
0	1	0	Continuous high or low *
0	1	1	1 Hertz Toggle pulse

* Note: Continuous high or low depends on the polarity bit of GP13 or GP17 configuration registers.

7.2.4 General Purpose Address Decoder

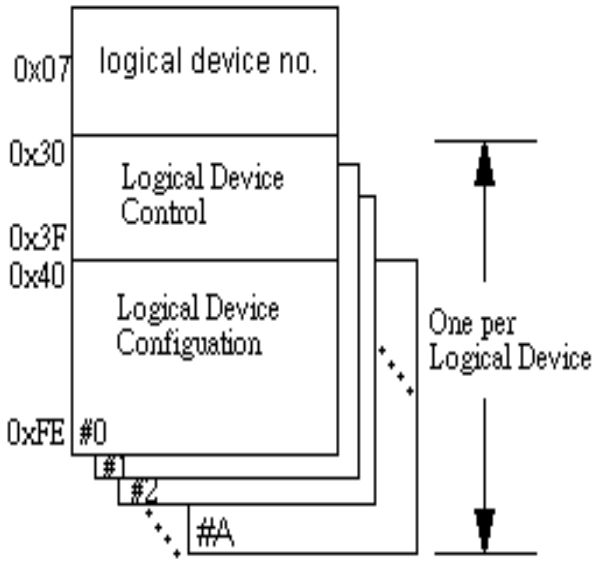
General Purpose Address Decoder provides two address decode as AEN equal to logic 0. The address base is stored at CR62, CR63 of logical device 7 for GP14 and at CR62-65 of logical device 9 for GP32 and GP33. The decoding output is normally active low. Users can alter its polarity through the polarity bit of the GP14, GP32, and GP33's configuration register.

7.2.5 General Purpose Write Strobe

General Purpose Write Strobe is an address decoder that performs like General Purpose Address Decoder, but it has to be qualified by $\overline{\text{IOW}}$ and AEN. Its output is normally active low. Users can alter its polarity through the polarity bit of the GP15's configuration register.

8. PLUG AND PLAY CONFIGURATION

The W83977TF uses Compatible PNP protocol to access configuration registers for setting up different types of configurations. In W83977TF, there are nine Logical Devices (from Logical Device 0 to Logical Device A with the exception of logical device 4 and 6 for compatibility) which correspond to nine individual functions: FDC (logical device 0), PRT (logical device 1), UART1 (logical device 2), UART2 (logical device 3), KBC (logical device 5), GPIO1 (logical device 7), GPIO2 (logical device 8), GPIO3 (logical device 9), and ACPI ((logical device A). Each Logical Device has its own configuration registers (above CR30). Host can access those registers by writing an appropriate logical device number into logical device select register at CR7.



8.1 Compatible PnP

8.1.1 Extended Function Registers

In Compatible PnP, there are two ways to enter Extended Function and read or write the configuration registers. HEFRAS (CR26 bit 6) can be used to select one out of these two methods of entering the Extended Function mode as follows:

HEFRAS	ADDRESS AND VALUE
0	write 87h to the location 3F0h twice
1	write 87h to the location 370h twice

After Power-on reset, the value on $\overline{\text{RTSA}}$ (pin 43) is latched by HEFRAS of CR26. In Compatible PnP, a specific value (87h) must be written twice to the Extended Functions Enable Register (I/O port address 3F0h or 370h). Secondly, an index value (02h, 07h-FFh) must be written to the Extended Functions Index Register (I/O port address 3F0h or 370h same as Extended Functions Enable Register) to identify which configuration register is to be accessed. The designer can then access the desired configuration register through the Extended Functions Data Register (I/O port address 3F1h or 371h).

After programming of the configuration register is finished, an additional value (AAh) should be written to EFERs to exit the Extended Function mode to prevent unintentional access to those configuration registers. The designer can also set bit 5 of CR26 (LOCKREG) to high to protect the configuration registers against accidental accesses.

The configuration registers can be reset to their default or hardware settings only by a cold reset (pin MR = 1). A warm reset will not affect the configuration registers.

8.1.2 Extended Functions Enable Registers (EFERs)

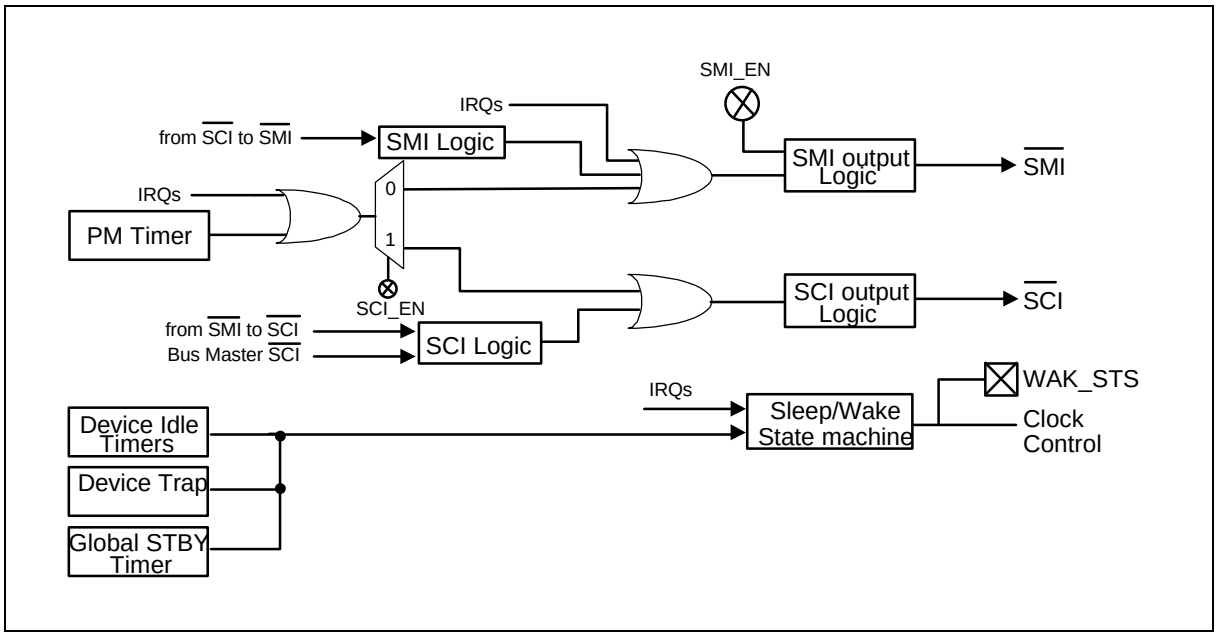
After a power-on reset, the W83977TF enters the default operating mode. Before the W83977TF enters the extended function mode, a specific value must be programmed into the Extended Function Enable Register (EFER) so that the extended function register can be accessed. The Extended Function Enable Registers are write-only registers. On a PC/AT system, their port addresses are 3F0h or 370h (as described in previous section).

8.1.3 Extended Function Index Registers (EFIRs), Extended Function Data Registers(EFDRs)

After the extended function mode is entered, the Extended Function Index Register (EFIR) must be loaded with an index value (02h, 07h-FEh) to access Configuration Register 0 (CR0), Configuration Register 7 (CR07) to Configuration Register FE (CRFE), and so forth through the Extended Function Data Register (EFDR). The EFIRs are write-only registers with port address 3F0h or 370h (as described in section 8.1.1) on PC/AT systems; the EFDRs are read/write registers with port address 3F1h or 371h (as described in section 8.1.1) on PC/AT systems.

9. ACPI REGISTERS FEATURES

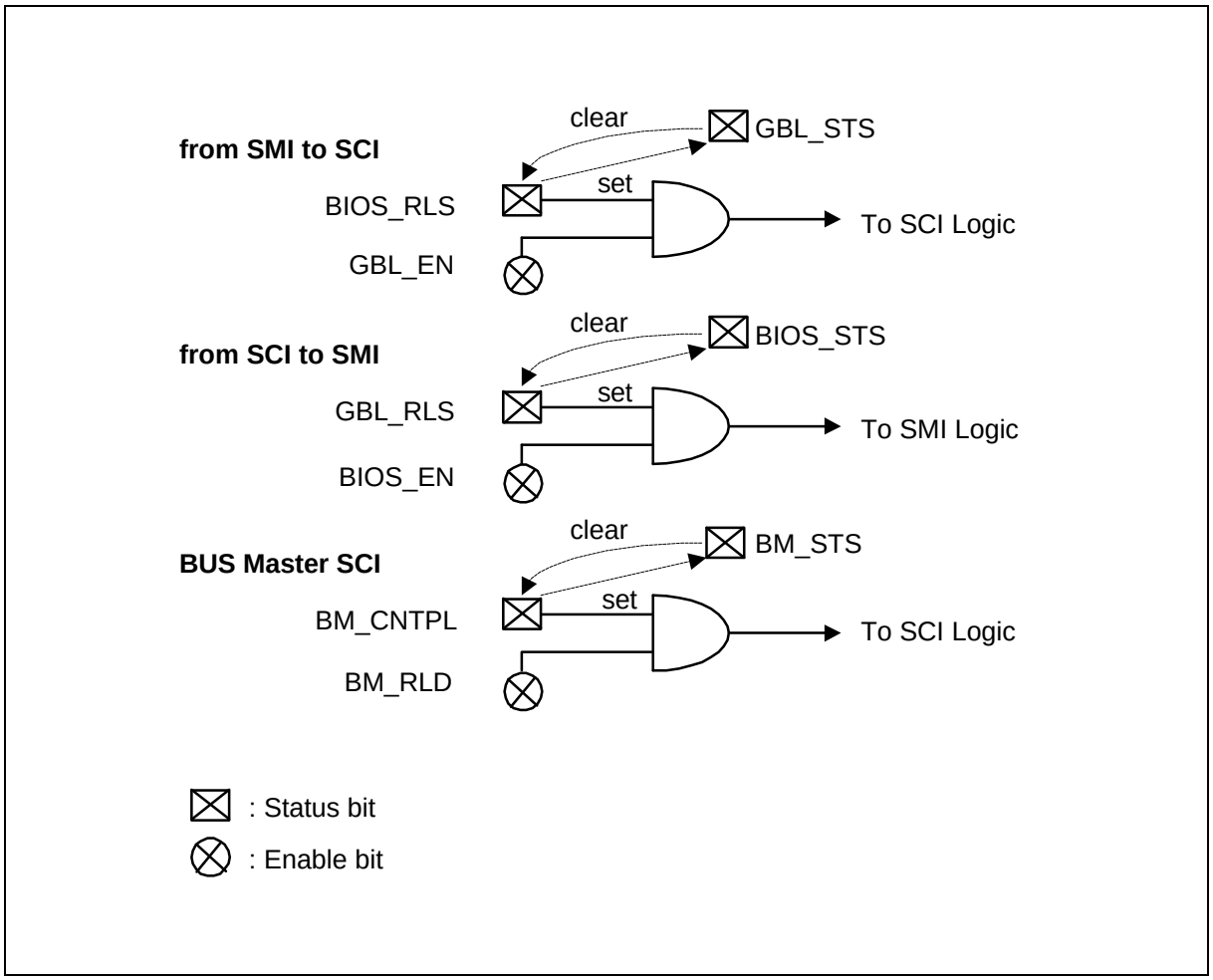
W83977TF supports both ACPI and legacy power managements. The switch logic of the power managment block generates an $\overline{SMI}$ interrupt in the legacy mode and an $\overline{SCI}$ interrupt in the ACPI mode. For the legacy mode, the SMI_EN bit is used. If it is set, it routes the power management events to the $\overline{SMI}$ interrupt logic. For the ACPI mode, the SCI_EN bit is used. If it is set, it route the power management events to the $\overline{SCI}$ interrupt logic. The SMI_EN bit is located in the configuration register block of Device A and the SCI_EN bit is located in the PM1 register block. See the following figure for illustration.



The $\overline{SMI}$ interrupt is routed to pin $\overline{SMI}$, which is dedicated for the $\overline{SMI}$ interrupt output. Another way to output the $\overline{SMI}$ interrupt is to route to pin IRQSER, which is the signal pin in the Serial IRQ mode. The $\overline{SCI}$ interrupt can be routed to pin $\overline{SCI}$, which is dedicated for the $\overline{SCI}$ function. Or it can be routed to one interrupt request pin, which is selected through CR70.bit3 - 0 of logical device 9. Another way is to output the $\overline{SCI}$ interrupt to pin IRQSER if serial IRQ mode is enabled.

9.1 SMI to SCI/SCI to SMI and Bus Master

The following figure illustrates the process of generating an interrupt from $\overline{SMI}$ to $\overline{SCI}$ or from $\overline{SCI}$ to $\overline{SMI}$.



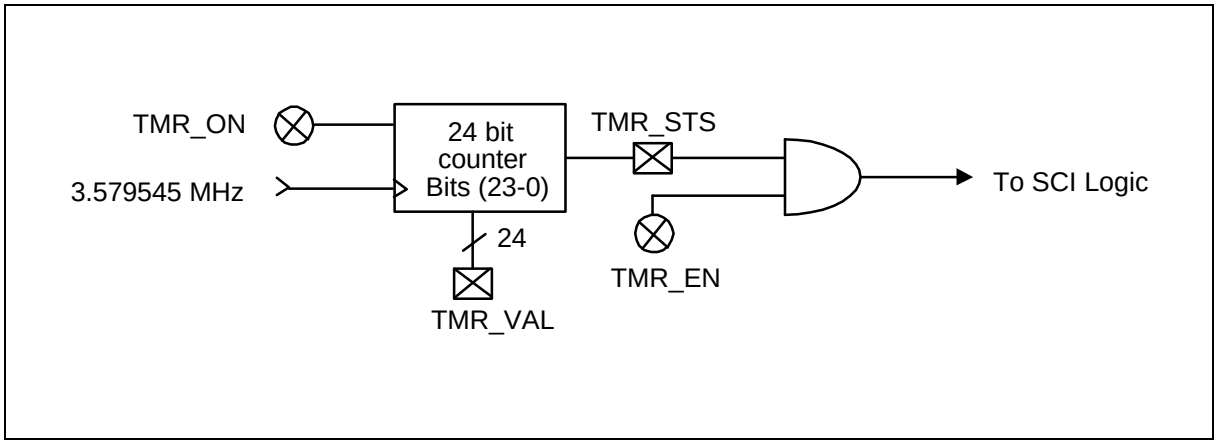
For the BIOS software to raise an event to the ACPI software, BIOS_RLS, GBL_EN, and GBL_STS bits are involved. GBL_EN is the enable bit and the GBL_STS is the status bit. Both are controlled by the ACPI software. If BIOS_RLS is set by the BIOS software and GBL_EN is set by the ACPI software, an $\overline{SCI}$ interrupt is raised. Writing a 1 to BIOS_RLS sets it to logic 1 and also sets GBL_STS to logic 1. Writing a 0 to BIOS_RLS has no effect. Wrinting a 1 to GBL_STS clears it to logic 0 and also clears BIOS_RLS to logic 0. Writing a 0 to GBL_STS has no effect.

For the ACPI software to raise an event to the BIOS software, GBL_RLS, BIOS_EN, and BIOS_STS bits are involved. BIOS_EN is the enable bit and the BIOS_STS is the status bit. Both are controlled by the BIOS software. If GBL_RLS is set by the ACPI software and BIOS_EN is set by the BIOS software, an $\overline{SMI}$ is raised. Writing a 1 to GBL_RLS sets it to logic 1 and also sets BIOS_STS to logic 1. Writing a 0 to GBL_RLS has no effect. Wrinting a 1 to BIOS_STS clears it to logic 0 and also clears GBL_RLS to logic 0. Writing a 0 to BIOS_STS has no effect.

For the bus master to raise an event to the ACPI software, BM_CNTRL, BM_RLD, and BM_STS bits are involved. Both BM_RLD and BM_STS are controlled by the ACPI software. If BM_CNTRL is set by the BIOS software and BM_RLD is set by the ACPI software, an $\overline{SCI}$ interrupt is raised. Writing a 1 to BM_CNTRL sets it to logic 1 and also sets BM_STS to logic 1. Writing a 0 to BM_CNTRL has no effect. Wrinting a 1 to BM_STS clears it to logic 0 and also clears BM_CNTRL to logic 0. Writing a 0 to BM_STS has no effect.

9.2 Power Management Timer

In the ACPI specification, it requires a power management timer. The power management timer is a 24-bit fixed rate free running up-count timer that runs off a 3.579545 MHZ clock. The power management timer corresponds to status bit (TMR_STS) and enable bit (TMR_EN). The TMR_STS bit is set any time the last bit of the timer (bit 23) goes from 0 to 1 or from 1 to 0. If the TMR_EN bit is set, the setting of the TMR_STS bit will generate an $\overline{SCI}$ interrupt. Three registers are used to read the timer value which are located in the PM1 register block. The power management timer has one enabel bit (TMR_ON) to turn ii on or off. The TMR_ON is located in GPE register block. If it is cleared to 0, the power management timer function would not work. There are no timer reset requirements, except that the timer should function after power-up. See the following figure for illustration.



9.3 ACPI Registers (ACPIRs)

The ACPI register model consists of the fixed register blocks that perform the ACPI functuions. A register block may be a event register block which deals with ACPI events or a control register block which deals with control features. The order in the event register block is a status register followed by an enable register.

Each event register, if implemented, contains two two register: a status register and an enable register, of 16 bits wide each. The status register indicates which event triggers the ACPI System Control Interrupt ($\overline{SCI}$). When the hardware event occurs, the corresponding status bit will be set. However, the corresponding enable bit is also required to be set before an $\overline{SCI}$ interrupt could be raised. If the enable bit is not set, the software can examine the state of the hardware event by reading the status bit without generating an $\overline{SCI}$ interrupt.

Any status bit, unless otherwise noted, can only be set by specific hardware event. It is cleared by writing a 1 to its bit position and writing a 0 has no effect. Except some special status bits, every status bit has the corresponding enable bit on the same bit position in the enable register. Those status bits which have no corresponding enable bit are read for special purpose. Reverved or unimplemented enable bits always return zero, and writing to these bits should has no effect.

The control bit in the control register provides some special control function over the hardware event, or some special control over $\overline{SCI}$ event. Reserved or unimplemented control bits always return zero, and writing to those bits should has no effect.

Table 9-1 (sec. 9.3.21) lists the PM1 register block and its registers. The base address of PM1 register block is named as PM1a_EVT_BLK in the ACPI specification and is specified in CR60, 61 of logical device A.

Table 9-2 (sec. 9.3.21) lists the GPE register block and its registers. The base address of general-purpose event block GPE0 is named as GPE0_BLK in the ACPI specification and is specified in CR62, 63 of logical device A. The base address of general-purpose event block GPE1 is named as GPE1_BLK in the ACPI specification and is specified in CR64, 65 of logical device A.

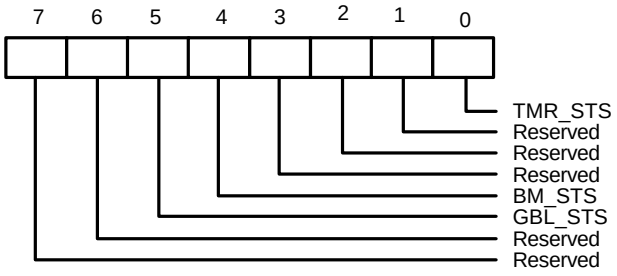
9.3.1 Power Management 1 Status Register 1 (PM1STS1)

Register Location: <CR60, 61> System I/O Space

Default Value: 00h

Attribute: Read/write

Size: 8 bits



BIT	NAME	DESCRIPTION
0	TMR_STS	This bit is the timer carry status bit. This bit is set anytime the bit 23 of the 24-bit counter changes (whenever the MSB changes from low to high or high to low). When TMR_EN and TMR_STS are set, a power magement event is raised. This bit is only set by hardware and can only be cleared by writing a 1 to this bit position. Writing a 0 has no effect.
1-3	Reserved	Reserved.
4	BM_STS	This is the bus master status bit. Writing a 1 to BM_CNTRL also sets BM_STS. Writing a 1 clears this bit and also clears BM_CNTRL. Writing a 0 has no effect.
5	GBL_STS	This is the global status bit. This bit is set when the BIOS wants the attention of the $\overline{\text{SCI}}$ handler. BIOS sets this bit by setting BIOS_RLS and can only be cleared by writing a 1 to this bit position. Writing a 1 to this bit position also clears BIOS_RLS. Writing a 0 has no effect.
6-7	Reserved	Reserved. These bits always return zeros.

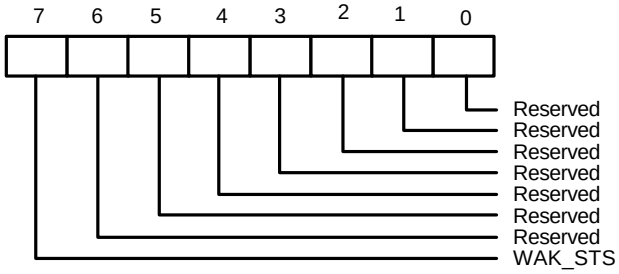
9.3.2 Power Management 1 Status Register 2 (PM1STS2)

Register Location: <CR60, 61> + 1H System I/O Space

Default Value: 00h

Attribute: Read/write

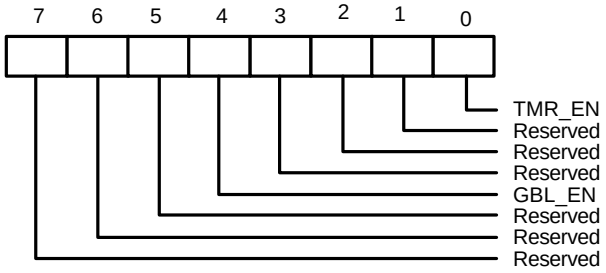
Size: 8 bits



BIT	NAME	DESCRIPTION
0-6	Reserved	Reserved.
7	WAK_STS	This bit is set when the system is in the sleeping state and an enabled resume event occurs. Upon setting this bit, the sleeping/working state machine will transition the system to the working state. This bit is only set by hardware and is cleared by writing a 1 to this bit position or by the sleeping/working state machine automatically when the global standby timer expires. Writing a 0 has no effect. When the WAK_STS is cleared and all devices are in sleeping state, the whole chip enters the sleeping state.

9.3.3 Power Management 1 Enable Register 1(PM1EN1)

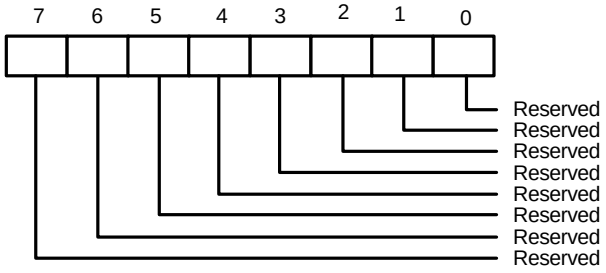
Register Location: <CR60, 61> + 2H System I/O Space
Default Value: 00h
Attribute: Read/write
Size: 8 bits



BIT	NAME	DESCRIPTION
0	TMR_EN	This is the timer carry interrupt enable bit. When this bit is set then an $\overline{SCI}$ event is generated whenever the TMR_STS bit is set. When this bit is reset then no interrupt is generated even when the TMR_STS bit is set.
1-4	Reserved	Reserved. These bits always return a value of zero.
5	GBL_EN	The global enable bit. When both the GBL_EN bit and the GBL_STS bit are set, an $\overline{SCI}$ interrupt is raised.
6-7	Reserved	Reserved.

9.3.4 Power Management 1 Enable Register 2 (PM1EN2)

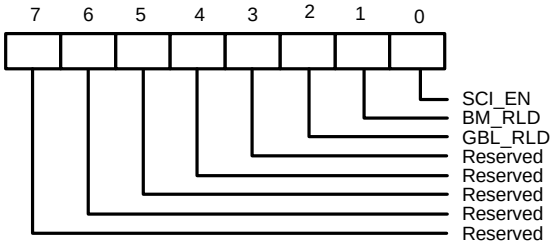
Register Location: <CR60, 61> + 3H System I/O Space
Default Value: 00h
Attribute: Read/write
Size: 8 bits



BIT	NAME	DESCRIPTION
0-7	Reserved	Reserved. These bits always return zeros.

9.3.5 Power Management 1 Control Register 1 (PM1CTL1)

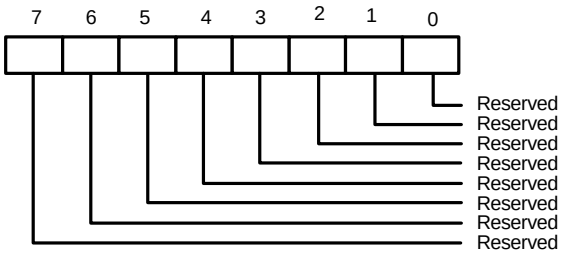
Register Location: <CR60, 61> + 4H System I/O Space
Default Value: 00h
Attribute: Read/write
Size: 8 bits



BIT	NAME	DESCRIPTION
0	SCI_EN	Select whether the power management event triggers an $\overline{SCI}$ or an $\overline{SMI}$ interrupt. When this bit is set, then the power management events will generate an $\overline{SCI}$ interrupt. When this bit is reset and SMI_EN bit is set, then the power management events will generate an $\overline{SMI}$ interrupt.
1	BM_RLD	This is the bus master reload enable bit. If this bit is set and BM_CNTRL is set, an $\overline{SCI}$ interrupt is raised.
2	GBL_RLS	The global release bit. This bit is used by the ACPI software to raise an event to the BIOS software. The BIOS software has a corresponding enable and status bit to control its ability to receive the ACPI event. Setting GBL_RLS sets BIOS_STS, and it generates an $\overline{SMI}$ interrupt if BIOS_EN is also set.
3-7	Reserved	Reserved. These bits always return zeros.

9.3.6 Power Management 1 Control Register 2 (PM1CTL2)

Register Location: <CR60, 61> + 5H System I/O Space
Default Value: 00h
Attribute: Read/write
Size: 8 bits



BIT	NAME	DESCRIPTION
0-7	Reserved	Reserved. These bits always return zeros.

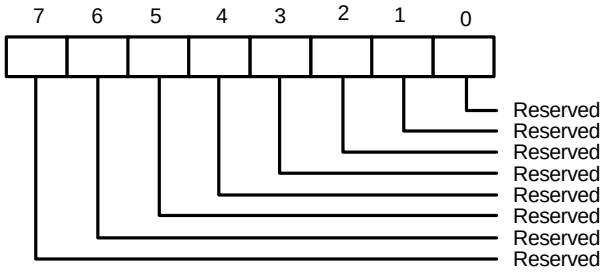
9.3.7 Power Management 1 Control Register 3 (PM1CTL3)

Register Location: <CR60, 61> + 6H System I/O Space

Default Value: 00h

Attribute: Read/write

Size: 8 bits



BIT	NAME	DESCRIPTION
0-7	Reserved	Reserved. These bits always return zeros.

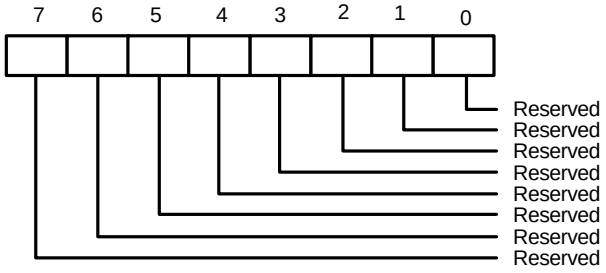
9.3.8 Power Management 1 Control Register 4 (PM1CTL4)

Register Location: <CR60, 61> + 7H System I/O Space

Default Value: 00h

Attribute: Read/write

Size: 8 bits



BIT	NAME	DESCRIPTION
0-7	Reserved	Reserved. These bits always return zeros.

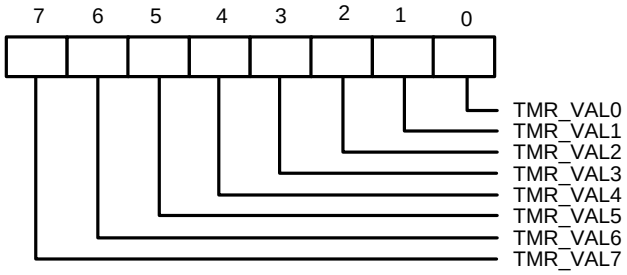
9.3.9 Power Management 1 Timer 1 (PM1TMR1)

Register Location: <CR60, 61> + 8H System I/O Space

Default Value: 00h

Attribute: Read only

Size: 8 bits



BIT	NAME	DESCRIPTION
0-7	TMR_VAL	This read-only field returns the running count of the power management timer. This is a 24-bit counter that runs off of a 3.579545 MHZ clock, and counts in the working state. The timer is reset and then continues counting until the CLKIN input the the chip is stopped. If the clock is restarted without a MR reset, then the counter will resume counting from where it stopped. The TMR_STS bit is set any time the last bit of the timer (bit 23) goes from 0 to 1 or from 1 to 0. If the TMR_EN bit is set, the setting of the TMR_STS bit will generate an $\overline{SCI}$ interrupt.

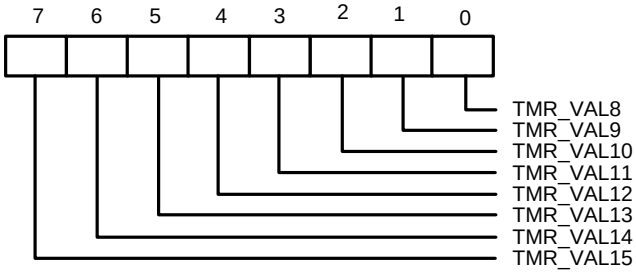
9.3.10 Power Management 1 Timer 2 (PM1TMR2)

Register Location: <CR60, 61> + 9H System I/O Space

Default Value: 00h

Attribute: Read only

Size: 8 bits



BIT	NAME	DESCRIPTION
0-7	TMR_VAL	This read-only field returns the running count of the power management timer. This is a 24-bit counter that runs off of a 3.579545 MHz clock, and counts in the working state. The timer is reset and then continues counting until the CLKIN input the the chip is stopped. If the clock is restarted without a MR reset, then the counter will resume counting from where it stopped. The TMR_STS bit is set any time the last bit of the timer (bit 23) goes from 0 to 1 or from 1 to 0. If the TMR_EN bit is set, the setting of the TMR_STS bit will generate an $\overline{SCI}$ interrupt.

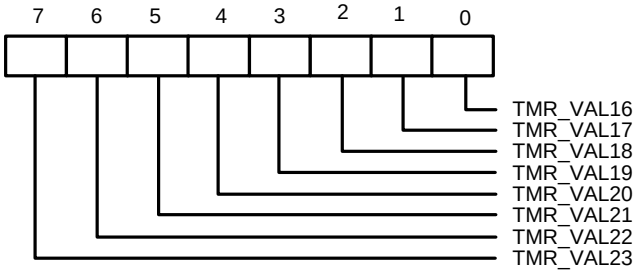
9.3.11 Power Management 1 Timer 3 (PM1TMR3)

Register Location: <CR60, 61> + AH System I/O Space

Default Value: 00h

Attribute: Read only

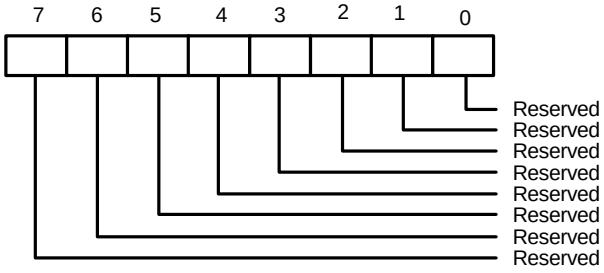
Size: 8 bits



BIT	NAME	DESCRIPTION
0-7	TMR_VAL	This read-only field returns the running count of the power management timer. This is a 24-bit counter that runs off of a 3.579545 MHZ clock, and counts in the working state. The timer is reset and then continues counting until the CLKIN input the the chip is stopped. If the clock is restarted without a MR reset, then the counter will resume counting from where it stopped. The TMR_STS bit is set any time the last bit of the timer (bit 23) goes from 0 to 1 or from 1 to 0. If the TMR_EN bit is set, the setting of the TMR_STS bit will generate an $\overline{SCI}$ interrupt.

9.3.12 Power Management 1 Timer 4 (PM1TMR4)

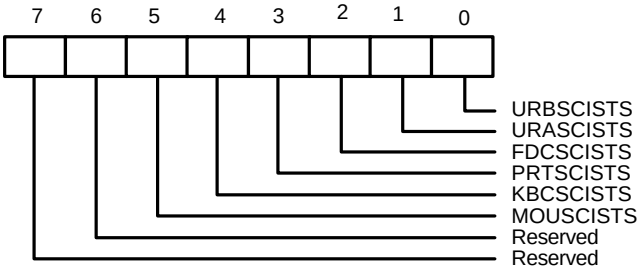
Register Location: <CR60, 61> + BH System I/O Space
Default Value: 00h
Attribute: Read only
Size: 8 bits



BIT	NAME	DESCRIPTION
0-7	Reserved	Reserved. These bits always return zeros.

9.3.13 General Purpose Event 0 Status Register 1 (GP0STS1)

Register Location: <CR62, 63> System I/O Space
Default Value: 00h
Attribute: Read/write
Size: 8 bits



These bits indicate the status of the $\overline{SCI}$ input, which is set when the device's IRQ is raised. If the corresponding enable bit in the $\overline{SCI}$ interrupt enable register (in GP0EN1) is set, an $\overline{SCI}$ interrupt is raised and routed to the output pin. Wrinting a 1 clears the bit, and wrinting a 0 has no effect. If the bit is not cleared, new IRQ to the $\overline{SCI}$ logic input is ignored and no $\overline{SCI}$ interrupt will be raised.

Bit	Name	Description
0	URBSCISTS	UART B $\overline{SCI}$ status, which is set by the UART B IRQ.
1	URASCISTS	UART A $\overline{SCI}$ status, which is set by the UART A IRQ.
2	FDCSCISTS	FDC $\overline{SCI}$ status, which is set by the FDC IRQ.
3	PRTSCISTS	PRT $\overline{SCI}$ status, which is set by the printer port IRQ.
4	KBCSCISTS	KBC $\overline{SCI}$ status, which is set by the KBC IRQ.
5	MOUSCISTS	MOUSE $\overline{SCI}$ status, which is set by the MOUSE IRQ.
6-7	Reserved	Reserved.

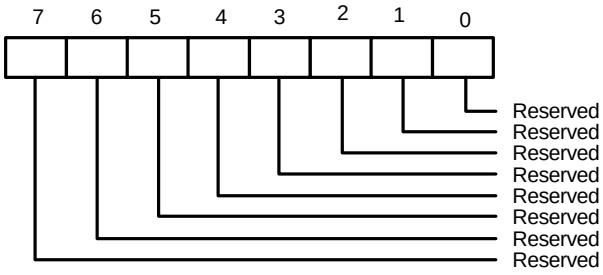
9.3.14 General Purpose Event 0 Status Register 2 (GP0STS2)

Register Location: <CR62, 63> + 1H System I/O Space

Default Value: 00h

Attribute: Read/write

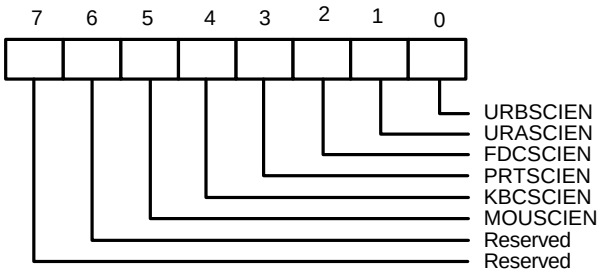
Size: 8 bits



BIT	NAME	DESCRIPTION
0-7	Reserved	Reserved. These bits always return zeros.

9.3.15 General Purpose Event 0 Enable Register 1 (GP0EN1)

Register Location: <CR62, 63> + 2H System I/O Space
Default Value: 00h
Attribute: Read/write
Size: 8 bits



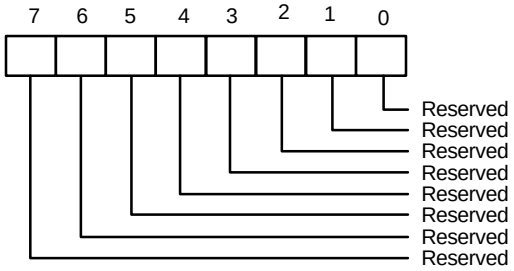
These bits are used to enable the device's IRQ sources into the $\overline{SCI}$ logic. The $\overline{SCI}$ logic output for the IRQs is as follows:

SCI logic output = (URBSCIEN and URBSCISTS) or (URASCIEN and URASCISTS) or (FDCSCIEN and FDCSCISTS) or (PRTSCIEN and PRTSCISTS) or (KBCSCIEN and KBCSCISTS) or (MOUSCIEN and MOUSCISTS)

BIT	NAME	DESCRIPTION
0	URBSCIEN	UART B $\overline{SCI}$ enable, which controls the UART B IRQ.
1	URASCIEN	UART A $\overline{SCI}$ enable, which controls the UART A IRQ.
2	FDCSCIEN	FDC $\overline{SCI}$ enable, which controls the FDC IRQ.
3	PRTSCIEN	printer port $\overline{SCI}$ enable, which controls the printer port IRQ.
4	KBCSCIEN	KBC $\overline{SCI}$ enable, which controls the KBC IRQ.
5	MOUSCIEN	MOUSE $\overline{SCI}$ enable, which controls the MOUSE IRQ.
6-7	Reserved	Reserved.

9.3.16 General Purpose Event 0 Enable Register 2 (GP0EN2)

Register Location: <CR62, 63> + 3H System I/O Space
Default Value: 00h
Attribute: Read/write
Size: 8 bits



BIT	NAME	DESCRIPTION
0-7	Reserved	Reserved. These bits always return zeros.

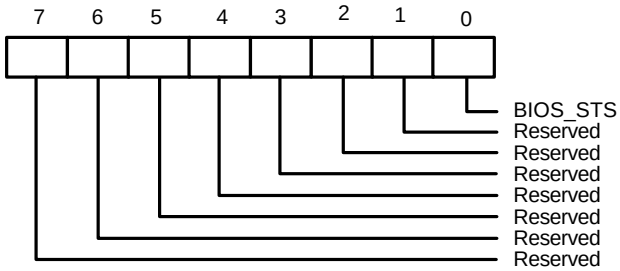
9.3.17 General Purpose Event 1 Status Register 1 (GP1STS1)

Register Location: <CR64, 65> System I/O Space

Default Value: 00h

Attribute: Read/write

Size: 8 bits



BIT	NAME	DESCRIPTION
0	BIOS_STS	The BIOS status bit. This bit is set when GBL_RLS is set. If BIOS_EN is set, setting GBL_RLS will raise an $\overline{\text{SMI}}$ event. Writing a 1 to its bit location clears BIOS_STS and also clears GBL_RLS. Writing a 0 has no effect.
1-7	Reserved	Reserved.

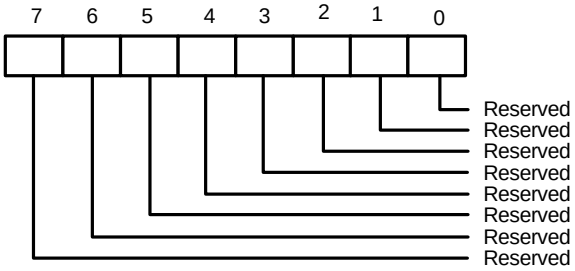
9.3.18 General Purpose Event 1 Status Register 2 (GP1STS2)

Register Location: <CR64, 65> + 1H System I/O Space

Default Value: 00h

Attribute: Read/write

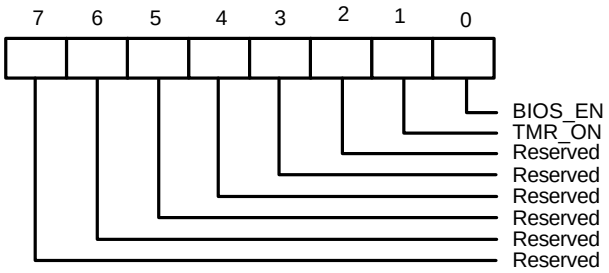
Size: 8 bits



BIT	NAME	DESCRIPTION
0-7	Reserved	Reserved. These bits always return zeros.

9.3.19 General Purpose Event 1 Enable Register 1 (GP1EN1)

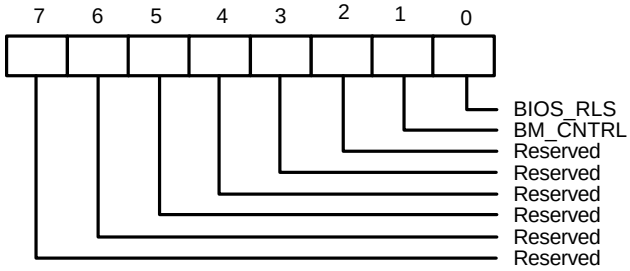
Register Location: <CR64, 65> + 2H System I/O Space
Default Value: 00h
Attribute: Read/write
Size: 8 bits



BIT	NAME	DESCRIPTION
0	BIOS_EN	This bit is raise the $\overline{SMI}$ event. When this bit is set and the ACPI software writes a 1 to the GBL_RLS bit, an $\overline{SMI}$ event is raised on the $\overline{SMI}$ logic output.
1	TMR_ON	This bit is used to turn on the power management timer. 1 = timer on; 0 = timer off.
2-7	Reserved	Reserved.

9.3.20 General Purpose Event 1 Enable Register 2 (GP1EN2)

Register Location: <CR64, 65> + 3H System I/O Space
Default Value: 00h
Attribute: Read/write
Size: 8 bits



BIT	NAME	DESCRIPTION
0	BIOS_RLS	The BIOS release bit. This bit is used by the BIOS software to raise an event to the ACPI software. The ACPI software has a corresponding enable and status bit to control its ability to receive the ACPI event. Setting BIOS_RLS sets GBL_STS, and it generates an $\overline{SCI}$ interrupt if GBL_EN is also set. Writing a 1 to its bit position sets this bit and also sets the BM_STS bit. Writing a 0 has no effect. This bit is cleared by writing a 1 to the GBL_STS bit.
1	BM_CNTRL	This bit is used to set the BM_STS bit and if the BM_RLD bit is also set, then an SCI interrupt is generated. Writing a 1 sets BM_CNTRL to 1 and also sets BM_STS. Writing a 0 has no effect. Wrinting a 1 to BM_STS clears BM_STS and also clears BM_CNTRL.
2-7	Reserved	Reserved.

9.3.21 Bit Map Configuration Registers

Table 9-1: Bit Map of PM1 Register Block

Register	Address	Power-On Reset Value	D7	D6	D5	D4	D3	D2	D1	D0
PM1STS1	<CR60,61>	0000 0000	0	0	GBL_STS	BM_STS	0	0	0	TMR_STS
PM1STS2	<CR60,61> +1H	0000 0000	WAK_STS	0	0	0	0	0	0	0
PM1EN1	<CR60,61> +2H	0000 0000	0	0	GBL_EN	0	0	0	0	TMR_EN
PM1EN2	<CR60,61> +3H	0000 0000	0	0	0	0	0	0	0	0
PM1CTL1	<CR60,61> +4H	0000 0000	0	0	0	0	0	GBL_RLS	BM_RLD	SCI_EN
PM1CTL2	<CR60,61> +5H	0000 0000	0	0	0	0	0	0	0	0
PM1CTL3	<CR60,61> +6H	0000 0000	0	0	0	0	0	0	0	0
PM1CTL4	<CR60,61> +7H	0000 0000	0	0	0	0	0	0	0	0
PM1TMR1	<CR60,61> +8H	0000 0000	TMR_VAL7	TMR_VAL6	TMR_VAL5	TMR_VAL4	TMR_VAL3	TMR_VAL2	TMR_VAL1	TMR_VAL0
PM1TMR2	<CR60,61> +9H	0000 0000	TMR_VAL15	TMR_VAL14	TMR_VAL13	TMR_VAL12	TMR_VAL11	TMR_VAL10	TMR_VAL9	TMR_VAL8
PM1TMR3	<CR60,61> +AH	0000 0000	TMR_VAL23	TMR_VAL22	TMR_VAL21	TMR_VAL20	TMR_VAL19	TMR_VAL18	TMR_VAL17	TMR_VAL16
PM1TMR4	<CR60,61> +BH	0000 0000	0	0	0	0	0		0	0

Table 9-2: Bit Map of GPE Register Block

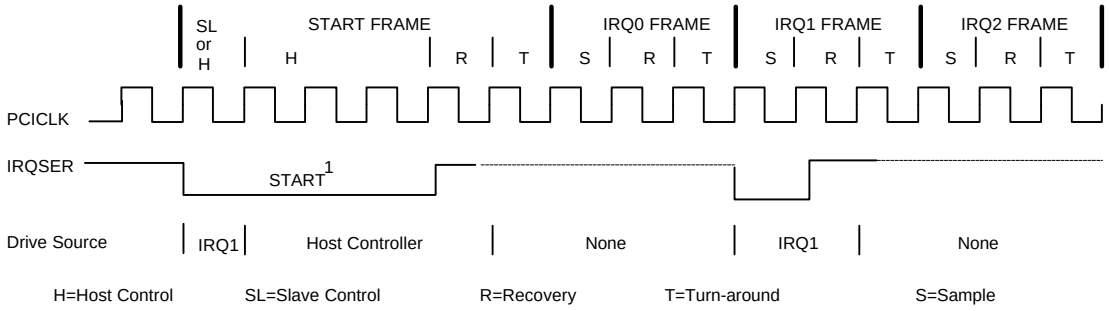
Register	Address	Power-On Reset Value	D7	D6	D5	D4	D3	D2	D1	D0
GP0STS1	<CR62,63>	0000 0000	0	0	MOUSCISTS	KBCSCISTS	PRTSCISTS	FDCSCISTS	URASCISTS	URBSCISTS
GP0STS2	<CR62,63> +1H	0000 0000	0	0	0	0	0	0	0	0
GP0EN1	<CR62,63> +2H	0000 0000	0	0	MOUSCIEN	KBCSCIEN	PRTSCIEN	FDCSCIEN	URASCIEN	URBSCIEN
GP0EN2	<CR62,63> +3H	0000 0000	0	0	0	0	0	0	0	0
GP1STS1	<CR64,65>	0000 0000	0	0	0	0	0	0	0	BIOS_STS
GP1STS2	<CR64,65> +1H	0000 0000	0	0	0	0	0	0	0	0
GP1EN1	<CR64,65> +2H	0000 0000	0	0	0	0	0	0	TMR_ON	BIOS_EN
GP1EN2	<CR64,65> +3H	0000 0000	0	0	0	0	0	0	BM_CNTRL	BIOS_RLS

10. SERIAL IRQ

W83977TF supports a serial IRQ scheme. This allow a signal line to be used to report the legacy ISA interrupt rerquests. Because more than one device may need to share the signal serial IRQ signal line, an open drain signal scheme is used. The clock source is the PCI clock. The serial interrupt is transfered on the IRQSER signal, one cycle consisting of three frames types: a start frame, several IRQ/Data frame, and one Stop frame. The serial interrupt scheme adheres to the *Serial IRQ Specification for PCI System, Version 6.0.*

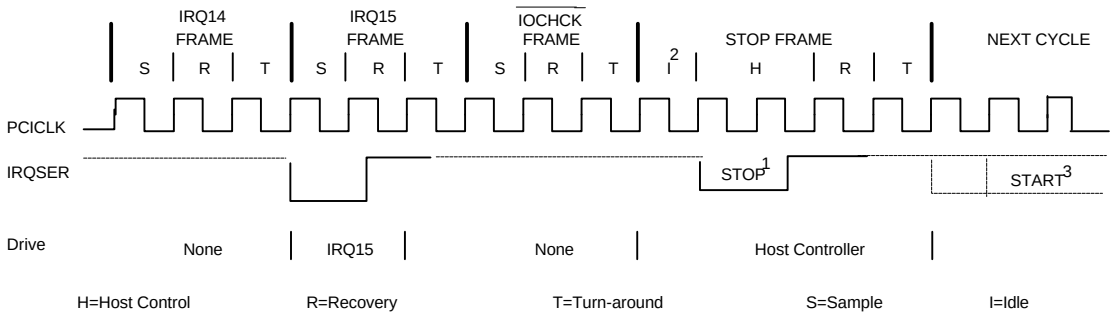
Timing Diagrams For IRQSER Cycle

Start Frame timing with source sampled a low pulse on IRQ1



1. Start Frame pulse can be 4-8 clocks wide.

Stop Frame Timing with Host using 17 IRQSER sampling period



1. Stop pulse is 2 clocks wide for Quiet mode, 3 clocks wide for Continuous mode.
2. There may be none, one or more Idle states during the Stop Frame.
3. The next IRQSER cycle's Start Frame pulse may or may not start immediately after the turn-around clock of the Stip Frame.

10.1 Start Frame

There are two modes of operation for the IRQSER Start frame: Quiet mode and Continuous mode.

In the Quiet mode, the peripheral drives the SERIRQ signal active low for one clock, and then tri-states it. This brings all the states machines of the peripherals from idle to active states. The host controller will then take over driving IRQSER signal low in the next clock and will continue driving the IRQSER low for programmable 3 to 7 clock periods. This makes the total number of clocks low for 4 to 8 clock periods. After these clocks, the host controller will drive the IRQSER high for one clock and then tri-states it.

In the Continuous mode, only the host controller initiates the START frame to update IRQ/Data line information. The host controller drives the IRQSER signal low for 4 to 8 clock periods. Upon a reset, the IRQSER signal is defaulted to the Continuous mode for the host controller to initiate the first Start frame.

10.2 IRQ/Data Frame

Once the start frame has been initiated, all the peripherals must start counting frames based on the rsing edge of the start pulse. Each IRQ/Data Frame is three clocks: Sample phase, Recovery phase, and Turn-around phase.

During the Sample phase, the peripheral drives SERIRQ low if the corresponding IRQ is active. If the corresponding IRQ is inactive, then IRQSER must be left tri-stated. During the Recovery phase, the peripheral device drives the IRQSER high. During the Turn-around phase, the peripheral device left the IRQSER tri-stated.

The IRQ/Data Frame has a number of specific order, as shown in Table 10-1.

10.3 Stop Frame

After all IRQ/Data Frames have completed, the host controller will terminate IRQSER by a Stop frame. Only the host controller can initiate the Stop frame by driving IRQSER low for 2 or 3 clocks. If the Stop Frame is low for 2 clocks, the next IRQSER cycle's Sample mode is the Quiet mode. If the Stop Frame is low for 3 clocks, the next IRQSER cycle's Sample mode is the Continuous mode.

Table 10-1 IRQSER Sampling periods

IRQ/DATA FRAME	SIGNAL SAMPLED	# OF CLOCKS PAST START
1	IRQ0	2
2	IRQ1	5
3	$\overline{\text{SMI}}$	8
4	IRQ3	11
5	IRQ4	14
6	IRQ5	17
7	IRQ6	20
8	IRQ7	23
9	IRQ8	26
10	IRQ9	29
11	IRQ10	32
12	IRQ11	35
13	IRQ12	38
14	IRQ13	41
15	IRQ14	44
16	IRQ15	47
17	$\overline{\text{IOCHCK}}$	50
18	$\overline{\text{INTA}}$	53
19	$\overline{\text{INTB}}$	56
20	$\overline{\text{INTC}}$	59
21	$\overline{\text{INTD}}$	62
32:22	Unassigned	95

10.4 Reset and Initialization

After MR reset, IRQSER Slaves are put into the Continuous(Idle) mode. The Host Controller is responsible for starting the initial IRQSER Cycle to collect system's IRQ/Data default values. The system then follows with the Continuous/Quiet mode protocol (Stop Frame pulse width) for subsequent IRQSER cycles. It's the Host Controller's responsibility to provide the default values to 8259's and other system logic before the first IRQSER cycle is performed. For IRQSER system suspend, insertion, or removal application, the Host controller should be programmed into Continuous(Idle) mode first. This is to guarantee IRQSER bus in the Idle state before the system configuration changes.