Winbond Electronics Corp.

WINBOND I/O

GENERAL DESCRIPTION

The W83977TF is an evolving product from Winbond's most popular I/O chip W83877F --- which integrates the disk drive adapter, serial port (UART), IrDA 1.0 SIR, parallel port, configurable plug-and-play registers for the whole chip --- plus additional powerful features: **ACPI**, 8042 keyboard controller with PS/2 mouse support, 23 general purpose I/O ports, full 16-bit address decoding, OnNow keyboard wake-up, OnNow mouse wake-up.

The disk drive adapter functions of W83977TF include a floppy disk drive controller compatible with the industry standard 82077/ 765, data separator, write pre-compensation circuit, decode logic, data rate selection, clock generator, drive interface control logic, and interrupt and DMA logic. The wide range of functions integrated into the W83977TF greatly reduces the number of components required for interfacing with floppy disk drives. The W83977TF supports four 360K, 720K, 1.2M, 1.44M, or 2.88M disk drives and data transfer rates of 250 Kb/s, 300 Kb/s, 500 Kb/s,1 Mb/s, and 2 Mb/s.

The W83977TF provides two high-speed serial communication ports (UARTs), one of which supports serial Infrared communication. Each UART includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem control capability, and a processor interrupt system. Both UARTs provide legacy speed with baud rate up to 115.2k bps and also advanced speed with baud rates of **230k**, **460k**, or **921k bps** which support higher speed modems.

The W83977TF supports one PC-compatible printer port (SPP), Bi-directional Printer port (BPP) and also Enhanced Parallel Port (EPP) and Extended Capabilities Port (ECP). Through the printer port interface pins, also available are: Extension FDD Mode and Extension 2FDD Mode allowing one or two external floppy disk drives to be connected.

The configuration registers support mode selection, function enable/disable, and power down function selection. Furthermore, the configurable PnP features are compatible with the plug-and-play feature demand of Windows 95™, which makes system resource allocation more efficient than ever.

W83977TF provides functions that comply with **ACPI** (*Advanced Configuration and Power Interface*), which includes support of legacy and ACPI power management through $\overline{\text{SMI}}$ or $\overline{\text{SCI}}$ function pins. W83977TF also has auto power management to reduce power consumption.

The keyboard controller is based on 8042 compatible instruction set with a 2K Byte programmable ROM and a 256-Byte RAM bank. Keyboard BIOS firmware is available with optional AMIKEY™ -2, Phoenix MultiKey/42™, or customer code.

The W83977TF provides a set of flexible I/O control functions to the system designer through a set of General Purpose I/O ports. These GPIO ports may serve as simple I/O or may be individually configured to provide a predefined alternate function.

W83977TF is made to fully comply with **Microsoft PC97 Hardware Design Guide**. IRQs, DMAs, and I/O space resource are flexible to adjust to meet ISA PnP requirement. Moreover W83977TF is made to meet the specification of PC97's requirement in the power management: **ACPI** and **DPM** (Device Power Management).

Another benifit is that W83977TF has the same pin assignment as W83977AF, W83977F, W83977ATF. This makes the design very flexible.

FEATURES

General

- Plug & Play 1.0A compatible
- Support 13 IRQs, 4 DMA channels, full 16-bit address decoding
- Capable of ISA Bus IRQ Sharing
- Compliant with **Microsoft PC97** Hardware Design Guide
- Support **DPM** (Device Power Management), **ACPI**
- Report ACPI status interrupt by $\overline{SCI}$ signal issued from any of the 13 IQRs pins or GPIO xx
- Programmable configuration settings
- Single 24/48 MHz clock input

FDC

- Compatible with IBM PC AT disk drive systems
- Variable write pre-compensation with track selectable capability
- Support vertical recording format
- DMA enable logic
- 16-byte data FIFOs
- Support floppy disk drives and tape drives
- Detects all overrun and underrun conditions
- Built-in address mark detection circuit to simplify the read electronics
- FDD anti-virus functions with software write protect and FDD write enable signal (write data signal was forced to be inactive)
- Support up to four 3.5-inch or 5.25-inch floppy disk drives
- Completely compatible with industry standard 82077
- 360K/720K/1.2M/1.44M/2.88M format; 250K, 300K, 500K, 1M, 2M bps data transfer rate
- Support **3-mode FDD, and its Win95 driver**

UART

- Two high-speed 16550 compatible UARTs with 16-byte send/receive FIFOs
- MIDI compatible
- Fully programmable serial-interface characteristics:
  --- 5, 6, 7 or 8-bit characters
  --- Even, odd or no parity bit generation/detection
  --- 1, 1.5 or 2 stop bits generation
- Internal diagnostic capabilities:
  --- Loop-back controls for communications link fault isolation
  --- Break, parity, overrun, framing error simulation
- Programmable baud generator allows division of 1.8461 MHz and 24 MHz by 1 to (2^{16}-1)
- Maximum baud rate up to 921k bps for 14.769 MHz and 1.5M bps for 24 MHz

Infrared

- Support IrDA version 1.0 SIR protocol with maximum baud rate up to 115.2K bps
- Support SHARP ASK-IR protocol with maximum baud rate up to 57,600 bps
- **Support S/W driver for Windows95™ and Windows98™ (Memphis™)**

Parallel Port

- Compatible with IBM parallel port
- Support PS/2 compatible bi-directional parallel port
- Support Enhanced Parallel Port (EPP) – Compatible with IEEE 1284 specification
- Support Extended Capabilities Port (ECP) – Compatible with IEEE 1284 specification
- Extension FDD mode supports disk drive B; and Extension 2FDD mode supports disk drives A and B through parallel port
- Enhanced printer port back-drive current protection

Keyboard Controller

- 8042 based with optional F/W from AMIKKEY™-2, Phoenix MultiKey/42™ or customer code with 2K bytes of programmable ROM, and 256 bytes of RAM
- Asynchronous Access to Two Data Registers and One status Register
- Software compatibility with the 8042 and PC87911 microcontrollers
- Support PS/2 mouse
- Support port 92
- Support both interrupt and polling modes
- **Fast Gate A20 and Hardware Keyboard Reset**
- 8 Bit Timer/ Counter
- Support binary and BCD arithmetic
- 6 MHz, 8 MHz, 12 MHz, or 16 MHz operating frequency

General Purpose I/O Ports

- 23 programmable general purpose I/O ports; 3 dedicate, 20 optional
- General purpose I/O ports can serve as simple I/O ports, interrupt steering inputs, watching dog timer output, power LED output, infrared I/O pins, general purpose address decoder, KBC control I/O pins

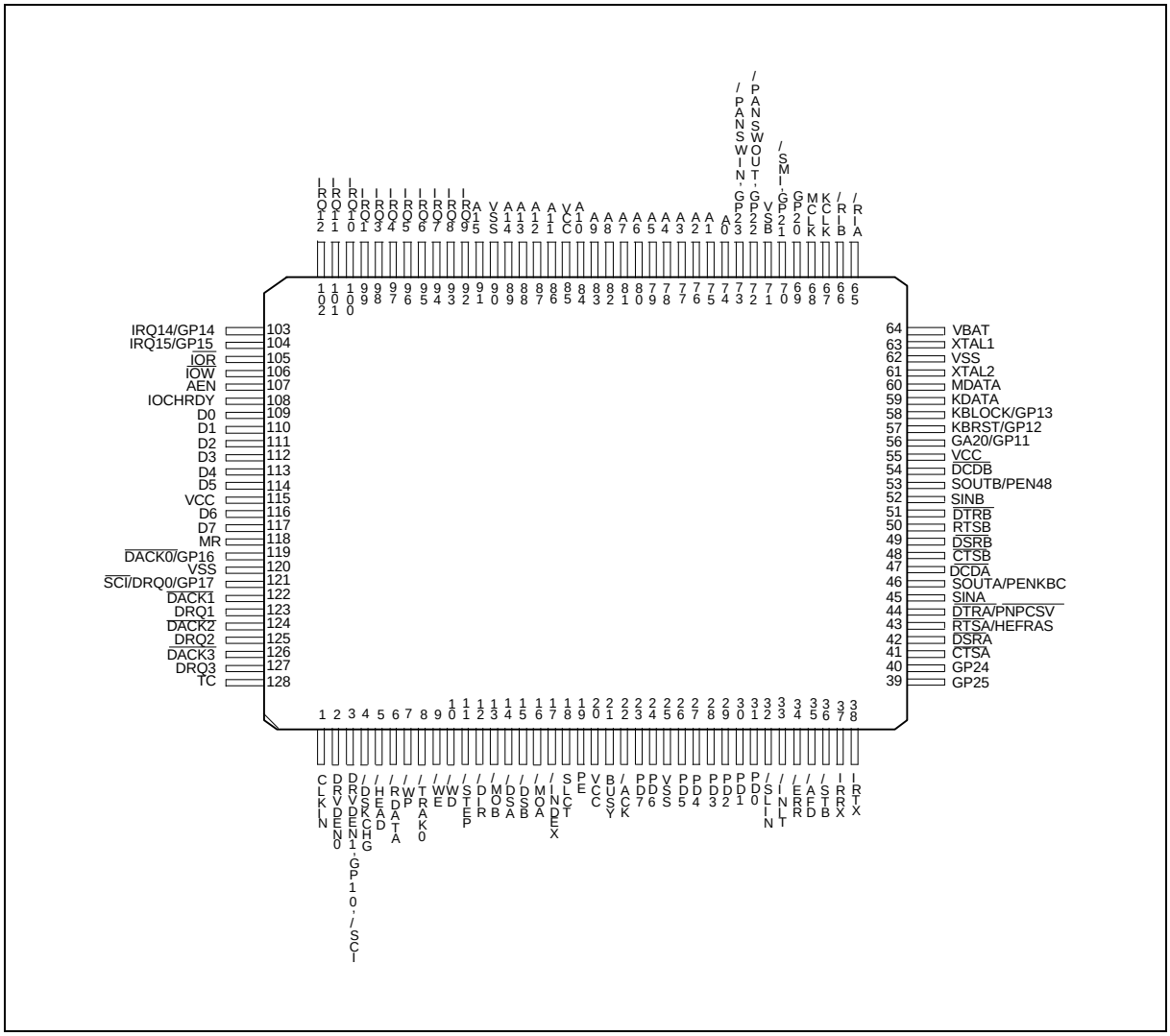
OnNow Funtions

- Keyboard wake-up by programmable keys
- Mouse wake-up by programmable buttons

Package

- 128-pin PQFP

PIN CONFIGURATION



1. PIN DESCRIPTION

Note: Please refer to Section 11.2 DC CHARACTERISTICS for details.

I/O_{6t} - TTL level bi-directional pin with 6 mA source-sink capability

I/O_{8t} - TTL level bi-directional pin with 8 mA source-sink capability

I/O_{8} - CMOS level bi-directional pin with 8 mA source-sink capability

I/O_{12t} - TTL level bi-directional pin with 12 mA source-sink capability

I/O_{12} - CMOS level bi-directional pin with 12 mA source-sink capability

I/O_{16u} - CMOS level bi-directional pin with 16 mA source-sink capability with internal pull-up resistor

I/OD_{16u} - CMOS level bi-directional pin open drain output with 16 mA sink capability with internal pull-up resistor

I/O_{24t} - TTL level bi-directional pin with 24 mA source-sink capability

OUT_{8t} - TTL level output pin with 8 mA source-sink capability

OUT_{12t} - TTL level output pin with 12 mA source-sink capability

OD_{12} - Open-drain output pin with 12 mA sink capability

OD_{24} - Open-drain output pin with 24 mA sink capability

IN_{t} - TTL level input pin

IN_{c} - CMOS level input pin

IN_{cu} - CMOS level input pin with internal pull-up resitor

IN_{cs} - CMOS level Schmitt-triggered input pin

IN_{ts} - TTL level Schmitt-triggered input pin

IN_{tsu} - TTL level Schmitt-triggered input pin with internal pull-up resistor

1.1 Host Interface

SYMBOL	PIN	I/O	FUNCTION
A0–A10	74-84	IN_t	System address bus bits 0-10
A11-A14	86-89	IN_t	System address bus bits 11-14
A15	91	IN_t	System address bus bit 15
D0–D5	109-114	I/O_{12t}	System data bus bits 0-5
D6–D7	116-117	I/O_{12t}	System data bus bits 6-7
$\overline{IOR}$	105	IN_{ts}	CPU I/O read signal
$\overline{IOW}$	106	IN_{ts}	CPU I/O write signal
AEN	107	IN_{ts}	System address bus enable
IOCHRDY	108	OD_{24}	In EPP Mode, this pin is the IO Channel Ready output to extend the host read/write cycle.
MR	118	IN_{ts}	Master Reset; Active high; MR is low during normal operations.

1.1 Host Interface, continued

SYMBOL	PIN	I/O	FUNCTION
$\overline{DACK0}$	119	IN_{tsu}	DMA Channel 0 Acknowledge signal. (CR2C bit 5_4 = 00, default)
GP16		I/O_{12t}	General purpose I/O port 1bit 6. (CR2C bit 5_4 = 01)
(WDTO)			Alternate function from GP16: Watch dog timer output
P15		I/O_{12t}	KBC P15 I/O port. (CR2C bit 5_4 = 10)
DRQ0	121	OUT_{12t}	DMA Channel 0 request signal. (CR2C bit 7_6 = 00, default)
GP17		I/O_{12t}	General purpose I/O port 1bit 7. (CR2C bit 7_6 = 01)
(PLEDO)			Alternate Function from GP17: Power LED output.
P14		I/O_{12t}	KBC P14 I/O port (CR2C bit 7_6 = 10)
$\overline{SCI}$		OUT_{12t}	System Control Interrupt (CR2C bit 7_6 = 11)
$\overline{DACK1}$	122	IN_{ts}	DMA Channel 1 Acknowledge signal
DRQ1	123	OUT_{12t}	DMA Channel 1 request signal
$\overline{DACK2}$	124	IN_{ts}	DMA Channel 2 Acknowledge signal
DRQ2	125	OUT_{12t}	DMA Channel 2 request signal
$\overline{DACK3}$	126	IN_{ts}	DMA Channel 3 Acknowledge signal
DRQ3	127	OUT_{12t}	DMA Channel 3 request signal
TC	128	IN_{ts}	Terminal Count. When active, this pin indicates termination of a DMA transfer.
IRQ1	99	OUT_{12t}	Interrupt request 1
IRQ3	98	OUT_{12t}	Interrupt request 3
IRQ4	97	OUT_{12t}	Interrupt request 4
IRQ5	96	OUT_{12t}	Interrupt request 5
IRQ6	95	OUT_{12t}	Interrupt request 6
IRQ7	94	OUT_{12t}	Interrupt request 7
IRQ8	93	OUT_{12t}	Interrupt request 8
IRQ9	92	OUT_{12t}	Interrupt request 9
IRQ10	100	OUT_{12t}	Interrupt request 10
IRQ11	101	OUT_{12t}	Interrupt request 11
IRQ12	102	OUT_{12t}	Interrupt request 12

1.1 Host Interface, continued

SYMBOL	PIN	I/O	FUNCTION
IRQ14	103	OUT_{12t}	Interrupt request 14. (CR2C bit 1_0 = 00, default)
GP14		I/O_{12t}	General purpose I/O port 1 bit 4. (CR2C bit 1_0 = 01)
($\overline{GPACS}$)			Alternate Function 1 from GP14: General purpose address decode output.
(P17)			Alternate Function 2 from GP14: KBC P17 I/O port.
PLEDO		OUT_{12t}	Power LED output. (CR2C bit 1_0 = 10)
IRQ15	104	OUT_{12t}	Interrupt request 15.(CR2C bit 3_2 = 00, default)
GP15		I/O_{12t}	General purpose I/O port 1 bit 5. (CR2C bit 3_2 = 01)
($\overline{GPAWE}$)			Alternate Function 1 from GP15: General purpose address write enable output.
(P12)			Alternate Function 2 from GP15: KBC P12 I/O port.
WDT		OUT_{12t}	Watch-Dog timer output. (CR2C bit 3_2 = 10)
CLKIN	1	IN_t	24 or 48 MHz clock input, selectable through bit 5 of CR24.

1.2 General Purpose I/O Port

SYMBOL	PIN	I/O	FUNCTION
GP20	69	I/O_{12t}	General purpose I/O port 2 bit 0.
(KBRST)			Alternate Function from GP20: Keyboard reset (KBC P20)
$\overline{SMI}$	70	OUT_{12t}	For the power management, the $\overline{SMI}$ is active low by the power management events, that generate and $\overline{SCI}$ in ACPI mode. (CR2B bit 4_3 = 00, default)
GP21		I/O_{12t}	General purpose I/O port 2 bit 1. (CR2B bit 4_3 = 01)
(P13)			Alternate Function from GP21: KBC P13 I/O port.
P16		I/O_{12t}	KBC P16 I/O port. (CR2B bit 4_3 = 10)
$\overline{PANSWOUT}$	72	OUT_{12t}	Panel Switch output. (CR2B bit 5 = 0, default)
GP22		I/O_{12t}	General purpose I/O port 2 bit 2. (CR2B bit 5 = 1)
(P14)			Alternate Function from GP22: KBC P14 I/O port.
$\overline{PANSWIN}$	73	IN_{12t}	Panel Switch input. (CR2B bit 7_6 = 00, default)
GP23		I/O_{12t}	General purpose I/O port 2 bit 3. (CR2B bit 7_6 = 01)
(P15)			Alternate Function from GP23: KBC P15 I/O port
GP24	40	I/O_{12t}	General purpose I/O port 2 bit 4 (CR2A bit 5_4 = 01)
(P16)			Alternate Function from GP24: KBC P16 I/O port
P13		I/O_{12t}	KBC P13 I/O port. (CR2A bit 5_4 = 10)
GP25	39	I/O_{12}	General purpose I/O port 2 bit 5.
(GA20)			Alternate Function from GP25: GATE A20 (KBC P21)

1.3 Serial Port Interface

SYMBOL	PIN	I/O	FUNCTION
$\overline{\text{CTSA}}$ $\overline{\text{CTSB}}$	41 48	IN_t	Clear To Send is the modem control input. The function of these pins can be tested by reading Bit 4 of the handshake status register.
$\overline{\text{DSRA}}$ $\overline{\text{DSRB}}$	42 49	IN_t	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
$\overline{\text{RTSA}}$ HEFRAS	43	I/O_{8t}	UART A Request To Send. An active low signal informs the modem or data set that the controller is ready to send data. During power-on reset, this pin is pulled down internally and is defined as HEFRAS, which provides the power-on value for CR26 bit 6 (HEFRAS). A 4.7 kΩ is recommended if intends to pull up. (select 370H as configuration I/O port's address)
$\overline{\text{RTSB}}$	50	I/O_{8t}	UART B Request To Send. An active low signal informs the modem or data set that the controller is ready to send data.
$\overline{\text{DTRA}}$ $\overline{\text{PNPCSV}}$	44	I/O_{8t}	UART A Data Terminal Ready. An active low signal informs the modem or data set that the controller is ready to communicate. During power-on reset, this pin is pulled down internally and is defined as $\overline{\text{PNPCSV}}$, which provides the power-on value for CR24 bit 0 ($\overline{\text{PNPCSV}}$). A 4.7 kΩ is recommended if intends to pull up. (clear the default value of FDC, UARTs, and PRT)
$\overline{\text{DTRB}}$	51	I/O_{8t}	UART B Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate.
SINA SINB	45, 52	IN_t	Serial Input. Used to receive serial data through the communication link.
SOUTA PENKBC	46	I/O_{8t}	UART A Serial Output. Used to transmit serial data out to the communication link. During power-on reset, this pin is pulled down internally and is defined as PENKBC, which provides the power-on value for CR24 bit 2 (ENKBC). A 4.7 kΩ resistor is recommended if intends to pull up. (enable KBC)
SOUTB PEN48	53	I/O_{8t}	UART B Serial Output. During power-on reset, this pin is pulled down internally and is defined as PEN48, which provides the power-on value for CR24 bit 6 (EN48). A 4.7 kΩ resistor is recommended if intends to pull up.
$\overline{\text{DCDA}}$ $\overline{\text{DCDB}}$	47 54	IN_t	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.

1.3 Serial Port Interface, continued

SYMBOL	PIN	I/O	FUNCTION
$\overline{RIA}$ $\overline{RIB}$	65 66	IN_t	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.

1.4 Infrared Interface

SYMBOL	PIN	I/O	FUNCTION
IRRX	37	IN_{cs}	Infrared Receiver input.
IRTX	38	OUT_{12t}	Infrared Transmitter Output.

1.5 Multi-Mode Parallel Port

The following pins have alternate functions, which are controlled by CR28 and L3-CRF0.

SYMBOL	PIN	I/O	FUNCTION
SLCT	18	IN_t	PRINTER MODE: SLCT An active high input on this pin indicates that the printer is selected. This pin is pulled high internally. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: $\overline{WE2}$ This pin is for Extension FDD B; its function is the same as the $\overline{WE}$ pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE: $\overline{WE2}$ This pin is for Extension FDD A and B; it function is the same as the $\overline{WE}$ pin of FDC.
PE	19	IN_t	PRINTER MODE: PE An active high input on this pin indicates that the printer has detected the end of the paper. This pin is pulled high internally. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: $\overline{WD2}$ This pin is for Extension FDD B; its function is the same as the $\overline{WD}$ pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE: $\overline{WD2}$ This pin is for Extension FDD A and B; its function is the same as the $\overline{WD}$ pin of FDC.

1.5 Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	FUNCTION
BUSY	21	IN_t	PRINTER MODE: BUSY An active high input indicates that the printer is not ready to receive data. This pin is pulled high internally. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: $\overline{MOB2}$ This pin is for Extension FDD B; the function of this pin is the same as the $\overline{MOB}$ pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE: $\overline{MOB2}$ This pin is for Extension FDD A and B; the function of this pin is the same as the $\overline{MOB}$ pin of FDC.
$\overline{ACK}$	22	IN_t	PRINTER MODE: $\overline{ACK}$ An active low input on this pin indicates that the printer has received data and is ready to accept more data. This pin is pulled high internally. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: $\overline{DSB2}$ This pin is for the Extension FDD B; its functions is the same as the $\overline{DSB}$ pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE: $\overline{DSB2}$ This pin is for Extension FDD A and B; it functions is the same as the $\overline{DSB}$ pin of FDC.
$\overline{ERR}$	34	IN_t	PRINTER MODE: $\overline{ERR}$ An active low input on this pin indicates that the printer has encountered an error condition. This pin is pulled high internally. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: $\overline{HEAD2}$ This pin is for Extension FDD B; its function is the same as the $\overline{HEAD}$ pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE: $\overline{HEAD2}$ This pin is for Extension FDD A and B; its function is the same as the $\overline{HEAD}$ pin of FDC.

1.5 Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	FUNCTION
$\overline{SLIN}$	32	OD_{12}	PRINTER MODE: $\overline{SLIN}$ Output line for detection of printer selection. This pin is pulled high internally. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: $\overline{STEP2}$ This pin is for Extension FDD B; its function is the same as the $\overline{STEP}$ pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE: $\overline{STEP2}$ This pin is for Extension FDD A and B; its function is the same as the $\overline{STEP}$ pin of FDC.
$\overline{INIT}$	33	OD_{12}	PRINTER MODE: $\overline{INIT}$ Output line for the printer initialization. This pin is pulled high internally. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: $\overline{DIR2}$ This pin is for Extension FDD B; its function is the same as the $\overline{DIR}$ pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE: $\overline{DIR2}$ This pin is for Extension FDD A and B; its function is the same as the $\overline{DIR}$ pin of FDC.
$\overline{AFD}$	35	OD_{12}	PRINTER MODE: $\overline{AFD}$ An active low output from this pin causes the printer to auto feed a line after a line is printed. This pin is pulled high internally. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: DRVDEN0 This pin is for Extension FDD B; its function is the same as the DRVDEN0 pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE: DRVDEN0 This pin is for Extension FDD A and B; its function is the same as the DRVDEN0 pin of FDC.

1.5 Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	FUNCTION
$\overline{STB}$	36	OD_{12}	PRINTER MODE: $\overline{STB}$ An active low output is used to latch the parallel data into the printer. This pin is pulled high internally. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		-	EXTENSION FDD MODE: This pin is a tri-state output.
		-	EXTENSION 2FDD MODE: This pin is a tri-state output.
PD0	31	I/O_{24t}	PRINTER MODE: PD0 Parallel port data bus bit 0. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		IN_t	EXTENSION FDD MODE: $\overline{INDEX2}$ This pin is for Extension FDD B; the function of this pin is the same as the $\overline{INDEX}$ pin of FDC. It is pulled high internally.
		IN_t	EXTENSION 2FDD MODE: $\overline{INDEX2}$ This pin is for Extension FDD A and B; the function of this pin is the same as the $\overline{INDEX}$ pin of FDC. It is pulled high internally.
PD1	30	I/O_{24t}	PRINTER MODE: PD1 Parallel port data bus bit 1. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		IN_t	EXTENSION FDD MODE: $\overline{TRAK02}$ This pin is for Extension FDD B; the function of this pin is the same as the $\overline{TRAK0}$ pin of FDC. It is pulled high internally.
		IN_t	EXTENSION. 2FDD MODE: $\overline{TRAK02}$ This pin is for Extension FDD A and B; the function of this pin is the same as the $\overline{TRAK0}$ pin of FDC. It is pulled high internally.
PD2	29	I/O_{24t}	PRINTER MODE: PD2 Parallel port data bus bit 2. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		IN_t	EXTENSION FDD MODE: $\overline{WP2}$ This pin is for Extension FDD B; the function of this pin is the same as the $\overline{WP}$ pin of FDC. It is pulled high internally.
		IN_t	EXTENSION. 2FDD MODE: $\overline{WP2}$ This pin is for Extension FDD A and B; the function of this pin is the same as the $\overline{WP}$ pin of FDC. It is pulled high internally.

1.5 Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	FUNCTION
PD3	28	I/O_{24t}	PRINTER MODE: PD3 Parallel port data bus bit 3. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		IN_t	EXTENSION FDD MODE: $\overline{RDATA2}$ This pin is for Extension FDD B; the function of this pin is the same as the $\overline{RDATA}$ pin of FDC. It is pulled high internally.
		IN_t	EXTENSION 2FDD MODE: $\overline{RDATA2}$ This pin is for Extension FDD A and B; this function of this pin is the same as the $\overline{RDATA}$ pin of FDC. It is pulled high internally.
PD4	27	I/O_{24t}	PRINTER MODE: PD4 Parallel port data bus bit 4. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		IN_t	EXTENSION FDD MODE: $\overline{DSKCHG2}$ This pin is for Extension FDD B; the function of this pin is the same as the $\overline{DSKCHG}$ pin of FDC. It is pulled high internally.
		IN_t	EXTENSION 2FDD MODE: $\overline{DSKCHG2}$ This pin is for Extension FDD A and B; this function of this pin is the same as the $\overline{DSKCHG}$ pin of FDC. It is pulled high internally.
PD5	26	I/O_{24t}	PRINTER MODE: PD5 Parallel port data bus bit 5. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		-	EXTENSION FDD MODE: This pin is a tri-state output.
		-	EXTENSION 2FDD MODE: This pin is a tri-state output.
PD6	24	I/O_{24t}	PRINTER MODE: PD6 Parallel port data bus bit 6. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		-	EXTENSION FDD MODE: This pin is a tri-state output.
		OD_{24}	EXTENSION. 2FDD MODE: $\overline{MOA2}$ This pin is for Extension FDD A; its function is the same as the $\overline{MOA}$ pin of FDC.

1.5 Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	FUNCTION
PD7	23	I/O_{24t}	PRINTER MODE: PD7 Parallel port data bus bit 7. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		-	EXTENSION FDD MODE: This pin is a tri-state output.
		OD_{24}	EXTENSION 2FDD MODE: $\overline{DSA2}$ This pin is for Extension FDD A; its function is the same as the $\overline{DSA}$ pin of FDC.

1.6 FDC Interface

SYMBOL	PIN	I/O	FUNCTION
DRVDEN0	2	OD_{24}	Drive Density Select bit 0.
DRVDEN1	3	OD_{24}	Drive Density Select bit 1. (CR2A bit 1_0 = 00, default)
GP10		IO_{24t}	General purpose I/O port 1 bit 0. (CR2A bit 1_0 = 01)
(IRQIN1)			Alternate Function from GP10: Interrupt channel input.
P12		IO_{24t}	KBC P12 I/O port. (CR2A bit 1_0 = 10)
$\overline{SCI}$		OUT_{12t}	System Control Interrupt (CR2A bit 1_0 = 11)
$\overline{HEAD}$	5	OD_{24}	Head select. This open drain output determines which disk drive head is active. Logic 1 = side 0 Logic 0 = side 1
$\overline{WE}$	9	OD_{24}	Write enable. An open drain output.
$\overline{WD}$	10	OD_{24}	Write data. This logic low open drain writes pre-compensation serial data to the selected FDD. An open drain output.
$\overline{STEP}$	11	OD_{24}	Step output pulses. This active low open drain output produces a pulse to move the head to another track.
$\overline{DIR}$	12	OD_{24}	Direction of the head step motor. An open drain output. Logic 1 = outward motion Logic 0 = inward motion
$\overline{MOB}$	13	OD_{24}	Motor B On. When set to 0, this pin enables disk drive 1. This is an open drain output.
$\overline{DSA}$	14	OD_{24}	Drive Select A. When set to 0, this pin enables disk drive A. This is an open drain output.
$\overline{DSB}$	15	OD_{24}	Drive Select B. When set to 0, this pin enables disk drive B. This is an open drain output.

1.6 FDC Interface, continued

SYMBOL	PIN	I/O	FUNCTION
$\overline{MOA}$	16	OD_{24}	Motor A On. When set to 0, this pin enables disk drive 0. This is an open drain output.
$\overline{DSKCHG}$	4	IN_{cs}	Diskette change. This signal is active low at power on and whenever the diskette is removed. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
$\overline{RDATA}$	6	IN_{cs}	The read data input signal from the FDD. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
$\overline{WP}$	7	IN_{cs}	Write protected. This active low Schmitt input from the disk drive indicates that the diskette is write-protected. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
$\overline{TRAK0}$	8	IN_{cs}	Track 0. This Schmitt-triggered input from the disk drive is active low when the head is positioned over the outermost track. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
$\overline{INDEX}$	17	IN_{cs}	This Schmitt-triggered input from the disk drive is active low when the head is positioned over the beginning of a track marked by an index hole. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).

1.7 KBC Interface

SYMBOL	PIN	I/O	FUNCTION
KDATA	59	I/OD_{16u}	Keyboard Data
MDATA	60	I/OD_{16u}	PS2 Mouse Data
KCLK	67	I/OD_{16u}	Keyboard Clock
MCLK	68	I/OD_{16u}	PS2 Mouse Clock
GA20	56	I/O_{12t}	KBC GATE A20 (P21) Output. (CR2A bit 6 = 0, default)
GP11		I/O_{12t}	General purpose I/O port 1 bit 1. (CR2A bit 6 = 1)
(IRQIN2)			Alternate Function from GP11: Interrupt channel input.
KBRST	57	I/O_{12t}	W83C45 Keyboard Reset (P20) Output. (CR2A bit 7 = 0, default)
GP12		I/O_{12t}	General purpose I/O port 1 bit 2. (CR2A bit 7 = 1)
(WDTO)			Alternate Function 1 from GP12 : Watchdog timer output.

1.7 KBC Interface, continued

SYMBOL	PIN	I/O	FUNCTION
KBLOCK	58	IN_{ts}	W83C45 KINH (P17) Input. (CR2B bit 0 = 0, default)
GP13		I/O_{16t}	General purpose I/O port 1 bit 3. (CR2B bit 0 = 1)

1.8 POWER PINS

SYMBOL	PIN	FUNCTION
VCC	20, 55, 85, 115	+5V power supply for the digital circuitry
VSB	71	+5V stand-by power supply for the digital circuitry
GND	25, 62, 90, 120	Ground

1.9 ACPI Interface

SYMBOL	PIN	I/O	FUNCTION
VBAT	64	NA	battery voltage input
XTAL1	63	IN_C	32.768Khz Clock Input
XTAL2	61	O_{8t}	32.768Khz Clock Output

2. FDC FUNCTIONAL DESCRIPTION

2.1 W83977TF FDC

The floppy disk controller of the W83977TF integrates all of the logic required for floppy disk control. The FDC implements a PC/AT or PS/2 solution. All programmable options default to compatible values. The FIFO provides better system performance in multi-master systems. The digital data separator supports up to 2 M bits/sec data rate.

The FDC includes the following blocks: AT interface, Precompensation, Data Rate Selection, Digital Data Separator, FIFO, and FDC Core.

2.1.1 AT interface

The interface consists of the standard asynchronous signals: $\overline{RD}$, $\overline{WR}$, A0-A3, IRQ, DMA control, and a data bus. The address lines select between the configuration registers, the FIFO and control/status registers. This interface can be switched between PC/AT, Model 30, or PS/2 normal modes. The PS/2 register sets are a superset of the registers found in a PC/AT.

2.1.2 FIFO (Data)

The FIFO is 16 bytes in size and has programmable threshold values. All command parameter information and disk data transfers go through the FIFO. Data transfers are governed by the RQM and DIO bits in the Main Status Register.

The FIFO defaults to disabled mode after any form of reset. This maintains PC/AT hardware compatibility. The default values can be changed through the CONFIGURE command. The advantage of the FIFO is that it allows the system a larger DMA latency without causing disk errors. The following tables give several examples of the delays with a FIFO. The data are based upon the following formula:

THRESHOLD # $\times$ (1/DATA/RATE) *8 - 1.5 µS = DELAY

FIFO THRESHOLD	MAXIMUM DELAY TO SERVICING AT 500K BPS
	Data Rate
1 Byte	1 $\times$ 16 µS - 1.5 µS = 14.5 µS
2 Byte	2 $\times$ 16 µS - 1.5 µS = 30.5 µS
8 Byte	8 $\times$ 16 µS - 1.5 µS = 6.5 µS
15 Byte	15 $\times$ 16 µS - 1.5 µS = 238.5 µS
FIFO THRESHOLD	**MAXIMUM DELAY TO SERVICING AT 1M BPS**
	Data Rate
1 Byte	1 $\times$ 8 µS - 1.5 µS = 6.5 µS
2 Byte	2 $\times$ 8 µS - 1.5 µS = 14.5 µS
8 Byte	8 $\times$ 8 µS - 1.5 µS = 62.5 µS
15 Byte	15 $\times$ 8 µS - 1.5 µS = 118.5 µS

At the start of a command the FIFO is always disabled and command parameters must be sent based upon the RQM and DIO bit settings in the main status register. When the FDC enters the command execution phase, it clears the FIFO of any data to ensure that invalid data are not transferred.

An overrun and underrun will terminate the current command and the data transfer. Disk writes will complete the current sector by generating a 00 pattern and valid CRC. Reads require the host to remove the remaining data so that the result phase may be entered.

DMA transfers are enabled with the SPECIFY command and are initiated by the FDC by activating the DRQ pin during a data transfer command. The FIFO is enabled directly by asserting $\overline{\text{DACK}}$ and addresses need not be valid.

Note that if the DMA controller is programmed to function in verify mode a pseudo read is performed by the FDC based only on $\overline{\text{DACK}}$. This mode is only available when the FDC has been configured into byte mode (FIFO disabled) and is programmed to do a read. With the FIFO enabled the above operation is performed by using the new VERIFY command. No DMA operation is needed.¡@

2.1.3 Data Separator

The function of the data separator is to lock onto the incoming serial read data. When a lock is achieved the serial front end logic of the chip is provided with a clock which is synchronized to the read data. The synchronized clock, called the Data Window, is used to internally sample the serial data portion of the bit cell, and the alternate state samples the clock portion. Serial to parallel conversion logic separates the read data into clock and data bytes.

The Digital Data Separator (DDS) has three parts: control logic, error adjustment, and speed tracking. The DDS circuit cycles once every 12 clock cycles ideally. Any data pulse input will be synchronized and then adjusted by immediate error adjustment. The control logic will generate RDD and RWD for every pulse input. During any cycle where no data pulse is present, the DDS cycles are based on speed. A digital integrator is used to keep track of the speed changes in the input data stream.

2.1.4 Write Precompensation

The write precompensation logic is used to minimize bit shifts in the RDDATA stream from the disk drive. Shifting of bits is a known phenomenon in magnetic media and is dependent on the disk media and the floppy drive.

The FDC monitors the bit stream that is being sent to the drive. The data patterns that require precompensation are well known. Depending upon the pattern, the bit is shifted either early or late relative to the surrounding bits.

2.1.5 Perpendicular Recording Mode

The FDC is also capable of interfacing directly to perpendicular recording floppy drives. Perpendicular recording differs from the traditional longitudinal method in that the magnetic bits are oriented vertically. This scheme packs more data bits into the same area.

FDCs with perpendicular recording drives can read standard 3.5" floppy disks and can read and write perpendicular media. Some manufacturers offer drives that can read and write standard and perpendicular media in a perpendicular media drive.

A single command puts the FDC into perpendicular mode. All other commands operate as they normally do. The perpendicular mode requires a 1 Mbps data rate for the FDC. At this data rate the FIFO eases the host interface bottleneck due to the speed of data transfer to or from the disk.

2.1.6 FDC Core

The W83977TF FDC is capable of performing twenty commands. Each command is initiated by a multi-byte transfer from the microprocessor. The result can also be a multi-byte transfer back to the microprocessor. Each command consists of three phases: command, execution, and result.

Command

The microprocessor issues all required information to the controller to perform a specific operation.

Execution

The controller performs the specified operation.

Result

After the operation is completed, status information and other housekeeping information is provided to the microprocessor.

2.1.7 FDC Commands

Command Symbol Descriptions:

C:	Cylinder number 0 - 256
D:	Data Pattern
DIR:	Step Direction
	DIR = 0, step out
	DIR = 1, step in
DS0:	Disk Drive Select 0
DS1:	Disk Drive Select 1
DTL:	Data Length
EC:	Enable Count
EOT:	End of Track
EFIFO:	Enable FIFO
EIS:	Enable Implied Seek
EOT:	End of track
FIFOTHR:	FIFO Threshold
GAP:	Gap length selection
GPL:	Gap Length
H:	Head number
HDS:	Head number select
HLT:	Head Load Time
HUT:	Head Unload Time
LOCK:	Lock EFIFO, FIFOTHR, PTRTRK bits prevent affected by software reset
MFM:	MFM or FM Mode
MT:	Multitrack
N:	The number of data bytes written in a sector
NCN:	New Cylinder Number
ND:	Non-DMA Mode
OW:	Overwritten
PCN:	Present Cylinder Number
POLL:	Polling Disable
PRETRK:	Precompensation Start Track Number

R: Record
RCN: Relative Cylinder Number
R/W: Read/Write
SC: Sector/per cylinder
SK: Skip deleted data address mark
SRT: Step Rate Time
ST0: Status Register 0
ST1: Status Register 1
ST2: Status Register 2
ST3: Status Register 3
WG: Write gate alters timing of WE

(1) Read Data

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	0	0	1	1	0	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
	W	---------- DTL ----------								
Execution										Data transfer between the FDD and system
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after command execution
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(2) Read Deleted Data

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	0	1	1	0	0	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
	W	---------- DTL ----------								
Execution										Data transfer between the FDD and system
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after command execution
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(3) Read A Track

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	0	0	1	0	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
	W	---------- DTL ----------								
Execution										Data transfer between the FDD and system; FDD reads contents of all cylinders from index hole to EOT
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after command execution
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(4) Read ID

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	1	0	1	0	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
Execution										The first correct ID information on the cylinder is stored in Data Register
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Disk status after the command has been completed
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(5) Verify

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	1	0	1	1	0	Command codes
	W	EC	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
		---------- DTL/SC ----------								
Execution										No data transfer takes place
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after command execution
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(6) Version

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	0	0	Command code
Result	R	1	0	0	1	0	0	0	0	Enhanced controller

(7) Write Data

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	0	0	0	1	0	1	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to Command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
	W	---------- DTL ----------								
Execution										Data transfer between the FDD and system
Result	R	---------- ST0 ----------								Status information after Command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after Command execution
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(8) Write Deleted Data

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	0	0	1	0	0	1	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
	W	---------- DTL ----------								
Execution										Data transfer between the FDD and system
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after command execution
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(9) Format A Track

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	1	1	0	1	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- N ----------								Bytes/Sector
	W	---------- SC ----------								Sectors/Cylinder
	W	---------- GPL ----------								Gap 3
	W	---------- D ----------								Filler Byte
Execution for Each Sector Repeat:	W	---------- C ----------								Input Sector Parameters
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- Undefined ----------								
	R	---------- Undefined ----------								
	R	---------- Undefined ----------								
	R	---------- Undefined ----------								

(10) Recalibrate

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	1	1	1	Command codes
	W	0	0	0	0	0	0	DS1	DS0	
Execution										Head retracted to Track 0 Interrupt

(11) Sense Interrupt Status

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	0	0	0	Command code
Result	R	---------- ST0 ----------								Status information at the end of each seek operation
	R	---------- PCN ----------								

(12) Specify

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	0	1	1	Command codes
	W	| ---------SRT ---------- | --------- HUT ---------- |								
	W	|---------- HLT ----------| ND								

(13) Seek

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	1	1	1	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- NCN ----------								
Execution	R									Head positioned over proper cylinder on diskette

(14) Configure

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	1	1	Configure information
	W	0	0	0	0	0	0	0	0	
	W	0	EIS	EFIFO	POLL | ------ FIFOTHR ----|					
	W	| ----------PRETRK ---------- |								
Execution										Internal registers written

(15) Relative Seek

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	1	DIR	0	0	1	1	1	1	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	| ---------- RCN ---------- |								

(16) Dumpreg

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	1	1	0	Registers placed in FIFO
Result	R	---------- PCN-Drive 0----------								
	R	---------- PCN-Drive 1 ----------								
	R	---------- PCN-Drive 2----------								
	R	---------- PCN-Drive 3 ----------								
	R	--------SRT ---------- | --------- HUT --------								
	R	---------- HLT ----------| ND								
	R	---------- SC/EOT ----------								
	R	LOCK	0	D3	D2	D1	D0	GAP	WG	
	R	0	EIS	EFIFO	POLL | ------ FIFOTHR --------					
	R	----------PRETRK ----------								

(17) Perpendicular Mode

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	1	0	Command Code
	W	OW	0	D3	D2	D1	D0	GAP	WG	

(18) Lock

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	LOCK	0	0	1	0	1	0	0	Command Code
Result	R	0	0	0	LOCK	0	0	0	0	

(19) Sense Drive Status

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	1	0	0	Command Code
	W	0	0	0	0	0	HDS	DS1	DS0	
Result	R	---------- ST3 ----------								Status information about disk drive

(20) Invalid

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	---------- Invalid Codes ----------								Invalid codes (no operation- FDC goes to standby state)
Result	R	---------- ST0 ----------								ST0 = 80H

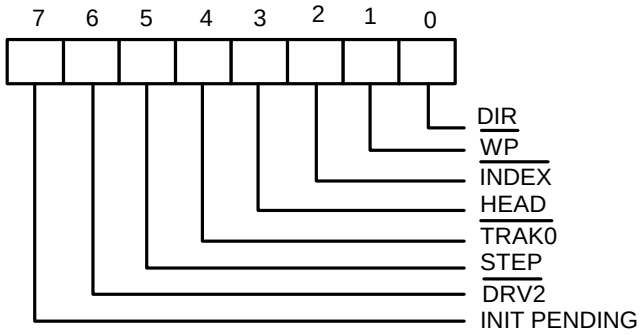
2.2 Register Descriptions

There are several status, data, and control registers in W83977TF. These registers are defined below:

ADDRESS OFFSET	REGISTER	
	READ	WRITE
base address + 0	SA REGISTER	
base address + 1	SB REGISTER	
base address + 2		DO REGISTER
base address + 3	TD REGISTER	TD REGISTER
base address + 4	MS REGISTER	DR REGISTER
base address + 5	DT (FIFO) REGISTER	DT (FIFO) REGISTER
base address + 7	DI REGISTER	CC REGISTER

2.2.1 Status Register A (SA Register) (Read base address + 0)

This register is used to monitor several disk interface pins in PS/2 and Model 30 modes. In PS/2 mode, the bit definitions for this register are as follows:



INIT PENDING (Bit 7):

This bit indicates the value of the floppy disk interrupt output.

$\overline{\text{DRV2}}$ (Bit 6):

0 A second drive has been installed

1 A second drive has not been installed

STEP (Bit 5):

This bit indicates the complement of $\overline{\text{STEP}}$ output.

$\overline{\text{TRAK0}}$ (Bit 4):

This bit indicates the value of $\overline{\text{TRAK0}}$ input.

HEAD (Bit 3):

This bit indicates the complement of $\overline{\text{HEAD}}$ output.

0 side 0

1 side 1

$\overline{\text{INDEX}}$ (Bit 2):

This bit indicates the value of $\overline{\text{INDEX}}$ output.

$\overline{\text{WP}}$ (Bit 1):

0disk is write-protected

1disk is not write-protected

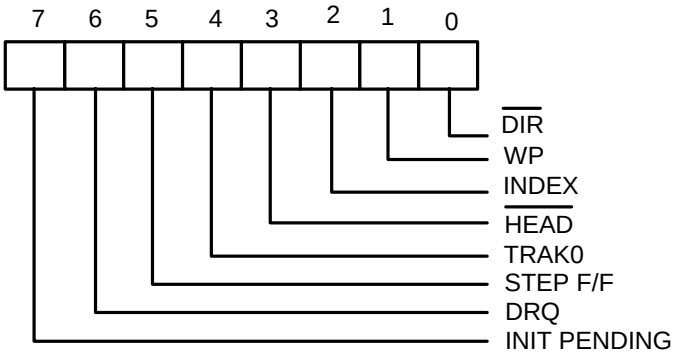
DIR (Bit 0)

This bit indicates the direction of head movement.

0 outward direction

1 inward direction

In PS/2 Model 30 mode, the bit definitions for this register are as follows:



INIT PENDING (Bit 7):

This bit indicates the value of the floppy disk interrupt output.

DRQ (Bit 6):

This bit indicates the value of DRQ output pin.

STEP F/F (Bit 5):

This bit indicates the complement of latched $\overline{\text{STEP}}$ output.

TRAK0 (Bit 4):

This bit indicates the complement of $\overline{\text{TRAK0}}$ input.

$\overline{\text{HEAD}}$ (Bit 3):

This bit indicates the value of $\overline{\text{HEAD}}$ output.

0 side 1

1 side 0

INDEX (Bit 2):

This bit indicates the complement of $\overline{\text{INDEX}}$ output.

WP (Bit 1):

0 disk is not write-protected

1 disk is write-protected

$\overline{\text{DIR}}$ (Bit 0)

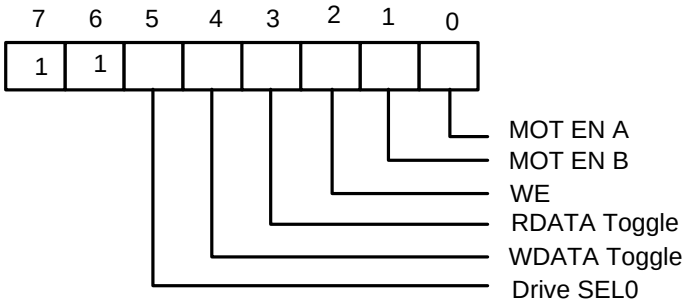
This bit indicates the direction of head movement.

0 inward direction

1 outward direction

2.2.2 Status Register B (SB Register) (Read base address + 1)

This register is used to monitor several disk interface pins in PS/2 and Model 30 modes. In PS/2 mode, the bit definitions for this register are as follows:



Drive SEL0 (Bit 5):

This bit indicates the status of DO REGISTER bit 0 (drive select bit 0).

WDATA Toggle (Bit 4):

This bit changes state at every rising edge of the $\overline{\text{WD}}$ output pin.

RDATA Toggle (Bit 3):

This bit changes state at every rising edge of the $\overline{\text{RDATA}}$ output pin.

WE (Bit 2):

This bit indicates the complement of the $\overline{\text{WE}}$ output pin.

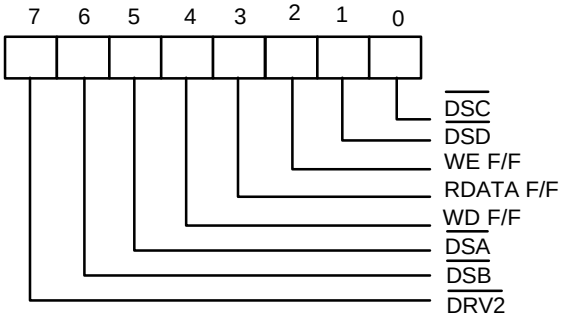
MOT EN B (Bit 1)

This bit indicates the complement of the $\overline{\text{MOB}}$ output pin.

MOT EN A (Bit 0)

This bit indicates the complement of the $\overline{\text{MOA}}$ output pin.

In PS/2 Model 30 mode, the bit definitions for this register are as follows:



$\overline{DRV2}$ (Bit 7):

0 A second drive has been installed

1 A second drive has not been installed

$\overline{DSB}$ (Bit 6):

This bit indicates the status of $\overline{DSB}$ output pin.

$\overline{DSA}$ (Bit 5):

This bit indicates the status of $\overline{DSA}$ output pin.

WD F/F(Bit 4):

This bit indicates the complement of the latched $\overline{WD}$ output pin at every rising edge of the $\overline{WD}$ output pin.

RDATA F/F(Bit 3):

This bit indicates the complement of the latched $\overline{RDATA}$ output pin .

WE F/F (Bit 2):

This bit indicates the complement of latched $\overline{WE}$ output pin.

$\overline{DSD}$ (Bit 1):

0 Drive D has been selected

1 Drive D has not been selected

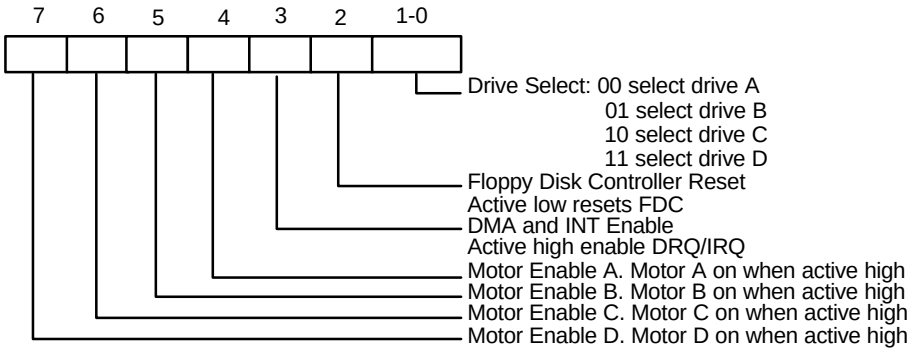
$\overline{DSC}$ (Bit 0):

0 Drive C has been selected

1 Drive C has not been selected

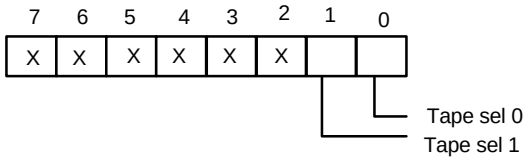
2.2.3 Digital Output Register (DO Register) (Write base address + 2)

The Digital Output Register is a write-only register controlling drive motors, drive selection, DRQ/IRQ enable, and FDC resetting. All the bits in this register are cleared by the MR pin. The bit definitions are as follows:

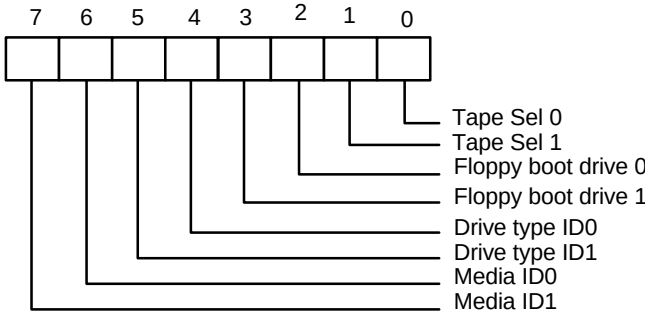


2.2.4 Tape Drive Register (TD Register) (Read base address + 3)

This register is used to assign a particular drive number to the tape drive support mode of the data separator. This register also holds the media ID, drive type, and floppy boot drive information of the floppy disk drive. In normal floppy mode, this register includes only bit 0 and 1. The bit definitions are as follows:



If three mode FDD function is enabled (EN3MODE = 1 in Logical Device 0 CRF0 bit:0), the bit definitions are as follows:



Media ID1 Media ID0 (Bit 7, 6):

These two bits are read only. These two bits reflect the value of Logical Device 0 CRF1 bit 4,5.

Drive type ID1 Drive type ID0 (Bit 5, 4):

These two bits reflect two of the bits of Logical Device 0 CRF2. Which two bits are reflected depends on the last drive selected in the DO REGISTER.

Floppy Boot drive 1, 0 (Bit 3, 2):

These two bits reflect the value of Logical Device 0 CRF1 bit 7,6.

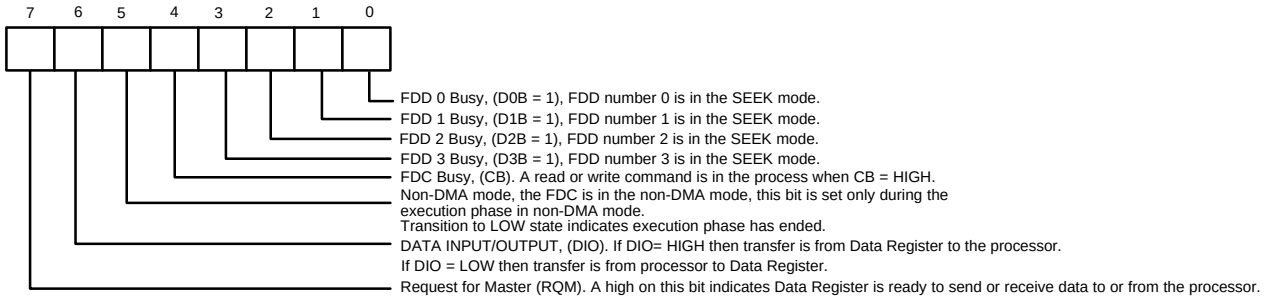
Tape Sel 1, Tape Sel 0 (Bit 1, 0):

These two bits assign a logical drive number to the tape drive. Drive 0 is not available as a tape drive and is reserved as the floppy disk boot drive.

TAPE SEL 1	TAPE SEL 0	DRIVE SELECTED
0	0	None
0	1	1
1	0	2
1	1	3

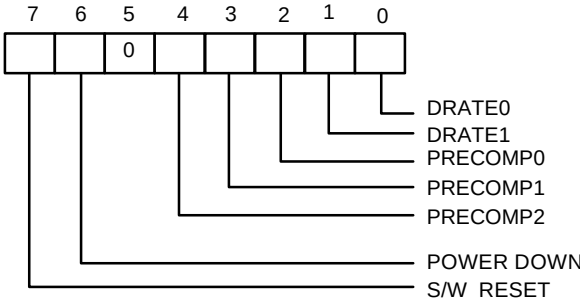
2.2.5 Main Status Register (MS Register) (Read base address + 4)

The Main Status Register is used to control the flow of data between the microprocessor and the controller. The bit definitions for this register are as follows:



2.2.6 Data Rate Register (DR Register) (Write base address + 4)

The Data Rate Register is used to set the transfer rate and write precompensation. The data rate of the FDC is programmed by the CC REGISTER for PC-AT and PS/2 Model 30 and PS/2 mode, and not by the DR REGISTER. The real data rate is determined by the most recent write to either of the DR REGISTER or CC REGISTER.



S/W RESET (Bit 7):

This bit is the software reset bit.

POWER-DOWN (Bit 6):

0 FDC in normal mode

1 FDC in power-down mode

PRECOMP2 PRECOMP1 PRECOMP0 (Bit 4, 3, 2):

These three bits select the value of write precompensation. The following tables show the precompensation values for the combination of these bits.

PRECOMP	PRECOMPENSATION DELAY	
2 1 0	250K - 1 Mbps	2 Mbps Tape drive
0 0 0	Default Delays	Default Delays
0 0 1	41.67 nS	20.8 nS
0 1 0	83.34 nS	41.17 nS
0 1 1	125.00 nS	62.5nS
1 0 0	166.67 nS	83.3 nS
1 0 1	208.33 nS	104.2 nS
1 1 0	250.00 nS	125.00 nS
1 1 1	0.00 nS (disabled)	0.00 nS (disabled)

DATA RATE	DEFAULT PRECOMPENSATION DELAYS
250 KB/S	125 nS
300 KB/S	125 nS
500 KB/S	125 nS
1 MB/S	41.67 nS
2 MB/S	20.8 nS

DRATE1 DRATE0 (Bit 1, 0):
These two bits select the data rate of the FDC and reduced write current control.

00 500 KB/S (MFM), 250 KB/S (FM), $\overline{RWC}$ = 1

01 300 KB/S (MFM), 150 KB/S (FM), $\overline{RWC}$ = 0

10 250 KB/S (MFM), 125 KB/S (FM), $\overline{RWC}$ = 0

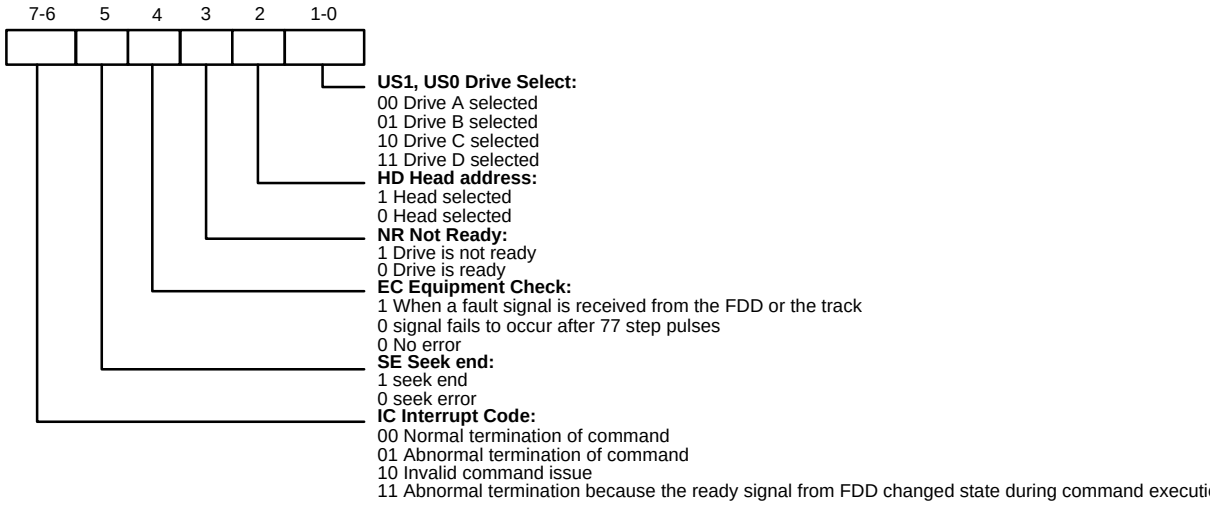
11 1 MB/S (MFM), Illegal (FM), $\overline{RWC}$ = 1

The 2 MB/S data rate for Tape drive is only supported by setting 01 to DRATE1 and DRATE0 bits, as well as setting 10 to DRT1 and DRT0 bits which are two of the Configure Register CRF4 or CRF5 bits in logic device 0. Please refer to the function description of CRF4 or CRF5 and data rate table for individual data rates setting.

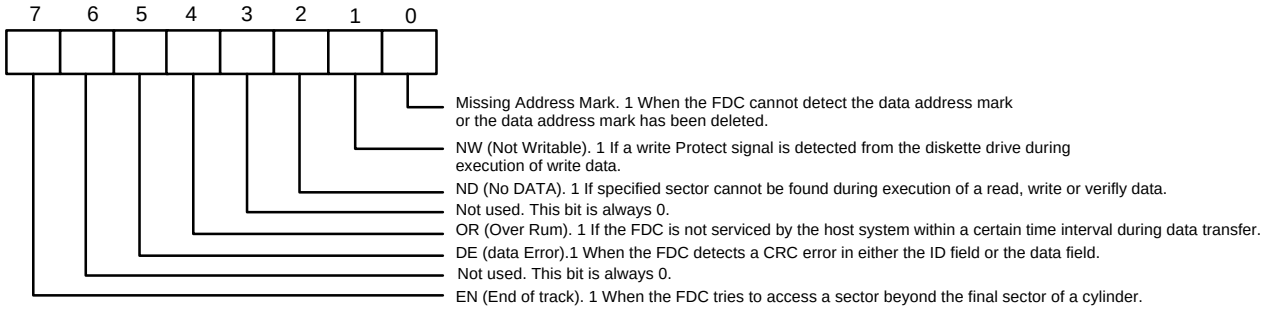
2.2.7 FIFO Register (R/W base address + 5)

The Data Register consists of four status registers in a stack with only one register presented to the data bus at a time. This register stores data, commands, and parameters and provides diskette-drive status information. Data bytes are passed through the data register to program or obtain results after a command. In the W83977TF, this register defaults to FIFO disabled mode after reset. The FIFO can change its value and enable its operation through the CONFIGURE command.

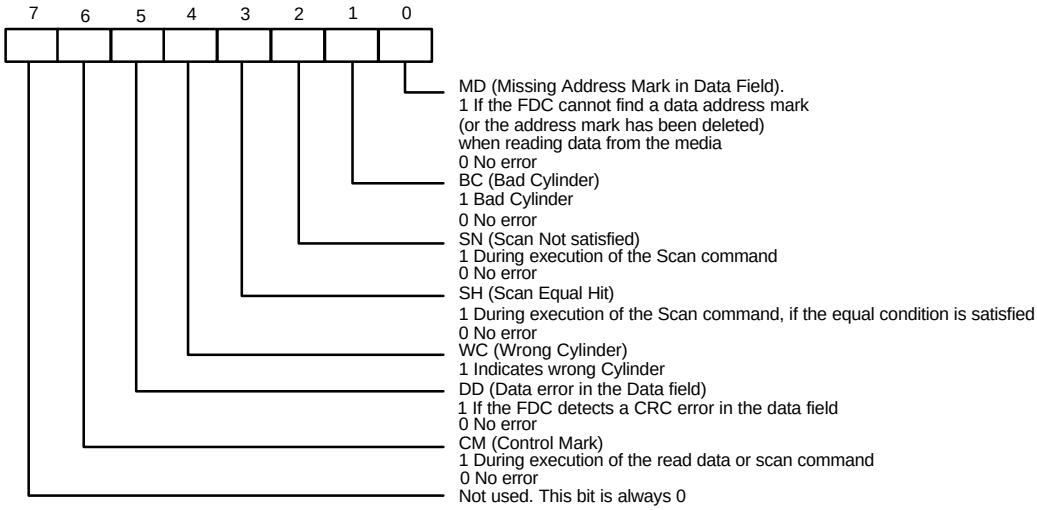
Status Register 0 (ST0)



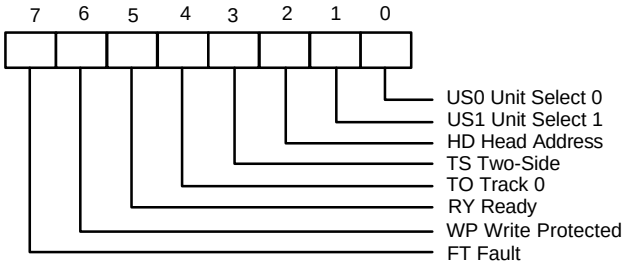
Status Register 1 (ST1)



Status Register 2 (ST2)

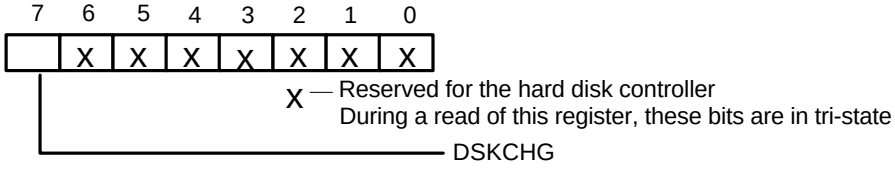


Status Register 3 (ST3)

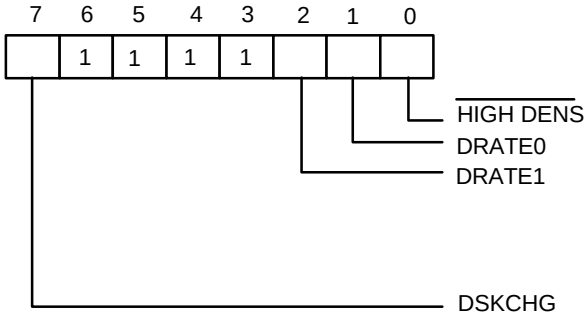


2.2.8 Digital Input Register (DI Register) (Read base address + 7)

The Digital Input Register is an 8-bit read-only register used for diagnostic purposes. In a PC/XT or AT only Bit 7 is checked by the BIOS. When the register is read, Bit 7 shows the complement of $\overline{\text{DSKCHG}}$, while other bits of the data bus remain in tri-state. Bit definitions are as follows:



In the PS/2 mode, the bit definitions are as follows:



DSKCHG (Bit 7):

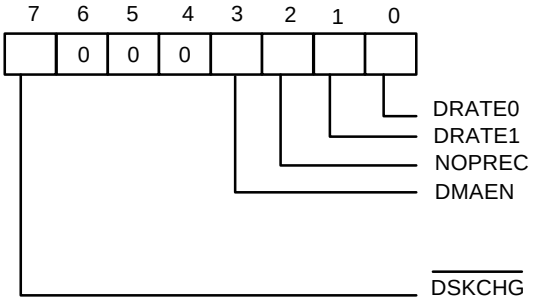
This bit indicates the complement of the $\overline{\text{DSKCHG}}$ input.

Bit 6-3: These bits are always a logic 1 during a read.

DRATE1 DRATE0 (Bit 2, 1):
These two bits select the data rate of the FDC. Refer to the DR register bits 1 and 0 for the settings corresponding to the individual data rates.

$\overline{\text{HIGH DENS}}$ (Bit 0):
0 500 KB/S or 1 MB/S data rate (high density FDD)
1 250 KB/S or 300 KB/S data rate

In the PS/2 Model 30 mode, the bit definitions are as follows:



DSKCHG (Bit 7):
This bit indicates the status of $\overline{\text{DSKCHG}}$ input.

Bit 6-4: These bits are always a logic 1 during a read.

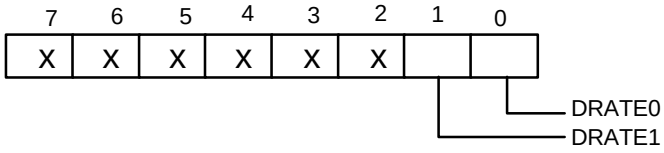
DMAEN (Bit 3):
This bit indicates the value of DO REGISTER bit 3.

NOPREC (Bit 2):
This bit indicates the value of CC REGISTER NOPREC bit.

DRATE1 DRATE0 (Bit 1, 0):
These two bits select the data rate of the FDC.

2.2.9 Configuration Control Register (CC Register) (Write base address + 7)

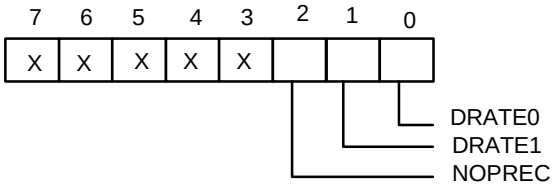
This register is used to control the data rate. In the PC/AT and PS/2 mode, the bit definitions are as follows:



X: Reserved

Bit 7-2: Reserved. These bits should be set to 0.

DRATE1 DRATE0 (Bit 1, 0):
These two bits select the data rate of the FDC.
In the PS/2 Model 30 mode, the bit definitions are as follows:



X: Reserved

Bit 7-3: Reserved. These bits should be set to 0.

NOPREC (Bit 2):
This bit indicates no precompensation. It has no function and can be set by software.

DRATE1 DRATE0 (Bit 1, 0):
These two bits select the data rate of the FDC.