PRELIMINARY DATA SHEET

VSP 94x2A
PRIMUS
Powerful Scan Rate Converter including Multistandard Color Decoder

Edition Oct. 24, 2001
6251-552-3PD

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VSP 94x2A **Revision History:**	**10.2001** Preliminary
Previous Versions:	
2.0a	
2.0f	
2.0k	
2.1a	A22
3.0	A31

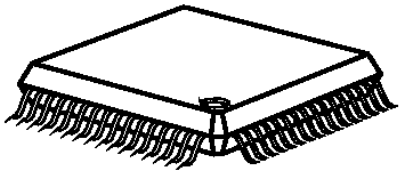
Preliminary

Powerful scanRate converter Including **VSP 94x2A**

MUltiStandard color decoder

Version 3.4 **CMOS**

1 General Description



P-MQFP-80-1

The VSP 94x2A (PRIMUS) is a new component of the Micronas MEGAVISION® IC set in a CMOS embedded DRAM technology. The VSP 94x2A comprises all main functions of a digital featurebox in one monolithic IC. The amount of features is limited in favour of a low-cost solution. But no trade-off has been made concerning picture quality. The family is ideally suited to work in conjunction with the deflection processors SDA9380 (9402/32) and DDP3315C (9412/42). In combination with the 'digital TV decoder' MDE 9500 double-scan iDTV are possible. The package is pin-upward compatible to other medium-range and high-end devices of the VSP94xy family. A 50/60Hz derivative is also available (9432, 9442).

Version	Scan-rate-conversion	digital input	digital output	analog output
9402A	100i/120i	(X)[1)]	(X)[1)]	X
9412A[2)]	100i/120i	X	X	
9432A	50i/60i	(X)[1)]	(X)[1)]	X
9442A[2)]	50i/60i	X	X	

1) Input and output can not be used at same time (pin sharing)

2) under development

Table 1- 1 Primus' versions

The device comprises a digital multistandard color decoder, a RGB interface with fast-blank capability (SCART), digital ITU656 input, scaling units including panorama, embedded DRAM for upconversion, picture improvements, temporal noise reduction as well as A/D and D/A converter.

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2 Features

- **Integrated Video Matrix switch**
  - Up to seven CVBS inputs, up to two Y/C inputs,
  - Up to three CVBS outputs (even when Y/C input)
  - 9 bit amplitude resolution for CVBS, Y/C A/D converter
  - AGC (Automatic Gain Control)
- **Multi-standard color decoder**
  - PAL/NTSC/SECAM including all substandards
  - Automatic recognition of chroma standard
  - Only one crystal necessary for all standards
- **RGB-FBL or YUV-H-V input**
  - 8 bit amplitude resolution for RGB or YUV
  - 8 bit amplitude resolution for FBL or H
- **ITU656 support** (version dependent, refer to next chapter)
  - ITU656 input/output
  - DS656 output (double-scan ’656like’ output)
- **Noise reduction**
  - Motion adaptive temporal noise reduction
  - Field-based temporal noise reduction for luminance and chrominance
  - Different motion detectors for luminance and chrominance or identical
  - Flexible programming of the temporal noise reduction parameters
  - Automatic measurement of the noise level
- **Horizontal scaling of the $1f_H$ signal**
  - Split-screen possible with additional PiP or Text processor
- **Flexible digital horizontal scaling of the $2f_H$ signal**
  - Scaling factors: 3, ... [2 pixel resolution], ..., 0.75 including 16:9 compatibility
  - 5 zone panorama generator
- **Embedded memory**
  - On-chip memory controller
  - Embedded DRAM core for field memory
  - SRAM for PAL/SECAM delay line
- **Data format 4:2:2**
- **Flexible clock and synchronization concept**
  - Horizontal line-locked or free-running mode
  - Vertical locked or free-running mode
- **Scan-rate-conversion**
  - Simple interlaced modes (100/120 Hz): AABB, AAAA, BBBB (9402A/9412A only)
  - No scan-rate-conversion modes (50/60 Hz): AB, AA, BB (9432A/9442A only)
- **Flexible output sync controller**
  - Flexible positioning of the output signal
  - Flexible programming of the output sync raster
  - ’Blank signal’ generation

- **Signal manipulations**
  - Still field
  - Insertion of colored background
  - Windowing
  - Vertical chrominance shift for improved VCR picture quality
- **Sharpness improvement**
  - Digital color transition improvement (DCTI)
  - Peaking (luminance)
- **Three D/A converters**
  - 9 bit amplitude resolution for Y, -(R-Y), -(B-Y) output
  - 72 MHz clock frequency
  - Two-fold oversampling for Anti-imaging
  - Simplification of external analog postfiltering
- **1920 active pixel/per line in default configuration**
- **I²C-bus control (400 kHz)**
  - selectable I²C address
- **1.8V± 5% and 3.3V ± 5% supply voltages**
- **P-MQFP-80 package**

3 Block Diagram

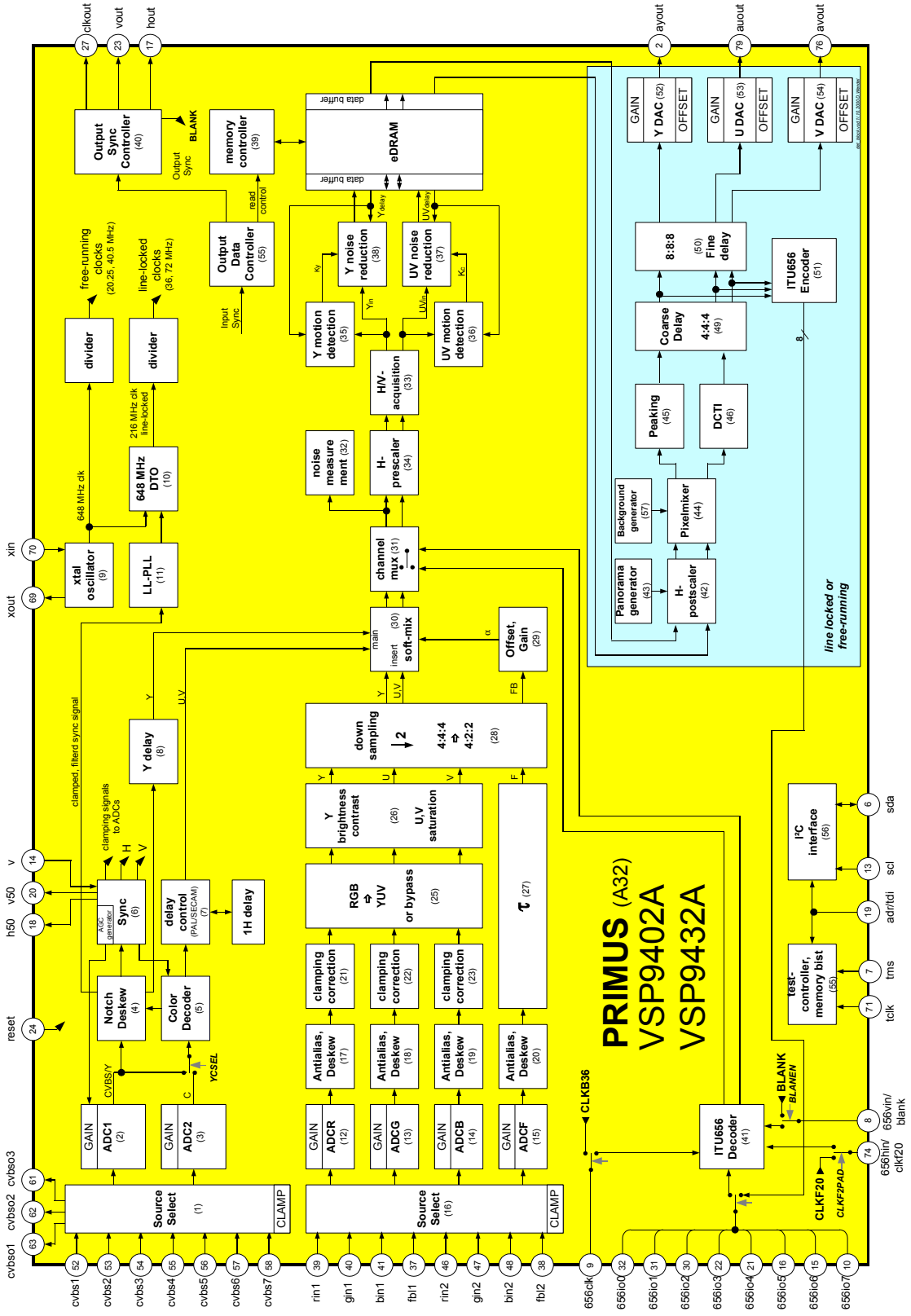

Figure 3-1 Block Diagram

4 Pin Description

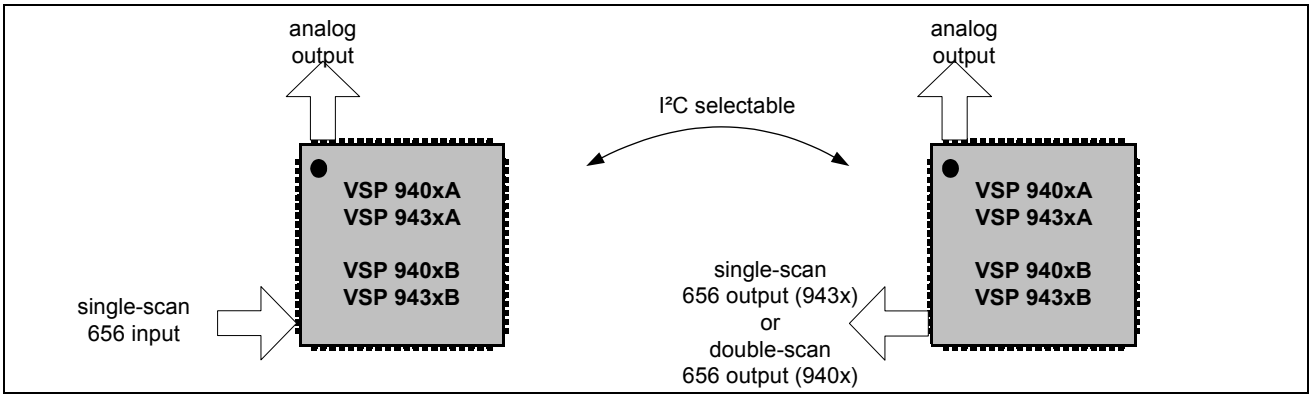

Figure 4-1 Signal flow 940x, 943x

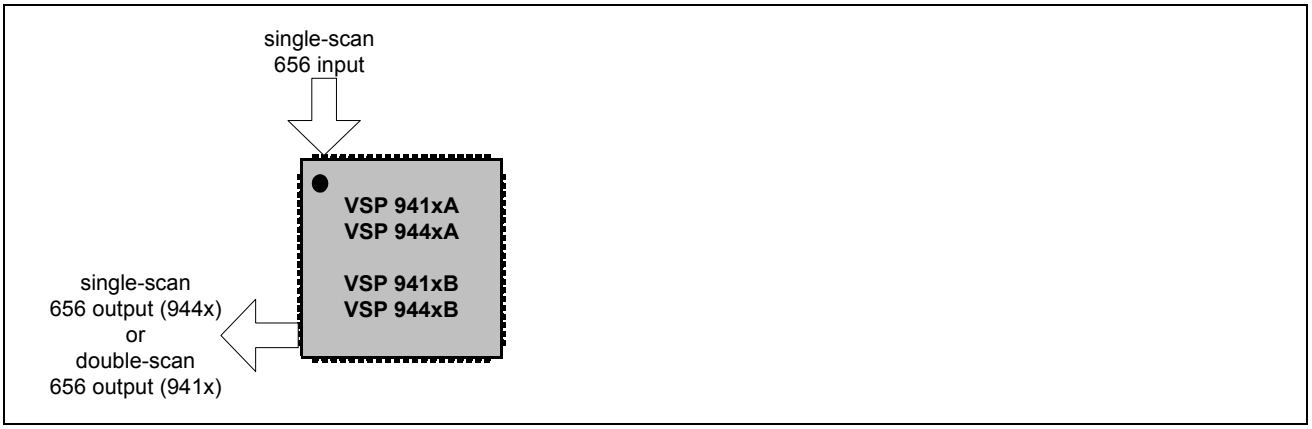

Figure 4-2 Signal flow 941x, 944x, 942x

Hardware compatible[1)]	suited backend IC		
	DDP3310B	DDP3315C	SDA9380
VSP 94**02A**, VSP 94**32A** VSP 94**05B**, VSP 94**35B** VSP 94**07B,** VSP 94**37B** VSP 94**09C**		● (no ITU656 input possible)	●
VSP 94**12A,** VSP 94**42A** VSP 94**15B**, VSP 94**45B** VSP 94**17B**, VSP 94**47B** VSP 94**19C**		●	
VSP 94**25B,** VSP 94**27B** VSP 94**29C**	●	●	●

1) with some restrictions. Please refer to pin description and/or respective application note

Table 4-1 Hardware compatibility and suited backend ICs

4.1 Pin list

pin	9402/32	9412/42	I/O	9402/32	9412/42	remark	if not used,..
52	cvbs1		I	CVBS input		analog input	connect to vss
53	cvbs2		I	CVBS input		analog input	connect to vss
54	cvbs3		I	CVBS input		analog input	connect to vss
55	cvbs4		I	CVBS input or Y1		analog input	connect to vss
56	cvbs5		I	CVBS input or C1		analog input	connect to vss
57	cvbs6		I	CVBS input or Y2		analog input	connect to vss
58	cvbs7		I	CVBS input or C2		analog input	connect to vss
63	cvbso1		O	CVBS output 1		analog output	leave open
62	cvbso2		O	CVBS output 2		analog output	leave open
61	cvbso3		O	CVBS output 3		analog output	leave open
70	xin		I	Crystal connection 1			
69	xout		O	Crystal connection 2			
23	vout		O	vertical output		single or double scan, dependent on version	leave open
17	hout		O	horizontal output			leave open
3	vssdacy	i656i7	S/I	DAC (Y)	656 input (MSB)		
2	ayout	i656i6	O/I	Y output	656 input		
1	vdddacy	i656i5	S/I	DAC (Y)	656 input		
80	vssdacu	i656i4	S/I	DAC (U)	656 input		
79	auout	i656i3	O/I	U output	656 input		
78	vdddacu	i656i2	S/I	DAC (U)	656 input		
77	vssdacv	i656i1	S/I	DAC (V)	656 input		leave open
76	avout	i656i0	O/I	V output	656 input (LSB)		leave open
75	vdddacv	i656iclk	S/I	DAC (V)	656 input clock	27 MHz nom.	leave open
39	rin1		I	R or V in1		analog input	connect to vss
40	gin1		I	G or Y in1		analog input	connect to vss
41	bin1		I	B of U in1		analog input	connect to vss
37	fbl1		I	Fast Blank input 1 (H1)		analog input	connect to vss
46	rin2		I	R or V in2		analog input	connect to vss
47	gin2		I	G or Y in2		analog input	connect to vss

Pin Description

pin	9402/32	9412/42	I/O	9402/32	9412/42	remark	if not used,..
48	bin2		I	B of U in2		analog input	connect to vss
38	fbl2		I	Fast Blank input 2 (H2)		analog input	connect to vss
14	v[1)]		I	vertical pulse for RGB input			connect to vss
6	sda		I/O	I²C-Bus data			
13	scl		I	I²C-Bus clk			
7	tms		I	testmode select		connect to vdd33	
19	adr / tdi		I	I²C address / test data in			
24	reset		I	Reset input		reset, when low	
27	clkout		O	Output clock		27 MHz	leave open
59	vdd33c		S	supply voltage CVBS		3.3 V	
60	vss33c		S	supply voltage CVBS		0 V	
50	vddac1		S	supply voltage CVBS1		1.8 V	
51	vssac1		S	supply voltage CVBS1		0 V	
64	vddac2		S	supply voltage CVBS2		1.8 V	
65	vssac2		S	supply voltage CVBS2		0 V	
44	vdd33rgb		S	supply voltage RGB		3.3 V	
45	vss33rgb		S	supply voltage RGB		0 V	
42	vddargb		S	supply voltage for RGB		1.8 V	
43	vssargb		S	supply voltage for RGB		0 V	
35	vddafbl		S	supply voltage for FBL		1.8 V	
36	vssafbl		S	supply voltage for FBL		0 V	
68	vddapll		S	supply voltage for PLL		1.8 V	
66	vddd1		S	supply voltage for digital		1.8 V digital	
67	vssd1		S	supply voltage for digital		0 V digital	
5	vddd2		S	supply voltage for digital		1.8 V digital	
4	vssd2		S	supply voltage for digital		0 V digital	
28	vddd3		S	supply voltage for DRAM		1.8 V digital	
29	vssd3		S	supply voltage for digital		0 V digital	
34	vddd4		S	supply voltage for digital		1.8 V digital	
33	vssd4		S	supply voltage for digital		0 V digital	
72	vddp1		S	supply voltage for digital		3.3 V pad	
73	vssp1		S	supply voltage for digital		0 V pad	

pin	9402/32	9412/42	I/O	9402/32	9412/42	remark	if not used,..
12	vddp2		S	supply voltage for digital		3.3 V pad	
11	vssp2		S	supply voltage for digital		0 V pad	
25	vddp3		S	supply voltage for digital		3.3 V pad	
26	vssp3		S	supply voltage for digital		0 V pad	
71	tclk		I	testclock		connect to vss	
18	h50 *2)*		O	Hout 50 Hz		(with skew)	leave open
20	v50 *3)*		O	Vout 50 Hz			leave open
32	656io0		I/O	Digital input / output		LSB	leave open
31	656io1		I/O	Digital input / output			leave open
30	656io2		I/O	Digital input / output			leave open
22	656io3		I/O	Digital input / output			leave open
21	656io4		I/O	Digital input / output			leave open
16	656io5		I/O	Digital input / output			leave open
15	656io6		I/O	Digital input / output			leave open
10	656io7		I/O	Digital input / output		MSB	leave open
9	656clk		I/O	Digital input / output clock			leave open
74	656hin/clkf20		I/O	separate H input for 656 / 20.25 clock output			connect to vss and disable clock
8	656vin/blank[4)]		I/O	separate V input for 656 / BLANK output			connect to vss and disable blank
49	vssd5 *5)*		S	supply voltage for digital		0V	connect to vss

1) In VSP94xxB and VSP94xxC this pin is shared by v and intr (C800 controller output)

2) In VSP94xxB and VSP94xxC this pin is shared by h50 and irq (Data-slicer-interrupt)

3) In VSP94xxB and VSP94xxC this pin is shared by v50 and blank

4) In 9402 A31 (and higher) and in VSP94xxA/B/C, this pin is shared by 656vin and blank

5) This pin is not used and not bonded in VSP94xxA. The use of this pin in VSP94xxB/C will be V_{SS}. For upgradability it is recommended to not leave this pin open.

Table 4- 2 Pin Description

4.2 Pin Configuration P-MQFP80

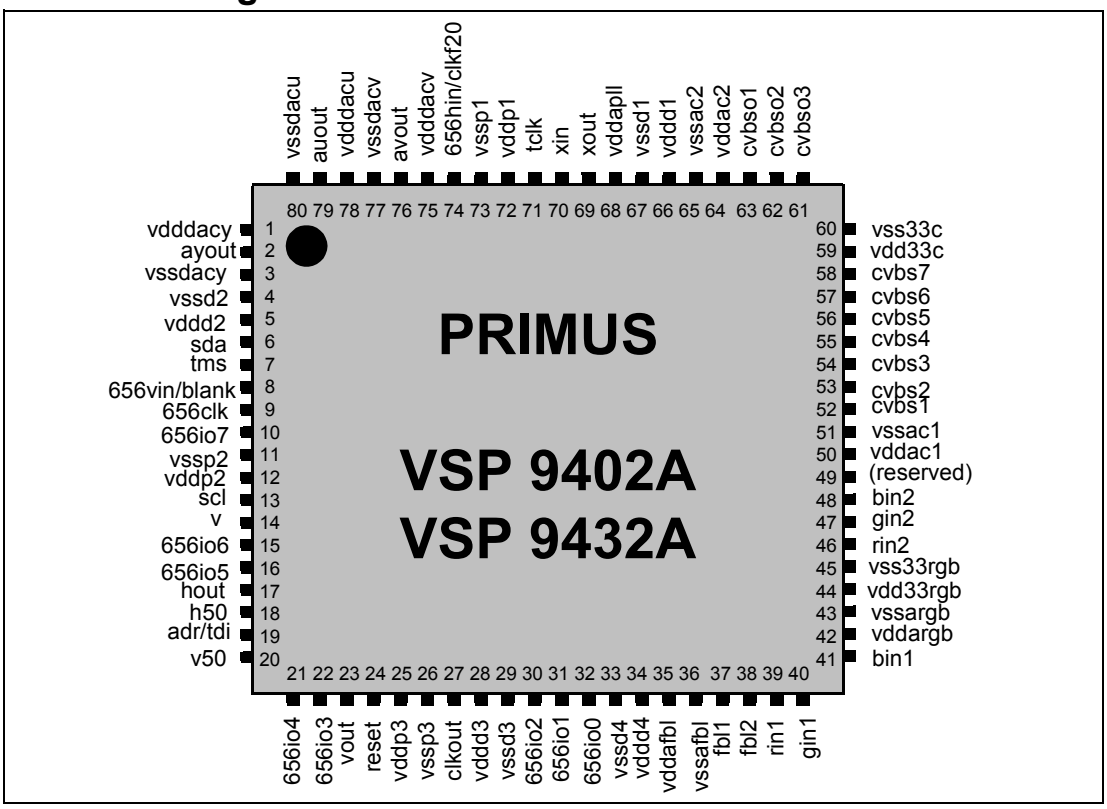

Figure 4-3 P-MQFP-80

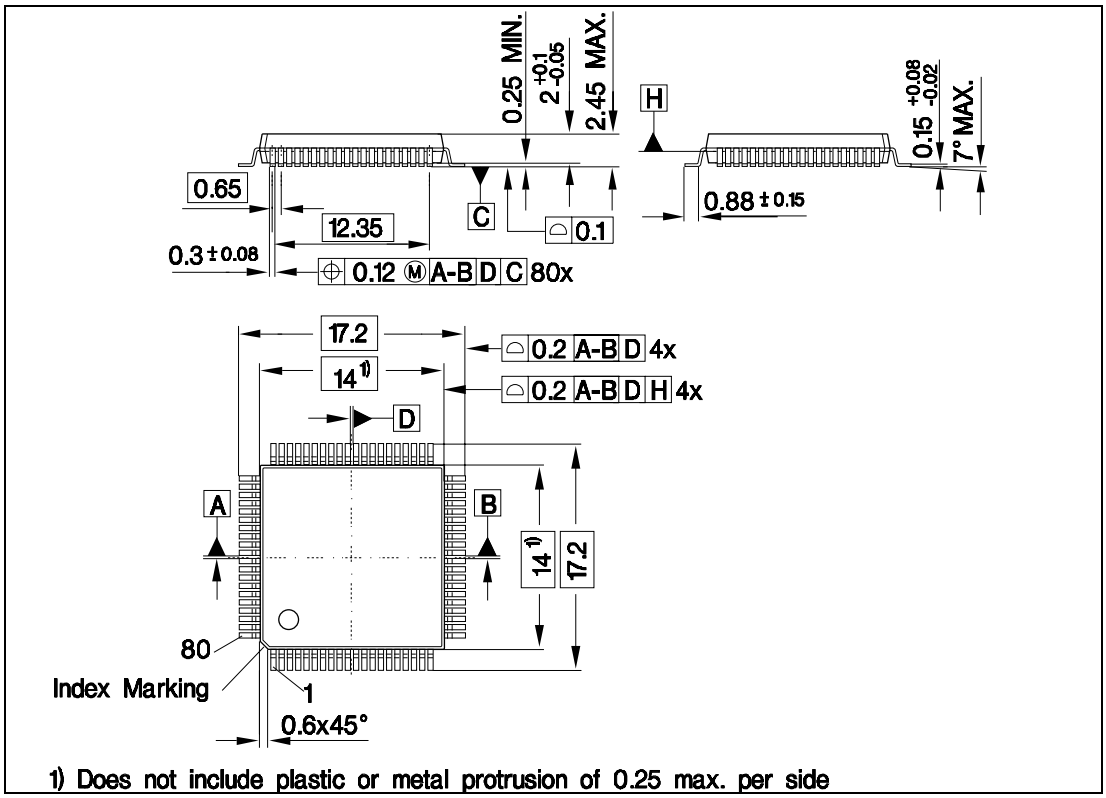

Figure 4-4 Package outlines P-MQFP-80

5 System Description

All I²C bus registers mentioned are printed in bold and italics (e.g. ***YCDEL***)

5.1 CVBS Frontend

The CVBS frontend consists of the color-decoding circuit itself, a sync processing circuit for generation of H/V signals out of the CVBS signal, and the luminance processing. The main task of the luminance processing is to remove the color carrier by means of a notch filter. For PAL and SECAM operation a baseband delay line is used for U and V signals. This can be used as comb filter in NTSC operation (only for chrominance). The RGB input can either be used as an overlay for the CVBS channel (RGB+FBL) or as a full master channel (RGB+H/V). The overlay is done by means of a soft-mix and can be used e.g. for 'SCART' connector. This block incorporates a matrix (for RGB signals) which is switched off for YUV (e.g. YPbPr) input signals. A CBS (contrast, brightness, saturation) control makes the input signal adjustable.

5.1.1 Source select

Figure 5-1 shows the analog frontend. The analog CVBS signal can be fed to the inputs CVBS1...7 of VSP 94x2A (amplitude 0.5...1.5V_{pp}). One signal is selected via ***CVBSEL1*** and fed to first ADC. A second signal is selected via ***CVBSEL2*** and fed to the other ADC. CVBS4&5 or CVBS6&7 are intended to use as separate Y/C inputs (***YCSEL***). After clamping to the back porch (switchable to sync-tip clamping by ***CLPSTGY***) both signals are AD-converted with an amplitude resolution of 9 bit. The conversion is done using a 20.25 MHz free-running stable crystal clock. Before this the signals are lowpassed by antialias filter. Three inputs can be looped back to output CVBSO1-3 (***CVBOSEL1***, ***CVBOSEL2***, ***CVBSELO3***). A signal addition is performed to output a CVBS signal even when separate Y/C signals are used at input. Inputs that are not used are roughly clamped to fit in the allowed voltage region. For stand-by operation (power-down mode), A/D and D/A converter are switched off by ***STANDBY*** keeping the source-selector operational.

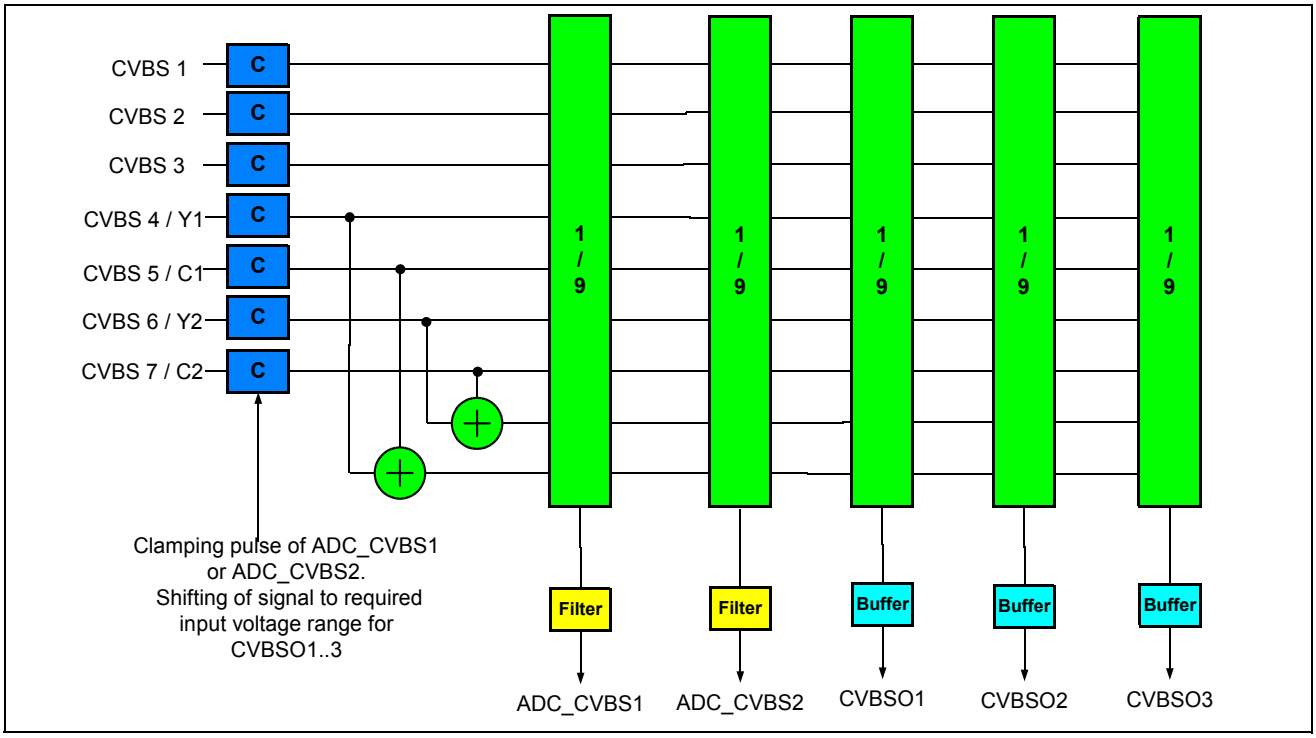

Figure 5-1 Input selection

5.1.2 Signal Magnitudes and Gain Control

To adjust to different CVBS input voltages a digitally working automatic gain control with 64 linear steps is implemented for input voltages in the range from 0.6 to 1.8V_{pp}. For best signal-to-noise ratio the maximum available CVBS amplitude is recommended. The AGC behavior can be chosen from four possible modes (***AGCMD***):

AGCMD	AGC operation mode
00	AGC uses the height of the sync pulse as a reference and additionally reduces amplification when ADC overflows
01	AGC uses the height of the sync pulse as a reference
10	AGC uses only ADC overflows
11	AGC is disabled and the ADC fits to the values given in **AGCADJ1**

Table 5- 1 AGC modes

When using the sync height, the A/D gain rises or falls depending on the incoming signal. When using overflow detection only, the gain is set to maximum and is reduced whenever an ’overflow’ occurs. The signal is lowpassed so that chrominance and noise are not used for detection. The threshold can be adjusted by ***PWTHD***. A setting of ’11’

equals 511 and means an overflow of the ADC. Other settings react for a lower level. The gain only becomes higher when a change of the channel is detected or is manually reset by ***AGCRES***. ***AGCFRZE*** holds the current AGC value. With ***AGCADJ1*** and ***AGCADJ2***, both ADCs are gain controlled manually.

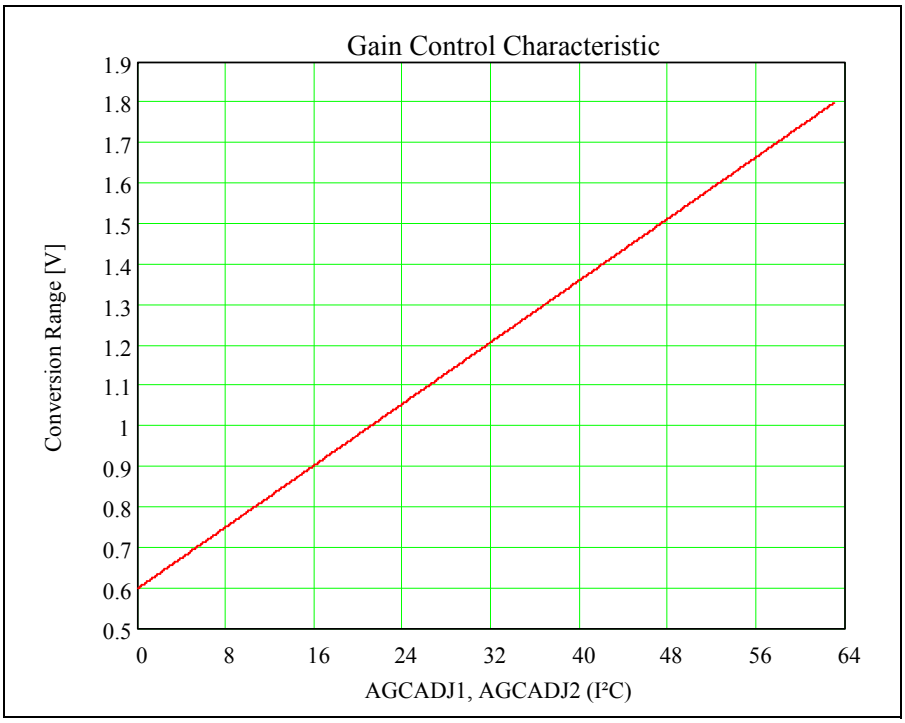

Figure 5-2 CVBS ADC characteristic

The conversion range (CR) is bigger than the signal range (SRY, SRC) leaving a headroom for overshoots (**Figure 5-3**)

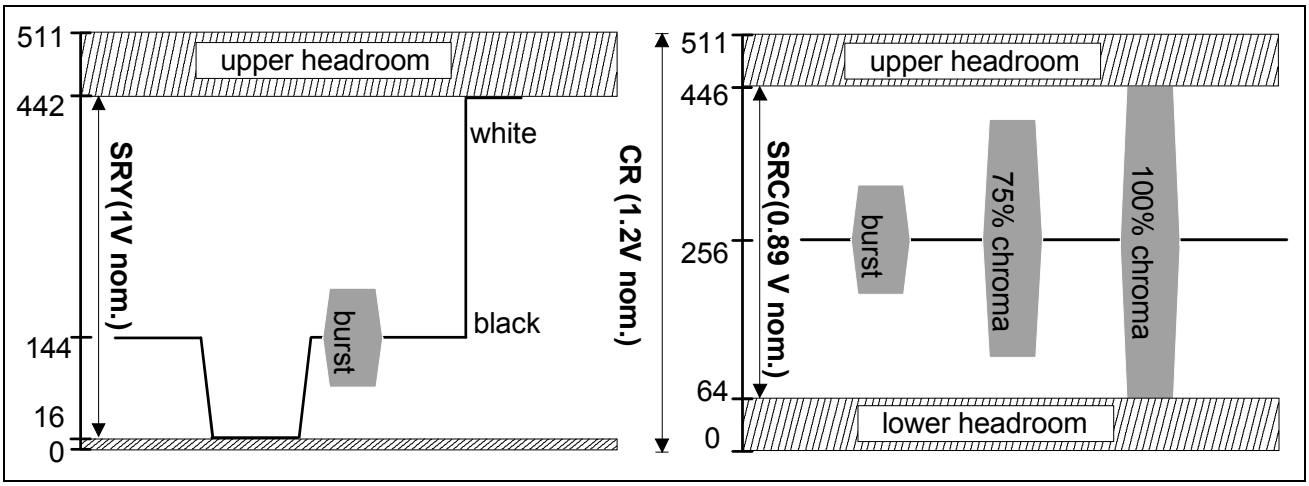

Figure 5-3 CVBS, Y and C amplitude characteristics

5.1.3 Clamping

The clamp timing for the analog inputs is generated from its corresponding CVBS signal. The clamping algorithm works with a split *measurement* pulse and a *clamping* pulse. The measurement pulse is used to detect the clamping error. The clamping pulse is used to enable current sources for reducing the detected clamping errors. The start and length of the measurement signal is adjustable independently for both channels (***CLMPST1***, ***CLMPD1***, ***CLMPST2***, ***CLMPD2***). The start and length of the clamping signal is adjustable for both channels independently (***CLMPST1S***, ***CLMPD1S***, ***CLMPST2S***, ***CLMPD2S***). Clamping signals for RGB-channel are not split. Clamping for these ADC are controlled by ***CLMPST2S*** and ***CLMPD2S*** only. Clamping can be suppressed for some lines by ***CLMPLOW*** and ***CLMPHIGH*** to ignore copyprotection information. No external sync signals are required.

signal	description
CLMPST1	measurement pulse start for ADC1
CLMPD1	measurement pulse duration for ADC1
CLMPST1S	clamping pulse start for ADC1
CLMPD1S	clamping pulse duration for ADC1
CLMPST2	(measurement pulse start for ADC2)
CLMPD2	(measurement pulse duration for ADC2)
CLMPST2S	measure and clamp start for RGBF-ADC (clamping start for ADC2)
CLMPD2S	measure and clamp duration for RGBF-ADC (clamping duration for ADC2

Table 5- 2 Clamping adjustment

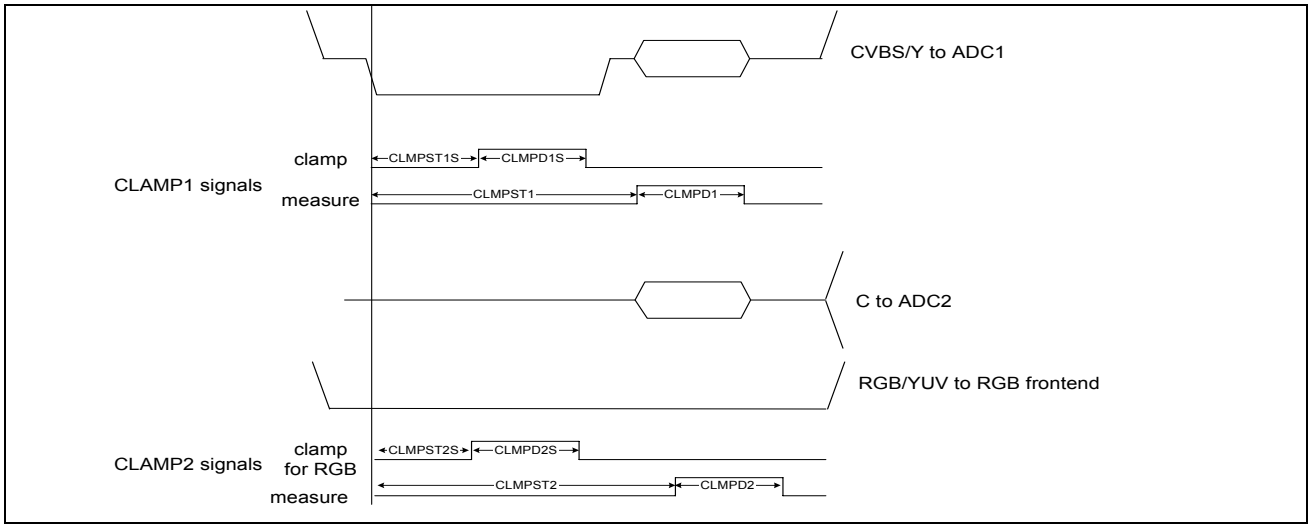

Figure 5-4 Clamping signals

5.1.4 Synchronization

After elimination of the high frequency components of the CVBS signal by a low pass filter, horizontal and vertical sync pulses are separated. Horizontal sync pulses are generated by a digital phase locked loop. The time constant can be adjusted between fast and slow behavior in four steps (***PLLTC***) to accommodate different input sources (e.g. VCR). The time-constant can be changed during normal operation without visible picture degradation. A fine tuning of the PLL time constant can be done by ***NSRED***.

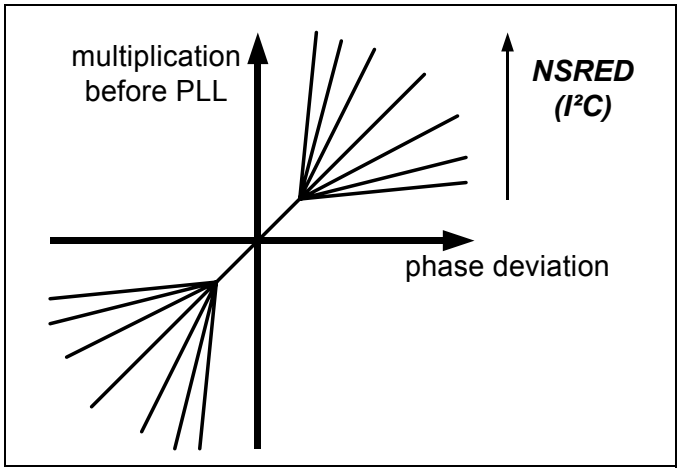

Figure 5-5 NSRED characteristic

Additionally weak input signals from a satellite dish (’fish’) become more stable when ***SATNR*** is enabled. Vertical sync pulses are separated by integration of equalizing pulses. A vertical flywheel mode improves vertical sync separation for weak signals (***VFLYWHL, VFLYWHLMD***). Additionally, v-syncs may be gated by ***VTHRL*** and ***VTHRH*** to reject invalid v-syncs. When no input signal is connected the device switches to a free-running mode. The device can be configured to switch-on background color when no or only a weak signal is applied (***NOSIGB***). 50 Hz or 60 Hz operation for sync separation may be forced separately or selected to work automatically (***FLNSTRD***)

5.1.5 Chroma Decoder

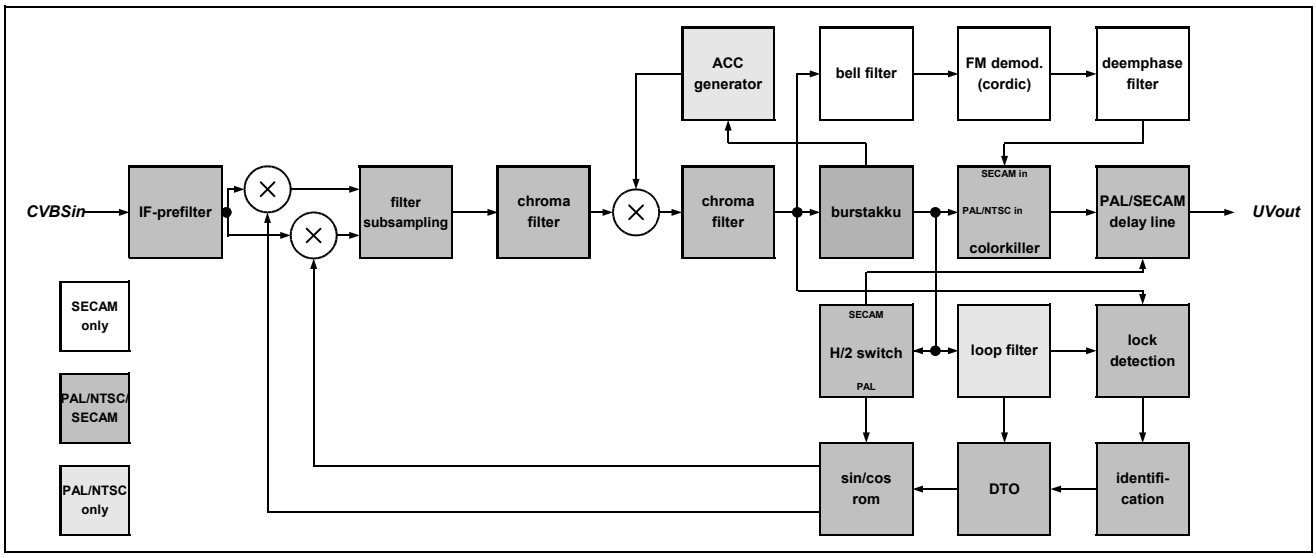

Figure 5-6 Chroma decoding overview

The digital multistandard chroma decoder is able to decode NTSC and PAL signals with a subcarrier frequency of 3.58MHz and 4.43MHz (PAL B[1)]/M/N/60[2)], NTSC M/4.4) as well as SECAM signals with automatic standard detection. Alternatively a standard can be forced. The demodulation is done with a regenerated color-carrier. For use of non-standard crystals or factory adjustment, the frequency of the free-running regenerated subcarrier can be adjusted via ***SCADJ***. For this purpose the crystal deviation (***SCDEV***) can be read out via I²C after chroma PLL locking (indicated by ***SCOUTEN***) and can be stored in µC ROM for ***SCADJ***. For test purposes, ***CPLLOF*** allows a loop opening of the chroma PLL

For adjustment to the specific operational area an automatic norm detection is selectable. Available 50 Hz color standards are PAL B, PAL N and SECAM. Available 60 Hz color standards are NTSC M, PAL M, PAL60 and NTSC44. For each line standard, one or more color standards can be chosen for automatic standard detection. In addition, a standard can be forced as well. Within each line standard, the standard is detected by consequently switching from one to another. This standard detection process can be set to slow or fast behavior **(*LOCKSP*).** In slow behavior, 25 fields are used to detect the standard, whereas 15 fields are used in fast behavior. If unsuccessful within this time period the system tries to detect another standard. For SECAM detection, a choice between different recognition levels is possible (***SCMIDL, SCMREL***) and the evaluated burst position is shiftable (***BGPOS***).

Color standard (***STDET***), line standard (***LNSTDRD***) and color killer status (***CKSTAT***) can be read out.

1) PAL B is representative for PAL B/G/H/I/N

2) PAL60 and NTSC44 are nonstandard signals which are generated by some VCR or DVD player

Standard	CSTAND				Standard	CSTAND		
(60 Hz)	D6	D5	D4	D3	(50 Hz)	D2	D1	D0
none	0	0	0	0	none	0	0	0
PAL60	0	0	0	1	PAL N	0	0	1
PAL M	0	0	1	0	PAL B	0	1	0
NTSC M	0	1	0	0	SECAM	1	0	0
NTSC44	1	0	0	0				
automatic PAL M / NTSC M	0	1	1	0	automatic PAL BG / SECAM	1	1	0
automatic NTSC M / NTSC44/ PAL60	1	1	0	0(!)				

Table 5- 3 Allowed combinations for color-standard search

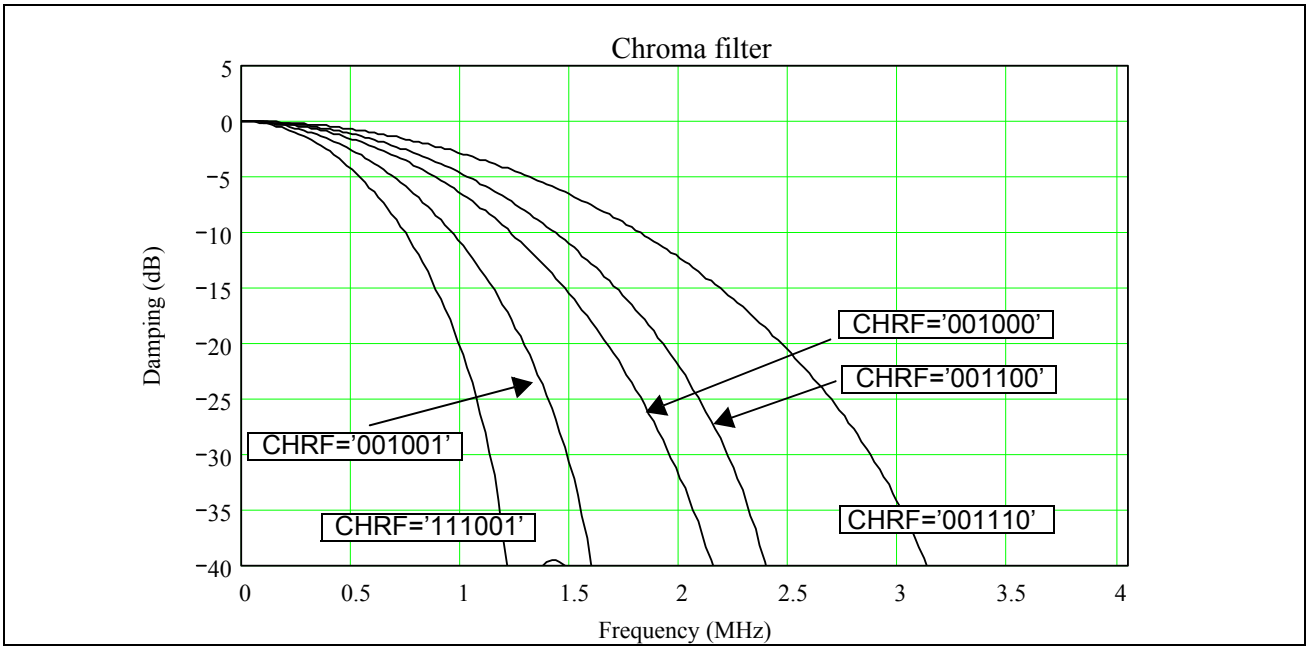

Figure 5-7 Chroma filter characteristics

An Automatic Chroma Control (ACC) produces a stable output for input chroma variations from (approximately) -30 dB to +6 dB compared to nominal burst value. The

ACC reference value is programmable for NTSC and PAL independently (***NTSCREF***, ***PALREF***) to ensure correct color saturation. With ***ACCFIX***, the ACC is disabled and a constant value (dependent on ***NTSCREF*** and ***PALREF***) is used instead. ***ACCFRZ*** holds the current ACC value. The maximum amplification of the ACC can be limited by ***ACCLIM.*** This results a smooth attenuation of color intensity for weak color carrier (**Figure 5-8**).

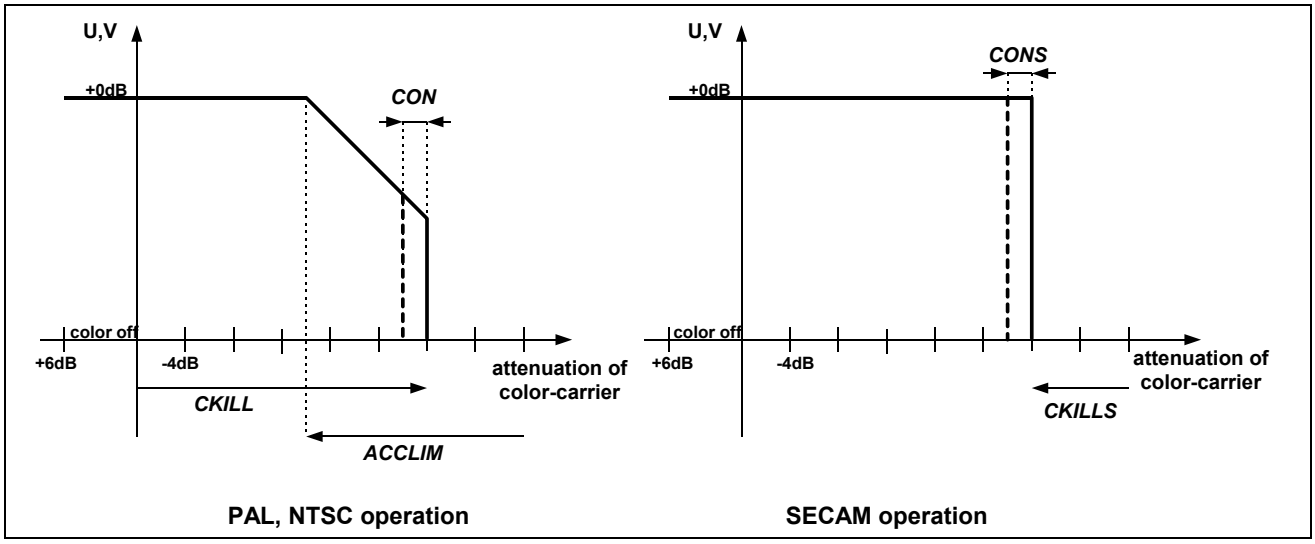

Figure 5-8 Color killer adjustment

If the chrominance signal is below an adjustable threshold (***CKILL*** (PAL; NTSC) or ***CKILLS*** (SECAM)) the color is switched off. To prevent on / off switching, a hysteresis is given by **CON** or **CONS** which is the value of switching on the color.

COLON switches on the color under any circumstance. The output of the colordecoder can be set to UV or CrCb data by ***CRCB.*** For NTSC only, the color impression (tint) can be adjusted by the Hue Control between -88° and 90° in steps of 0.7° (***HUE***). Low chrominance values (+/- 1...3 LSB) may be deleted by UV-coring (***UVCOR***). The Chroma bandwidth can be adjusted by ***CHRF***. The value of ***CHRF*** has no linear dependency on effective bandwidth. The proper constellations are shown in Figure 5-7. A filter with asymmetrical characteristic around the color carrier is available (***IFCOMP***) (Figure 5-9).

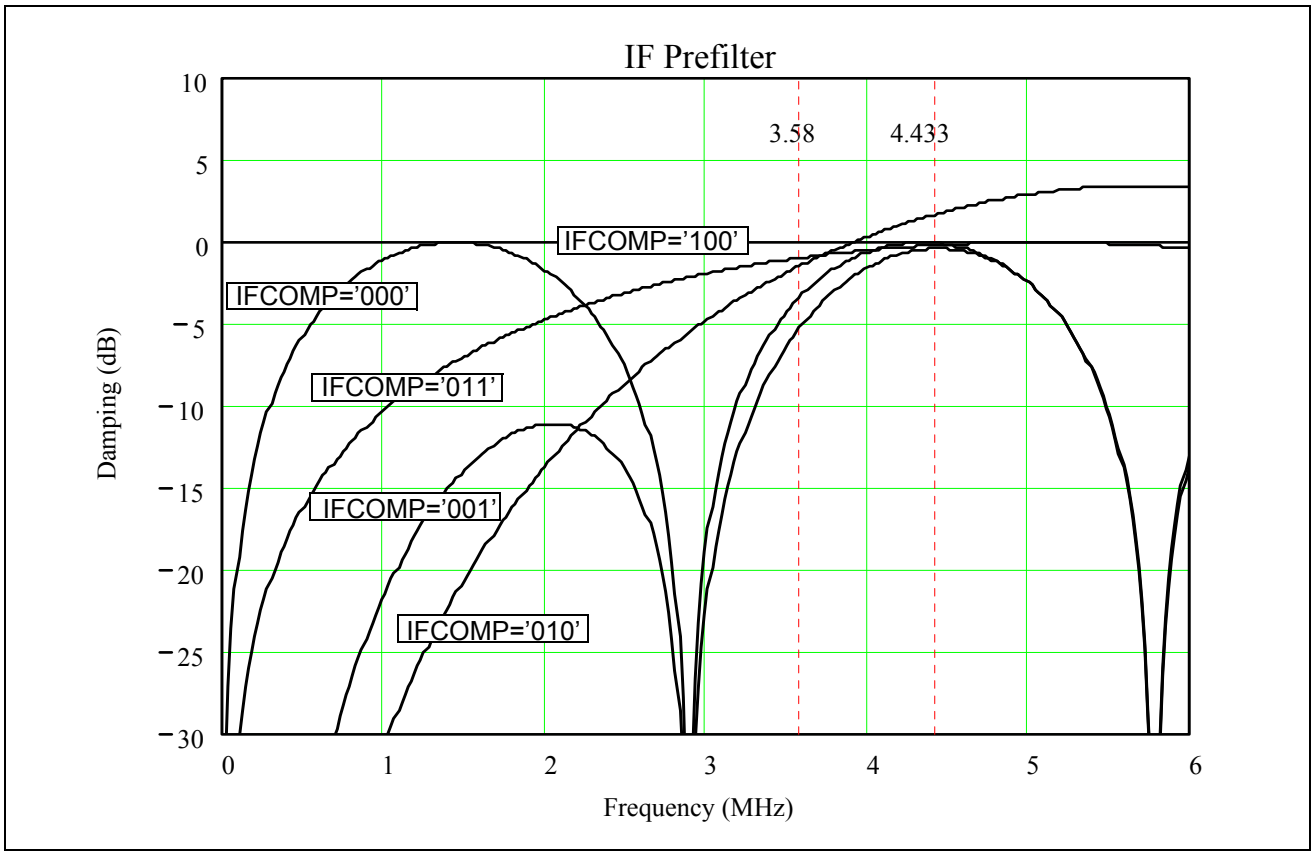

Figure 5-9 IF prefilter

For SECAM mode, the de-emphasis filter can be adjusted by ***DEEMPFIR*** and ***DEEMPIIR***. The bell filter can be adjusted by ***BELLFIR*** and ***BELLIIR***.

The delay between Y and C is well aligned and can also be adjusted in steps of 50ns (***YCDEL***). No picture shifting occurs when switching between different color standards (e.g. SECAM -> PAL). A delay-line is implemented for PAL and SECAM signals. It acts as a simple chrominance comb-filter for NTSC and can be disabled by ***COMB.*** This improves the vertical chroma resolution, but cross-color remains.

5.1.6 Luminance Processing

A luminance notch filter is implemented to reject the chroma information from luminance. Depending on the color standard, one of three different notch characteristics is chosen ('PAL', 'NTSC', 'SECAM'). For PAL and SECAM standards, five different characteristics are available. For NTSC standard, four different characteristics are available. They can be selected by ***NTCHSEL***. Alternatively, no notch should be used for Y/C input (***NOTCHOFF***). The filter characteristics can be found in **Figure 5-10**...**Figure 5-13**. In SECAM operation, the notch filter can be fixed to one frequency or toggle between 4.4 and 4.25 MHz depending on the transmitted color (Dr, Db) (***SECNTCH***). A simple

lowpass-filter can be enabled by ***LPPOST*** to further reduce high-frequency noise component from the CVBS signal.

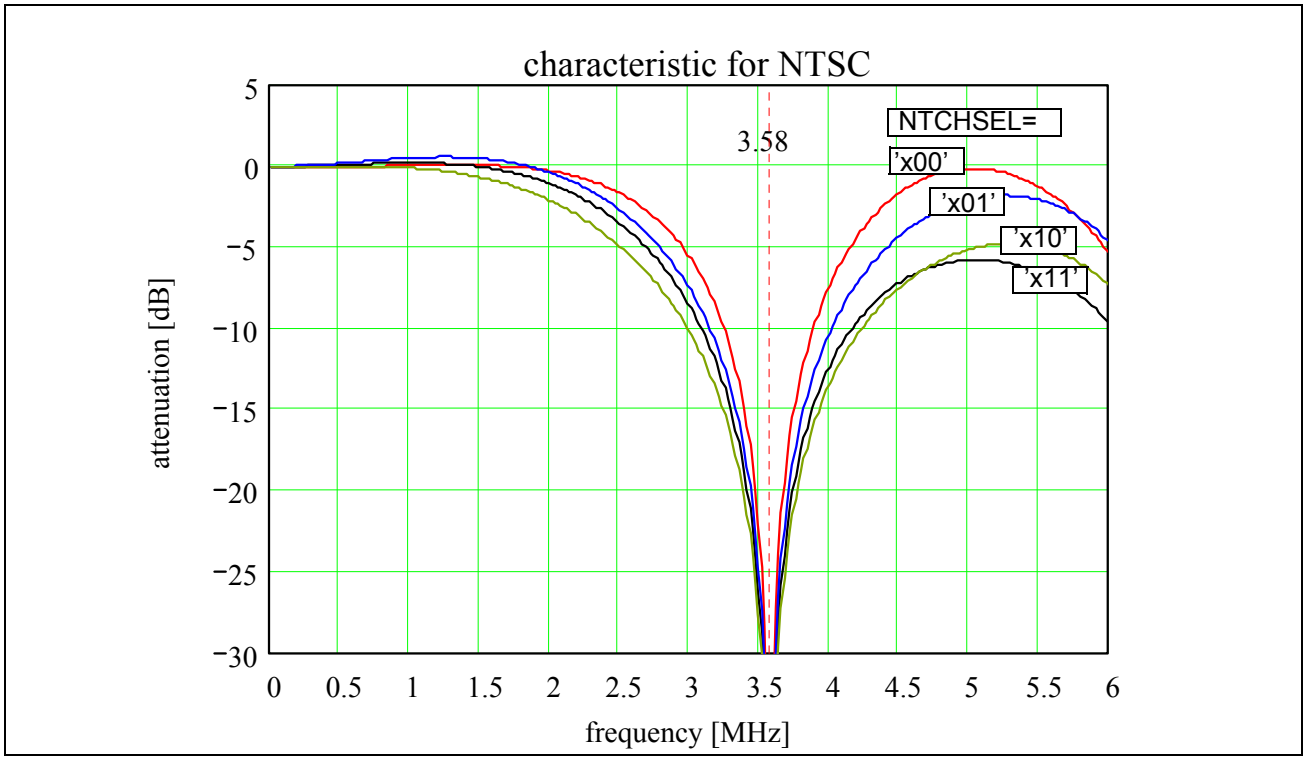

Figure 5-10 Filter characteristics for NTSC, PAL M and PAL N

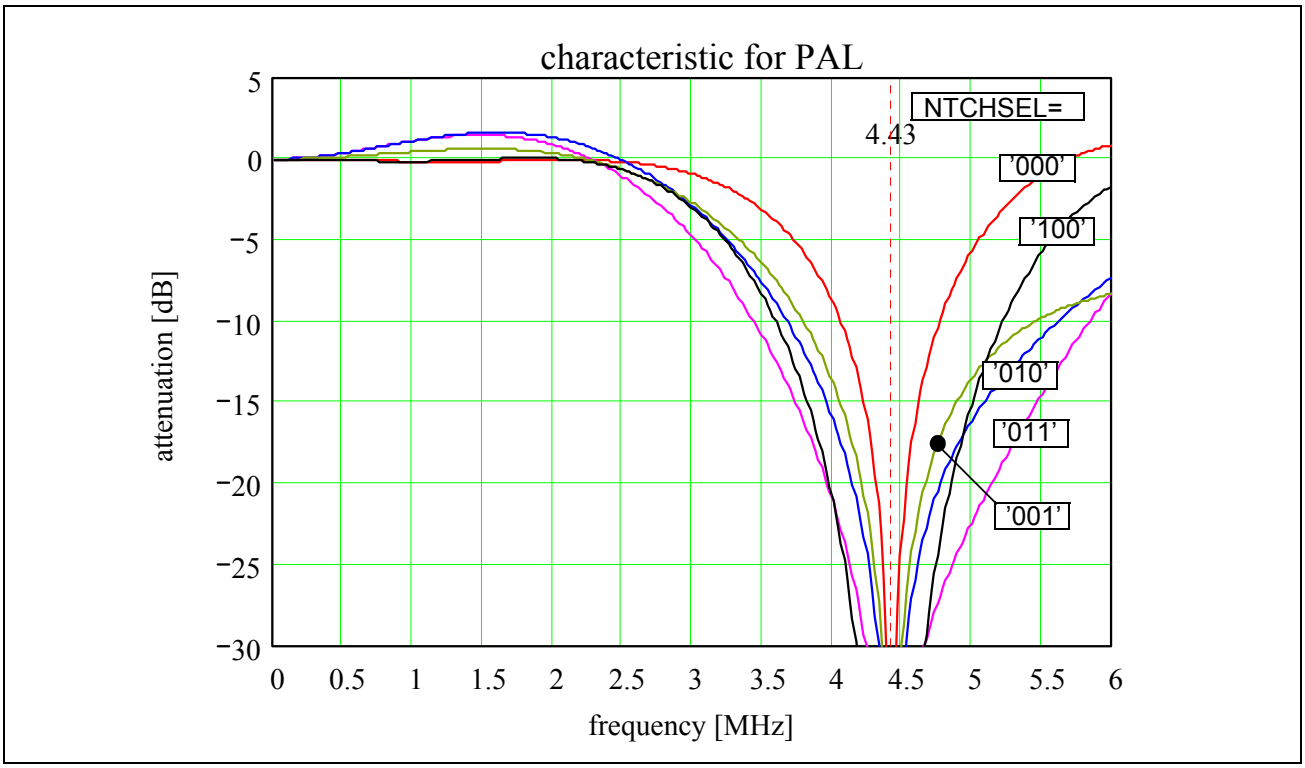

Figure 5-11 Filter characteristics for PAL B/G, NTSC44, PAL60

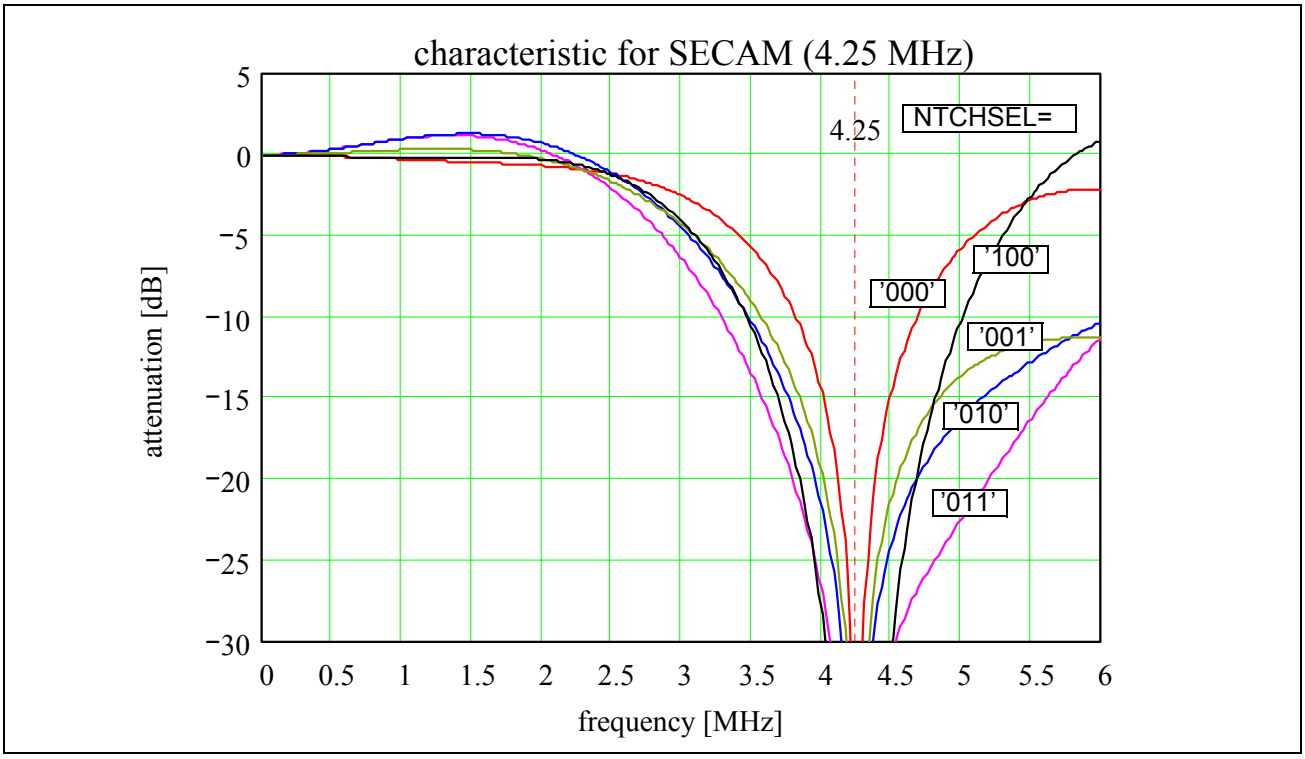

Figure 5-12 Filter characteristics for SECAM (*SECNTCH*='01', 4.25 MHz)

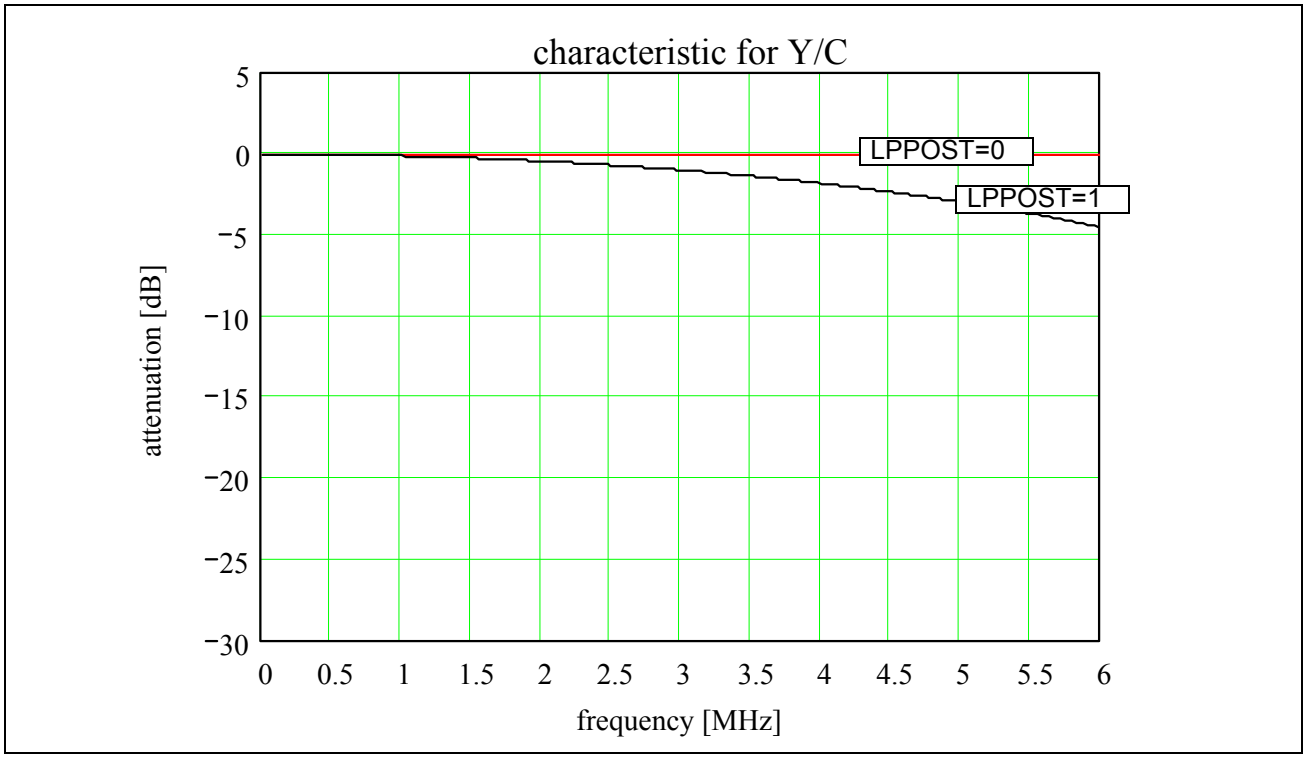

Figure 5-13 Filter characteristics for Y/C mode

For applications for which a black offset is not desired, controlling may be done using ***LMOFST***. The positive or negative offset is added to the Y signal before scaling.

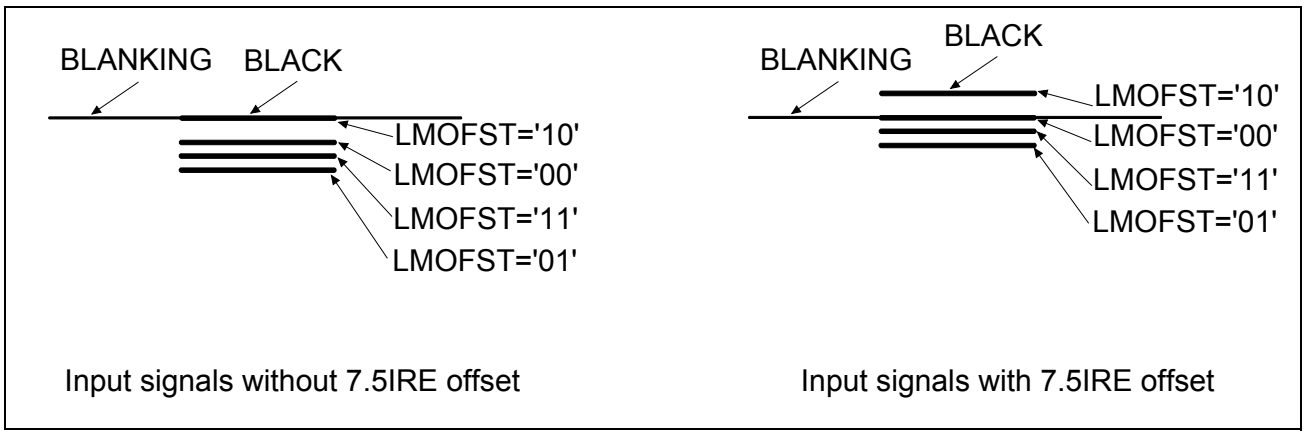

Figure 5-14 Adjustment of ’Black-’ to ’Blankingvalue’ at analog output

5.2 RGB-Frontend

An analog RGB input port for an external RGB or YUV source is available. The incoming signal is clamped to the back porch by a clamping pulse. As the memory is only able to store a 4:2:2 picture, the YUV input signal is downconverted to 4:2:2. There are two

operation modes available. The first one uses this input as an overlay input (soft mix). The RGB or YUV signal must then be synchronized to the main CVBS/YC signal. The so called independent mode uses RGB / YUV including sync or H/V signals. This can be used, for example, for a DVD player or set-top-box. When using H sync from a non CVBS input (e.g. separate H-sync) this must be indicated by ***HINP***. The usage of separate V sync must be set by ***VINP***.

Input signal	**FBL_{IN}**	**V_{IN}**	**sync separation**	**remark**	**Hinp**	**Vinp**
RGB	CVBS[1)]		sync on CVBS		1	0
YUV	CVBS[1)]		sync on CVBS		1	0
RGB	H[1)]	V	sync on H	e.g. set-top-box	1	1
YUV	H[1)]	V	sync on H	e.g. set-top-box	1	1
RGB	FBL		synchron to CVBS/ YC	soft mix	0	0
YUV	FBL		synchron to CVBS/ YC	soft mix	0	0
RGB (incl. sync)			sync on G (maybe on R/B)	no external sync	1	0
YUV (incl. sync)			sync on Y	no external sync e.g. DVD	1	0

[1)] instead of FBL input, CVBS input can be used when Hinp=0

Table 5- 4 Possible input signals for RGB Frontend

The delay of luminance and fast-blank can be adjusted by ***YFDEL***, and chrominance can be delay adjusted by ***UVDEL***. If necessary, fast-blank can be adjusted fine by ***FBLDEL***.

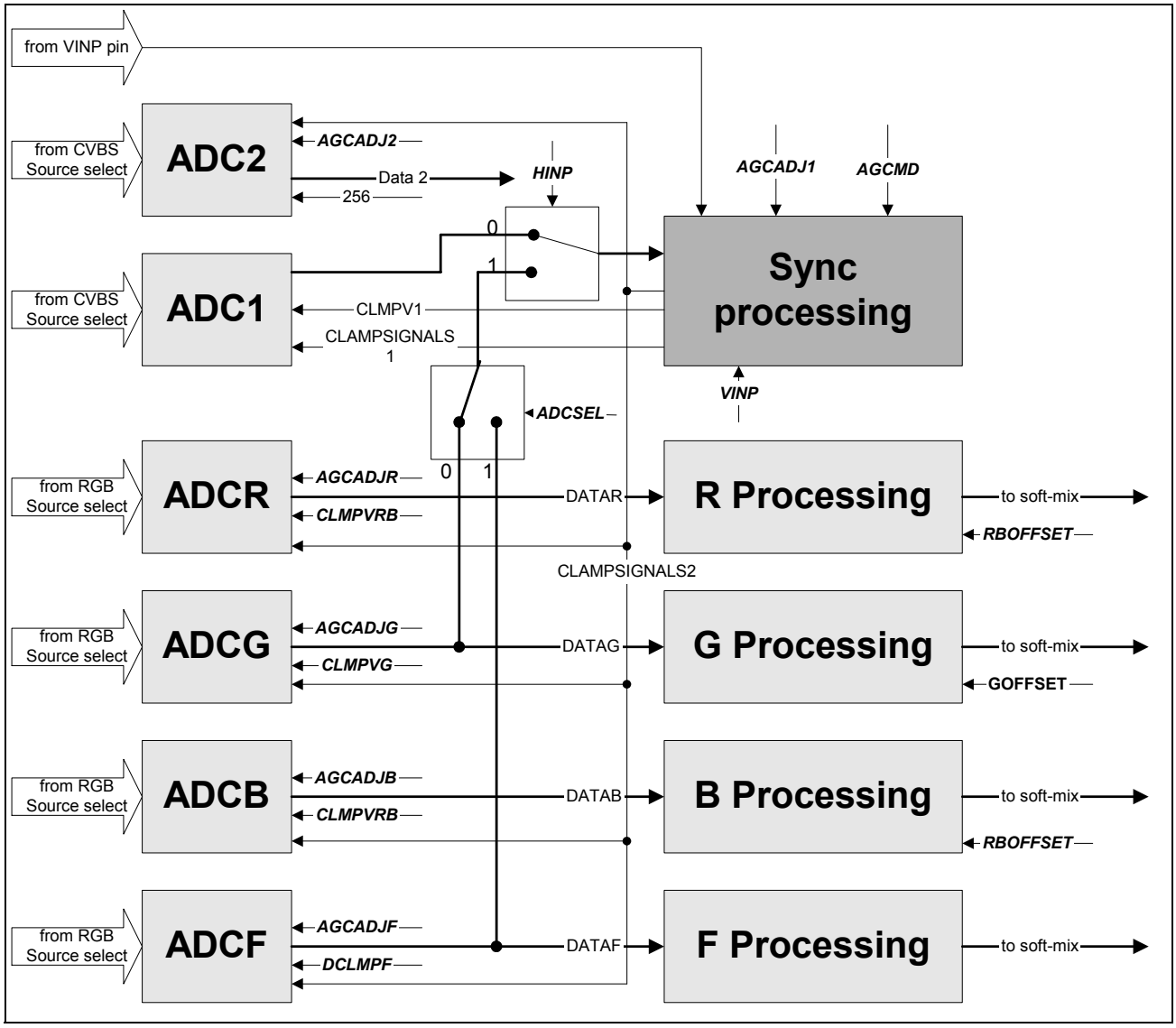

Figure 5-15 Signal and Clamping organization

5.2.1 Source Select

Two inputs are available. The choice between the first or second input is made by ***RGBSEL***.

5.2.2 Signal Magnitudes and Gain Control

Each ADC can be gain adjusted by ***AGCADJR***, ***AGCADJG***, ***AGCADJB***, ***AGCADJF***.

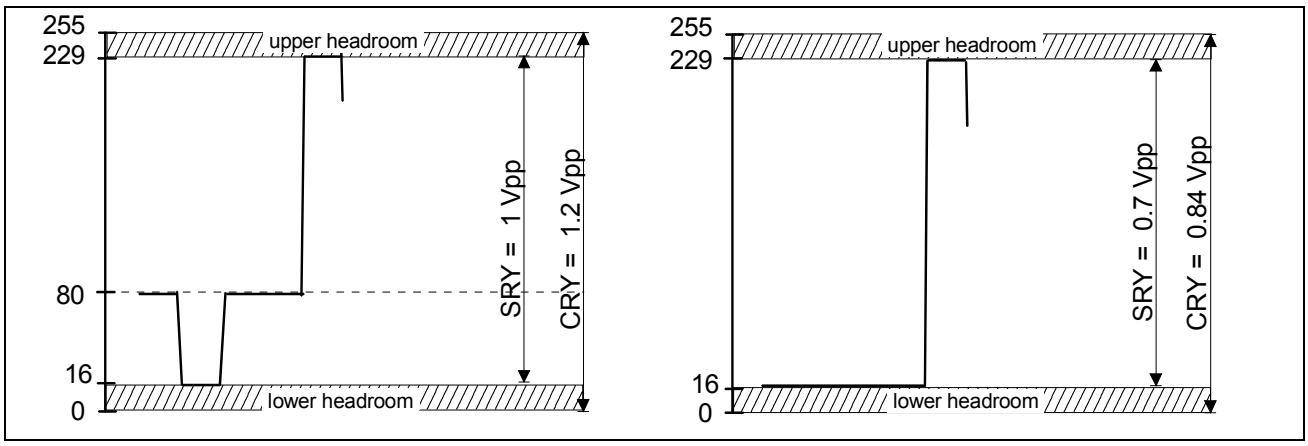

Figure 5-16 Y/RGBF amplitude characteristics (with or without sync)

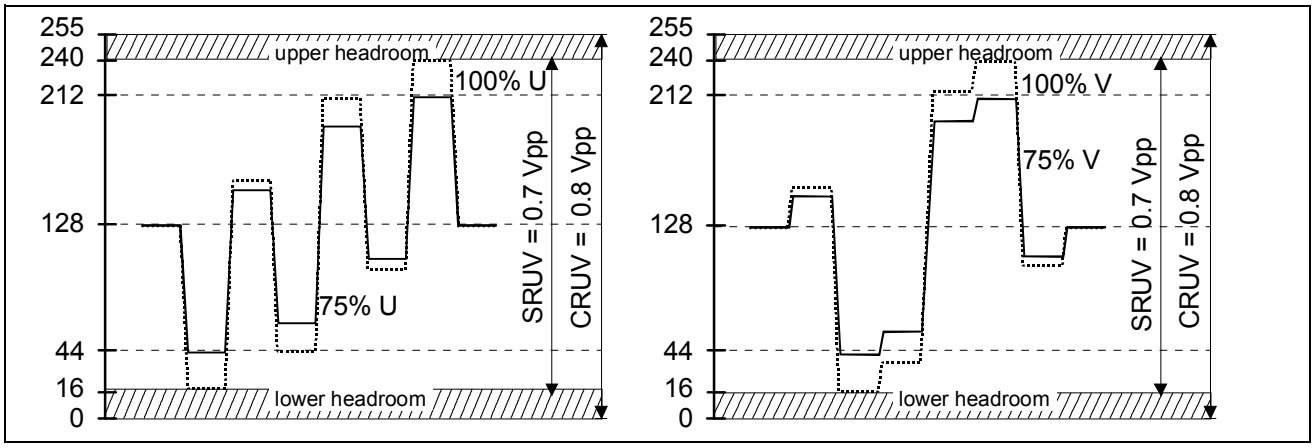

Figure 5-17 UV amplitude characteristics

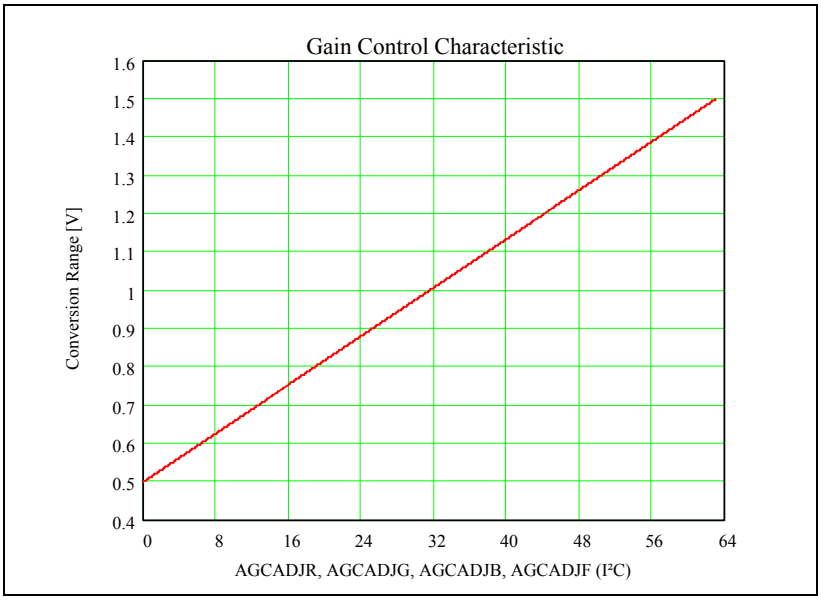

Figure 5-18 RGB ADC characteristic, Fast-blank ADC with clamping (*DCLMPF*=0)

5.2.3 Clamping

When using the dynamic softmix-mode with fast-blank, clamping of fast-blank input must be disabled by ***DCLMPF***. The analog clamping value of red and blue input (V and U resp.) can be adjusted by ***CLMPVRB***. The analog clamping value of green input (Y resp.) can be adjusted by ***CLMPVG***. Depending on the input signal format (YUV, RGB, sync signal or not) these bits must be set accordingly. On the digital side, a correction of the analog clamping value must be performed to reconstruct the blacklevel. This is achieved by ***RBOFST*** and ***GOFST***.

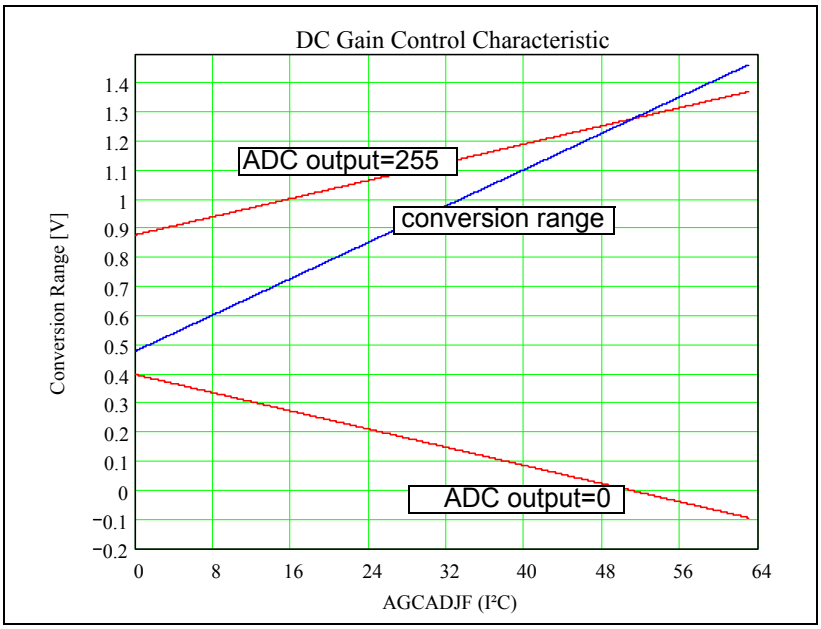

Figure 5-19 Fast-blank ADC characteristic without clamping (*DCLMPF*=1)

mode	CLMPVG	CLMPVRB	GOFST	RBOFST	DCLMPF
YUV, sync on Y	80	128	64	128	don't care
YUV, sync on H,V	16	128	0	128	0 (clamping enabled)
RGB, sync on G	80	16	64	0	don't care
RGB, sync on RGB	80	80	64	64	don't care
RGB, sync on H,V	16	16	0	0	0 (clamping enabled)
RGB with fast-blank, synchron to CVBS	16	16	0	0	1 (clamping disabled)
YUV with fast-blank, synchron to CVBS	16	128	0	128	1 (clamping disabled)

Table 5- 5 Configurations of input signals

5.2.4 Digital Prefiltering

A digital prefiltering can be enabled. This reduces the bandwidth of very steep input signals, such as a display of characters. A band limitation is required, because the succeeding deskewing filter performs best below 14 MHz. The filtering is performed in all four channels and can be disabled by ***AABYP***. For signal conversion to 4:2:2, an additional chrominance lowpass can be enabled by ***CHRSF***. The deskewing filter can be disabled by ***SKEWSEL***. This is necessary when using the HOUT50-pin in connection with a Micronas picture-in-picture device (e.g. SDA938x, SDA948x, SDA958x). In this application, the RGB input (in1, in2, in3) of the PiP can not be used for other RGB signals (e.g. 'SCART' is not possible).

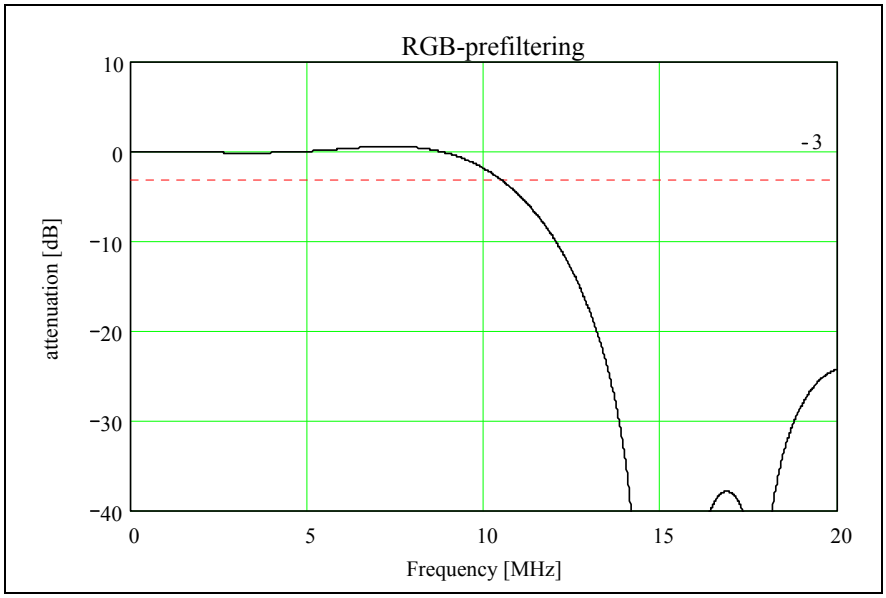

Figure 5-20 Digital Prefiltering of RGB input

5.2.5 RGB->YUV Matrix

RGB or YUV signals are selected by ***YUVSEL***. The matrix coefficients are set according to ITU recommendations.

$$\begin{bmatrix} Y \\ U \\ V \end{bmatrix} = \begin{bmatrix} R \\ G \\ B \end{bmatrix} \cdot \begin{bmatrix} 0{,}299 & 0{,}587 & 0{,}114 \\ -0{,}147 & -0{,}289 & 0{,}436 \\ 0{,}615 & -0{,}515 & -0{,}100 \end{bmatrix}$$

Formula 5-6 RGB to YUV matrix

5.2.7 Contrast, Brightness and Saturation Control of Input signal

The YUV signal can be manipulated in order to fit to the main channel. The contrast can be adjusted between 0 and 1.97 in 64 steps (***CONADJ***). The brightness is adjustable in 255 steps (***BRTADJ***). Due to the independent chroma adjustment of U and V (64 steps each, ***USAT***, ***VSAT***), UV as well as CrCb input signals can both be displayed correctly.

5.2.8 Soft Mix

The soft-mixing is done by means of alpha-mixing. Alpha is derived from the fast blank input (FBL), which indicates a signal insertion. The value of α is between ’0’ and ’128’. ’0’ means that only the main signal is fed through to the output. ’128’ means that only the inserted signal becomes visible. Obviously the formula is:

$$\text{out} = \frac{\text{YUV}_{\text{main}} \cdot (128 - \alpha) + \text{YUV}_{\text{inserted}} \cdot \alpha}{128}$$

The mixing is done once for the luminance and once for the chrominance in the subsampled domain (4:2:2). To fix the displayed picture to each main (CVBS) channel, RGB channel or softmix-mode, ***MIXOP*** is used. Two operation modes are possible (***SMOP***). The first is the static operation mode where Fast-blank input has no effect. Considering ***MIXGAIN***=3, α is obtained by

$$\alpha = 158 - 3 \cdot \text{FBLOFFST} \qquad [\alpha\text{limited to 0 and 128}]$$

The function is printed in **Figure 5-22** (right). The mixing is only controlled by ***FBLOFFST***.

The dynamic mode is used for mixing which is dependent on FB input. FB is the preprocessed digitized fast-blank input in the range from 0...127.

$$\alpha = \frac{\text{MIXGAIN}(\text{FB} - \text{FBLOFFST} \cdot 2)}{2} + 64 \qquad [\alpha\text{limited to 0 and 128}]$$

FBL manipulation is done both for luminance and chrominance FBL signal.

MIXOP	*SMOP*	Softmix-mode
00	0	dynamic Soft-Mix (***DECTWO*** must be set to ’1’)
00	1	static Soft-Mix (***DECTWO*** must be set to ’1’)
01	x	only RGB/YUV path visible
10	x	only CVBS path visible
11	x	(reserved)

Table 5- 6 RGB operation modes

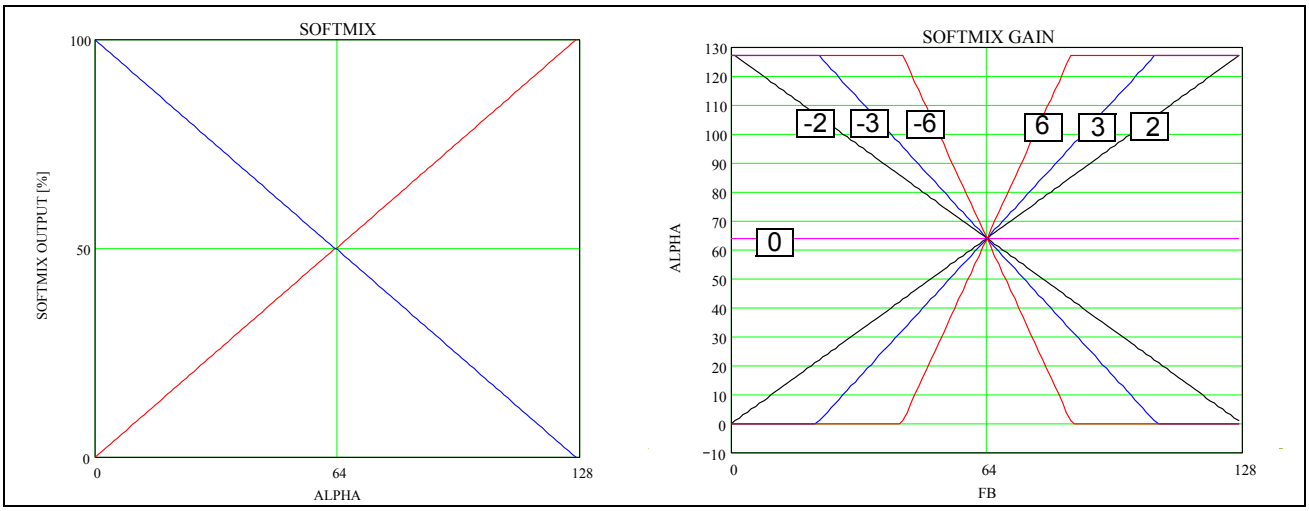

Figure 5-21 Softmix: Visualization of formulas

There is a great variety of FBL signal manipulations. First, there is a delay adjustable by ***FBLDEL*** in the range of -2...4 clock cycles. Then an offset is applied to the FBL signal (***FBLOFFST***). The result is multiplied by an adjustable factor (***MIXGAIN***).

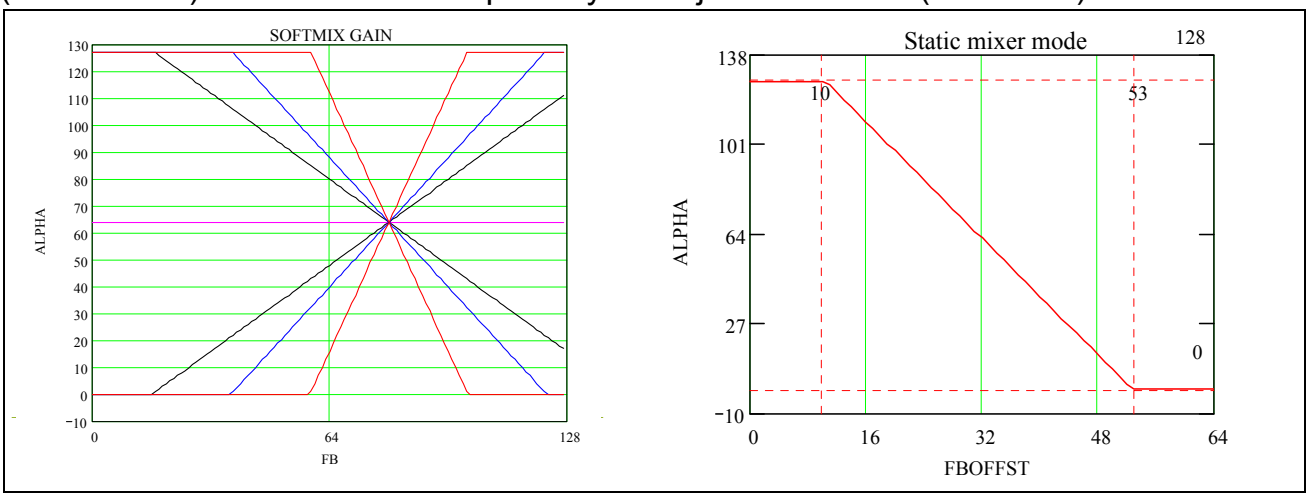

Figure 5-22 Varied FBLOFFST output and static operation mode

5.2.9 FBL activity and overflow detection

It is important to know whether the FBL input is used or not. Therefore a detection circuit gives information via the I²C bus to the microcontroller. The circuit uses the FBL value as input. If it is greater than a threshold for one or five clock cycles (***FBLCONF***), the I²C register ***FBLACTIVE*** is set. This register is reset when it is read by the microcontroller. ***PFBL***, ***PG***, ***PR***, ***PB*** indicate an overflow of the corresponding ADC (upper limit: ADC=255) exceeding 5 clock cycles duration. These signals are also set by overflow and reset by I²C reading only.

5.3 Input Processing

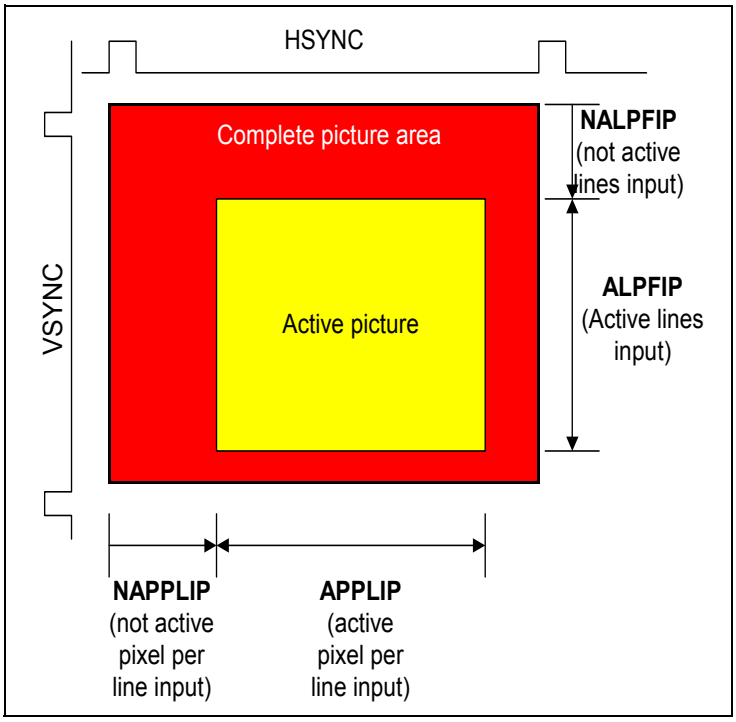

Figure 5-23 Image format before memory

5.3.1 Horizontal Prescaler (sample-rate-converter)

The main application is the conversion of the data coming from the 40.5/20.25MHz pixel clock domain down to the number of pixels stored in the memory (factor 2/3). Generally the number of incoming pixels can be decimated by a factor between 1 and 64 in a granularity of 2 output pixels. The horizontal scaler reduces the number of incoming pixels by subsampling. To prevent the introduction of alias distortion low pass filters are used for luminance and chrominance processing (Figure 5-24). In case of ITU656 input, the lowpass filter must be disabled by ***HAAPRESC***.

The horizontal prescaler consists of two main subsampling stages. The first stage is a scaler for rational decimation factors in a range of 1 to 2, controlled by ***HSCPRESC***. The

second stage is a MTA (moving target average) filter for integer decimation factors (1,2,3,4...32), controlled by ***HDCPRESC***. Due to its architecture the MTA filter automatically adapts its low pass filter characteristic to the used subsampling factor.

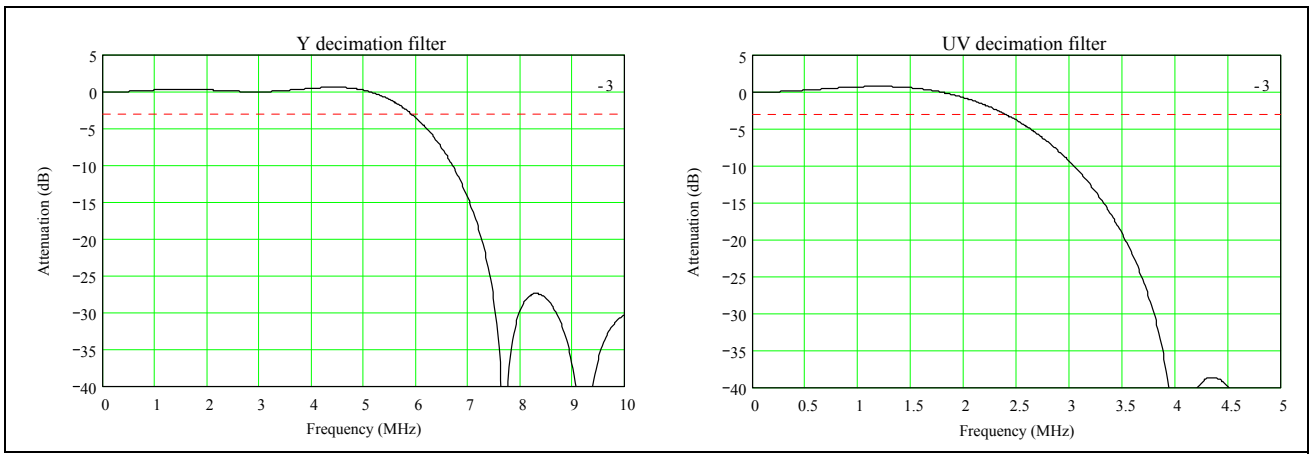

Figure 5-24 Y and C decimation filter characteristic for standard operation (1.5)

5.3.2 Noise Reduction

The Figure 5-25 shows a block diagram of the motion adaptive temporal noise reduction (first order IIR filter). The structure of the temporal motion adaptive noise reduction is the same for luminance as for chrominance signal. Noise reduction is enabled by ***NRON***.

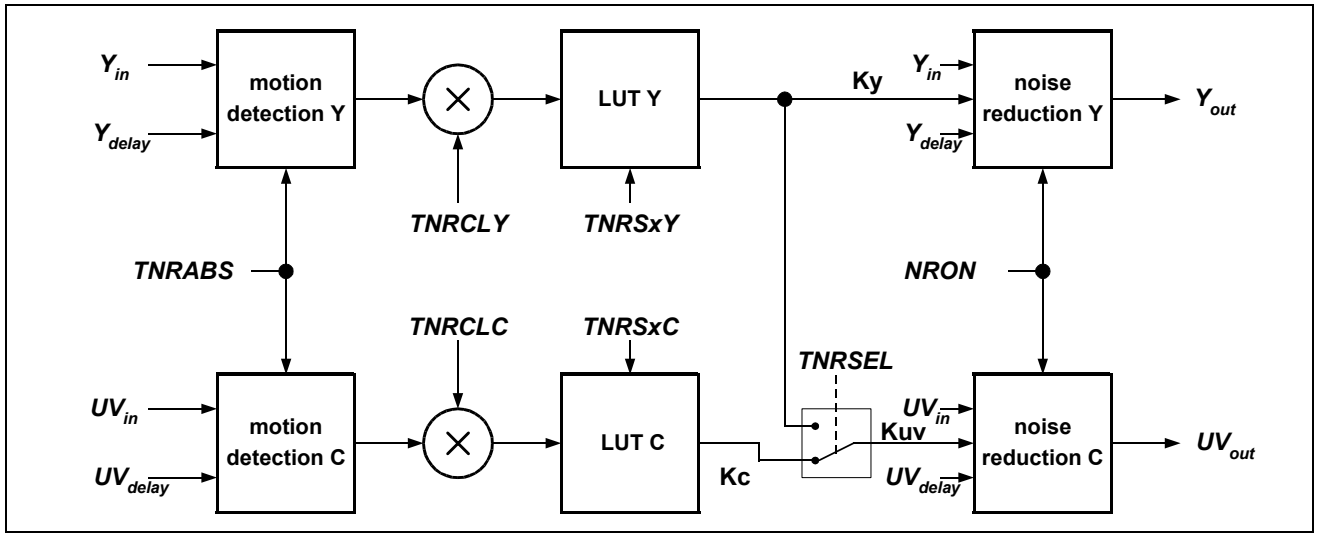

Figure 5-25 Temporal noise reduction

The equation below describes the behavior of the temporal adaptive noise reduction filter. The same equation is valid for the chrominance signal. Depending on the motion in the input signal, the K-factor Ky (Kuv) is adjustable between 0 (no motion) and 15

(motion) by the motion detector. The K-factor for the chrominance filter can be either Ky (output of the luminance motion detector, ***TNRSEL***=0) or Kuv (output of the chrominance motion detector, ***TNRSEL***=1). The delay of the feedback path is a field delay.

$$Y_{out} = \left(\frac{1+Ky}{16}\right)(Y_{in} - Y_{delay}) + Y_{delay}$$

$$UV_{out} = \left(\frac{1+Kuv}{16}\right)(UV_{in} - UV_{delay}) + UV_{delay}$$

The output of the motion detector is weighted ***TNRCLC*** and ***TNRCLY***. The output is mapped to the values Ky and Kc by look-up-tables (LUT Y and LUT C). The input value range is separated into 8 segments, where segment 0 covers the range 0...3, segment 1 covers the range 4...7 etc. and segment 7 covers the range 48...63 of motion value.

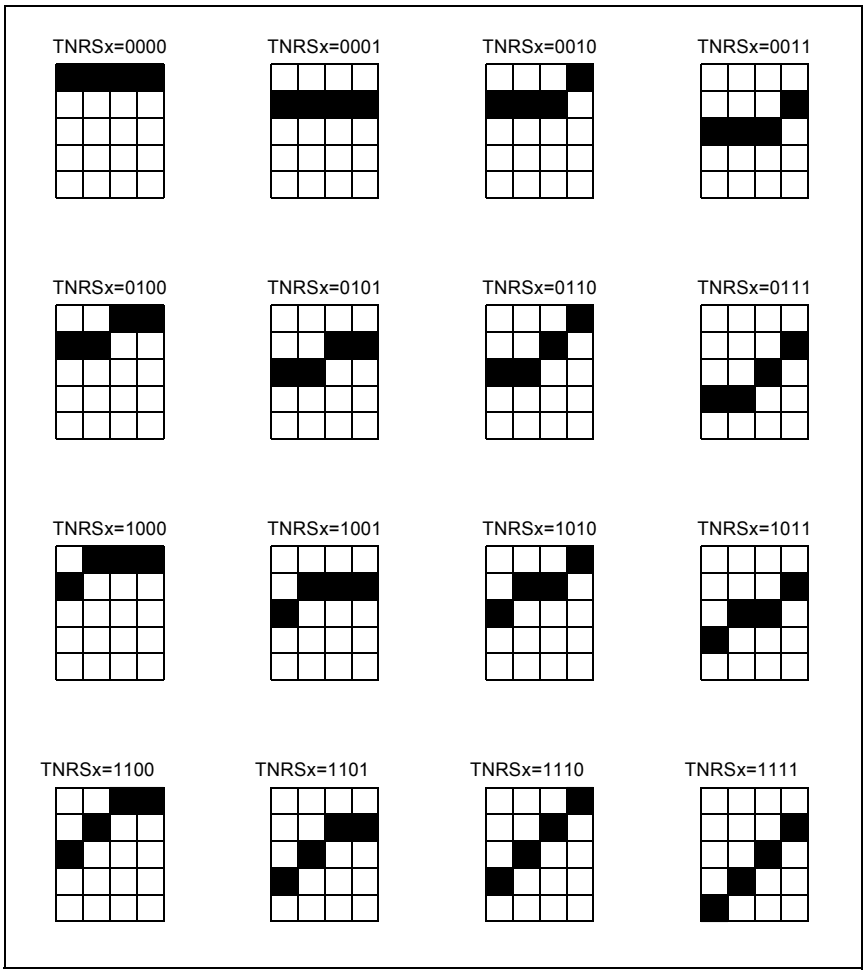

Figure 5-26 Segments of LUT

It is possible to define a predefined curve characteristic for each segment. The curve characteristics can be programmed by the parameters ***TNRSxY*** for luminance and ***TNRSxC*** for chrominance. The curve-start is defined by ***TNRSSY*** (***TNRSSC***) at the end of the last segment. The overall curve is now constructed by connecting the end of segment 6 to the beginning of segment 7 and so on. Negative values of Ky (Kuv) are not possible and clipped to zero. A continuous mapping of 64 motion values to 16 Ky (Kuv) values is the result.

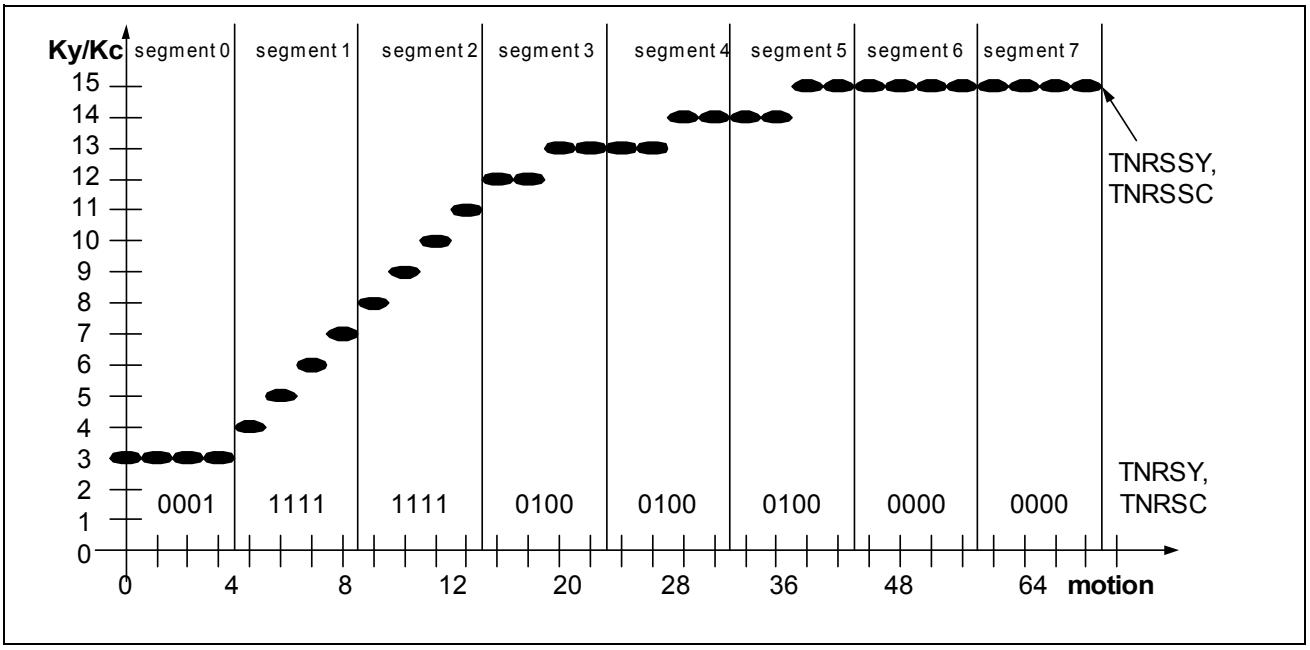

Figure 5-27 Predefined curve characteristics for LUT

5.3.3 Noise Measurement

The noise measurement algorithm can be used to change the parameters of the temporal noise reduction processing depending on the actual noise level of the input signal. This is done by the TV- microcontroller which reads the noise level (***NOISEME***), and sends different parameter sets to the temporal noise reduction registers of the VSP 94x2A depending on this value (0=no noise, 30=strong noise). Value 31 indicates an overflow status which means that the measurement failed. The line taken for noise measurement is selected by ***NMLINE***. When ***NOISEME*** contains updated data which was not read so far, ***NMSTATUS*** is set. ***NMSTATUS*** is reset when read.

5.4 Output Processing

5.4.1 Horizontal Postscaler

After field memory, the display processing is performed using a different clock. In this way a decoupling of input and output clocks is achieved.

The conversion to the display clock is done by an interpolation filter. This can be used for horizontal expansion in the range of 1...4 in steps of 2 pixels (***HSCPOSC***). Due to increased clock frequency in the backend part (36 MHz instead of 27MHz), the horizontal expansion factors result as 0.75 ... 3. This ensures that the factor 0.75 gives no loss of resolution. This is used to show a 4:3 picture on a 16:9 tube.

HSCPOSC	horizontal filter expansion	overall expansion	remark
1024 (minimum)	4	3	biggest picture
2048	2	1.5	
3072	1.33	1	16:9 picture on 16:9 tube or 16:9 picture on 4:3 tube or 4:3 picture on 4:3 tube
4095 (maximum)	1	0.75	4:3 picture on 16:9 tube

Table 5- 7 Horizontal expansion factors

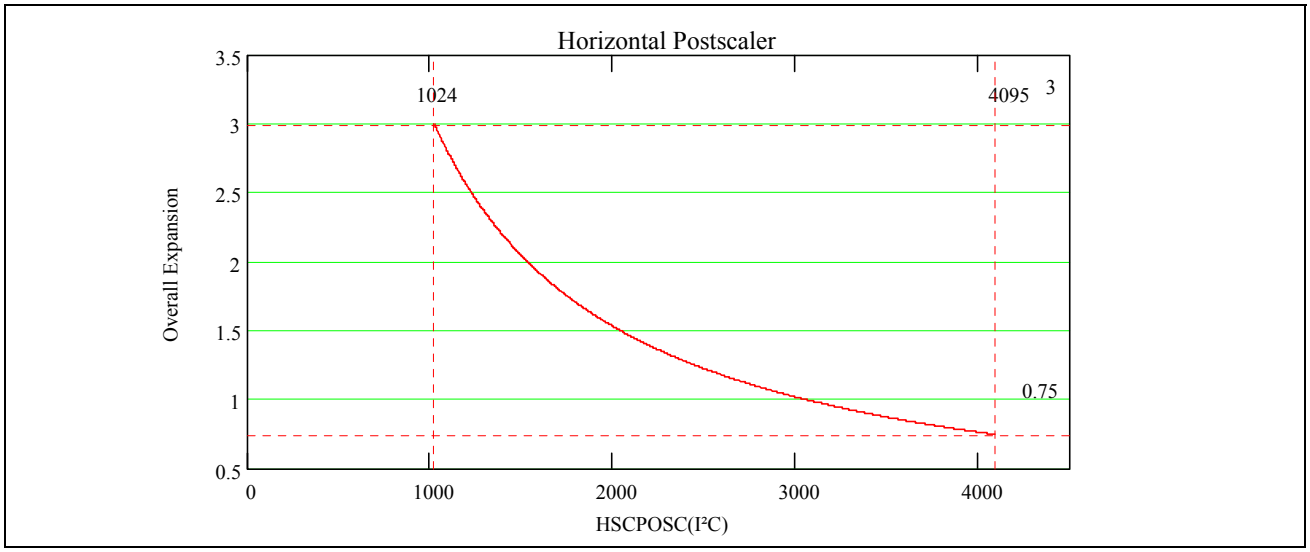

Figure 5-28 Expansion factor of horizontal postscaler dependent on *HSCPOSC*

Because of the nonlinear characteristic and integer number of pixel, sometimes different ***HSCPOSC*** values result in the same decimation factors.

5.4.2 Panorama Mode

The picture can be geometrically distorted in horizontal direction for an improved impression in the case of expansions of 4:3 pictures to a 16:9 ratio tube. It is enabled by ***HPANON***. The idea behind this panorama mode is to keep the middle part of the picture in a 4:3 ratio and to stretch the left and the right to fill the entire width of the 16:9 screen. For the adjustment of the expansion process, the picture is divided into 5 segments. For each of these segments the increment value for the expansion factor can be defined separately.

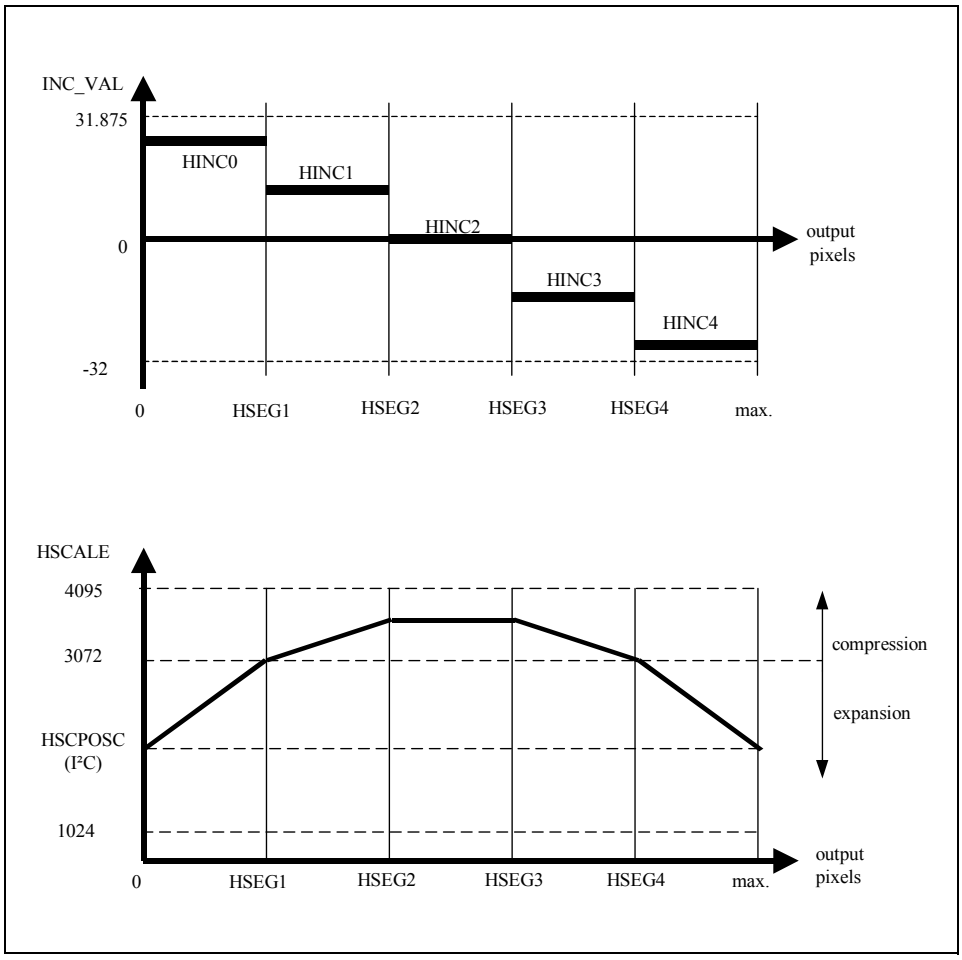

Figure 5-29 Visualization of panorama segments

Each end of a segment can be defined individually in a granularity of two output pixels. For every segment an increment value can be defined (***HINC0***...***HINC4***) which indicates the amount of decimation/expansion. One LSB is equivalent to an offset of 0.125 to ***HSCPRESC*** per double pixel. This means that with ***HINC***, ***HSCPRESC*** is altered in the range from -32...31.875 per double pixel. The segments are distributed among the

maximum number of pixels, which is adjusted by ***PPLOP***. The first four segments are defined by (***HSEG1***...***HSEG4***). The last one goes from ***HSEG4*** to ***PPLOP***.

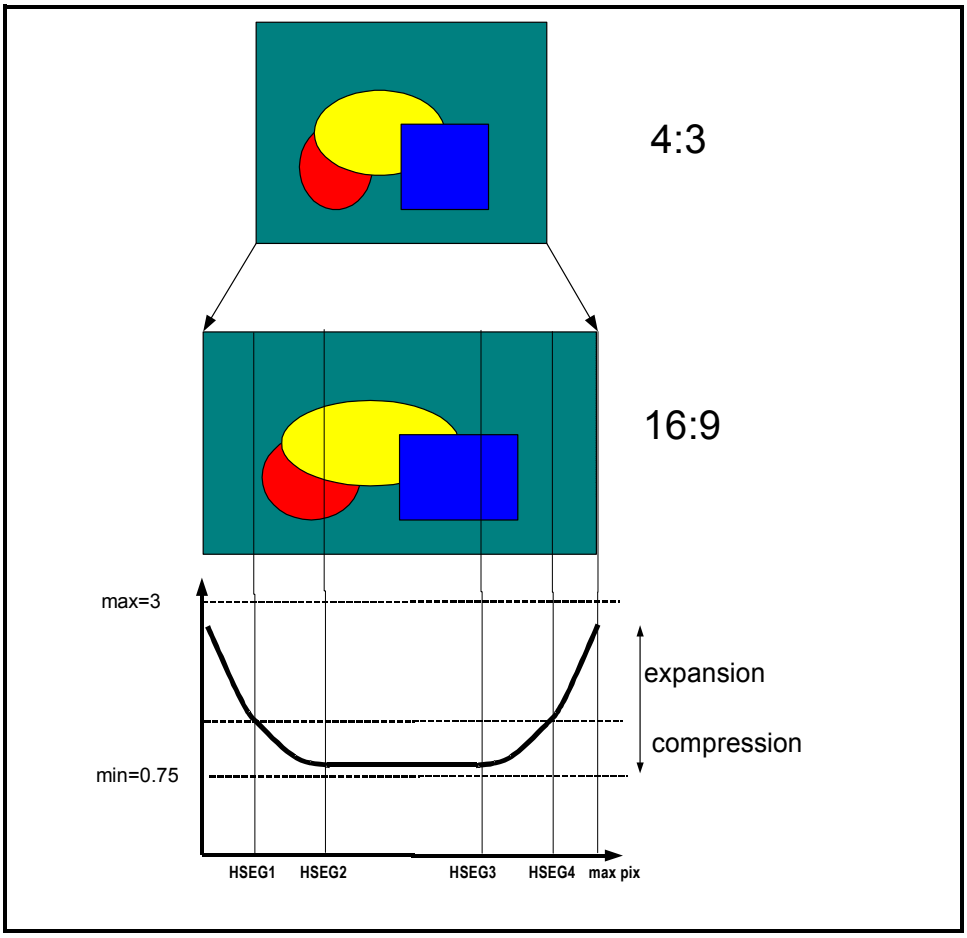

Figure 5-30 Panorama expansion

Examples are given in the **Table 5-8**:

Function	panorama	extreme pan.	lens	custom
HSCPOSC	2099_d	1023_d	3999_d	
HSEG1	96_d	96_d	96_d	
HSEG2	192_d	192_d	192_d	
HSEG3	288_d	288_d	288_d	
HSEG4	384_d	384_d	384_d	
HINC0	40_d	85_d	472_d	
HINC1	20_d	43_d	492_d	
HINC2	000_d	000_d	000_d	
HINC3	492_d	469_d	20_d	
HINC4	472_d	427_d	40_d	
APPLOP	960_d	960_d	960_d	

Table 5- 8 Examples of panorama modes

5.4.3 Operation Modes

There are four operation modes defined. The first mode is simple AABB, where each stored field in the memory is displayed double times on the TV screen. The second and third mode are AAAA and BBBB, in which only one field phase will be displayed on the TV screen. There is also an AAAA mode with $\alpha\beta\alpha\beta$ raster possible. The Figure 5-31 explains the picture and the display raster.

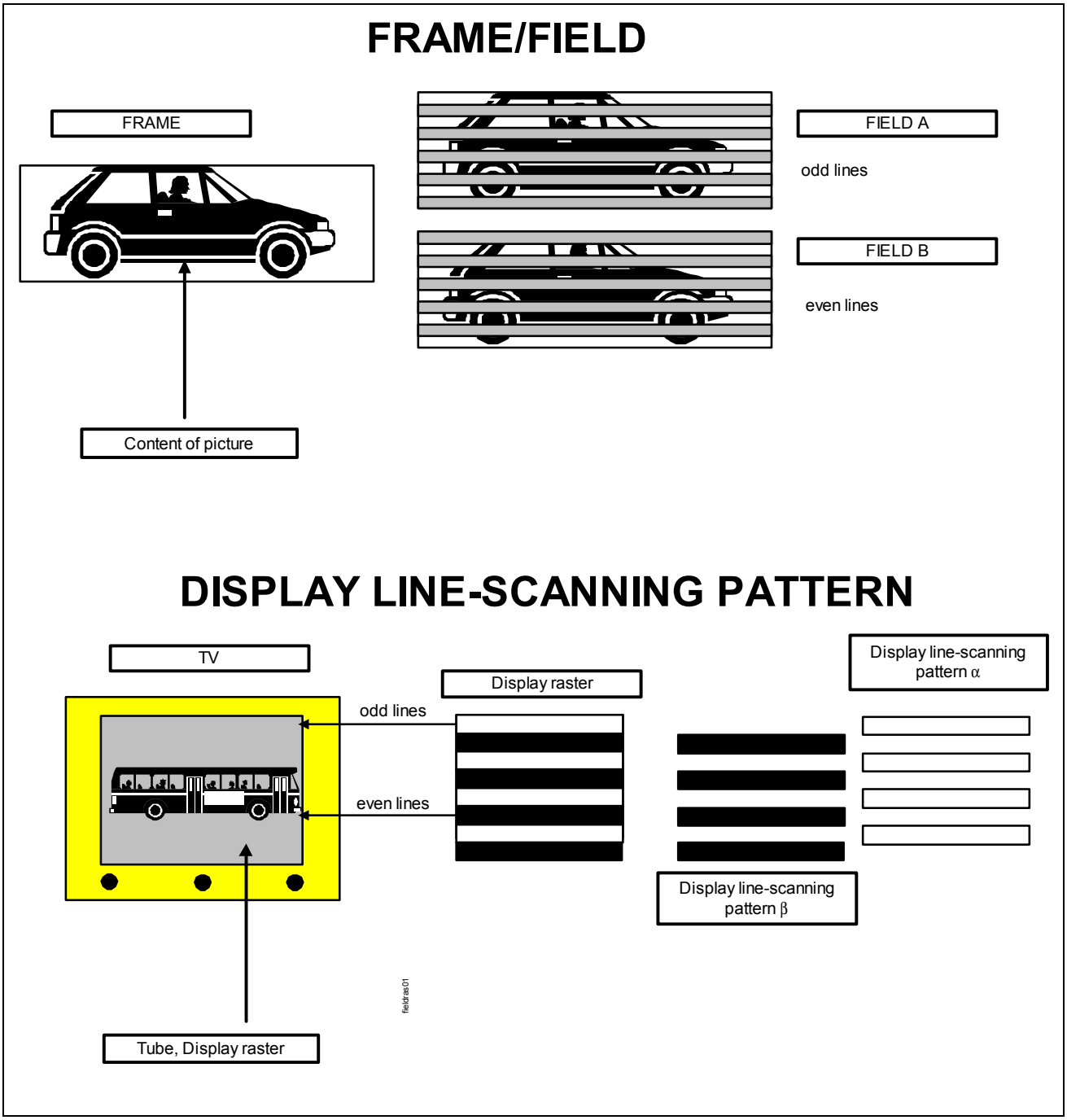

Figure 5-31 Explanation of field and display line-scanning pattern

The interlaced input signal (e.g. 50 Hz PAL or 60 Hz NTSC) is composed of a field A (odd lines) and a field B (even lines).

A^n - Input signal, field A at time n,

B^n - Input signal, field B at time n

The field information describes the picture content. The output signal, which could contain different picture contents (e.g. field A, field B), can be displayed with the display raster α or β.

(A^n,α) - Output signal, field A at time n, displayed as raster α,

(A^n,β) - Output signal, field A at time n, displayed as raster β,

The **Table 5- 9** describes the different scan rate conversion algorithms of VSP 94x2A and the corresponding raster sequences.

		Input field A		Input field B	
STOPMODE	**Scan rate conversion**	**Output field phase 0**	**Output field phase 1**	**Output field phase 2/0**	**Output field phase 3/1**
00	AABB mode	A^n,α	A^n,α	B^n,β	B^n,β
01	AAAA mode	A^n,α	A^n,α	A^n,α	A^n,α
10	AAAA mode	A^n,α	A^n,β	A^n,α	A^n,β
11	BBBB mode	B^{n-1},β	B^{n-1},β	B^n,β	B^n,β

Table 5- 9 Operation modes for scan-rate conversion

The Figure 5-32 explains the 50/60Hz interlaced to the 100/120 Hz interlaced conversion including the field signal, the raster organization and the memory timing for AABB.

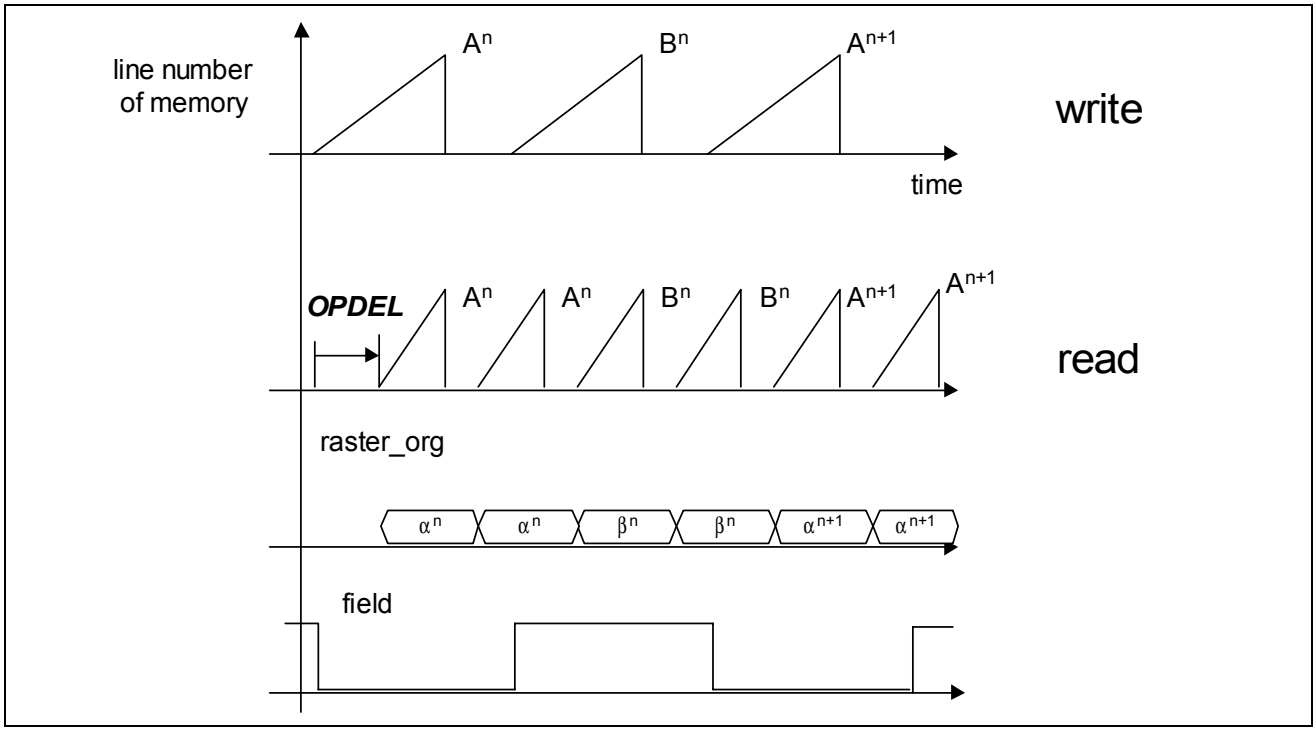

Figure 5-32 50/60 Hz interlaced to 100/120 Hz interlaced conversion (AABB)

A still field can be displayed using ***FREEZE*** command. For the improvement of VCR signals, the chrominance can be shifted one line upwards by ***CHRSHFT***

5.5 Display processing

The display processing part contains an integrated triple 9-bit DAC and performs digital enhancements and manipulations of the digital video component signal. The Figure 5-33 shows the block diagram of the display processing part.

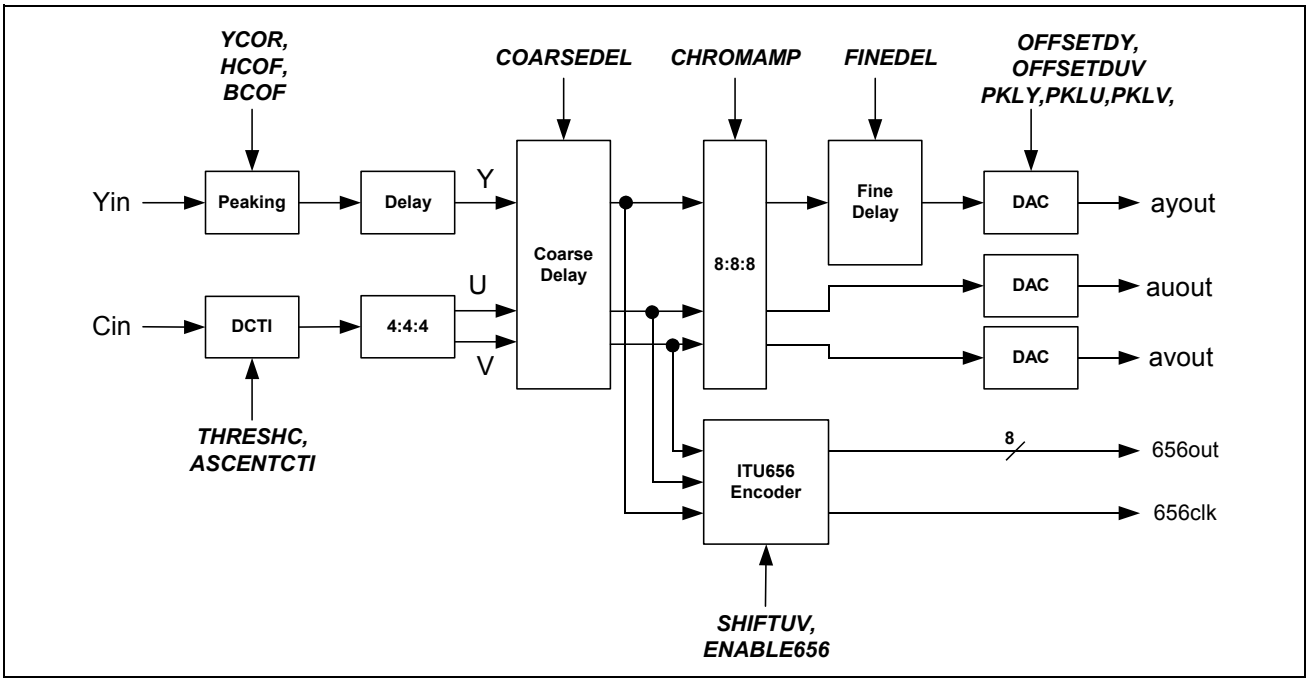

Figure 5-33 Block diagram of Display processing

5.5.1 Peaking

The luminance peaking filter improves the overall frequency response of the luminance channel. It consists of two filters working in parallel. They have high pass (HP) and band pass (BP) characteristics. Their gain factors are programmable separately (***BCOF***, ***HCOF***). Values greater than 4 peak the signal, whereas values less than 4 attenuate the signal. The high pass and the band pass filters are equipped with a common coring algorithm. It is optimized to achieve a smooth display of grey scales, not to improve the signal-to-noise ratio. Therefore no artifacts are produced. Coring can be switched off (***YCOR***). The Figure 5-34 shows the block diagram of the peaking block.

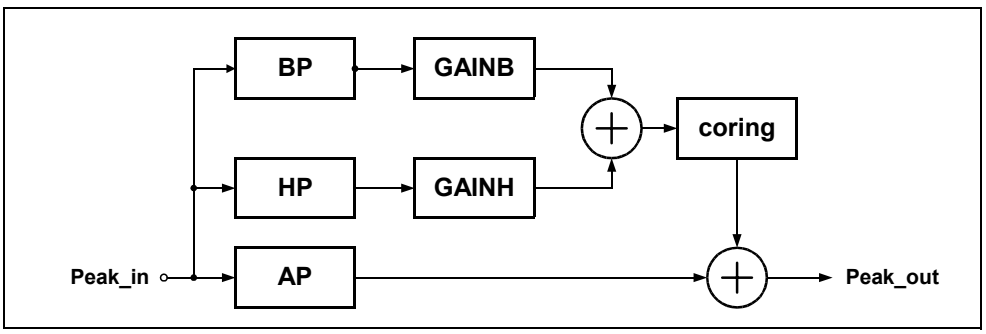

Figure 5-34 Block diagram peaking

The transfer function of the separate filters are listed below:

$$PEAKING(z) = GAINH \cdot \frac{(1-z^{-1})^4}{16} - GAINB \cdot \frac{(1-z^{-2})^2}{8} + z^{-2}$$

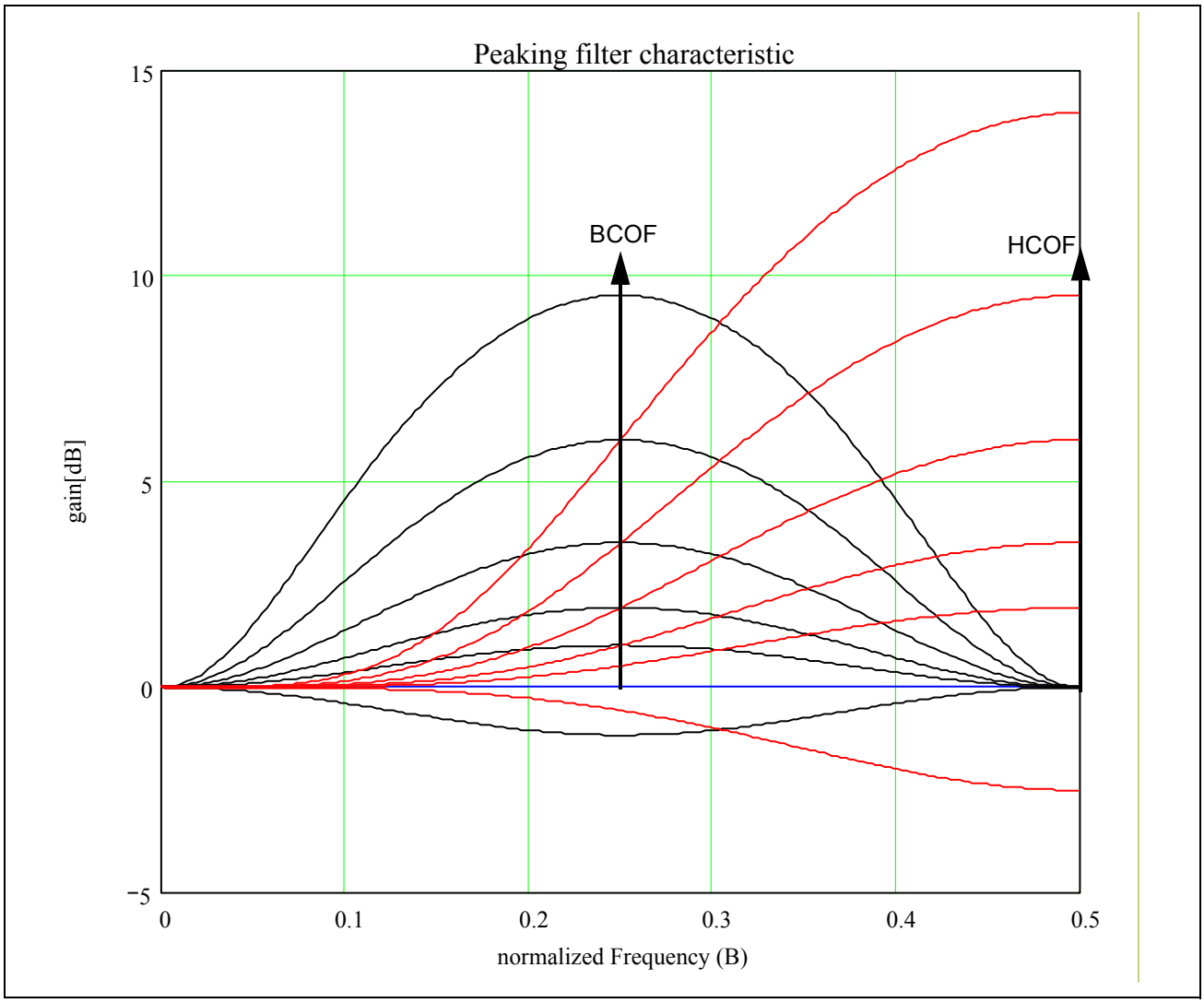

Figure 5-35 Peaking filter: Bandpass and Highpass filter

The peaking filter clock frequency is CLKB36 (36 MHz). The maximum signal frequency of the picture stored in the memory is 6.75 MHz. Due to a peaking after postscaler, the frequency range of the peaking filter varies with the expansion factor of the postscaler.

expansion factor of postscaler	corresponding frequency of input signal for center frequency bandpass (B=0.25)	corresponding frequency of input signal for center frequency highpass (B=0.5)
0.75	3.375 MHz	6.75 MHz
...	...	...
1	4.5 MHz	9 MHz
...	...	...
3	13.5 MHz	27 MHz

Table 5- 10 Peaking filter adaption

BCOF	GAINBP		HCOF	GAINHP
0	-1		0	-1
1	-0.75		1	-0.75
2	-0.50		2	-0.50
3	-0.25		3	-0.25
4	0.00		4	0.00
5	0.25		5	0.25
6	0.50		6	0.50
7	0.75		7	0.75
8	1.00		8	1.00
9	1.25		9	1.25
10	1.50		10	1.50
11	1.75		11	1.75
12	2.00		12	2.00
13	2.50		13	2.50
14	3.00		14	3.00
15	4.00		15	4.00

Table 5- 11 Conversion table between HCOF/BCOF and GAINHP/GAINBP

5.5.2 Digital color transition improvement (DCTI)

A new digital algorithm is implemented to improve horizontal transitions of the chrominance signals resulting in a better picture sharpness. A correction signal proportional to the slope of the detected horizontal transition of the input signal is added to the original input signal. Different correction signals are selected according to the bandwidth of the input signal. The amplitude of the correction signal is adjustable by the I²C bus parameter ***ASCENTCTI***.

The exact position of a color transition is calculated by detecting the corresponding zero transition of the second derivative of both chrominance signals. Low pass filtering is performed to avoid noise sensitivity. The I²C bus parameter ***THRESHC*** modifies the sensitivity of the DCTI circuit. High values of ***THRESHC*** result in an improvement only of significant color transitions. Small color variations remain unchanged.

To eliminate “wrong color” transitions, which are caused by over- and undershoots at the chroma transition, the sharpened chroma signals are automatically limited to a proper value.

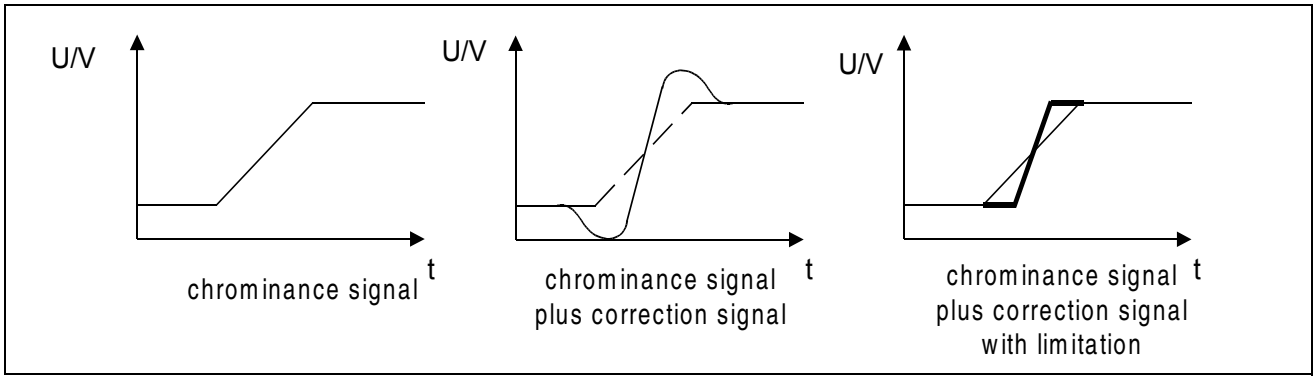

Figure 5-36 Principles of DCTI

5.5.3 Coarse and fine delay

Before digital-to-analog conversion an adjustment of the phase of the luminance is performed. A coarse delay from -8 to +7 in steps of 1 pixel CLKB36 (~28 ns) are possible (***COARSEDEL***). ***FINEDEL*** shifts the luminance one CLKB72 (~14 ns) pixel. This can be used to compensate delays, when Y and UV are externally processed differently (e.g. lowpass filtered).

5.5.4 Oversampling and DAC

After conversion into 8:8:8 format (CLKB72=72MHz), three 9-bit digital-to-analog converters are used for analog YUV output. This twofold-oversampling generates 1920 active pixels per line (when using recommended settings) and simplifies the external

postfiltering. Output voltage is determined by ***PKLY***, ***PKLU*** and ***PKLV*** in a range of 0.4 ...1.9 V (fullscale). The DC value for 'black' can be influenced by ***OFFSETDY*** and ***OFFSETDUV***. When AC coupling to backend processor (normally used), it should be set to zero.

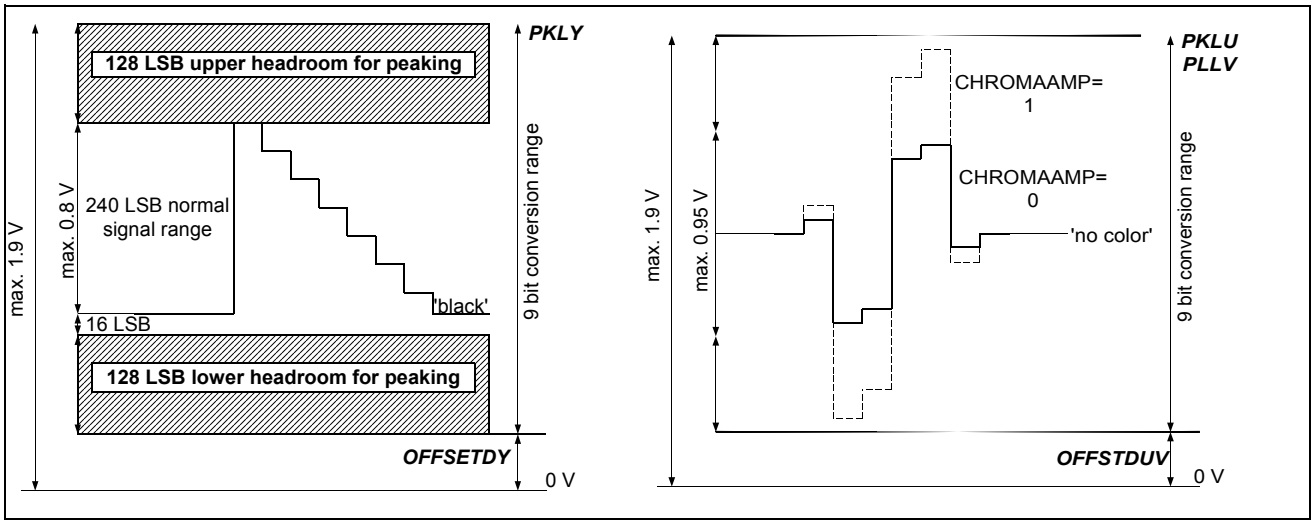

Figure 5-37 DAC output signals

8 bits of the luminance D/A converter are used for the entire signal. The 9th bit is used for over- and undershoots caused by the peaking to prevent or reduce clipping artifacts. As the CTI block seldomly produces such overshoots, a full-scale operation can be activated by ***CHROMAMP***. The output voltages may be calculated by:

$$\mathrm{VoltageY} = 1\mathrm{V} \cdot \frac{\mathbf{OFFSETDY}}{64} + \left(1.56\mathrm{V} \cdot \frac{\mathbf{PKLY}}{256} + 0.36\mathrm{V}\right) \cdot \mathrm{signalY}$$

$$\mathrm{signalY} = \frac{160....400}{512} \text{ for unpeaked signals max.}$$

$$\mathrm{signalY} = \frac{0....511}{512} \text{ for peaked signals max.}$$

$$\mathrm{VoltageU,V} = 1\mathrm{V} \cdot \frac{\mathbf{OFFSETDUV}}{64} + \left(1.56\mathrm{V} \cdot \frac{\mathbf{PKLU,V}}{256} + 0.36\mathrm{V}\right) \cdot \mathbf{CHROMAMP} \cdot \mathrm{signalUV}$$

$$\mathrm{signalUV} = \frac{128....384}{512}$$

5.5.5 Output-Sync Controller

The output sync controller generates horizontal and vertical synchronization signals for the scanrate-converted output signal.

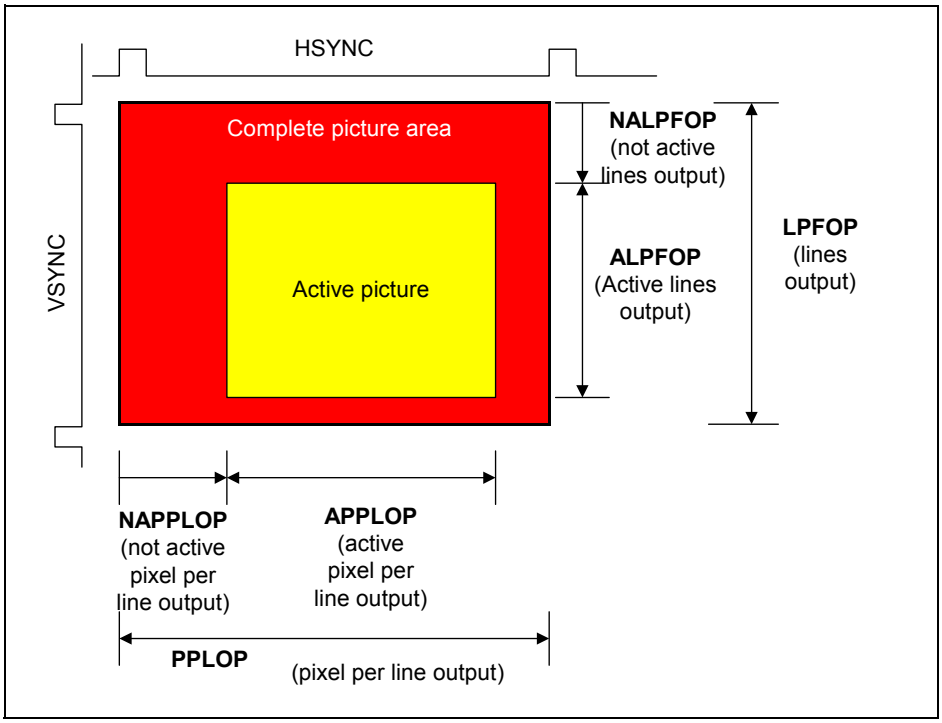

Figure 5-38 Image format behind memory

The number of pixels per line is 4*__PPLOP__. The default value of 288 results in 1152 pixels/line. With CLKB=36MHz, the horizontal output frequency is 31.25 kHz, which is twice the PAL horizontal frequency. Out of these pixels, 16*__APPLOP__ are displayed as active picture area, which are 960 by default. The position on the screen depends on the __NAPPLOP__. It marks the picture area not active in horizontal direction and moves the active picture in horizontal direction. The number of lines per field is 2*__LPFOP.__ This value is only used in the vertical free-running mode. In vertical locked mode, the number of lines per field is derived from the CVBS signal itself and not adjustable. The active and non-active picture areas are marked by __ALPFOP__ and __NALPFOP__, respectively.

Both generators have a so called “locked-mode” and “freerunning-mode”. Not all combinations of these modes make sense.The **Table 5- 12** shows ingenious configurations.

Mode	HOUTFR	VOUTFR
’H-and-V-locked’ mode	0	0
’H-freerunning / V-locked’ mode	1	0
’H-and V freerunning’ mode	1	1

Table 5- 12 Ingenious configurations of the HOUT and VOUT generator

For freerun mode the backend part works stand alone without analyzing the input signals. The clock domains, input data part and output data part of the IC, are not related to each other. If the output processing works in the freerun mode, the output signals of the OSC are generated depending on I²C-bus settings. For locked mode the backend part works with a line locked clock. This means that the frontend and the backend of the IC depend on each other. The generation of the controlling signals depends on output signals from the frontend. This mode will be the default and the most used mode for standard TV applications.

With activated vertical freerun mode the phase of the generated vsync signal has no correlation to the incoming vsync signal. A hard switch from freerun mode to locked mode would therefore cause visible synchronization problems in the deflection unit of the TV set concerning the vertical picture positioning. To avoid these problems a circuit is implemented which synchronizes the free running vsync signal to the vsync derived from the CVBS signal, to enable a soft transition to locked mode (***PDGSR***, ***LPFOPOFF***). This synchronization is only possible when the number of CVBS input lines corresponds to the programmed value of ***LPFOP***.

When no or very weak signal is connected to the CVBS input, the IC can be configured to automatically switch into freerunning mode. This stabilizes the display which may contain OSD information, e.g. during channel-tune. The configuration, whether the IC switches to H-freerun, V-freerun or both can be configured by ***AUTOFRRN***.

5.5.5.1 HOUT Generator

The HOUT generator has two operation modes, which can be selected by the parameter ***HOUTFR***. The HOUT signal is active high for 64 clock cycles (CLKB36). In the freerunning-mode the HOUT signal is generated depending on the ***PPLOP*** parameter. In the locked-mode the HOUT signal is locked on the incoming H-Sync signal derived from CVBS. The polarity of the HOUT signal is programmable by the parameter ***HOUTPOL***.

5.5.5.2 VOUT Generator

The VOUT generator has two operation modes, which can be selected by the parameter ***VOUTFR***. In the freerunning-mode (***VOUTFR***=1) the VOUT signal is generated depending on the ***LPFOP*** parameter.

In the locked-mode the VOUT signal is synchronized by the incoming V-Sync signal derived from CVBS, delayed by some lines (***OPDEL***). During one incoming V-Sync signal, two VOUT pulses have to be generated. The polarity of the VOUT signal is programmable by the parameter ***VOUTPOL***. The VOUT signal is active high for two output lines.

.

Display line scanning pattern sequence	1. to 2.	2. to 3.	3. to 4.	4. to 5.(1.)
α α α α	312	313	312	313
β β β β	313	312	313	312
α α β β	312	312.5	313	312.5
α β α β	312.5	312.5	312.5	312.5

Table 5- 13 Display line scanning pattern sequence

5.5.5.3 BLANK Generator

The BLANK signal is used to horizontally mark active picture area. It is enabled by ***BLANEN*** and its polarity can be chosen by ***BLANPOL***. Referred to hsync, the start is given by ***BLANDEL*** und its length is given by ***BLANLEN***, both adjustable in 4 pixel resolution.

5.5.5.4 Background Generator

This generator is able to realize an automatic closing and opening of the displayed picture. This means that with every picture the displayed colored background, defined by ***UBORDER***, ***VBORDER*** and ***YBORDER*** will get bigger or smaller. The original picture data will be replaced by the background values and vice versa. There is also the possibility to realize a fixed border via the I²C bus (***BORDPOSH*** and ***BORDPOSV***). 4096 different colors are available.

BORDPOSH and ***BORDPOSV*** also influence the window generation. This means the automatic opening and closing of the picture will start or end at the position which is defined with these values. The border is calculated with the following formula: The horizontal border on the left side of the TV screen is 2*__BORDPOSH__ and 2*__BORDPOSH__ on the right side of the TV screen. This means, that 4*__BORDPOSH__ pixels are overwritten with border values. The same applies to the vertical direction. 4*__BORDPOSV__ lines in total are overwritten with background values. ***BORDERV*** decides whether upper or lower or both borders are displayed. ***BORDERH*** decides whether left or right or both borders are displayed.

5.5.5.5 Window function

The Figure 5-39 shows the functionality of the horizontal window function. The window can be closed or opened.

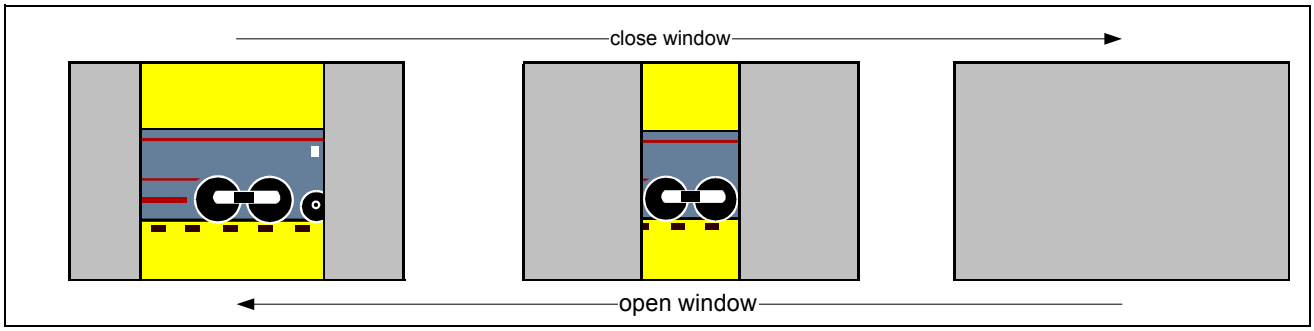

Figure 5-39 Horizontal windowing

The windowing feature can be enabled by the ***WINDHON*** parameter. The ***WINDHST*** and the ***WINDHDR*** parameter determine, what status (opened or closed) the window has, and what can be done with the window (open or close). With each enabling of the window function by the ***WINDHON*** parameter, the status of the window will be as defined by ***WINDHST*** and ***WINDHDR***. To change from „close“ to „open“ or vice versa only the ***WINDHDR*** parameter has to be toggled. The speed of the window can be defined by the ***WINDHSP*** parameter. The Figure 5-40 shows the functionality of the vertical window function.

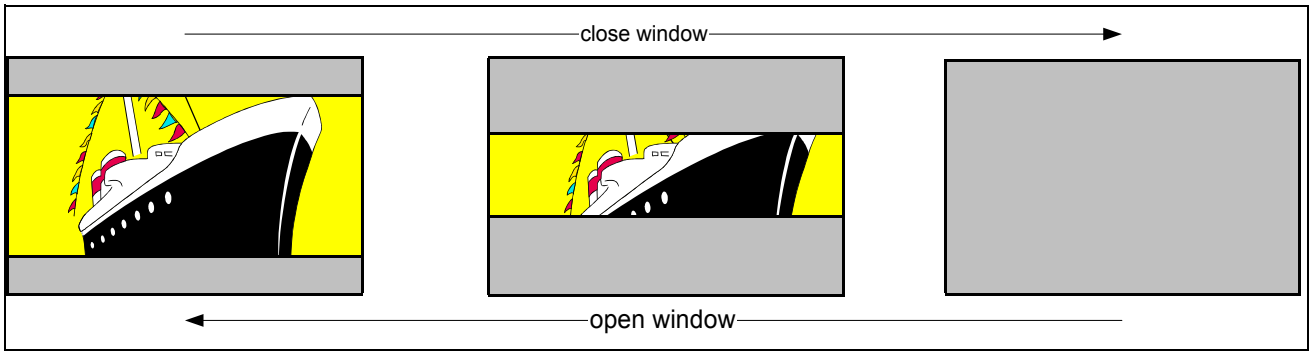

Figure 5-40 Vertical windowing

All settings are also available in vertical direction. All I²C parameters exist for both directions (e.g. ***WINDHON*** and ***WINDVON*** for horizontal and vertical window enabling). Combinations of both window functions (horizontal and vertical) are also possible.

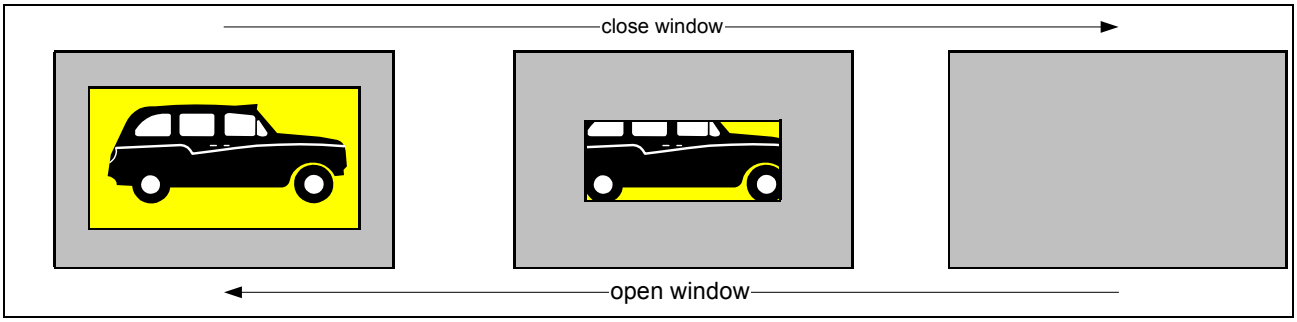

Figure 5-41 Horizontal and vertical windowing

5.5.6 Digital 656 input

The IC decodes a digital 8bit@27MHz data stream according to ITU.BT656 standard. The input is selected by EN656.

EN_656	ENABLE656	656 operation
0	0	input disabled / output disabled
0	1	input disabled / output enabled
1	0	input enabled / output disabled
1	1	(reserved)

Table 5- 14 656 input / output selection

Four modes are supported:

IMODE	656 operation
00	full ITU mode (automatic) information about active picture is taken from data-stream
01	full ITU mode (manual) information about active picture is taken from ***APLLIP***, ***NAPPLIP***, ***ALPFIP***, ***NALPFIP***
10	ITU656 only data, H/V-sync according PAL/NTSC
11	ITU656 only data, H/V-sync according ITU656

Table 5- 15 656 modes

To adjust the input to sources, which deviate from the standard, the field information may be inverted (***F_POL***) and the chrominance format can be chosen between unsigned and

2's complement format (***CFORMAT***). The polarity of H an V can be inverted by ***H_POL*** and ***V_POL*** respectively.

5.5.7 Digital 656 output

The output data format corresponds to CCIR 656 (8-bit bus at a data rate of 27 MHz). Timing reference codes (SAV, EAV) are inserted according to the specification. The output can be enabled by ***ENABLE656***. The display clock should be set to linelocked-clock (***HOUTFR***) with 27 MHz (***PPLIP***) and 720 pixels per line (***APPLOP***). The chrominance information can be inverted by ***CHRMSIGN656***. As digital input and output use the same pins, no digital input is possible when digital output is chosen (9402/9432). The versions 9412 and 9442 are equipped with a double-scan '656-like' output. All frequencies and data-rates are doubled compared to standard ITU656 signals.

5.6 Clock Concept

A single 20.25 MHz crystal at fundamental mode is used as clock reference. All other clocks are derived from this source. The CVBS frontend works with 20.25 MHz, the RGB frontend works with 40.5 MHz, the oversampling DACs use 72.0 MHz and the memory and all parts behind the memory are clocked with 36 MHz.

Three different clock concepts are supported. The difference is the behavior in clocking the memory output. The frontend part of the VSP 94x2A uses a free-running but crystal-stable clock (CLKF). After deskewing, an orthogonal picture is written into the memory. The read out is done using the (CLKB) clock.

The horizontal sync-signal output (HOUT) is derived from a counter running with CLKB. The VOUT is directly derived from the input vertical signal, which is generated by the sync-separation block. This '*H-freerunning-V-locked mode*' is only possible together with a DC coupled deflection controller.

In '*H-and-V-locked mode*' CLKB is line-locked to the incoming signal. The freerunning YUV picture data and the internal H signal are converted to the line-locked domain. Now HOUT and the sync signal in the $1f_H$ domain are directly coupled.

In case of '*H-and-V-freerunning mode*' the HOUT and VOUT signals are derived from counters running with CLKB. There is no connection to the incoming signal. This mode can be used for stable pictures when no signal is applied (e.g. channel search with OSD insertion)

name	clock	nominal frequency	'H-and-V-locked' mode	'H-freerunning-V-locked' mode	'H-and V freerunning' mode
CLKF20	CVBS frontend	20.25 MHz	FR	FR	FR
CLKF40	RGB frontend, input processing	40.5 MHz	FR	FR	FR
CLKB36	output and display processing	9402: 36 MHz (analog out) 9412: 27 MHz (digital out) 9432: 18 MHz (analog out) 9442: 13.5 MHz (digital out)	LL	FR	FR
CLKB72	oversampling, DAC	9402: 72 MHz 9412: 54 Mhz 9432: 36 MHz 9442: 27 MHz	LL	FR	FR
CLKB27	CLKOUT-pin	9402: 27 MHz 9432: 13.5 MHz (analog out) 9412: 20.26 MHz 9442: 10.13 MHz	LL	FR	FR

Table 5- 16 Clock system

A clock output of 27MHz (50 Hz version:13.5 MHz) is possible (pin 27:*clkout*). This clock is 3/4 of CLKB36. HOUT and VOUT are in line with this sampling clock. The clock output can be disabled by ***CLKOUTON***. Additionally a 20.25 MHz clock can be output to pin 74 (*656hin/clkf20*) to supply other ICs (e.g. PiP) with the same clock (***CLKF2PAD***). When enabled, 656-input with separate H/V-sync is not possible. For 656-output operation, CLKB36 is given to pin 9 (*656clk*).

5.6.1 Linelocked Clock Generator

The clock generation system derives all clocks from one 20.25 MHz crystal oscillator clock source. An internal PLL multiplies this by 32, generating a clock of 648 MHz which is used as reference for all clocks needed.

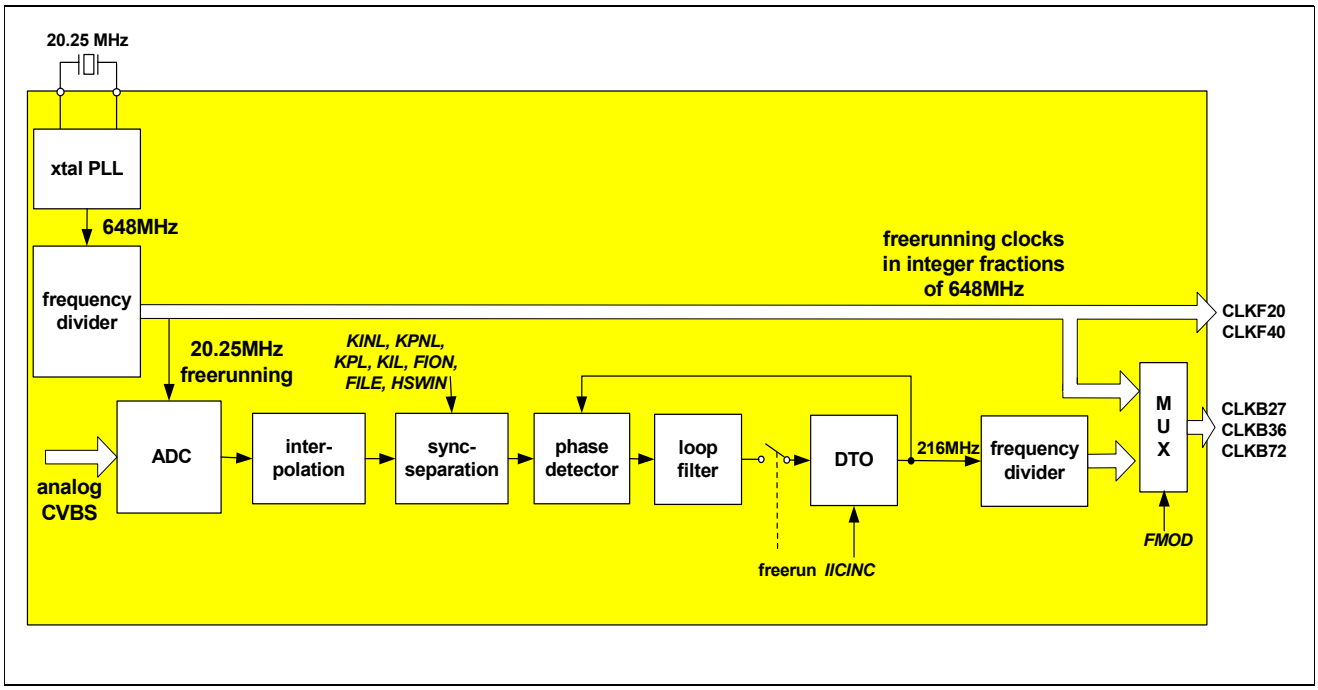

Figure 5-42 Linelocked clock generation

Linelocked horizontal sync pulses are generated by a digital phase locked loop. The time constant can be adjusted between fast and slow behavior (***KPL, KIL***) to accommodate different input sources (e.g. VCR). Noisy input signals become more stable when a noise-reduction is enabled (***HSWIN***). The PLL control can be frozen up to 15 lines before v-sync (***FION***) for a duration up to 15 lines (***FILE***). This may be used to reduce disturbances by h-phase errors which are produced by VCR's. Because of the delay between read and write pointer of field memory (Figure 5-32), the incoming 50Hz v-sync lies in the active picture area.

The output frequency for the 100/120 Hz version dependent on IICINCR is

$$f_{display} = IICINC \cdot 103Hz$$

The value is internally divided by two for the 50/60 Hz version.

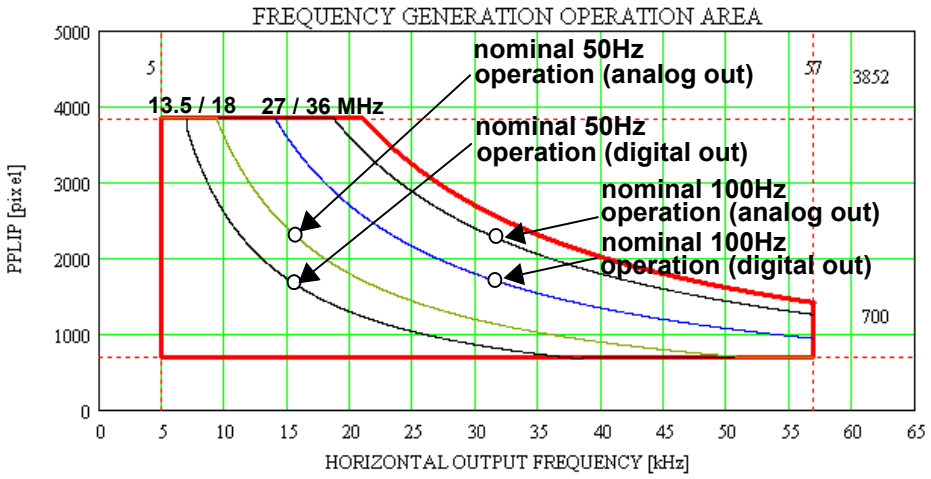

Figure 5-43 Allowed operation area for clock generation

The number of pixels generated by the PLL is given by **PPLIP**. For linelocked clock generation the following equation must be fulfilled:

$$\mathbf{PPLIP} = 2 \cdot \mathbf{PPLOP} \quad \text{(9402A, 9412A)}$$

$$\mathbf{PPLIP} = \mathbf{PPLOP} \quad \text{(9432A, 9442A)}$$

Operation	PPLIP	IICINCR	PPLOP	CLKB36	f_H
100/120 Hz (analog out)	2304	349525	1152	36 MHz	31.25 kHz
50/60 Hz (analog out)	2304	349525	1152	18 MHz	15.625 kHz
100/120 Hz (digital out)	1728	262229	864	27 MHz	31.25 kHz
50/60 Hz (digital out)	1728	262229	864	13.5 MHz	15.625 kHz

Table 5- 17 LL-PLL settings

The PLL settings for different operation modes can be seen in **Table 5- 17**

6 I²C-bus

6.1 I²C bus slave address

When pin 19 (adr/tdi) is connected to Vss, VSP94x2A reacts on first I²C address. The second address is active , when pin 19 is connected to Vdd

Write Address1: **B0h**									Read Address1: **B1h**							
1	**0**	**1**	**1**	**0**	**0**	**0**	**0**		**1**	**0**	**1**	**1**	**0**	**0**	**0**	**1**

Write Address2: **B2h**									Read Address2: **B3h**							
1	**0**	**1**	**1**	**0**	**0**	**1**	**0**		**1**	**0**	**1**	**1**	**0**	**0**	**1**	**1**

6.2 I²C bus format

The VSP 94x2A I²C bus interface acts as a slave receiver and a slave transmitter and provides two different access modes (write, read). All modes run with a subaddress auto increment. The interface supports the normal 100 kHz transmission speed as well as the high speed 400 kHz transmission.

write:

S	1	0	1	1	0	0	x	0	A	Subad-dress	A	Data Byte	A	*****	A	P

S: Start condition

SR: Repeated Start condition
A: Acknowledge
P: Stop condition
NA: Not Acknowledge

read:

S	1	0	1	1	0	0	x	0	A	Subad-dress	A	S R	1	0	1	1	0	0	x	1	A	Data Byte	A

Data Byte	NA	P

The transmitted data is internally stored in registers. The registers are located in four different clock domains. The Figure 6-1 shows the four different clock domains of the VSP 94x2A. The clock domains are called CP - CVBS processing block (20.25 MHz domain, clkf20), FP - Front end processing block (40.5 MHz domain, clkf40), BP - Back end processing block (36.0 MHz domain, clkb36) and PP - PLL processing block (36.0 MHz domain, clkf36).

Domain		Description	Clock
CP	CP-CD	CVBS frontend	CLKF20
	CP-PP	LL-PLL	CLKF20
	CP-I2C	I²C read	CLKF20
FP	FP-PRE	prescaler	CLKF40
	FP-MC	memory-controller	CLKF40
	FP-RGB	RGB Frontend	CLKF40
	FP-TNR	temporal noise reduction	CLKF40
	FP-I2C	I²C read	CLKF40
PP	PP	LL-PLL	CLKF36
	PP-I2C	I²C read	CLKF36
BP	BP-DP	display processing	CLKB36
	BP-PM	Pixel-Mixer	CLKB36
	BP-ODC	output data control	CLKB36
	BP-ODC/MC	output data control/ memory-controller	CLKB36
	BP-POS	postscaler	CLKB36
	BP-DAC	DAC processing	CLKB72
	BP-I2C	I²C read	CLKB36

Table 6- 1 I²C bus clock domains

The registers themselves are grouped in an I²C bus interface block, one in each domain. The transmitted data is received by the I²C bus kernel. The I²C bus kernel itself is located in the CP domain. This means that the working frequency is 20.25 MHz. The data is transmitted to the I²C bus interface blocks via an internal serial bus.

For the write process, the I²C bus master has to write a ’don’t care’ byte to the subaddress **FFh** (store command) to make the register values available to the four I²C

bus interface blocks (except for the not-take-over registers). In order to have a defined time step for the several blocks in the different domains, where the data will be available from the I²C bus interface blocks, the data are made valid with internal V-sync related signals (rising edge), depending on the different clock domains. The subaddresses, where the data are made valid with the V-sync signal of the 20.25 MHz domain are indicated in the overview of the subaddresses with „V20“, the others are called “V40”, “V36F” and “V36B”, respectively. The I²C parameter ***V20STAT***, ***V40STAT*** and ***V36BSTAT*** reflect the state of the register values. If these bits are read as ’1’, then the store command was sent, but the data is not made available yet. If these bits are ’0’ then the data was made valid and a new write or read cycle can start. The bits ***V20STAT***, ***V40STAT*** and ***V36BSTAT*** may be checked before writing or reading new data, otherwise data can be lost by overwriting. No *V36FSTAT* register exist. To make the register values available to the four I²C bus interface immediately after sending, the I²C bus master has to write a ’don’t care’ byte to the subaddress **FEh** (store command).

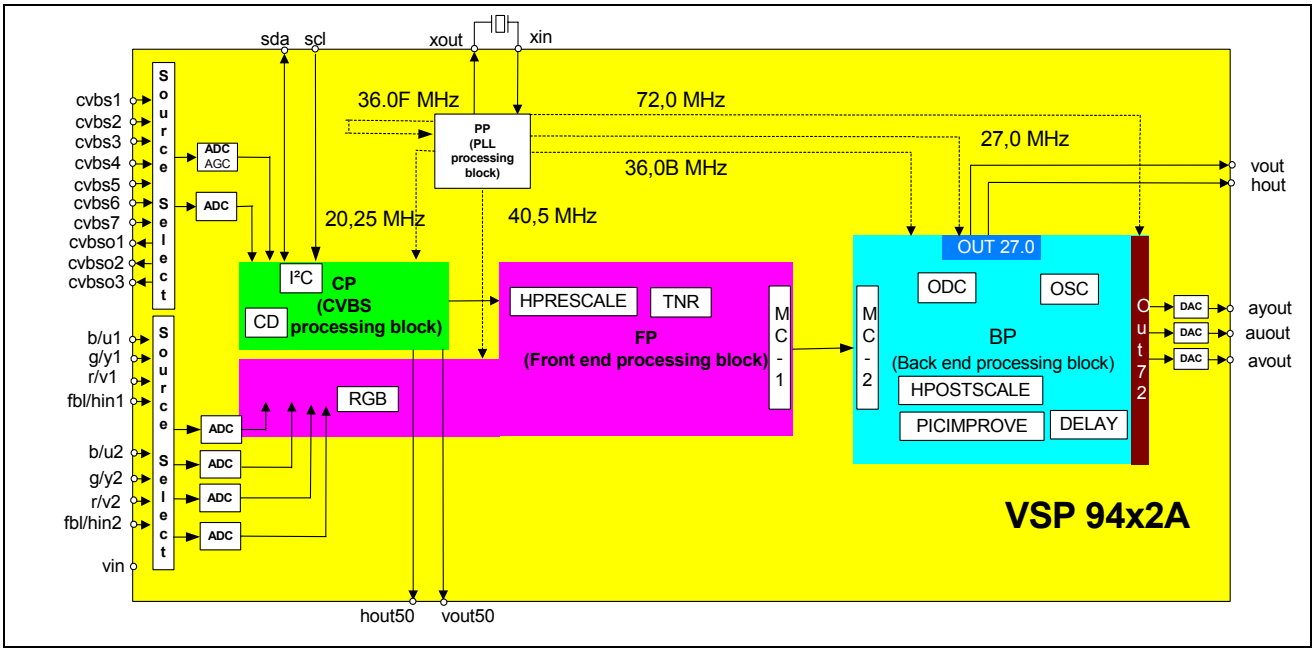

Figure 6-1 I²C bus clock domains

For the read process, the I²C bus master must not send a store command. In order to have a defined time step for the I²C bus interface blocks in the different domains, where the data will be available from the different blocks, the data is made valid with the same V-Sync related signals mentioned above for the write process. The VSP 94x2A distinguishes between two different types of read-registers. The behavior of the “normal” read registers does not differ from the behavior of the write registers.Only the direction of the data flow is opposite. The “rs typ” read registers behave differently. They can be only set (means value 1) by the internal blocks using the rising edge of a corresponding signal. After reading by the I²C bus master, the registers will be automatically reset

(means value 0) by the I²C bus kernel/interface. For example the register ***NMSTATUS*** belongs to the “rs typ” read registers. ***NMSTATUS*** signalizes a new value for ***NOISEME***. So if ***NMSTATUS*** is read as ’0’ the current noise measurement has not been updated. If the ***NMSTATUS*** is read as ’1’ a new noise measurement value can be read. All other “rs typ” read registers work in the same way. The “rs typ” read registers will be marked in the overview with the short cut “rstyp” or will have the additional hint “**Note**: reset automatically when read/write” in the detailed I²C bus command description.

By default all registers are made valid by the internal V-Sync related signals and, in addition, a store command has to be sent for write registers. The registers, which should also be made available immediately as for writing and reading, are marked with the short cut NTO (No take over mechanism).

Registers which need a hand-shake mechanism between the I²C bus interface and the different blocks are marked with the shortcut HS (Hand shake mechanism). This means that all bits of the registers are used when the last register is written. After ***PPLIP9-2*** is written, ***PPLIP1-0*** must be written to allow these bits to have effect.

The registers for the write parameter ***STOPMODE*** are directly connected to the read registers of the parameter ***SMMIRROR***. So it is possible to check the I²C bus protocol by writing and reading to the register ***STOPMODE*** and ***SMMIRROR***, respectively.

The transmitted data is internally stored in registers. Writing to or reading from a non - existant register is permitted and does not generate a fault by the IC.

After switching on the IC, all bits of the VSP 94x2A are set to defined states, (refer to **Table 6- 2**). ***POR*** is set after reset to pin 24. It stays ’1’, until it is cancled via software ***PORCNCL***. This can be used to decide during TV operation, whether to program all registers (e.g. after power failure reset) or only altered ones (normal TV operation).

Subaddress	Default	R/W	take-over	Subaddress	Default	R/W	take-over
00h	AAh	W	V40	**1Dh**	44h	W	V40
01h	CAh	W	V40	**1Eh**	00h	W	V40
02h	B0h	W	V40	**1Fh**	FFh	W	V40
03h	C8h	W	V40	**20h**	1Fh	W	V40
04h	16h	W	V40	**21h**	F4h	W	V40
05h	10h	W	V40	**22h**	44h	W	V40
06h	20h	W	V40	**23h**	00h	W	V40
07h	01h	W	V40	**24h**	FFh	W	V40
08h	F0h	W	V40	**25h**	AAh	W	NTO
09h	3Eh	W	V40	**26h**	AAh	W	NTO
0Ah	00h	W	V40	**27h**	05h	W	NTO/HS
0Bh	A0h	W	V40	**28h**	00h	W	NTO/rstyp
0Ch	00h	W	V40	**29h**	60h	W	NTO
0Dh	90h	W	V40	**2Ah**	60h	W	NTO
0Eh	80h	W	V40	**2Bh**	90h	W	NTO
0Fh	00h	W	V40	**2Ch**	00h	W	NTO/HS
10h	20h	W	V40	**2Dh**	04h	W	NTO
11h	20h	W	V40	**2Eh**	00h	W	NTO
12h	00h	W	V40	**2Fh**	(spare)		
13h	00h	W	V40	**30h**	2Dh	W	V36B
14h	00h	W	V40	**31h**	44h	W	V36B
15h	00h	W	V40	**32h**	D4h	W	V36B
16h	00h	W	V40	**33h**	20h	W	V36B
17h	00h	W	V40	**34h**	00h	W	V36B
18h	16h	W	V40	**35h**	00h	W	V36B
19h	00h	W	V40	**36h**	01h	W	V36B
1Ah	03h	W	V40	**37h**	00h	W	V36B
1Bh	1Fh	W	V40	**38h**	E0h	W	V36B
1Ch	F4h	W	V40	**39h**	01h	W	V36B

Subaddress	Default	R/W	take-over	Subaddress	Default	R/W	take-over
3Ah	00h	W	V36B	**58h**	80h	W	V36B
3Bh	00h	W	V36B	**59h**	80h	W	V36B
3Ch	26h	W	V36B	**5Ah**	80h	W	V36B
3Dh	3Ch	W	V36B	**5Bh**	44h	W	V20
3Eh	01h	W	V36B	**5Ch**	40h	W	V20
3Fh	00h	W	V36B	**5Dh**	C0h	W	V20
40h	04h	W	V36B	**5Eh**	5Ch	W	V20
41h	40h	W	V36B	**5Fh**	66h	W	V20
42h	20h	W	V36B	**60h**	40h	W	V20
43h	9Ch	W	V36B	**61h**	40h	W	V20
44h	AAh	W	V36B	**62h**	00h	W	V20
45h	00h	W	V36B	**63h**	00h	W	V20
46h	18h	W	V36B	**64h**	A5h	W	V20
47h	0Bh	W	V20	**65h**	5Fh	W	V20
48h	00h	W	V36B	**66h**	0Fh	W	V20
49h	00h	W	V36B	**67h**	00h	W	V20
4Ah	00h	W	V36B	**68h**	00h	W	V20
4Bh	00h	W	V36B	**69h**	3Ch	W	V20
4Ch	00h	W	V36B	**6Ah**	03h	W	V20
4Dh	00h	W	V36B	**6Bh**	07h	W	V20
4Eh	55h	W	V36B	**6Ch**	07h	W	V20
4Fh	0Bh	W	V36B	**6Dh**	1Ch	W	V20
50h	00h	W	V36B	**6Eh**	5Ch	W	V20
51h	00h	W	V36B	**6Fh**	00h	W	V20
52h	00h	W	V36B	**70h**	00h	W	V20
53h	00h	W	V36B	**71h**	E4h	W	V20
54h	00h	W	V36B	**72h**	00h	W	V20
55h	00h	W	V36B	**73h**	00h	W	V20
56h	3Fh	W	V36B	**74h**	00h	W	V20
57h	3Fh	W	V36B	**75h**	7Fh	W	V20

Subaddress	Default	R/W	take-over	Subaddress	Default	R/W	take-over
76h	00h	W	V20	**86-8F**		R	NTO
77h	00h	W	V20	**90h-95h**	(spare)		
78h	1Ch	W	V20	**96h**		R	V40
79h	1Ch	W	V20	**97h**	(spare)		
7Ah	FCh	W	V20	**98h**		R	V36B
7Bh	77h	W	V20	**99h**		R	V20
7Ch	02h	W	V20	**A0h**	00h	W	NTO
7Dh	6Ch	W	V20	**A1h**	00h	W	NTO
7Eh	00h	W	V20	**A2h**	FFh	W	NTO
7Fh	15h	W	V20	**A3h**	FFh	W	NTO
80h	00h	W	V20	**A4h**	00h	W	NTO
81h	00h	W	V20	**A5h-F5h**	(spare)		
82h (no autoincrement)	00h	W	V20	**F6h**		R	NTO
83h		R	NTO	**F7h-FDh**	(spare)		
84h (no autoincrement)		R	NTO	**FEh**		W	
85h		R	no/rstyp	**FFh**		W	

take-over mechanism			**register types**	
NTO	no take-over mechanism		**W**	write register
V20	take-over with V-sync in 20 MHz domain		**R**	read register
V40	take-over with V-sync in 40 MHz domain		**Rrstyp**	reset register after reading
V36B	take-over with V-sync in backend 36.0 MHz domain			
HS	hand-shake mechanism required			

Table 6- 2 I²C bus register characterization

6.3 I²C bus list in alphabetical order

AABYP	0Ch
ACCFIX	5Bh
ACCFRZ	5Bh
ACCLIM	7Ah
ADCSEL	0Ch
ADLCK	81h
ADLCKCC	81h
ADLCKSEL	81h
AGCADJ1	67h
AGCADJ2	68h
AGCADJB	16h
AGCADJF	17h
AGCADJG	15h
AGCADJR	14h
AGCFRZE	68h
AGCMD	67h
AGCRES	68h
ALPFIP	05h
ALPFOP	32h
APENSEL	05h
APPLIP	01h
APPLOP	3Dh
ASCENTCTI	30h
AUTOFRRN	32h
BCOF	31h
BELLFIR	7Dh
BELLIIR	7Dh
BGPOS	47h
BLANDEL	07h
BLANEN	36h
BLANLEN	08h
BLANPOL	36h
BORDERH	45h
BORDERV	45h
BORDPOSH	35h
BORDPOSV	34h
BRTADJ	0Ah
CFORMAT	18h
CHRF	5Eh
CHRMSIGN656	55h
CHROMAMP	57h
CHROMSIGN	57h
CHRSF	0Bh
CHRSHFT	3Dh
CKILL	60h
CKILLS	61h
CKSTAT	88h
CLKF2PAD	16h
CLKOUTON	30h
CLKT	2Eh
CLMPD1	6Bh
CLMPD1S	7Bh
CLMPD2	6Ch
CLMPD2S	7Bh
CLMPHIGH	69h
CLMPLOW	6Ah
CLMPST1	6Dh
CLMPST1S	78h
CLMPST2	6Eh
CLMPST2S	79h
CLMPVG	10h
CLMPVRB	0Dh
CLPSTGY	6Bh
CLRANGE	5Dh
COARSEDEL	32h
COLON	5Bh
COMB	5Fh
CON	5Ch
CONADJ	0Bh
CONS	5Bh
CPLLOF	5Bh
CPLLRES	80h
CRCB	5Bh
CSTAND	5Fh
CVBOSEL1	6Ah
CVBOSEL2	70h
CVBOSEL3	70h
CVBSEL1	6Fh
CVBSEL2	6Fh
DCLMPF	10h
DECTWO	0Bh
DEEMPFIR	7Dh
DEEMPIIR	5Eh
DEEMPSTD	82h
DETHPOL	88h
DETVPOL	88h
DISALLRES	80h
DISCHCH	6C
DISRES	27h
EIA770	7Ch
EN_656	18h
ENABLE656	56h
ENLIM	7Eh
F_POL	18h
FBLACTIVE	83h
FBLCONF	0Dh
FBLDEL	0Dh
FBLOFFST	0Ch
FHDET	6Ch
FHFRRN	71h
FIELDBINV	54h
FILE	2Eh
FINEDEL	32h
FIOFFOFF	54h
FION	2Dh
FKOI	A4h
FKOIHYS	A4h
FLDINV	6Bh
FLINE	6Bh
FLNSTRD	7Eh
FMOD	29h
FREEZE	3Fh
FREQSEL	7Ch
GOFST	0Eh
H_POL	18h
HAAPRESC	09h
HCOF	31h
HDCPRESC	05h
HDTOTEST	2Eh
HINC0	48h
HINC1	49h
HINC2	4Ah
HINC3	4Bh
HINC4	4Ch
HINCREXT	29h
HINP	6Dh
HORPOS	3Ah
HORWIDTH	38h
HOUTDEL	3Eh
HOUTFR	41h
HOUTPOL	41h
HPANON	4Fh
HPOL	6Ch
HRES	28h
HSCPOSC	4Eh
HSCPRESC	01h
HSEG1	50h
HSEG2	51h
HSEG3	52h
HSEG4	53h
HSWIN	29h
HTESTW	2Ah
HUE	63h
HWID	2Eh
IFCOMP	7Ah
IICINCR	25h
IMODE	18h
INT	89h
ISHFT	7Eh
KD2	29h
KIL	A1h
KINL	A1h
KOIH	2Ah
KOIWID	2Ah
KPL	A0h
KPNL	A0h
LIMII	A3h
LIMIP	A2h
LIMLR	A4h
LMOD	29h
LMOFST	5Dh
LNL	2Dh
LNSTDRD	89h
LOCKSP	47h
LPCDEL	72h
LPFLD	8Ah
LPFOP	43h
LPFOPFF	3Ch
LPPOST	62h
MIXGAIN	0Fh
MIXOP	0Dh
MLL	09h
NALPFIP	04h
NALPFOP	45h
NAPIPPHI	17h
NAPPLIP	02h
NAPPLOP	3Fh
NMLINE	19h
NMSTATUS	85h
NOISEME	84h
NOSIGB	6Dh
NOSYNC	3Ch
NOTCHOFF	5Ch
NRON	1Ah
NRPIXEL	8Bh
NSRED	72h/ 7Eh
NTCHSEL	80h
NTSCREF	64h
OFFSETDUV	57h
OFFSETDY	56h
OPDEL	44h
OSCPD	7Ch
PALDEL	47h
PALDET	8Ch
PALID	88h
PALIDL0	75h
PALIDL1	74h
PALIDL2	81h
PALINC1	82h
PALINC2	82h
PALREF	65h
PB	85h
PDGSR	3Fh
PFBL	85h
PG	85h
PKLU	59h
PKLV	5Ah
PKLY	58h
PLLTC	6Eh
POR	8Ch
PORCNCL	80h
PPLIP	2Bh
PPLOFF	3Ch
PPLOP	41h
PR	85h
PWTHD	5Dh
RBOFST	0Eh
RDCTRLDIS	45h
REFRON	41h
REFRPER	41h
REFTRIM	76h
REFTRIMCV	77h
REFTRIMCVRD	8Eh
REFTRIMEN	72h
REFTRIMRD	8Dh
REFTRIMRGB	77h
REFTRIMRGBRD	8Eh
REV	F6h
RGBSEL	0Fh
SATNR	72h
SCADJ	66h
SCDEV	89h
SCMIDL	79h
SCMREL	7Fh
SCOUTEN	88h
SECACC	7Fh
SECACCL	81h
SECDIV	7Fh
SECINC1	7Fh
SECINC2	7Fh
SECNTCH	5Ch
SETSTABL	29h
SHAPERDIS	7Ch
SHIFTUV	56h
SKEWSEL	0Eh
SLLTHD	66h
SLLTHDV	7Ch
SLLTHDVP	78h
SLS	8Fh/ F6h
SMMIRROR	87h
SMOP	0Eh
STAB	8Ch
STABLL	86h

STANDBY	11h
STDET	88h
STOPMODE	3Fh
THRESHC	30h
THRSEL	78h
TNRABS	1Ah
TNRCLC	24h
TNRCLY	24h
TNRS0C	20h
TNRS0Y	1Bh
TNRS1C	20h
TNRS1Y	1Bh
TNRS2C	21h
TNRS2Y	1Ch
TNRS3C	21h
TNRS3Y	1Ch
TNRS4C	22h
TNRS4Y	1Dh
TNRS5C	22h
TNRS5Y	1Dh
TNRS6C	23h
TNRS6Y	1Eh
TNRS7C	23h
TNRS7Y	1Eh
TNRSEL	1Ah
TNRSSC	1Fh

TNRSSY	1Fh
TRAPBLU	80h
TRAPRED	80h
TSTSHAPERI	7Ch
UBORDER	37h
USATADJ	10h
UVCOR	5Ch
UVDEL	13h
V_POL	18h
V20STAT	99h
V36BSTAT	98h
V40STAT	96h
VBORDER	37h
VDEL_EN	55h
VDELF_EN	03h
VDETIFS	5Dh
VDETITC	5Dh
VERSION	8Fh/ F6h
VFLYWHL	7Dh
VFLYWHLMD	81h
VINP	72h
VLP	7Eh
VOUTFR	41h
VOUTPOL	41h
VPOL	62h

VSATADJ	11h
VSHIFT	73h
VSIGNAL	18h
VTHRH	75h
VTHRL	74h
WINDHDR	3Bh
WINDHON	3Bh
WINDHSP	3Bh
WINDHST	3Bh
WINDVDR	39h
WINDVON	39h
WINDVSP	39h
WINDVST	39h
WRCTRLDIS	09h
YBORDER	36h
YCDEL	62h
YCOR	30h
YCSEL	6Bh
YFDEL	12h
YUVSEL	0Eh

6.4 I²C bus Command Table

Note: Bits written with grey background are intended not to be user adjustable and should be set to the default value written in this data sheet or according to an updated list (’application note I²C settings’) available from Micronas.

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Subadd (Hex)	Data Byte								
	D7	D6	D5	D4	D3	D2	D1	D0	
00h	APPLIP8	APPLIP7	APPLIP6	APPLIP5	APPLIP4	APPLIP3	APPLIP2	APPLIP1	Input processing
01h	APPLIP0	HSCPRESC11	HSCPRESC10	HSCPRESC9	HSCPRESC8	HSCPRESC7	HSCPRESC6	HSCPRESC5	
02h	HSCPRESC4	HSCPRESC3	HSCPRESC2	HSCPRESC1	HSCPRESC0	NAPPLIP9	NAPPLIP8	NAPPLIP7	
03h	VDELF_EN	NAPPLIP6	NAPPLIP5	NAPPLIP4	NAPPLIP3	NAPPLIP2	NAPPLIP1	NAPPLIP0	
04h	NALPFIP7	NALPFIP6	NALPFIP5	NALPFIP4	NALPFIP3	NALPFIP2	NALPFIP1	NALPFIP0	
05h	**APENSEL**	NALPFIP8	ALPFIP9	ALPFIP8	HDCPRESC3	HDCPRESC2	HDCPRESC1	HDCPRESC0	
06h	ALPFIP7	ALPFIP6	ALPFIP5	ALPFIP4	ALPFIP3	ALPFIP2	ALPFIP1	ALPFIP0	
07h	**BLANDEL7**	**BLANDEL6**	**BLANDEL5**	**BLANDEL4**	**BLANDEL3**	**BLANDEL2**	**BLANDEL1**	**BLANDEL0**	
08h	**BLANLEN7**	**BLANLEN6**	**BLANLEN5**	**BLANLEN4**	**BLANLEN3**	**BLANLEN2**	**BLANLEN1**	**BLANLEN0**	
09h		WRCTRLDIS	**HAAPRESC1**	**HAAPRESC0**	MLL3	MLL2	MLL1	MLL0	
0Ah	BRTADJ7	BRTADJ6	BRTADJ5	BRTADJ4	BRTADJ3	BRTADJ2	BRTADJ1	BRTADJ0	RGB frontend
0Bh	DECTWO	CHRSF	CONADJ5	CONADJ4	CONADJ3	CONADJ2	CONADJ1	CONADJ0	
0Ch	ADCSEL	AABYP	FBLOFFST5	FBLOFFST4	FBLOFFST3	FBLOFFST2	FBLOFFST1	FBLOFFST0	
0Dh	CLMPVRB1	CLMPVRB0	FBLDEL2	FBLDEL1	FBLDEL0	MIXOP1	MIXOP0	FBLCONF	
0Eh	YUVSEL	SMOP	SKEWSEL	RBOFST2	RBOFST1	RBOFST0	GOFST1	GOFST0	
0Fh	RGBSEL	MIXGAIN6	MIXGAIN5	MIXGAIN4	MIXGAIN3	MIXGAIN2	MIXGAIN1	MIXGAIN0	
10h	CLMPVG	DCLMPF	USATADJ5	USATADJ4	USATADJ3	USATADJ2	USATADJ1	USATADJ0	
11h	STANDBY1	STANDBY0	VSATADJ5	VSATADJ4	VSATADJ3	VSATADJ2	VSATADJ1	VSATADJ0	
12h			YFDEL5	YFDEL4	YFDEL3	YFDEL2	YFDEL1	YFDEL0	
13h			UVDEL5	UVDEL4	UVDEL3	UVDEL2	UVDEL1	UVDEL0	
14h			AGCADJR5	AGCADJR4	AGCADJR3	AGCADJR2	AGCADJR1	AGCADJR0	
15h			AGCADJG5	AGCADJG4	AGCADJG3	AGCADJG2	AGCADJG1	AGCADJG0	
16h		CLKF2PAD	AGCADJB5	AGCADJB4	AGCADJB3	AGCADJB2	AGCADJB1	AGCADJB0	
17h	NAPIPPHI1	NAPIPPHI0	AGCADJF5	AGCADJF4	AGCADJF3	AGCADJF2	AGCADJF1	AGCADJF0	
18h	IMODE1	IMODE0	VSIGNAL	CFORMAT	F_POL	H_POL	V_POL	EN_656	
19h	NMLINE7	NMLINE6	NMLINE5	NMLINE4	NMLINE3	NMLINE2	NMLINE1	NMLINE0	Noise reduction
1Ah					NMLINE8	TNRABS	NRON	TNRSEL	
1Bh	TNRS0Y3	TNRS0Y2	TNRS0Y1	TNRS0Y0	TNRS1Y3	TNRS1Y2	TNRS1Y1	TNRS1Y0	
1Ch	TNRS2Y3	TNRS2Y2	TNRS2Y1	TNRS2Y0	TNRS3Y3	TNRS3Y2	TNRS3Y1	TNRS3Y0	
1Dh	TNRS4Y3	TNRS4Y2	TNRS4Y1	TNRS4Y0	TNRS5Y3	TNRS5Y2	TNRS5Y1	TNRS5Y0	
1Eh	TNRS6Y3	TNRS6Y2	TNRS6Y1	TNRS6Y0	TNRS7Y3	TNRS7Y2	TNRS7Y1	TNRS7Y0	
1Fh	TNRSSY3	TNRSSY2	TNRSSY1	TNRSSY0	TNRSSC3	TNRSSC2	TNRSSC1	TNRSSC0	
20h	TNRS0C3	TNRS0C2	TNRS0C1	TNRS0C0	TNRS1C3	TNRS1C2	TNRS1C1	TNRS1C0	
21h	TNRS2C3	TNRS2C2	TNRS2C1	TNRS2C0	TNRS3C3	TNRS3C2	TNRS3C1	TNRS3C0	
22h	TNRS4C3	TNRS4C2	TNRS4C1	TNRS4C0	TNRS5C3	TNRS5C2	TNRS5C1	TNRS5C0	
23h	TNRS6C3	TNRS6C2	TNRS6C1	TNRS6C0	TNRS7C3	TNRS7C2	TNRS7C1	TNRS7C0	
24h	TNRCLY3	TNRCLY2	TNRCLY1	TNRCLY0	TNRCLC3	TNRCLC2	TNRCLC1	TNRCLC0	

Subadd (Hex)	Data Byte								
	D7	D6	D5	D4	D3	D2	D1	D0	
25h	IICINCR18	IICINCR17	IICINCR16	IICINCR15	IICINCR14	IICINCR13	IICINCR12	IICINCR11	Line-locked clock PLL
26h	IICINCR10	IICINCR9	IICINCR8	IICINCR7	IICINCR6	IICINCR5	IICINCR4	IICINCR3	
27h					DISRES	IICINCR2	IICINCR1	IICINCR0	
28h								HRES	
29h	HSWIN2	HSWIN1	HSWIN0	SETSTABLL	KD2	HINCREXT	LMOD	FMOD	
2Ah	KOIWID1	KOIWID0	KOIH1	KOIH0	HTESTW3	HTESTW2	HTESTW1	HTESTW0	
2Bh	PPLIP9	PPLIP8	PPLIP7	PPLIP6	PPLIP5	PPLIP4	PPLIP3	PPLIP2	
2Ch							PPLIP1	PPLIP0	
2Dh	FION3	FION2	FION1	FION0					
2Eh	CLKT	CLKT	HWID	HDTOTEST	FILE3	FILE2	FILE1	FILE0	
2Fh									
30h	YCOR1	YCOR0	CLKOUTON	THRESHC2	THRESHC1	THRESHC0	ASCENTCTI1	ASCENTCTI0	Display processing
31h	HCOF3	HCOF2	HCOF1	HCOF0	BCOF3	BCOF2	BCOF1	BCOF0	
32h	**AUTOFRRN1**	**AUTOFRRN0**	ALPFOP9	ALPFOP8	FINEDEL	COARSEDEL2	COARSEDEL1	COARSEDEL0	
33h	ALPFOP7	ALPFOP6	ALPFOP5	ALPFOP4	ALPFOP3	ALPFOP2	ALPFOP1	ALPFOP0	
34h	BORDPOSV7	BORDPOSV6	BORDPOSV5	BORDPOSV4	BORDPOSV3	BORDPOSV2	BORDPOSV1	BORDPOSV0	
35h	BORDPOSH7	BORDPOSH6	BORDPOSH5	BORDPOSH4	BORDPOSH3	BORDPOSH2	BORDPOSH1	BORDPOSH0	
36h	**BLANPOL**	**BLANEN**	BORDPOSH9	BORDPOSH8	YBORDER3	YBORDER2	YBORDER1	YBORDER0	
37h	UBORDER3	UBORDER2	UBORDER1	UBORDER0	VBORDER3	VBORDER2	VBORDER1	VBORDER0	
38h	HORWIDTH7	HORWIDTH6	HORWIDTH5	HORWIDTH4	HORWIDTH3	HORWIDTH2	HORWIDTH1	HORWIDTH0	
39h	WINDVSP1	WINDVSP0	WINDVST	WINDVDR	WINDVON	HORWIDTH10	HORWIDTH9	HORWIDTH8	
3Ah	HORPOS7	HORPOS6	HORPOS5	HORPOS4	HORPOS3	HORPOS2	HORPOS1	HORPOS0	
3Bh	WINDHSP1	WINDHSP0	WINDHST	WINDHDR	WINDHON	HORPOS10	HORPOS9	HORPOS8	
3Ch	NOSYNC	PPLOFF2	PPLOFF1	PPLOFF0	LPFOPFF3	LPFOPFF2	LPFOPFF1	LPFOPFF0	
3Dh	CHRSHFT	APPLOP6	APPLOP5	APPLOP4	APPLOP3	APPLOP2	APPLOP1	APPLOP0	
3Eh	HOUTDEL7	HOUTDEL6	HOUTDEL5	HOUTDEL4	HOUTDEL3	HOUTDEL2	HOUTDEL1	HOUTDEL0	
3Fh	NAPPLOP9	NAPPLOP8	PDGSR	FREEZE	STOPMODE1	STOPMODE0	HOUTDEL9	HOUTDEL8	
40h	NAPPLOP7	NAPPLOP6	NAPPLOP5	NAPPLOP4	NAPPLOP3	NAPPLOP2	NAPPLOP1	NAPPLOP0	
41h	PPLOP9	PPLOP8	REFRPER	REFRON	HOUTPOL	VOUTPOL	HOUTFR	VOUTFR	
42h	PPLOP7	PPLOP6	PPLOP5	PPLOP4	PPLOP3	PPLOP2	PPLOP1	PPLOP0	
43h	LPFOP7	LPFOP6	LPFOP5	LPFOP4	LPFOP3	LPFOP2	LPFOP1	LPFOP0	
44h	OPDEL7	OPDEL6	OPDEL5	OPDEL4	OPDEL3	OPDEL2	OPDEL1	OPDEL0	
45h	BORDERV1	BORDERV0	BORDERH1	BORDERH0	RDCTRLDIS	LPFOP8	NALPFOP8	OPDEL8	
46h	NALPFOP7	NALPFOP6	NALPFOP5	NALPFOP4	NALPFOP3	NALPFOP2	NALPFOP1	NALPFOP0	
47h		PALDEL.1	PALDEL.0	**LOCKSP1**	**LOCKSP0**	BGPOS2	BGPOS1	BGPOS0	CVBS

Subadd (Hex)	Data Byte								
	D7	D6	D5	D4	D3	D2	D1	D0	
48h	HINC0_7	HINC0_6	HINC0_5	HINC0_4	HINC0_3	HINC0_2	HINC0_1	HINC0_0	Panorama scaler
49h	HINC1_7	HINC1_6	HINC1_5	HINC1_4	HINC1_3	HINC1_2	HINC1_1	HINC1_0	
4Ah	HINC2_7	HINC2_6	HINC2_5	HINC2_4	HINC2_3	HINC2_2	HINC2_1	HINC2_0	
4Bh	HINC3_7	HINC3_6	HINC3_5	HINC3_4	HINC3_3	HINC3_2	HINC3_1	HINC3_0	
4Ch	HINC4_7	HINC4_6	HINC4_5	HINC4_4	HINC4_3	HINC4_2	HINC4_1	HINC4_0	
4Dh				HINC4_8	HINC3_8	HINC2_8	HINC1_8	HINC0_8	
4Eh	HSCPOSC7	HSCPOSC6	HSCPOSC5	HSCPOSC4	HSCPOSC3	HSCPOSC2	HSCPOSC1	HSCPOSC0	
4Fh				HPANON	HSCPOSC11	HSCPOSC10	HSCPOSC9	HSCPOSC8	
50h	HSEG1_7	HSEG1_6	HSEG1_5	HSEG1_4	HSEG1_3	HSEG1_2	HSEG1_1	HSEG1_0	
51h	HSEG2_7	HSEG2_6	HSEG2_5	HSEG2_4	HSEG2_3	HSEG2_2	HSEG2_1	HSEG2_0	
52h	HSEG3_7	HSEG3_6	HSEG3_5	HSEG3_4	HSEG3_3	HSEG3_2	HSEG3_1	HSEG3_0	
53h	HSEG4_7	HSEG4_6	HSEG4_5	HSEG4_4	HSEG4_3	HSEG4_2	HSEG4_1	HSEG4_0	
54h	FIOFFOFF	FIELDBINV	HSEG2_10	HSEG2_9	HSEG2_8	HSEG1_10	HSEG1_9	HSEG1_8	
55h	CHRMSIG656	VDEL_EN	HSEG4_10	HSEG4_9	HSEG4_8	HSEG3_10	HSEG3_9	HSEG3_8	
56h	SHIFTUV	ENABLE656	OFFSETDY5	OFFSETDY4	OFFSETDY3	OFFSETDY2	OFFSETDY1	OFFSETDY0	DAC control
57h	CHROMSIGN	CHROMAMP	OFFSETDUV5	OFFSETDUV4	OFFSETDUV3	OFFSETDUV2	OFFSETDUV1	OFFSETDUV0	
58h	PKLY7	PKLY6	PKLY5	PKLY4	PKLY3	PKLY2	PKLY1	PKLY0	
59h	PKLU7	PKLU6	PKLU5	PKLU4	PKLU3	PKLU2	PKLU1	PKLU0	
5Ah	PKLV7	PKLV6	PKLV5	PKLV4	PKLV3	PKLV2	PKLV1	PKLV0	

Subadd (Hex)	Data Byte								
	D7	D6	D5	D4	D3	D2	D1	D0	
5Bh	CONS2	CONS1	CONS0	COLON	CPLLOF	CRCB	ACCFIX	ACCFRZ	CVBS Frontend
5Ch	CON2	CON1	CON0	UVCOR1	UVCOR0	NOTCHOFF	SECNTCH1	SECNTCH0	
5Dh	PWTHD1	PWTHD0	**CLRANGE1**	**CLRANGE0**	LMOFST1	LMOFST0	VDETIFS	VDETITC	
5Eh	DEEMPIIR.1	DEEMPIIR.0	CHRF5	CHRF4	CHRF3	CHRF2	CHRF1	CHRF0	
5Fh	COMB	CSTAND6	CSTAND5	CSTAND4	CSTAND3	CSTAND2	CSTAND1	CSTAND0	
60h	CKILL7	CKILL6	CKILL5	CKILL4	CKILL3	CKILL2	CKILL1	CKILL0	
61h	CKILLS7	CKILLS6	CKILLS5	CKILLS4	CKILLS3	CKILLS2	CKILLS1	CKILLS0	
62h	VPOL1	VPOL0	**LPPOST**	YCDEL4	YCDEL3	YCDEL2	YCDEL1	YCDEL0	
63h	HUE7	HUE6	HUE5	HUE4	HUE3	HUE2	HUE1	HUE0	
64h	NTSCREF7	NTSCREF6	NTSCREF5	NTSCREF4	NTSCREF3	NTSCREF2	NTSCREF1	NTSCREF0	
65h	PALREF7	PALREF6	PALREF5	PALREF4	PALREF3	PALREF2	PALREF1	PALREF0	
66h	SLLTHD1	SLLTHD0	SCADJ5	SCADJ4	SCADJ3	SCADJ2	SCADJ1	SCADJ0	
67h	AGCMD1	AGCMD0	AGCADJ15	AGCADJ14	AGCADJ13	AGCADJ12	AGCADJ11	AGCADJ10	
68h	AGCRES	AGCFRZE	AGCADJ25	AGCADJ24	AGCADJ23	AGCADJ22	AGCADJ21	AGCADJ20	
69h	CLMPHIGH7	CLMPHIGH6	CLMPHIGH5	CLMPHIGH4	CLMPHIGH3	CLMPHIGH2	CLMPHIGH1	CLMPHIGH0	
6Ah	CVBOSEL1_3	CVBOSEL1_2	CVBOSEL1_1	CVBOSEL1_0	CLMPLOW3	CLMPLOW2	CLMPLOW1	CLMPLOW0	
6Bh	FLINE	FLDINV	CLPSTGY	YCSEL	CLMPD1_3	CLMPD1_2	CLMPD1_1	CLMPD1_0	
6Ch	HPOL1	HPOL0	FHDET	DISCHCH	CLMPD2_3	CLMPD2_2	CLMPD2_1	CLMPD2_0	
6Dh	NOSIGB	HINP	CLMPST1_5	CLMPST1_4	CLMPST1_3	CLMPST1_2	CLMPST1_1	CLMPST1_0	
6Eh	PLLTC1	PLLTC0	CLMPST2_5	CLMPST2_4	CLMPST2_3	CLMPST2_2	CLMPST2_1	CLMPST2_0	
6Fh	CVBSEL2_3	CVBSEL2_2	CVBSEL2_1	CVBSEL2_0	CVBSEL1_3	CVBSEL1_2	CVBSEL1_1	CVBSEL1_0	
70h	CVBOSEL2_3	CVBOSEL2_2	CVBOSEL2_1	CVBOSEL2_0	CVBOSEL3_3	CVBOSEL3_2	CVBOSEL3_1	CVBOSEL3_0	
71h	FHFRRN7	FHFRRN6	FHFRRN5	FHFRRN4	FHFRRN3	FHFRRN2	FHFRRN1	FHFRRN0	
72h	REFTRIMEN	SATNR	VINP	NSRED1	NSRED0	LPCDEL2	LPCDEL1	LPCDEL0	
73h	VSHIFT7	VSHIFT6	VSHIFT5	VSHIFT4	VSHIFT3	VSHIFT2	VSHIFT1	VSHIFT0	
74h	PALIDL1	VTHRL6	VTHRL5	VTHRL4	VTHRL3	VTHRL2	VTHRL1	VTHRL0	
75h	PALIDL0	VTHRH6	VTHRH5	VTHRH4	VTHRH3	VTHRH2	VTHRH1	VTHRH0	
76h	REFTRIM7	REFTRIM6	REFTRIM5	REFTRIM4	REFTRIM3	REFTRIM2	REFTRIM1	REFTRIM0	
77h	REFTRIMCV3	REFTRIMCV2	REFTRIMCV1	REFTRIMCV0	REFTRIMRGB3	REFTRIMRGB2	REFTRIMRGB1	REFTRIMRGB0	
78h	**SLLTHDVP**	**THRSEL**	CLMPST1S5	CLMPST1S4	CLMPST1S3	CLMPST1S2	CLMPST1S1	CLMPST1S0	
79h	SCMIDL1	SCMIDL0	CLMPST2S5	CLMPST2S4	CLMPST2S3	CLMPST2S2	CLMPST2S1	CLMPST2S0	
7Ah	ACCLIM4	ACCLIM3	ACCLIM2	ACCLIM1	ACCLIM0	IFCOMP2	IFCOMP1	IFCOMP0	
7Bh	CLMPD2S3	CLMPD2S2	CLMPD2S1	CLMPD2S0	CLMPD1S3	CLMPD1S2	CLMPD1S1	CLMPD1S0	
7Ch	SLLTHDV1	SLLTHDV0	EIA770	SHAPERDIS	OSCPD	TSTSHAPERI	FREQSEL1	FREQSEL0	
7Dh	DEEMPFIR2	DEEMPFIR1	DEEMPFIR0	BELLFIR1	BELLFIR0	BELLIIR1	BELLIIR0	VFLYWHL	
7Eh	FLNSTRD1	FLNSTRD0	ENLIM	ISHFT1	ISHFT0	NSRED2	VLP1	VLP0	
7Fh	SECACC	SECDIV	SECINC1_1	SECINC1_0	SECINC2_1	SECINC2_0	SCMREL1	SCMREL0	
80h	**PORCNCL**	**NTCHSEL2**	**NTCHSEL1**	**NTCHSEL0**	**CPLLRES**	**DISALLRES**	**TRAPBLU**	**TRAPRED**	
81h	**ADLCK**	**ADLCKSEL**	**ADLCKCC**	**VFLYWHLMD1**	**VFLYWHLMD0**	**PALIDL2**	**SECACCL1**	**SECACCL0**	
82h						**DEEMPSTD**	**PALINC1**	**PALINC2**	

Subadd (Hex)	Data Byte								
	D7	D6	D5	D4	D3	D2	D1	D0	
83h								FBLACTIVE	Read register
84h				NOISEME4	NOISEME3	NOISEME2	NOISEME1	NOISEME0	
85h				PFBL	PG	PB	PR	NMSTATUS	
86h								STABLL	
87h							SMMIRROR1	SMMIRROR0	
88h	DETHPOL	DETVPOL	STDET2	STDET1	STDET0	SCOUTEN	PALID	CKSTAT	
89h	LNSTDRD	INT	SCDEV5	SCDEV4	SCDEV3	SCDEV2	SCDEV1	SCDEV0	
8Ah	LPFLD7	LPFLD6	LPFLD5	LPFLD4	LPFLD3	LPFLD2	LPFLD1	LPFLD0	
8Bh	NRPIXEL7	NRPIXEL6	NRPIXEL5	NRPIXEL4	NRPIXEL3	NRPIXEL2	NRPIXEL1	NRPIXEL0	
8Ch	**POR**					STAB		**PALDET**	
8Dh	REFTRIMRD7	REFTRIMRD6	REFTRIMRD5	REFTRIMRD4	REFTRIMRD3	REFTRIMRD2	REFTRIMRD1	REFTRIMRD0	
8Eh	REFTRIMCVRD3	REFTRIMCVRD2	REFTRIMCVRD1	REFTRIMCVRD0	REFTRIMRGBRD3	REFTRIMRGBRD2	REFTRIMRGBRD1	REFTRIMRGBRD0	
8Fh					SLS	VERSION2	VERSION1	VERSION0	
96h								V40STAT	
97h								(reserved)	
98h								V36BSTAT	
99h								V20STAT	
A0h	**KPNL3**	**KPNL2**	**KPNL1**	**KPNL0**	**KPL3**	**KPL2**	**KPL1**	**KPL0**	PP
A1h	**KINL3**	**KINL2**	**KINL1**	**KINL0**	**KIL3**	**KIL2**	**KIL1**	**KIL0**	
A2h	**LIMIP7**	**LIMIP6**	**LIMIP5**	**LIMIP4**	**LIMIP3**	**LIMIP2**	**LIMIP1**	**LIMIP0**	
A3h	**LIMII7**	**LIMII6**	**LIMII5**	**LIMII4**	**LIMII3**	**LIMII2**	**LIMII1**	**LIMII0**	
A4h	**FKOI**	**FKOIHYS**				**LIMLR2**	**LIMLR1**	**LIMLR0**	
F6h	**VERSION2**	**VERSION1**	**VERSION0**	**SLS**	**REV2**	**REV1**	**REV0**		read
FEh	take-over-indication (immediately)								
FFh	take-over-indication (after V-pulse)								

Table 6- 3 I²C register overview

6.5 I²C bus Command Description

Underlined values are initialized at power-on.

Subaddress 00h		
D7-D0	APPLIP8-1 [FP-PRE]	**Active Pixel Per Line** Number of pixels to be stored in memory Granularity: 2 pixel '000000000': 0 pixel '101010101': 682 pixel '111111111': 1022 pixel

Subaddress 01h		
D7	APPLIP0 [FP-PRE]	belongs to 00h
D6-D0	HSCPRESC1 1-5 [FP-PRE]	**Control Signal For HSCALE In Horizontal Pre-scaler** '000000000000': subsampling factor by scaler stage is 1 '100000000000': subsampling factor is 1.5 (720 pixel) '100101010110': subsampling factor is 1.583 (682 pixel) '111111111111': subsampling factor is 2 (540 pixel)

Subaddress 02h		
D7-D3	HSCPRESC4-0 [FP-PRE]	belongs to 01h
D2-D0	NAPPLIP9-7 [FP-PRE]	**Not Active Pixel Per Line** Granularity: 2 clock cycles (~50 ns) '0000000000': 0 clock cycles '0001001000': 144 clock cycles (~7.2 µs) '1111111111': 2046 clock cycles (~51 µs)

Subaddress 03h		
D7	VDELF_EN [FP-PRE]	**Vertical pulse delay frontend** '0': no delay '1': delayed
D6-D0	NAPPLIP6-0 [FP-PRE]	belongs to 02h

Subaddress 04h		
D7-D0	NALPFIP7-0 [FP-PRE]	**Not Active Lines Per Field (Input Processing)** '000000000': 0 lines '000010110': 22 lines '111111111': 511 lines

Subaddress 05h		
D7	APENSEL [FP-PRE]	**Active Pixel Enable Select** 0: count clock cycles (recommended for CVBS/RGB input) 1: count active pixels (recommended for ITU656 input)
D6	NALPFIP8 [FP-PRE]	belongs to 04h
D5-D4	ALPFIP9-8 [FP-PRE]	**Active Lines Per Field** '0000000000': no active line '0100100000': 288 active lines '1111111111': 1023 active lines

Subaddress 05h		
D3-D0	HDCPRESC	**Horizontal Pre-Scaler Decimates By** '0000': 1 '0001': 2 '0010': 3 '0011': 4 '0100': 6 '0101': 8 '0110': 12 '0111': 16 '1000': 24 '1001': 32

Subaddress 06h		
D7-D0	ALPFIP7-0	belongs to 05h

Subaddress 07h		
D7-D0	BLANDEL	**Blanking signal delay** Delay in pixels from hsync to active edge of blank signal: Blank_start=4*__BLANDEL__ '00000000': no delay '00000001': 4 pixel delay '11111111': 1020 pixel delay

Subaddress 08h		
D7-D0	BLANLEN	**Blanking signal length** Length in pixels from start of active blank signal: Blank_length=4*__BLANLEN__ ’00000000’: no pixel ’11110000’: 960 pixel ’11111111’: 1020 pixel length

Subaddress 09h		
D6	WRCTRLDIS [FP-MC]	**Memory Write Control Circuit Disable** ’0’: enabled ’1’: disabled
D5-D4	HAAPRESC [FP-MC]	**Horizontal Anti Alias Filter** ’00’: filter bypassed ’01’: force characteristic weak ’10’: force characteristic strong ’11’: automatic characteristic (weak or strong) *Note: For normal CVBS/RGB full-screen, filter should be set to weak or automatic characteristic. For ITU656 full-screen input, filter should be bypassed. Strong characteristic is for split-screen and PiP only.*
D3-D0	MLL [FP-MC]	**Minimum Line Length** effective number of clock periods: 600 + MLL*128 1110: corresponds to 2392 clock periods

Subaddress 0Ah		
D7-D0	BRTADJ [FP-RGB]	**Brightness Adjustment of RGB/YUV input** ’10000000’:-128 LSB (darkest picture) ’00000000’: 0 ’01111111’:+127 LSB (brightest picture)

Subaddress 0Bh		
D7	DECTWO [FP-RGB]	**Decimation by 2** decimation of RGB/YUV signal before soft-mix ’0’: no decimation ’1’: decimation by 2
D6	CHRSF [FP-RGB]	**Additional Chroma subsampling filter** ’0’: disabled ’1’: enabled
D5-D0	CONADJ [FP-RGB]	**Contrast Adjustment of RGB/YUV input** ’000000’: 0 ’000001’: 1/32 ’100000’: 1 ’111111’: 63/32

Subaddress 0Ch		
D7	ADCSEL [FP-RGB]	**Select ADC for sync signal conversion** ’0’: use ADC_G ’1’: use ADC_FBL
D6	AABYP [FP-RGB]	**Bypass RGB/YUV Antialiasfilter** ’0’: use filter ’1’: bypass

Subaddress 0Ch		
D5-D0	FBLOFFST [FP-RGB]	**Fast Blank Offset Correction** '000000': 0 LSB offset '111111': 63 LSB offset

Subaddress 0Dh		
D7-D6	CLMPVRB [FP-RGB]	**Clamping Value Red and Blue ADC** '00': 16 (B/R signal without sync) '01': 80 (B/R signal with sync) '10': 128 (U/V signal) '11': (reserved)
D5-D3	FBLDEL [FP-RGB]	**Fast Blank Delay vs. RGB/YUV Input** granularity: 25 ns '000': -50 ns delay '010': no delay '110': +100 ns delay '111': (reserved)
D2-D1	MIXOP [FP-RGB]	**Mixing Configuration** '00': enable Soft-Mix '01': only RGB path visible '10': only CVBS path visible '11': (reserved)
D0	FBLCONF [FP-RGB]	**Configuration of FBLACTIVE signal** '0': react after one clock (25ns) active FBL input '1': react after 5 clock (125ns) active FBL input

Subaddress 0Eh		
D7	YUVSEL [FP-RGB]	**YUV or RGB Input Selection** '0': YUV expected '1': RGB expected

Subaddress 0Eh		
D6	SMOP [FP-RGB]	**Softmix Operation Mode** '0':dynamic '1':static
D5	SKEWSEL [FP-RGB]	**SKEW Correction for RGB/YUV Channel** '0':SKEW correction enabled '1':SKEW correction disabled (for PiP3, PiP4 only)
D4-D2	RBOFST [FP-RGB]	**Clamping Correction for R/B ADC** '000': 0 (R/B, no pedestal offset visible) '001': 16 '010': 64 (R/B with sync, no pedestal offset visible) '011': 80 '100': 127 (UV negative pedestal offset) '101': 128 (UV) '110': 129 (UV positive pedestal offset) '111': (reserved)
D1-D0	GOFST [FP-RGB]	**Clamping correction for G ADC** '00': 0 (G/Y, no pedestal offset visible) '01': 16 '10': 64 (G/Y with sync, no pedestal offset visible) '11': 80

Subaddress 0Fh		
D7	RGBSEL [FP-RGB]	**Input selection** '0': use RGB/YUV input1 '1': use RGB/YUV input2
D6-D0	MIXGAIN [FP-RGB]	**Gain of Fast Blank Signal** **'**1000000**'**: -64 '0000000': 0 **'**0111111**'**: +63 *Note: For proper operation in dynamic softmix mode, absolute value of **MIXGAIN** must be bigger than 2 (e.g. 3)*

Subaddress 10h		
D7	CLMPVG [FP-RGB]	**Clamping Value G ADC** '0': 16 '1': 80
D6	DCLMPF [FP-RGB]	**Clamping Fast Blank input** '0': enable clamping '1': disable clamping (DC coupling)
D5-D0	USATADJ [FP-RGB]	**U Saturation Adjustment** '000000': 0 '000001': 1/32 '100000': 1 '111111': 63/32

Subaddress 11h		
D7-D6	STANDBY [FP-RGB]	**Standby Mode** '00': all analog cores active '01': RGB/FBL ADCs in Stand-By mode '10': RGB/FBL and CVBS ADCs and DACs in Stand-By mode '11': DACs in Stand-By mode
D5-D0	VSATADJ [FP-RGB]	**V Saturation Adjustment** '000000': 0 '000001': 1/32 '100000': 1 '111111': 63/32

Subaddress 12h		
D5-D0	YFDEL [FP-RGB]	**Y/FBL Delay Adjustment** Granularity: 50 ns '000000': no delay '111111': 3.15 us

Subaddress 13h		
D5-D0	UVDEL [FP-RGB]	**UV Delay Adjustment** Granularity: 50 ns '000000': no delay '111111': 3.15 us

Subaddress 14h		
D5-D0	AGCADJR [FP-RGB]	**Conversion Range Adjustment Red** '000000': 0.5 V input signal '111111': 1.5 V input signal

Subaddress 15h		
D5-D0	AGCADJG [FP-RGB]	**Conversion Range Adjustment Green** '000000': 0.5 V input signal '111111': 1.5 V input signal

Subaddress 16h		
D6	CLKF2PAD [FP-RGB]	**Frontend clock is given to pin 74** '0' pin 74 is used as h-input for ITU656 '1': CLKF20 (20.25 MHz) is given to pin 74
D5-D0	AGCADJB [FP-RGB]	**Conversion Range Adjustment Blue** '000000': 0.5 V input signal '111111': 1.5 V input signal

Subaddress 17h		
D7-D6	NAPIPPHI [FP-RGB]	**CbYCrY-phase shift** '0': no phase shift
D5-D0	AGCADJF [FP-RGB]	**Conversion Range Adjustment Fast Blank** '000000': 0.5 V input signal '111111': 1.5 V input signal

Subaddress 18h		
D7-D6	IMODE [FP-RGB]	**Input format** '00': full ITU mode (automatic) '01': full ITU mode (manual) '10': ITU656 only data, H/V-sync according PAL/NTSC '11': ITU656 only data, H/V-sync according ITU656
D5	VSIGNAL [FP-RGB]	**Input signal** '0': interlaced '1': non interlaced
D4	CFORMAT [FP-RGB]	**Chrominance data format** '0': unsigned '1': 2s complement

Subaddress 18h		
D3	F_POL [FP-RGB]	**Field polarity** '0': Field A=0, Field B=1 '1': Field A=1, Field B=0
D2	H_POL [FP-RGB]	**H656 polarity** '0': H656 active low '1': H656 active high
D1	V_POL [FP-RGB]	**V656 polarity** '0': V656 active low '1': V656 active high
D0	EN_656 [FP-RGB]	**ITU656-Input Interface** '0': ITUI disabled '1': ITUI enabled

Subaddress 19h		
D7-D0	NMLINE7-0 [FP-TNR]	**Line For Noise Measurement** 0_d: line 2 1_d: line 3 311_d: line 1 (PAL) 261_d: line 1 (NTSC) *Note: lines 3-260 are not standard dependent*

Subaddress 1Ah		
D3	NMLINE8 [FP-TNR]	belongs to 19h
D2	TNRABS [FP-TNR]	**Motion Detector Works on Absolute Values:** '0': absolute values not calculated '1': absolute values calculated

Subaddress 1Ah		
D1	NRON [FP-TNR]	**Temporal Noise Reduction** '0': disabled '1': enabled
D0	TNRSEL [FP-TNR]	**Chrominance Motion Values From:** '0': luminance motion detector '1': separate chrominance motion detector

Subaddress 1Bh		
D7-D4	TNRS0Y [FP-TNR]	**TNR Curve Characteristic of Luma Segment 0** default value: 0001
D3-D0	TNRS1Y [FP-TNR]	**TNR Curve Characteristic of Luma Segment 1** default value: 1111

Subaddress 1Ch		
D7-D4	TNRS2Y [FP-TNR]	**TNR Curve Characteristic of Luma Segment 2** default value: 1111
D3-D0	TNRS3Y [FP-TNR]	**TNR Curve Characteristic of Luma Segment 3** default value: 0100

Subaddress 1Dh		
D7-D4	TNRS4Y [FP-TNR]	**TNR Curve Characteristic of Luma Segment 4** default value: 0100
D3-D0	TNRS5Y [FP-TNR]	**TNR Curve Characteristic of Luma Segment 5** default value: 0100

Subaddress 1Eh		
D7-D4	TNRS6Y [FP-TNR]	**TNR Curve Characteristic of Luma Segment 6** default value: 0000
D3-D0	TNRS7Y [FP-TNR]	**TNR Curve Characteristic of Luma Segment 7** default value: 0000

Subaddress 1Fh		
D7-D4	TNRSSY [FP-TNR]	**TNR Start Value of Luma LUT** default value: 1111
D3-D0	TNRSSC [FP-TNR]	**TNR Start Value of Chroma LUT** default value: 1111

Subaddress 20h		
D7-D4	TNRS0C [FP-TNR]	**TNR Curve Characteristic of Chroma Segment 0** default value: 0001
D3-D0	TNRS1C [FP-TNR]	**TNR Curve Characteristic of Chroma Segment 1** default value: 1111

Subaddress 21h		
D7-D4	TNRS2C [FP-TNR]	**TNR Curve Characteristic of Chroma Segment 2** default value: 1111
D3-D0	TNRS3C [FP-TNR]	**TNR Curve Characteristic of Chroma Segment 3** default value: 0100

Subaddress 22h		
D7-D4	TNRS4C [FP-TNR]	**TNR Curve Characteristic of Chroma Segment 4** default value: 0100
D3-D0	TNRS5C [FP-TNR]	**TNR Curve Characteristic of Chroma Segment 5** default value: 0100

Subaddress 23h		
D7-D4	TNRS6C [FP-TNR]	**TNR Curve Characteristic of Chroma Segment 6** default value: 0000
D3-D0	TNRS7C [FP-TNR]	**TNR Curve Characteristic of Chroma Segment 7** default value: 0000

Subaddress 24h		
D7-D4	TNRCLY [FP-TNR]	**TNR Luminance Classification** ’0000’: strong noise reduction ’1111’: slight noise reduction
D3-D0	TNRCLC [FP-TNR]	**TNR Chrominance Classification** ’0000’: strong noise reduction ’1111’: slight noise reduction

Subaddress 25h		
D7-D0	IICINCR18-11 [PP]	**Set HDTO frequency** Granularity=103 Hz 33981_d (minimum: nominal pixel clock= 3.5 MHz) 349525_d (nominal pixel clock= 36 MHz) 388362_d (maximum: nominal pixel clock= 40 MHz)

Subaddress 26h		
D7-D0	IICINCR10-3 [PP]	belongs to 25h

Subaddress 27h		
D3	DISRES [PP]	**Reset of LL-PLL watchdog** '0': reset disabled '1': reset enabled
D2-D0	IICINCR2-0 [PP]	belongs to 25h

Subaddress 28h		
D0	HRES [PP]	**Reset of LL-HPLL** '0':no reset '1':reset *Note: reset automatically when written*

Subaddress 29h		
D7-D5	HSWIN [PP]	**Width of Noise Suppression Window of LL-HPLL** '000':+/-28µs '001':+/-24µs '010':+/-20µs '011':+/-16µs '100':+/-12µs '101':+/-8µs '110':+/-4µs '111':dynamic windowing. *Note: If PPLIP<269$_d$ (=1076 pixel) only '101' or '110' are allowed*
D4	SETSTABLL [PP]	**Stability Signal of LL_HPLL** '0': STABLL is generated by the HPLL '1': STABLL is forced to 1
D3	KD2 [PP]	**Phase Detector Steepness** '0': steepness for normal TV operation mode '1': steepness for operations where PPLIP is less than 288$_d$
D2	HINCREXT [PP]	**HDTO testmode** '0': normal mode '1': line-locked-clocks derived from frontend line-length
D1	LMOD [PP]	**Selects line locked mode** '0': line locked-clocks derived from HPLL '1': line-locked-clocks derived from frontend line-length
D0	FMOD [PP]	**Selects freerun mode** '0': freerun-clocks derived from crystal '1': freerun-clocks derived from HDTO *Note: Adjustable frequency is only possible when set to '1'. When set to '0', Backend clock is always 36 MHz (9432/42: 18MHz)*

Subaddress 2Ah		
D7-D6	KOIWID [PP]	**Window-Width of coincidence detector** '00': +/- 32 pixel (= +/- 0.9µs for TV application) '01': +/- 64 pixel (= +/- 1.8µs for TV application) '10': +/- 128 pixel (= +/- 3.6µs for TV application) '11': +/- 256 pixel (= +/- 7.2µs for TV application)
D5-D4	KOIH [PP]	**Hysteresis of coincidence detector** '00': 0 lines '01': 8 lines '10': 16 lines '11': 32 lines
D3-D0	HTESTW [PP]	**Test bits for HPLL** 00: default

Subaddress 2Bh		
D7-D0	PPLIP9-2 [PP]	**Pixel per Line Input (Input-Processing)** Granularity=4 pixel '175_d': 700 (minimum) '576_d': 2304 '963_d': 3852 (maximum)

Subaddress 2Ch		
D1-D0	PPLIP1-0 [PP]	belongs to 2Bh

Subaddress 2Dh		
D7-D4	FION [PP]	**Increment Freeze before V-sync** '0': no freeze '15': freeze starts 15 lines before V-sync
D0	LNL [PP]	**Dynamic Time Constant Control** '0': linear mode '1': non linear mode

Subaddress 2Eh		
D7-D6	CLKT [PP]	**Switch clkf20 and clkf40 to pads *cvbs1* or *bin2* (test only)** '00': no clock '01': cvbs1 is output of clkf40 '10': *bin2* is output of clkf20 '11': *cvbs1* is output of clkf40 and *bin2* is output of clkf20
D5	HWID [PP]	**Minimum width of H-sync** '0': $60*T_{clkllf36}$ '1': $15*T_{clkllf36}$
D4	HDTOTEST [PP]	**Test-bit for HPLL** '0': normal mode '1': test mode
D3-D0	FILE [PP]	**Increment Freeze duration** '0': no freeze '15': increment is frozen for 15 lines

Subaddress 30h		
D7-D6	YCOR [BP-DP]	**Luminance Coring** '00': off '01': 2 '10': 4 '11': 8
D5	CLKOUTON [BP-DP]	**clkout Pad:** '0': off (tristate) '1': on
D4-D2	THRESHC [BP-DP]	**Slope of DCTI function** '000': 255 (DCTI off) '001': 2 '010': 3 '011': 4 '100': 6 '101': 8 '110': 10 '111': 12
D1-D0	ASCENTCTI [BP-DP]	**Gain of DCTI function** '00': 1/4 '01': 1/2 '10': 1 '11': 2

Subaddress 31h		
D7-D4	HCOF [BP-DP]	**Peaking: High-Pass Filter Adjustments** '0000': 0 '0001': 1/4 ... '0100': 1 ... '1100': 12/4 '1101': 14/4 '1110': 16/4 '1111': 20/4
D3-D0	BCOF [BP-DP]	**Peaking: Band-Pass Filter Adjustments** '0000': 0 '0001': 1/4 ... '0100': 1 ... '1100': 12/4 '1101': 14/4 '1110': 16/4 '1111': 20/4

Subaddress 32h		
D7-D6	AUTOFRRN [BP-DP]	**Automatic freerun** when sync-separartion not stable '00': disabled (keep H/V locked, if selected) '01': use vertical freerun '10': use horizontal freerun '11': use horizontal and vertical freerun
D5-D4	ALPFOP9-8 [BP-DP]	**Active Lines Per Field Output** '0000000000': 0 (minimum) '0100100000': 288 (default) '1111111111': 1023 (maximum)

Subaddress 32h		
D3	FINEDEL [BP-DP]	**Luminance Fine Delay output** '0': no delay '1': +1 CLKB72 (13.9 ns for TV signal)
D2-D0	COARSEDEL [BP-DP]	**Luminance Coarse Delay output** Granularity: 1 CLKB36 (27.8 ns for TV signal) '000': -4 CLKB36 '100': no delay '111': +3 CLKB36

Subaddress 33h		
D7-D0	ALPFOP7-0 [BP-PM]	belongs to 32h

Subaddress 34h		
D7-D0	BORDPOSV [BP-PM]	**Borderposition Vertical** Granularity: 2 lines '00000000': no border '11111111': border at 512 lines at top and bottom

Subaddress 35h		
D7-D0	BORDPOSH7 -0 [BP-PM]	**Borderposition Horizontal** Granularity: 2 pixel '0000000000': no border '1111111111': border at 2048 pixel on left and right

Subaddress 36h		
D7	BLANPOL [BP-PM]	**Blanking signal polarity** '0': active high '1': active low
D6	BLANEN [BP-PM]	**Blanking signal enable** '0': disabled (pin 8 can be used as 656vin) '1': enabled
D5-D4	BORDPOSH 9-8 [BP-PM]	belongs to 35h
D3-D0	YBORDER [BP-PM]	**Luminance Value for Border** '0000':sub black '0001':black '1111':white

Subaddress 37h		
D7-D4	UBORDER [BP-PM]	**Chrominance (U) Value for Border** '1000': '0000': 'no color' U '0111':
D3-D0	VBORDER [BP-PM]	**Chrominance (V) Value for Border** '1000': '0000': 'no color' V '0111':

Subaddress 38h		
D7-D0	HORWIDTH7-0 [BP-PM]	**Horizontal Picture Width** Granularity: 2 pixel '00000000000': no display '00111100000': 960 pixel '11111111111': 4094 pixel *Note: Should be set equal to APPLOP (3Dh)*

Subaddress 39h		
D7-D6	WINDVSP [BP-PM]	**Vertical Windowing: Speed** '00': slow '01': medium '10': fast '11': very fast
D5	WINDVST [BP-PM]	**Vertical Windowing: Start** '0': window is closed '1': window is open
D4	WINDVDR [BP-PM]	**Vertical Windowing: Direction** '0': open the vertical window '1': close the vertical window
D3	WINDVON [BP-PM]	**Vertical Windowing: Enable** '0': off '1': on
D2-D0	HORWIDTH 10-8 [BP-PM]	belongs to 38h

Subaddress 3Ah		
D7-D0	HORPOS7-0 [BP-PM]	**Horizontal Position inside active picture area** Granularity: 2 pixel '00000000000': most left display position '11111111111': most right display position

Subaddress 3Bh		
D7-D6	WINDHSP [BP-PM]	**Horizontal Windowing: Speed** '00': slow '01': medium '10': fast '11': very fast
D5	WINDHST [BP-PM]	**Horizontal Windowing: Start** '0': window is closed '1': window is open
D4	WINDHDR [BP-PM]	**Horizontal Windowing: Direction** '0': open the horizontal window '1': close the horizontal window
D3	WINDHON [BP-PM]	**Horizontal Windowing: Enable** '0': off '1': on
D2-D0	HORPOS10-8 [BP-PM]	belongs to 3Ah

Subaddress 3Ch		
D7	NOSYNC [BP-ODC]	**No horizontal synchronization** '0': horizontal synchronization '1': no horizontal synchronization
D6-D4	PPLOFF [BP-ODC]	**Synchronization offset** (for switching from hor. freerun mode to locked mode) Granularity: 4 pixel '000': 0 '010': 8 '111': 28
D3-D0	LPFOPFF [BP-ODC]	**Lines per field offset:** (for switching from vertical freerun mode to locked mode) Granularity: 2 lines '0000': 0 '0110':12 '1111':31

Subaddress 3Dh		
D7	CHRSHFT [BP-O/M]	**Chrominance Shift** shifts the chrominance signal '0': no shift '1': one line upward
D6-D0	APPLOP [BP-O/M]	**Active Pixel Per Line Output:** Granularity: 16 pixel '0000000': 0 pixel '0111100': 960 pixel '1111111': 2032 pixel

Subaddress 3Eh		
D7-D0	HOUTDEL7-0 [BP-ODC]	**H Sync output Delay:** Granularity: 4 pixel '0000000000':no delay '0000000001': 4 pixel delay '1111111111':4092 pixel delay

Subaddress 3Fh		
D7-D6	NAPPLOP9-8 [BP-O/M]	**Not Active Pixel Per Line Output:** Granularity: 4 pixel '0000000100': 16 not active pixel '1111111111': 4092 not active pixel
D5	PDGSR [BP-O/M]	**Switch for Vsync transfer algorithm:** '0': Vsync transfer algorithm is enabled '1': Vsync transfer algorithm is disabled
D4	FREEZE [BP-O/M]	**Freeze picture** '0': live '1': frozen (data writing disabled)
D3-D2	STOPMODE [BP-O/M]	**Operation mode for scan rate conversion:** '00': AABB (Raster $\alpha\alpha\beta\beta$) '01': AAAA (Raster $\alpha\alpha\alpha\alpha$) '10': AAAA (Raster $\alpha\beta\alpha\beta$) '11': BBBB (Raster $\beta\beta\beta\beta$)
D1-D0	HOUTDEL9-8 [BP-O/M]	belongs to 3Eh

Subaddress 40h		
D7-D0	NAPPLOP7-0 [BP-ODC]	belongs to 3Fh

Subaddress 41h		
D7-D6	PPLOP9-8 [BP-O/M]	**Pixel Per Line Output:** Granularity:4 '0000000000': 0 pixel '0100100000': 1152 pixel '1111111111': 4092 pixel
D5	REFRPER [BP-O/M]	**Refresh period of the memory** '0': ~5 ms '1': ~2,5 ms
D4	REFRON [BP-O/M]	**Refresh on** '0': no memory refresh '1': memory refresh active
D3	HOUTPOL [BP-O/M]	**HOUT polarity:** '0': high active '1': low active
D2	VOUTPOL [BP-O/M]	**VOUT polarity:** '0': high active '1': low active
D1	HOUTFR [BP-O/M]	**HOUT freerun** '0': locked mode '1': freerun mode
D0	VOUTFR [BP-O/M]	**VOUT freerun** '0': locked mode '1': freerun mode

Subaddress 42h		
D7-D0	PPLOP7-0 [BP-O/M]	belongs to 41h

Subaddress 43h		
D7-D0	LPFOP7-0 [BP-ODC]	**Lines Per Field Output:** Only used for freerun mode Granularity: 2 lines '000000000': no lines '010011100': 312 lines '111111111:' 1022 lines

Subaddress 44h		
D7-D0	OPDEL7-0 [BP-ODC]	**V delay for output operation:** '000000000': no delay '010101010': 170 lines '111111111': 511 lines

Subaddress 45h		
D7-D6	BORDERV [BP-O/M]	**Border V** '00': both borders are displayed '01': only lower border is displayed '10': only upper border is displayed '11': (reserved)

Subaddress 45h		
D5-D4	BORDERH [BP-O/M]	**Border H** '00': both borders are displayed '01': only right border is displayed '10': only left border is displayed '11': (reserved)
D3	RDCTRLDIS [BP-O/M]	**Memory read control circuit disable** '0': enabled '1': disabled
D2	LPFOP8 [BP-O/M]	belongs to 43h
D1	NALPFOP8 [BP-O/M]	**Not Active Lines Output** NALPFOP-1 lines are not active lines. '000000001':all lines active '000011001':24 lines not active '111111111':510 lines not active
D0	OPDEL8 [BP-O/M]	belongs to 44h

Subaddress 46h		
D7-D0	NALPFOP7-0 [BP-ODC]	belongs to 45h

Subaddress 47h		
D6-D5	PALDEL [CP-CD]	**PAL/NTSC delay vs. SECAM (chrominance)** '00': PAL/NTSC most left '11': PAL/NTSC most right

Subaddress 47h		
D4-D3	LOCKSP [CP-CD]	**Duration Of Chroma PLL Search** ’00’: 25 fields ’01’: 20 fields ’10’: 17 fields ’11’: 15 fields
D2-D0	BGPOS [CP-CD]	**Burstgate Delay (SECAM only)** Granularity: 200 ns ’000’: most left (-400 ns) ’011’: 200 ns delay ’111’: most right (+1 us)

Subaddress 48h		
D7-D0	HINC0_7-0 [BP-POS]	**Horizontal Post-Scaler Increment 0** ’100000000’: -32 pixel ’000000000’: 0 pixel ’011111111’:31.875 pixel

Subaddress 49h		
D7-D0	HINC1_7-0 [BP-POS]	**Horizontal Post-Scaler Increment 1** ’100000000’: -32 pixel ’000000000’: 0 pixel ’011111111’:31.875 pixel

Subaddress 4Ah		
D7-D0	HINC2_7-0 [BP-POS]	**Horizontal Post-Scaler Increment 2** ’100000000’: -32 pixel ’000000000’: 0 pixel ’011111111’:31.875 pixel

Subaddress 4Bh		
D7-D0	HINC3_7-0 [BP-POS]	**Horizontal Post-Scaler Increment 3** ’100000000’: -32 pixel ’000000000’: 0 pixel ’011111111’:31.875 pixel

Subaddress 4Ch		
D7-D0	HINC4_7-0 [BP-POS]	**Horizontal Post-Scaler Increment 4** ’100000000’: -32 pixel ’000000000’: 0 pixel ’011111111’:31.875 pixel

Subaddress 4Dh		
D4	HINC4_8 [BP-POS]	belongs to 4Ch
D3	HINC3_8 [BP-POS]	belongs to 4Bh

Subaddress 4Dh		
D2	HINC2_8 [BP-POS]	belongs to 4Ah
D1	HINC1_8 [BP-POS]	belongs to 49h
D0	HINC0_8 [BP-POS]	belongs to 48h

Subaddress 4Eh		
D7-D0	HSCPOSC7-0 [BP-POS]	**Horizontal Scaling Factor For Post Scaler** ’010000000000’: factor is 4 ’101101010101’: factor is 1.407 (682 -> 960) ’110000000000’: factor is 4/3 (720 -> 960) ’111111111111’: factor is 1

Subaddress 4Fh		
D4	HPANON [BP-POS]	**Panorama Mode enable** ’0’: panorama mode disabled ’1’: panorama mode enabled
D3-D0	HSCPOSC 11-8 [BP-POS]	belongs to 4Eh

Subaddress 50h		
D7-D0	HSEG1_7-0 [BP-POS]	**Beginning of Segment 1 for Panorama Mode** Granularity: 2 pixel '00000000000': 0 pixel behind picture start '11111111111': 4094 pixel behind picture start

Subaddress 51h		
D7-D0	HSEG2_7-0 [BP-POS]	**Beginning of Segment 2 for Panorama Mode** Granularity: 2 pixel '00000000000': 0 pixel behind picture start '11111111111': 4094 pixel behind picture start

Subaddress 52h		
D7-D0	HSEG3_7-0 [BP-POS]	**Beginning of Segment 3 for Panorama Mode** Granularity: 2 pixel '00000000000': 0 pixel behind picture start '11111111111': 4094 pixel behind picture start

Subaddress 53h		
D7-D0	HSEG4_7-0 [BP-POS]	**Beginning of Segment 4 for Panorama Mode** Granularity: 2 pixel '00000000000': 0 pixel behind picture start '11111111111': 4094 pixel behind picture start

Subaddress 54h		
D7	FIOFFOFF [BP-POS]	**Fieldoffset for ITU656 NTSC signals** '0': disabled '1': enabled
D6	FIELDBINV [BP-POS]	**Backend field inversion** '0': no inversion '1': inversion
D5-D3	HSEG2_10-8 [BP-POS]	belongs to 51h
D2-D0	HSEG1_10-8 [BP-POS]	belongs to 50h

Subaddress 55h		
D7	CHRMSIG656 [BP-POS]	**Chrominance format for 656 output** '0': (R-Y), (B-Y) output '1': -(R-Y), -(B-Y) output
D6	VDEL_EN [BP-POS]	**Vertical pulse delay backend (test only)** '0': no delay '1': delayed
D5-D3	HSEG4_10-8 [BP-POS]	belongs to 53h
D2-D0	HSEG3_10-8 [BP-POS]	belongs to 52h

Subaddress 56h		
D7	SHIFTUV [BP-DAC]	**Shift UV subsampling at digital output** '0': take first UV couple '1': take second UV couple *Note: VSP9432/42 only*
D6	ENABLE656 [BP-DAC]	**Enable digital 656 Output** '0': disable output '1': enable output *Note: VSP9432/42 only*
D5-D0	OFFSETDY [BP-DAC]	**Offset Voltage for Y DAC** '000000': low offset '111111': high offset *Note: Should be set to 0, when backend is AC coupled to 94x2A*

Subaddress 57h		
D7	CHROMSIGN [BP-DAC]	**Chrominance sign** '0': (R-Y), (B-Y) output '1': -(R-Y), -(B-Y) output
D6	CHROMAMP [BP-DAC]	**Chrominance amplification** '0': amplification = 1 '1': amplification = 2
D5-D0	OFFSETDUV [BP-DAC]	**Offset Voltage for UV DAC** '000000': low offset '111111': high offset *Note: Should be set to 0, when backend is AC coupled to 94x2A*

Subaddress 58h		
D7-D0	PKLY [BP-DAC]	**Voltage Level for Y DAC Output** ’00000000’: 0.4 V ’10000000’: 1.0 V ’11111111’: 1.9 V *Note: including peaking overshoots. 0.9V for white max.*

Subaddress 59h		
D7-D0	PKLU [BP-DAC]	**Voltage Level for U DAC Output** ’00000000’: 0.4 V ’10000000’: 1.0 V ’11111111’: 1.9 V

Subaddress 5Ah		
D7-D0	PKLV [BP-DAC]	**Voltage Level for V DAC Output** ’00000000’: 0.4 V ’10000000’: 1.0 V ’11111111’: 1.9 V

Subaddress 5Bh		
D7-D5	CONS [CP-CD]	**Color Switched On (SECAM)** at level=CKILLS+CONS ’000’: min value ’010’: default ’111’: max value

Subaddress 5Bh		
D4	COLON [CP-CD]	**Force Color On** '0': color depends on color decoder status '1': color always on
D3	CPLLOF [CP-CD]	**Chroma PLL Open** '0': normal operation '1': chroma PLL opened
D2	CRCB [CP-CD]	**UV Or CrCb Output** '0': UV color space '1': CrCb color space
D1	ACCFIX [CP-CD]	**Fix ACC to Nominal Value** '0': ACC is working '1': ACC is fixed
D0	ACCFRZ [CP-CD]	**Freeze ACC** '0': ACC is working '1': ACC is frozen

Subaddress 5Ch		
D7-D5	CON [CP-CD]	**Color Switched On (PAL/NTSC)** at level=CKILL+CON '000': min value '010': default '111': max value
D4-D3	UVCOR [CP-CD]	**Chrominance coring** '00': off '01':+/- 1LSB '10':+/- 2LSB '11':+/- 3LSB
D2	NOTCHOFF [CP-CD]	**Luminance notch-filter** '0': notch-filter enabled '1': notch-filter bypassed

Subaddress 5Ch		
D1-D0	SECNTCH [CP-CD]	**Selection of Notch filter behavior in SECAM mode** '00':4.406 MHz '01':4.250 MHz '10':4.33 MHz '11':4.406 / 4.25 dependent on transmitted color

Subaddress 5Dh		
D7-D6	PWTHD [CP-CD]	**Selection Of 'Peak-White' Threshold** '00': 442 (e.g. for PAL / SECAM) '01': 433 (e.g. for NTSC sync-tip clamping) '10': 448 (e.g. for NTSC back-porch clamping) '11': 511
D5-D4	CLRANGE [CP-CD]	**Chroma lock-range** '00':+/- 425 Hz '01':+/- 463 Hz '10':+/- 505 Hz '11':+/- 550 Hz
D3-D2	LMOFST [CP-CD]	**Luminance Offset in color decoder during visible picture** '00':no offset '01':-32 LSB (- 7.5 IRE) '10':+32 LSB (+ 7.5 IRE) '11':-16 LSB (- 3.75 IRE) *Note: A 7.5 IRE offset is added during blanking in display processing. When choosing '10', the luminance offset is equal to the offset of the CVBS input as in both picture and blanking the same 7.5 IRE offset is used.*
D1	VDETIFS [CP-CD]	**Vertical Sync-Detection Slope** '0': normal '1': slow

Subaddress 5Dh		
D0	VDETITC [CP-CD]	**Vertical Sync-Detection Integration Time Constant** '0': long '1': short

Subaddress 5Eh		
D7-D6	DEEMPIIR [CP-CD]	**Deemphase filter IIR component** '00':5 '01':6 '10':7 '11':8
D5-D0	CHRF [CP-CD]	**Chroma Bandwidth** selects chroma bandwidth '011100': nominal bandwidth

Subaddress 5Fh		
D7	COMB [CP-CD]	**Delay Line** '0':use delay line '1':do not use delay line (only suited for NTSC)
D6-D0	CSTAND [CP-CD]	**Color Standard Assignment** '0000000': no color standard chosen '0000001':PAL N '0000010':PAL B '0000100':SECAM '0001000':PAL 60 '0010000':PAL M '0100000':NTSC M '1000000':NTSC 44 For allowed combinations please refer to chapter "Chroma Decoder" on page 5-22 '1100110': PALB/SECAM/NTSCM/NTSC44/PAL60

Subaddress 60h		
D7-D0	CKILL [CP-CD]	**Chroma Level For Color Off (PAL/NTSC)** ’00000000’: high burst amplitude ’01000000’: default ’11111111’: low burst amplitude

Subaddress 61h		
D7-D0	CKILLS [CP-CD]	**Chroma Level For Color Off (SECAM)** ’00000000’: low burst amplitude ’01000000’: default ’11111111’: high burst amplitude

Subaddress 62h		
D7-D6	VPOL [CP-CD]	**V Polarity at VINP** ’00’: use Vsync ’01’: use inverted Vsync ’10’: autodetect polarity ’11’: (reserved)
D5	LPPOST [CP-CD]	**Additional Filtering of Luminance** ’0’: no filtering ’1’: filtering
D4-D0	YCDEL [CP-CD]	**Luminance Delay** ’10000’: 800 ns ’0000’: no delay ’01111’: -700 ns

Subaddress 63h		
D7-D0	HUE [CP-CD]	**Hue Control (Tint)** ’10000000’: -89° ’00000000’: 0° ’01111111’: +88°

Subaddress 64h		
D7-D0	NTSCREF [CP-CD]	**ACC Reference Adjustment (NTSC)** ’00000000’: low reference value ’10100101’: nominal value ’11111111’: high reference value

Subaddress 65h		
D7-D0	PALREF [CP-CD]	**ACC Reference Adjustment (PAL)** ’00000000’: low reference value ’01011111’: nominal value ’11111111’: high reference value

Subaddress 66h		
D7-D6	SLLTHD [CP-CD]	**Slicing Level Threshold H** ’00’:no offset ’01’:small negative ’10’:small positive ’11’:large positive (adaptive)

Subaddress 66h		
D5-D0	SCADJ [CP-CD]	**Subcarrier Adjustment** ’000000’:-262 ppm ’001111’: 0 ppm ’111111’: 840 ppm

Subaddress 67h		
D7-D6	AGCMD [CP-CD]	**AGC method** ’00’:sync amplitude and peak white ’01’:sync amplitude only ’10’:peak white only ’11’:fixed to value AGCADJ1
D5-D0	AGCADJ1 [CP-CD]	**Automatic Gain Adjustment ADC1** ’000000’: 0.6 V input signal ’111111’: 1.8 V input signal

Subaddress 68h		
D7	AGCRES [CP-CD]	**AGC reset** ’0’: no reset ’1’: reset
D6	AGCFRZE [CP-CD]	**freeze AGC (ADC_CVBS)** ’0’: normal operation ’1’: freeze AGC at current value
D5-D0	AGCADJ2 [CP-CD]	**Automatic Gain Adjustment ADC2** ’000000’: 0.6 V input signal ’111111’: 1.8 V input signal

Subaddress 69h		
D7-D0	CLMPHIGH [CP-CD]	**Vertical End Of Clamping Pulse** Granularity:2 ’00000000’:line 256 ’00111100’:line 376 ’11111111’: line 766

Subaddress 6Ah		
D7-D4	CVBOSEL1 [CP-CD]	**Output select 1 for pin cvbso1** ’0000’:CVBS1 ’0001’:CVBS2 ’0010’:CVBS3 ’0011’:CVBS4 or Y1 ’0100’:CVBS5 or C1 ’0101’:CVBS6 or Y2 ’0110’:CVBS7 or C2 ’0111’:Y1 + C1 ’1000’:Y2 + C2
D3-D0	CLMPLOW [CP-CD]	**Vertical Start Of Clamping Pulse** ’0000’:line 0 ’0011:line 6 ’1111’: line30

Subaddress 6Bh		
D7	FLINE [CP-CD]	**Mode Selection** ’0’: interlace input ’1’: progressive input

Subaddress 6Bh		
D6	FLDINV [CP-CD]	**Field Inversion** '0': no inversion '1': inversion
D5	CLPSTGY [CP-CD]	**Clamping strategy** '0': back-porch clamping '1': sync-tip-clamping
D4	YCSEL [CP-CD]	**Y/C select** '0': CVBS input '1': Y/C input
D3-D0	CLMPD1 [CP-CD]	**Measurement duration ADC1** Granularity: 200ns '0000': 0 us '0111': 1.4 us '1111': 3 us

Subaddress 6Ch		
D7-D6	HPOL [CP-CD]	**H Polarity at HINP** '00': use Hsync '01': use inverted Hsync '10': autodetect polarity '11': (reserved)
D5	FHDET [CP-CD]	**Automatic Multisync capability** '0':disabled '1':enabled
D4	DISCHCH [CP-CD]	**Channel-change signal for color decoder** '0':color-decoder not reset after channel-change '1':color-decoder reset after channel-change

Subaddress 6Ch		
D3-D0	CLMPD2 [CP-CD]	**Measurement duration ADC2** Granularity: 200 ns '0000':0 us '0111':1.4 us '1111: 3 us

Subaddress 6Dh		
D7	NOSIGB [CP-CD]	**No signal behavior** '0':noisy screen when out of sync '1':colored background insertion instead
D6	HINP [CP-CD]	**Horizontal Pulse Detection** '0': from CVBS ADC1 '1': from RGBF ADC
D5-D0	CLMPST1 [CP-CD]	**Measurement start ADC1** '000000':0 us '011100':5.6 us '111111: 12.8 us

Subaddress 6Eh		
D7-D6	PLLTC [CP-CD]	**time constant HPLL (VCR...TV)** '00':very fast '01':fast '10':slow '11':very slow
D5-D0	CLMPST2 [CP-CD]	**Measurement start ADC2** '000000':0 us '011100':5.6 us '111111: 12.8 us

Subaddress 6Fh		
D7-D4	CVBSEL2 [CP-CD]	**Input select for ADC2** '0000': CVBS1 '0001': CVBS2 '0010': CVBS3 '0011': CVBS4 or Y1 '0100': CVBS5 or C1 '0101': CVBS6 or Y2 '0110': CVBS7 or C2 '0111': Y1 + C1 '1000': Y2 + C2 '1111':disabled
D3-D0	CVBSEL1 [CP-CD]	**Input select for ADC1** '0000': CVBS1 '0001': CVBS2 '0010': CVBS3 '0011': CVBS4 or Y1 '0100': CVBS5 or C1 '0101': CVBS6 or Y2 '0110': CVBS7 or C2 '0111': Y1 + C1 '1000': Y2 + C2 '1111':disabled

Subaddress 70h		
D7-D4	CVBOSEL2 [CP-CD]	**Output select for pin cvbso2** '0000': CVBS1 '0001': CVBS2 '0010': CVBS3 '0011': CVBS4 or Y1 '0100': CVBS5 or C1 '0101': CVBS6 or Y2 '0110': CVBS7 or C2 '0111': Y1 + C1 '1000': Y2 + C2
D3-D0	CVBOSEL3 [CP-CD]	**Output select for pin cvbso3** '0000': CVBS1 '0001': CVBS2 '0010': CVBS3 '0011': CVBS4 or Y1 '0100': CVBS5 or C1 '0101': CVBS6 or Y2 '0110': CVBS7 or C2 '0111': Y1 + C1 '1000': Y2 + C2

Subaddress 71h		
D7-D0	FHFRRN [CP-CD]	**Free Running Frequency Of Horizontal PLL** '00000000': 384 clocks (52.7 kHz) '11100100': 1296 clocks (15.625 kHz) '11111111': 1404 clocks (14.423 kHz)

Subaddress 72h		
D7	REFTRIMEN [CP-CD]	**Reference Value enable** '0': use fuses '1': uses programmed value
D6	SATNR [CP-CD]	**Noise reduction for satellite signal** '0': disabled '1:' enabled
D5	VINP [CP-CD]	**Vertical Pulse Detection** '0': from CVBS signal '1': from V-input pin
D4-D3	NSRED1-0 [CP-CD]	**Noise Reduction For Horizontal PLL** '000': 1/16 '001': 1/8 '010': 1/4 '011': 1/2 '100': 1 '101': 2 '110': 4 '111: 8 *Note: MSB is at address 7Eh, D2*
D2-D0	LPCDEL [CP-CD]	**Window Shift For Fine Error Calculation** '100': -4 clock cycles '000': no offset '011': +3 clock cycles

Subaddress 73h		
D7-D0	VSHIFT [CP-CD]	**Field Detection Window Shift** '00000000': no shift '11111111': shifted by 2048

Subaddress 74h		
D7	PALIDL1 [CP-CD]	**PAL/NTSC Identification Level 1** '0': less sensitive '1': more sensitive
D6-D0	VTHRL [CP-CD]	**Vertical Window Noise Suppression Opening** Granularity:4 '0000000': opening in first line '1111111': opening in line 508

Subaddress 75h		
D7	PALIDL0 [CP-CD]	**PAL/NTSC Identification Level 0** '0': less sensitive '1': more sensitive
D6-D0	VTHRH [CP-CD]	**Vertical Window Noise Suppression Closing** Granularity:4 Closing=262+4*VTHRH (60 Hz detected) Closing=312+4*VTHRH (50 Hz detected) '0000000':closing in line 262/312 '1111111': closing in line 770/820 *Note: Window is limited to 340 (50Hz) or 290 (60Hz). Full range is only possible when VINP (72h) is set.*

Subaddress 76h		
D7-D0	REFTRIM [CP-CD]	**Reference Value Bandgap** '01000000': low reference '00000000': medium reference '01111111': high reference '1XXXXXXX': reference disabled, resistor used

Subaddress 77h		
D7-D4	REFTRIMCV [CP-CD]	**Reference Value ADC CVBS (antialiasfilter)** '0000': narrow '1111': wide
D3-D0	REFTRIMRGB [CP-CD]	**Reference Value ADC RGBF (antialiasfilter)** '0000': narrow '1111': wide

Subaddress 78h		
D7	SLLTHDVP [CP-CD]	**Vertical Slicing Level Threshold Polarity** '0':positive '1':negative
D6	THRSEL [CP-CD]	**Slicing level threshold generation** '0':slow '1':fast
D5-D0	CLMPST1S [CP-CD]	**Clamping start for ADC1** '000000':0 us '011100':5.6 us '111111: 12.8 us

Subaddress 79h		
D7-D6	SCMIDL [CP-CD]	**SECAM identification level** '00':128 '01':64 '10':96 '11':80

Subaddress 79h		
D5-D0	CLMPST2S [CP-CD]	**Clamping start ADC2** ’000000’:0 us ’011100’:5.6 us ’111111: 12.8 us

Subaddress 7Ah		
D7-D3	ACCLIM [CP-CD]	**ACC-limitation for weak signals** ’00000’: strong limitation ’11111’: no limitation
D2-D0	IFCOMP [CP-CD]	**IF compensation filter** ’000’:pal prefiltering ’001’:pal prefiltering + IF ’010’:prefiltering ’011’:IF 6dB ’100’:flat *Note: ’000’ or ’001’ are not suited for 3.58MHz subcarrier color standards (PAL M, PAL N, NTSC M)*

Subaddress 7Bh		
D7-D4	CLMPD2S [CP-CD]	**Clamping duration for ADC2** Granularity: 200 ns ’0000’:0 us ’0111’:1.4 us ’1111: 3.2 us
D3-D0	CLMPD1S [CP-CD]	**Clamping duration for ADC1** Granularity: 200 ns ’0000’:0 us ’0111’:1.4 us ’1111: 3.2 us

Subaddress 7Ch		
D7-D6	SLLTHDV [CP-CD]	**Vertical Slicing Level Threshold** '00':no offset '01':8 '10':16 '11':adaptive (max. 24) *Note: polarity is selected by **SLLTHDVP** (78h)*
D5	EIA770 [CP-CD]	**EIA 770 support** '0': standard TV signals expected '1': progressive signals expected *Note: timing according to EIA 770.1 or EIA 770.2 when '1'*
D4	SHAPERDIS [CP-PP]	**Power Down Of Crystal Oscillator Shaper** '0': normal operation '1': power down active
D3	OSCPD [CP-PP]	**Power Down Of Crystal Oscillator Amplifier** '0': normal mode '1': power down mode
D2	TSTSHAPERI [CP-PP]	**Testmode Control Of Crystal Oscillator** '0': normal operation (shaper active) '1': external clock input (shaper replaced)
D1-D0	FREQSEL [CP-PP]	**Amplifier Current Setting Of Oscillator Pad** '00': 100 µA '01': 590 µA '10': 235 µA '11':1730 µA

Subaddress 7Dh		
D7-D5	DEEMPFIR [CP-CD]	**Deemphase filter FIR component** ’000’:18 ’011’:21 ’111’:25
D4-D3	BELLFIR [CP-CD]	**Bell filter FIR component** ’00’:116 ’01’:113 ’10’:110 ’11’:108
D2-D1	BELLIIR [CP-CD]	**Bell filter IIR component** ’00’:9 ’01’:10 ’10’:11 ’11’:12
D0	VFLYWHL [CP-CD]	**Vertical Flywheel** ’0’: disabled ’1’: enabled

Subaddress 7Eh		
D7-D6	FLNSTRD [CP-CD]	**Force line standard at CVBS/RGB frontend** ’00’: automatic ’01’: force 50 Hz ’10’: force 60 Hz ’11’: (reserved)
D5	ENLIM [CP-CD]	**Enable limiter** ’0’: disabled ’1’: enabled

Subaddress 7Eh		
D4-D3	ISHFT [CP-CD]	**I-adjustment for horizontal PLL** '00': *1 '01': *2 '10': *4 '11': *8
D2	NSRED2 [CP-CD]	belongs to 72h
D1-D0	VLP [CP-CD]	**Lowpass for vertical sync-separation** '00': none '01': weak '10': medium '11': strong

Subaddress 7Fh		
D7	SECACC [CP-CD]	**Secam acceptance** '0': disabled '1': enabled
D6	SECDIV [CP-CD]	**Secam Divider** '0': divide by 4 '1': divide by 2
D5-D4	SECINC1 [CP-CD]	**Secam increment 1** '00':2 '01':3 '10':4 '11':5
D3-D2	SECINC2 [CP-CD]	**Secam increment 2** '00':1 '01':2 '10':3 '11':4

Subaddress 7Fh		
D1-D0	SCMREL [CP-CD]	**Secam rejection level** ’00’:320 ’01’:384 ’10’:352 ’11’:1024

Subaddress 80h		
D7	**PORCNCL** [CP-CD]	**Reset control bit cancel** ’0’: no operation ’1’: reset ***POR*** bit (8Ch) *Note: after use, **PORCNCL** must be set to ’0’ again*
D6-D4	**NTCHSEL** [CP-CD]	**Luminance Notch selection** ’000’: sharp notch ’001’: medium 1 ’010’: medium 2 ’011’: broad notch ’100’: broad steep notch (PAL, SECAM only)
D3	CPLLRES [CP-CD]	**Force Chroma PLL reset** ’0’: no reset ’1’: reset chroma PLL *Note: after use, **CPLLRES** must be set to ’0’ again*
D2	DISALLRES [CP-CD]	**Disable all chroma resets** ’0’: resets allowed ’1’: resets disabled *Note: may only be used if ONE color standard is selected*
D1	TRAPBLU [CP-CD]	**Notchfrequency for 4,250 MHz** ’0’:4.25 MHz ’1’:4.2 MHz *Note: has only effect in SECAM mode*

Subaddress 80h		
D0	TRAPRED [CP-CD]	**Notchfrequency for 4,406 MHz** '0':4.406 MHz '1':4.356 MHz *Note: has only effect in SECAM mode*

Subaddress 81h		
D7	ADLCK [CP-CD]	**Additional lock-detection** '0':no used '1':used
D6	ADLCKSEL [CP-CD]	**Additional lock-detection selection** '0':PALID '1':PALDET
D5	ADLCKCC [CP-CD]	**Additional lock-detection color-killer** '0':do not use lock signal '1':use lock-signal
D4-D3	VFLYWHLMD [CP-CD]	**Vertical Flywheel Mode** '00': check for correct standard '01': 3 lines deviation allowed '10': 4 lines deviation allowed, no check for interlace '11': 5 lines deviation allowed, no check for interlace
D2	PALIDL2 [CP-CD]	**PAL/NTSC identifikation level 2** '0':less sensitive '1':more sensitive
D1-D0	**SECACCL** [CP-CD]	**Secam Acceptance level** '00':100 '01':84 '10':64 '11':32 *Note: must be enabled by **SECACC** (7Fh) to have an effect*

Subaddress 82h (no auto-increment)		
D2	DEEMPSTD [CP-CD]	**Deemphase Filtering For Standard Detection** '0': weak '1': strong
D1	PALINC1 [CP-CD]	**PAL/NTSC Detection: Increment 1** '0': +3 '1': +2
D0	PALINC2 [CP-CD]	**PAL/NTSC Detection: Increment 2** '0': -1 '1': -2

Subaddress 83h (Read-only)		
D0	FBLACTIVE [CP-I2C]	**Activity At FBL Input** '0': no activity '1': activity *Note: reset automatically when read*

Subaddress 84h (Read-only, no auto-increment))		
D4-D0	NOISEME [FP-TNR]	**Noise level of the input signal:** '00000': no noise '11110': strong noise '11111': strong noise or measurement failed *Note: no autoincrement possible*

Subaddress 85h (Read-only)		
D4	PFBL [FP-TNR]	**Indicates Overflow at FBL Input** '0': no overflow '1': overflow *Note: reset automatically when read*
D3	PG [FP-TNR]	**Indicates Overflow at GREEN Input** '0': no overflow '1': overflow *Note: reset automatically when read*
D2	PB [FP-TNR]	**Indicates Overflow at BLUE Input** '0': no overflow '1': overflow *Note: reset automatically when read*
D1	PR [FP-TNR]	**Indicates Overflow at RED Input** '0': no overflow '1': overflow *Note: reset automatically when read*
D0	NMSTATUS [FP-TNR]	**Indicates New Value of the Noise Measurement** 0: NOISEME has not been updated 1: New value of NOISEME available *Note: reset automatically when read*

Subaddress 86h (Read-only)		
D0	STABLL [PP]	**Shows LL-HPLL Lock Status** '0': LL_HPLL is not locked '1': LL_HPLL is locked

Subaddress 87h (Read-only)		
D1-D0	SMMIRROR [BP-O/M]	**Operation mode for scan rate conversion:** '00': AABB (Raster αααββ) '01': AAAA (Raster αααα) '10': AAAA (Raster αβαβ) '11': BBBB (Raster ββββ)

Subaddress 88h (Read-only)		
D7	DETHPOL [CP-CD]	**Detected Polarity Of HSync** '0': negative '1': positive
D6	DETVPOL [CP-CD]	**Detected Polarity Of V Sync** '0': negative '1': positive
D5-D3	STDET [CP-CD]	**Detected Color Standard** '000': non standard or standard not detected '001': NTSC M '010': PAL M '011': PAL60 / NTSC44 '100': non standard or standard not detected '101': PAL N '110': SECAM '111': PAL B/G
D2	SCOUTEN [CP-CD]	**SCDEV valid indication** '0': SCDEV not valid '1': SCDEV valid
D1	PALID [CP-CD]	**PAL identification (algorithm 1)** '0': not PAL '1': PAL

Subaddress 88h (Read-only)		
D0	CKSTAT [CP-CD]	**Colorkill status** '0': color off '1': color on

Subaddress 89h (Read-only)		
D7	LNSTDRD [CP-CD]	**Line Standard detection** '0': 60 Hz '1': 50 Hz
D6	INT [CP-CD]	**Interlace Detection** '0':progressive input '1':interlace input
D5-D0	SCDEV [CP-CD]	**Deviation Of Clock System or Color Carrier** '100000': max. negative deviation '000000': no deviation '011111': max. positive deviation

Subaddress 8Ah (Read-only)		
D7-D0	LPFLD [CP-CD]	**Nr. Of Lines Per Field (Input Signal)** '00000000': 129 lines or less '11111111': 383 lines or more LINES=***LPFLD***+129

Subaddress 8Bh (Read-only)		
D7-D0	NRPIXEL [CP-CD]	**Pixel number of input signal** Granularity: 4 '00000000': 384 or less '11111111': 1404 or more PIXEL=4*_**NRPIXEL**_+384

Subaddress 8Ch (Read-only)		
D7	POR [CP-CD]	**Reset indication** a reset at pin 24 (reset) sets _**POR**_. _**POR**_ is reset with _**PORCNCL**_ (80h) '0': no reset appeared '1': reset appeared
D2	STAB [CP-CD]	**Status of synchronization** '0': sync separation not locked '1': sync separation locked and stable
D0	PALDET [CP-CD]	**PAL identification (algorithm 2)** '0': not PAL '1': PAL

Subaddress 8Dh (Read-only)		
D7-D0	REFTRIMRD [CP-CD]	**Reference Value Bandgap** '01000000': low reference '00000000': medium reference '01111111': high reference '1XXXXXXX': reference disabled, resistor used *Note: contains fused value only when REFTRIMEN (72h)=0.*

Subaddress 8Eh (Read-only)		
D7-D4	REFTRIMCVRD [CP-CD]	**Reference Value CVBS ADC** '0000': narrow '1111': wide *Note: contains fused value only when REFTRIMEN (72h)=0.*
D3-D0	REFTRIMRGBRD [CP-CD]	**Reference Value RGB ADC** '0000': narrow '1111': wide *Note: contains fused value only when REFTRIMEN (72h)=0.*

Subaddress 8Fh (Read-only, NOT compatible to 940X family)		
D3	SLS [CP-I2C]	**Line Standard At Device Output** '0': 100 Hz '1': 50 Hz
D2-D0	VERSION [CP-I2C]	**Version Of VSP 94XX Family** '001': VSP 94x5B '010': VSP 94x2A '011': VSP 94x7B '101': VSP 94x9C others: reserved

Subaddress 96h (Read-only)		
D0	V40STAT [FP-I2C]	**V Status bit of 40.5 MHz domain** '0': New write or read cycle can start '1': No new write or read cycle can start

Subaddress 98h (Read-only)		
D0	V36BSTAT [BP-I2C]	**V Status bit of backend 36 MHz domain** '0': New write or read cycle can start '1': No new write or read cycle can start

Subaddress 99h (Read-only)		
D0	V20STAT [CP-I2C]	**V Status bit of 20.25 MHz domain** '0': New write or read cycle can start '1': No new write or read cycle can start

Subaddress A0h		
D7-D4	**KPNL** [PP]	**Proportional factor for loop filter if HPLL is not locked (KOI_HYS=0)** FACTOR_P=2^{KPNL-1} (if ***KPNL***>0) '0000': 0 '0001': 1 '0010': 2 '1111': 16384
D3-D0	KPL [PP]	**Proportional factor for loop filter if HPLL is locked (KOI_HYS=1)** FACTOR_P=2^{KPL-1} (if ***KPL***>0) '0000': 0 '0001': 1 '0010': 2 '1111': 16384

Subaddress A1h		
D7-D4	KINL [PP]	**Integrational factor for loop filter if HPLL is not locked (KOI_HYS=0)** FACTOR_I=2^{KINL-1} (if ***KINL***>0) ’0000’: 0 ’0001’: 1 ’0010’: 2 ’1111’: 16384
D3-D0	KIL [PP]	**Integrational factor for loop filter if HPLL is locked (KOI_HYS=1)** FACTOR_I=2^{KIL-1} (if ***KIL***>0) ’0000’: 0 ’0001’: 1 ’0010’: 2 ’1111’: 16384

Subaddress A2h		
D7-D0	LIMIP [PP]	**Limiter Control for P-part for increased dynamic range** LIMIT_P= +/- 16****LIMIP*** ’00000000’: +/-0 ’11111110’: +/- 4064 ’11111111’: no limitation

Subaddress A3h		
D7-D0	LIMII [PP]	**Limiter Control for I-part for increased dynamic range** LIMIT_I= +/- 16****LIMII*** ’00000000’: +/- 0 ’11111110’: +/- 4064 ’11111111’: no limitation

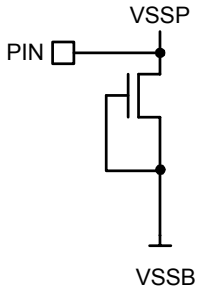
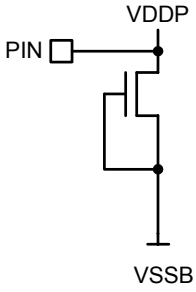
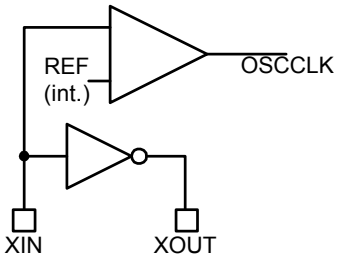
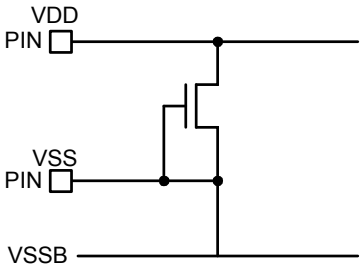
Subaddress A4h		
D7	FKOI [PP]	**Force Coincidence Bit** '0': coincidence bit dynamically changed '1': coincidence bit forced to 1
D6	FKOIHYS [PP]	**Force coincidence hysteresis bit** '0': coincidence hysteresis bit dynamically changed '1': coincidence hysteresis bit forced to 1
D2-D0	LIMLR [PP]	**Limit LL-PLL lock-in range** '000': full lock-in range of +/- 4.6% '001': limited to +/- 3% '010': limited to +/- 2% '011': limited to +/- 1% '100': limited to +/- 0.5% '101': limited to +/- 0.25% '110': limited to +/- 0.15% '111': limited to +/- 0.1%

Subaddress F6h (Read-only, compatible to 940X family)		
D7-D5	VERSION [CP-I2C]	**Version Of VSP 94XX Family:** '001': VSP 94x5B '010': VSP 94x2A '011': VSP 94x7B '101': VSP 94x9C others: reserved
D4	SLS [CP-I2C]	**Line Standard At Device Output** '0': 100 Hz (VSP 94xx) '1': 50 Hz (VSP 94xxS)
D3-D1	REV [CP-I2C]	**Revision of 9402(S)** '000': A23 or below '001': A31 or A32

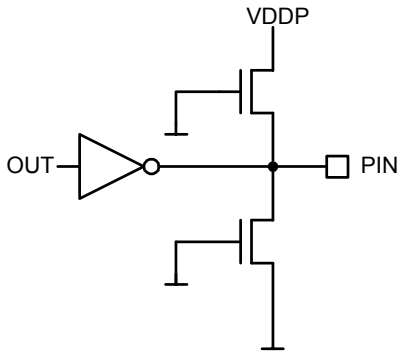
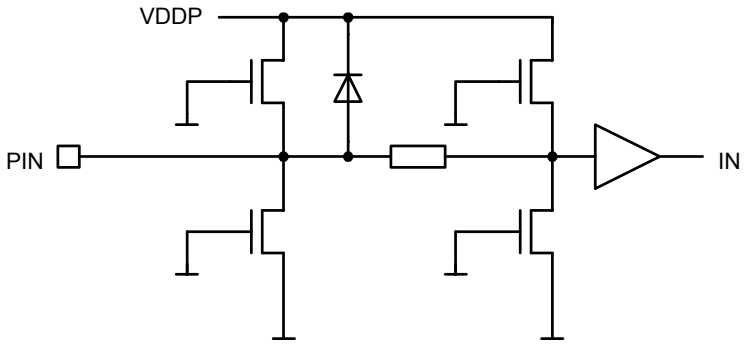
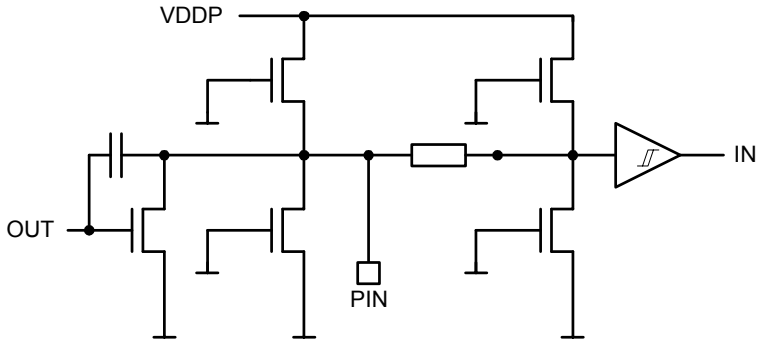
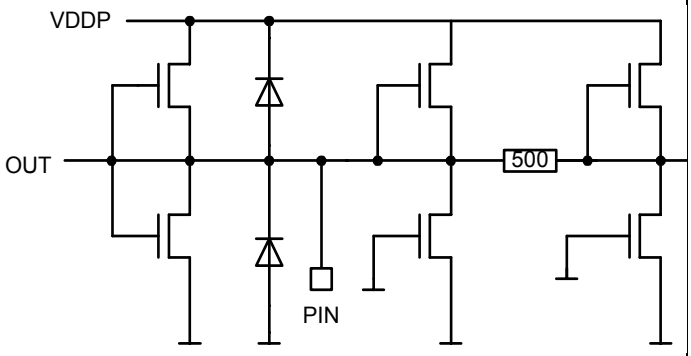
Subaddress FEh		
	FE	**any value to this subaddress executes previous I²C protocolls immediately**

Subaddress FFh		
	FF	**any value to this subaddress executes previous I²C protocolls according to the take-over-mechanism (dedicated v-pulse, V20, V40, V36)**

7 Pin schematic

pin	schematic	remark
vssdacy, vssdacu, vssdacv, vss33c, vss33rgb, vssp1, vssp2, vssp3		ground
vdddacy, vdddacu, vddacv, vdd33c, vdd33rgb, vddp1, vddp2, vddp3		power 3.3V
xin, xout		crystal connection
vddac1, vssac1, vddac2, vssac2, vddargb,vssargb, vddafbl, vssafbl, vddapll, vddd1, vsss1, vddd2, vsss2, vddd3, vsss3, vddd4, vsss4		power 1.8V and ground

Pin schematic

pin	schematic	remark
h50, v50, clkout, hout, vout,		digital output
v, tms, adr/tdi, reset		digital input
sda, scl		I²C bus
656ioX,656clk, 656hin/clkf20, 656vin/blank		digital input / output

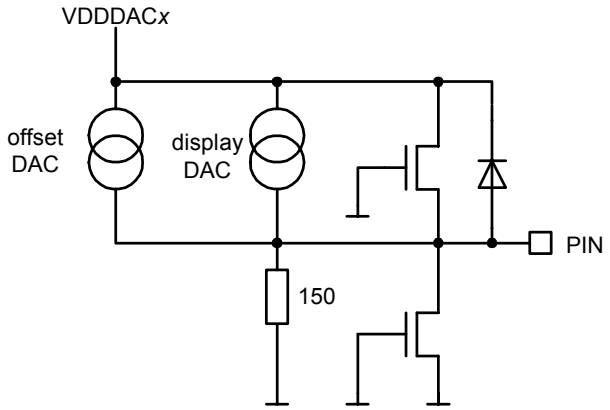
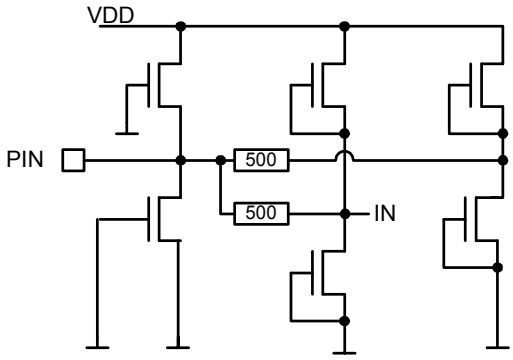
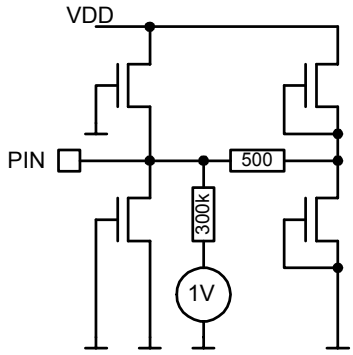
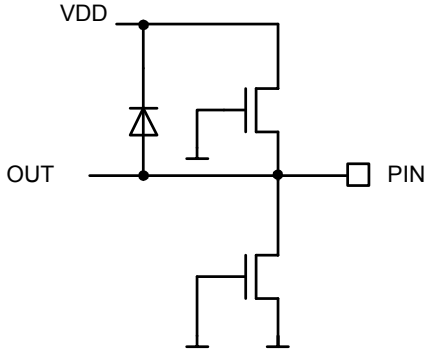
pin	schematic	remark
ayout, auout, avout		analog output
rin1, rin2, gin1, gin2, bin1, bin2, fbl1, fbl2, cvbs1...cvbs7 (if cvbsx is connected to any ADC)		analog input
cvbs1...cvbs7 (if cvbsx is not connected to any ADC)		analog input
cvbso1...cvbso3		analog output

Figure 7-1 Pin schematic

8 Absolute Maximum Ratings

All voltages listed are referenced to ground (0V, V_{SS}) except where noted.

Parameter	Symbol	Limit Values		Unit	Remark
		Min	Max		
Operating Temperature	T_A	0	70	°C	
Storage Temperature	T_{STG}	-65	125	°C	
Junction Temperature	T_J		125	°C	
Soldering Temperature	T_S		260	°C	
Soldering Time	ts		10	s	
Input Voltage	V_I	-0.3	V_{DD2}+0.3	V	not valid for V_{DD1} supply pins
Output Voltage	V_O	-0.3	V_{DD2}+0.3	V	not valid for V_{DD1} supply pins
Supply Voltages1	V_{DD1}	-0.3	2	V	
Supply Voltages2	V_{DD2}	-0.3	3.6	V	
Total Power Dissipation	P_{tot}		1	W	package limit
ESD Protection	ESD	tbd	tbd	kV	MIL STD 883C method 3015.6, 100pF,1500Ω
Latch-Up Protection		-100	100	mA	all inputs/outputs

Note: Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions or at any other condition beyond those indicated in the operational sections of this specification is not implied.

9 Recommended Operating Range

Parameter	Symbol	Limit Values			Unit	Remark
		min.	typ.	max.		
Ambient Temperature	T_A	0	25	70	°C	
3.3V power supply:						
Supply Voltages	V_{DDxx}	3.14	3.3	3.47	V	+/- 5%
Rise time	t_r				ns	
1.8V power supply:						
Supply Voltages	V_{DDxx}	1.71	1.8	1.89	V	+/- 5%
Rise time	t_r				ns	
CVBS/RGB frontend: cvbs1-7, rin1-2, gin1-2, bin1-2,fbl1-2						
Analoge CVBS input voltage	$V_{i,CVBS}$	0.6	1.2	1.8	V	
Analoge RGB input voltage	$V_{i,RGB}$	0.5	1.2	1.5	V	
Analoge FBL input voltage	$V_{i,FBL}$	0.5	1.2	1.5	V	
Analoge chroma input voltage			0.3		V	burst
Input Coupling Capacitors CVBS			100		nF	necessary for proper clamping
Input Coupling Capacitors RGB/FBL			47		nF	necessary for proper clamping
Source Resistance			0.1		kΩ	
Reset input:						
Rise-time					µs	
Active Time Reset	t_{RES}	1.3			µs	
Fast I²C Bus (All values are referred to min(V_{IH}) and max(V_{IL}))						
I²C Clock Frequency	f_{SCL}	0		400	kHz	
Inactive Time Before Start Of Transmission	t_{BUF}	1300			ns	
Set-Up Time Start Condition	$t_{SU;STA}$	600			ns	

Recommended Operating Range

Parameter	Symbol	Limit Values			Unit	Remark
		min.	typ.	max.		
Hold Time Start Condition	$t_{HD;STA}$	600			ns	
SCL Low Time	t_{LOW}	1300			ns	
SCL High Time	t_{HIGH}	600			ns	
Set-Up Time DATA	$t_{SU;DAT}$	100			ns	
Hold Time DATA	$t_{HD;DAT}$	0		900	ns	
SDA/SCL Rise/Fall Times	t_R, t_F	20+$		300	ns	$=0.1C_b/pF
Set-Up Time Stop Condition	$t_{SU;STO}$	600			ns	
Capacitive Load/Bus Line	C_b			400	pF	
I²C Bus pins: sda, scl						
Threshold rise	V_{IHr}		2.08		V	
Threshold fall	V_{IL}		1.8		V	
Digital To Analog Converters:ayout, auout, avout						
Load resistance	R_L	10			kΩ	
Load capacitance	C_L	tbf			pF	

Crystal Specification: xin, xout

Frequency (fundamental)	f_{xtal}	20.248	20.25	20.252	MHz	values outside this range may cause color decoding failures
Maximum Permissible Frequency Deviation	$\Delta f_{max}/f_{xtal}$	-100		100	ppm	values outside this range may cause color decoding failures
Recommended Permissible Frequency Deviation	$\Delta f/f_{xtal}$	-40	0	40	ppm	including adjustment, temperature and aging deviations
Load Capacitance	C_L		13		pF	
Series resistance	R_S		tbf	25	Ω	

Parameter	Symbol	Limit Values			Unit	Remark
		min.	typ.	max.		
Motional capacitance	C_1	20		30	fF	
Parallel capacitance	C_0		7		pF	
External Load capacitance to ground	$C_{L,EXT}$		13		pF	
All digital Inputs: tms, adr/tdi, v, tclk, reset, 656vin/blank, 656hin/clkf20, 656ioX, 656clk						
Input voltage Low	$V_{in,L}$			1.3	V	
Input voltage High	$V_{in,H}$	1.5			V	

In the operating range the functions given in the circuit description are fulfilled.

10 Characteristics

(Assuming Recommended Operating Conditions)

Parameter	Symbol	Limit Values			Unit	Remark
		min.	typ.	max.		
Average total supply current	I_{DDtot}		270		mA	
Average supply current in power-down-mode	I_{DDPD}		105		mA	***STANDBY*** ='10'
Total Power Dissipation	P_{tot}		0.56	0.8	W	
Total Power Dissipation in power-down-mode	P_{totPD}		0.17		W	***STANDBY*** ='10'
Digital Inputs						
Input Capacitance	C_I		7		pF	
Input Leakage Current		-10		10	µA	incl. leakage current of SDA output stage
Digital Outputs						
Output Voltage High	V_{OH}	2.5		V_{dd2}	V	
Output Voltage Low	V_{OL}			0.6	V	
Output Current High	I_{OH}				mA	
Output Current Low	I_{OL}				mA	
Clock Outputs						
CLKOUT cycle time	t		37		ns	
CLKOUT duty cycle			50		%	
656CLK cycle time	t		37		ns	
656CLK duty cycle			50		%	
delay-hold-time						
Analog CVBS Frontend						
Input Leakage Current		-100		100	nA	clamping inactive
Input Capacitance	C_I		7		pF	
Input Clamping Error		-1		1	LSB	settled state

Parameter	Symbol	Limit Values			Unit	Remark
		min.	typ.	max.		
Input Clamping Current	$\lvert\bar{I}_{CLP}\rvert$				µA	dependent on clamping error
Differential Nonlinearity	DNL	-0.5		0.5	LSB	nominal conditions
Integral Nonlinearity	INL	-1		1	LSB	nominal conditions
Crosstalk between CVBS Inputs	CT	-50			dB	f_{sig}<5MHz
Bandwidth	BW	7			MHz	-3 dB
Input Voltage	V_{in}	0.6	1.2	1.8	V	
CVBS output amplification	A_{cvbso}	0.9		1.1		

Analog RGBF Frontend

Input Leakage Current		-100		100	nA	clamping inactive
CVBS Input Capacitance	C_I		7		pF	
Input Clamping Error		-1		1	LSB	settled state
Input Clamping Current	$\lvert\bar{I}_{CLP}\rvert$				µA	dependent on clamping error
Differential Nonlinearity	DNL	-0.5		0.5	LSB	DC-ramp, nominal conditions
Integral Nonlinearity	INL	-1		1	LSB	DC-ramp, nominal conditions
Crosstalk between RGB Inputs	CT	-50			dB	
Bandwidth	BW	10			MHz	-3 dB
Input Voltage	V_{in}	0.5	1.2	1.5	V	

Digital To Analog Converters:

Differential Nonlinearity	DNL	-1		1	LSB	DC-ramp, nominal conditions

Parameter	Symbol	Limit Values			Unit	Remark
		min.	typ.	max.		
Integral Nonlinearity	INL	-2		2	LSB	DC-ramp, nominal conditions
Full Range Output Voltage	U_{OL}		0.4		V	nominal conditions PKLY/U/V=min
Full Range Output Voltage	U_{OH}		1.9		V	nominal conditions PKLY/U/V=max
output matching		-3		3	%	
Offset Range		0		1	V	

Colordecoder/Synchronization and Luminance Processing

Horizontal PLL pull-in-range	Δf_{Hf}		+/- 4.9		%	based on 15625 kHz
ACC range		-30		+6	dB	
AGC range		-7.5		+2	dB	
Chroma PLL pull-in-range	Δf_{SC}		+/- 500		Hz	nominal crystal frequency

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25°C and the given supply voltage.

11 Diagrams

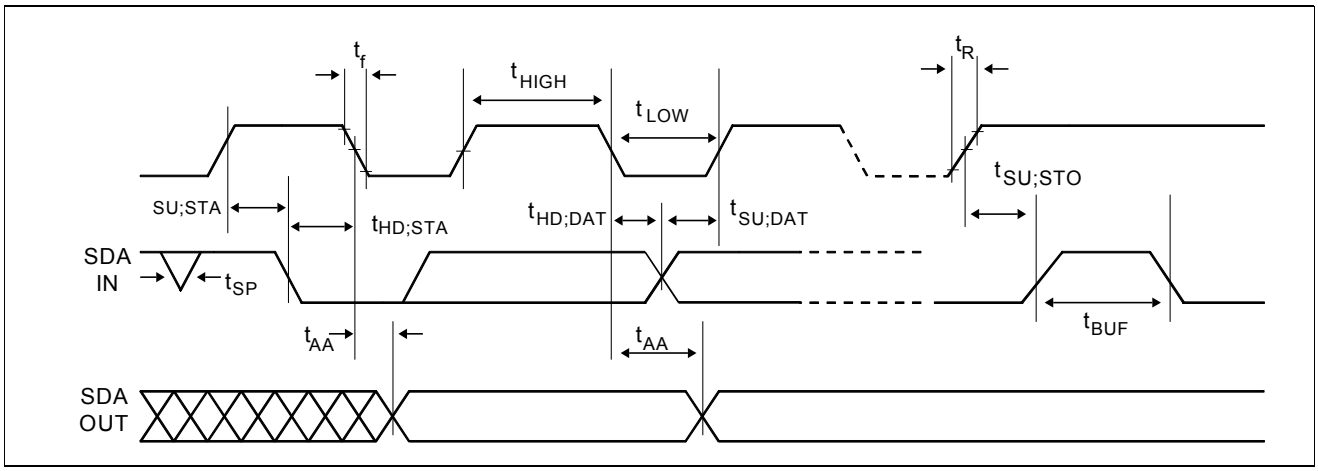


Figure 11-1 I²C bus timing data

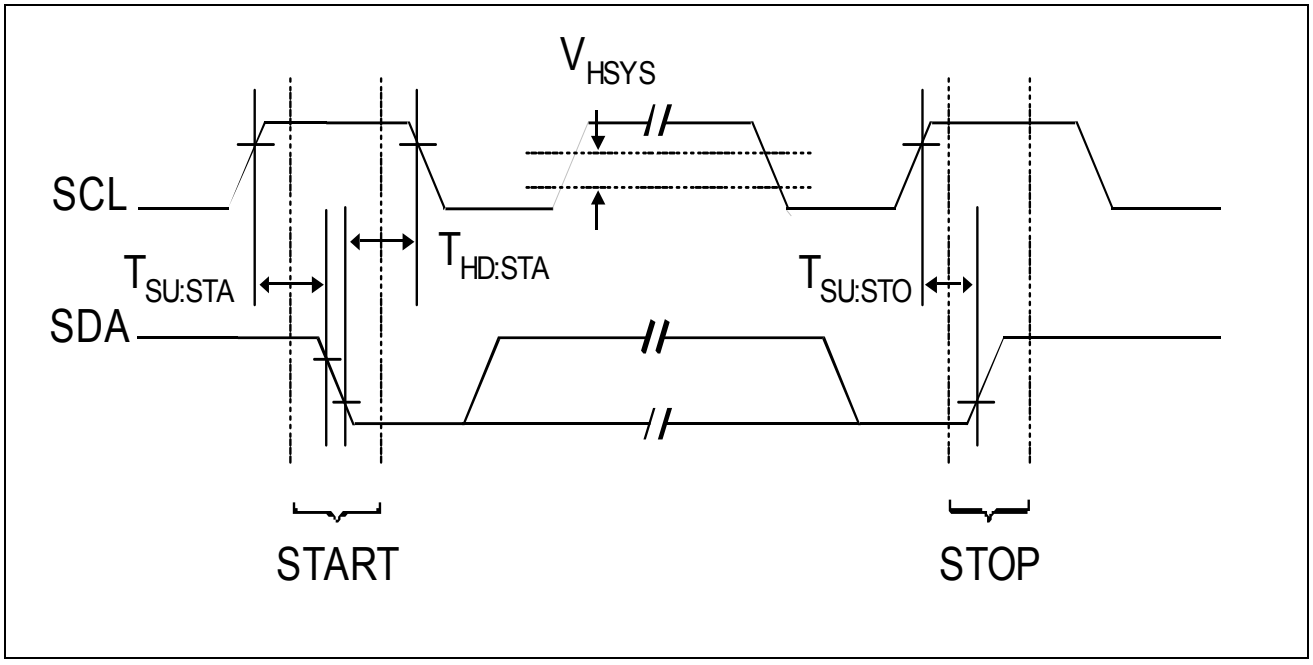


Figure 11-2 I²C Bus timing start/stop

12 Application Circuit

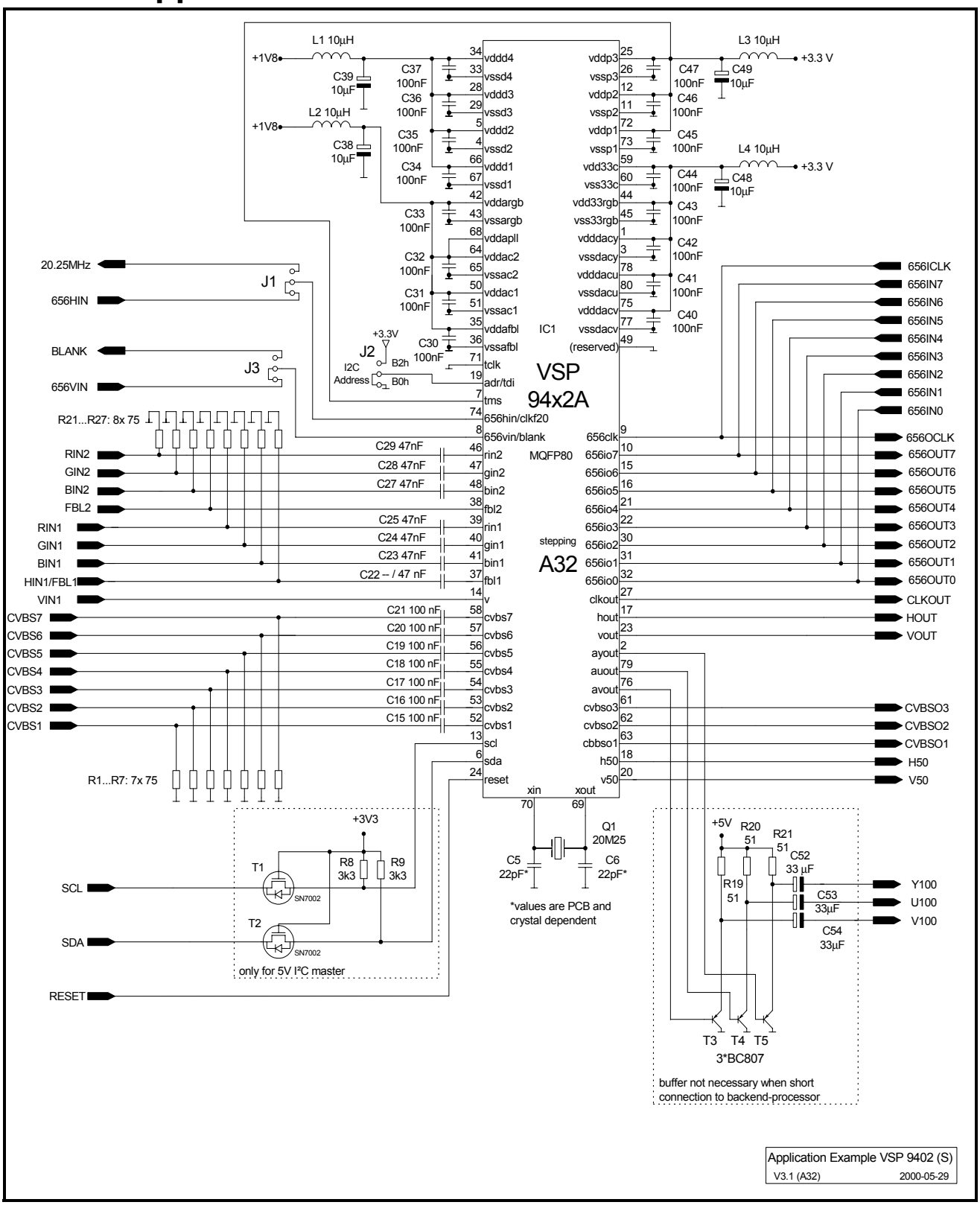


Figure 12-1 Application Example

12.1 Application overview

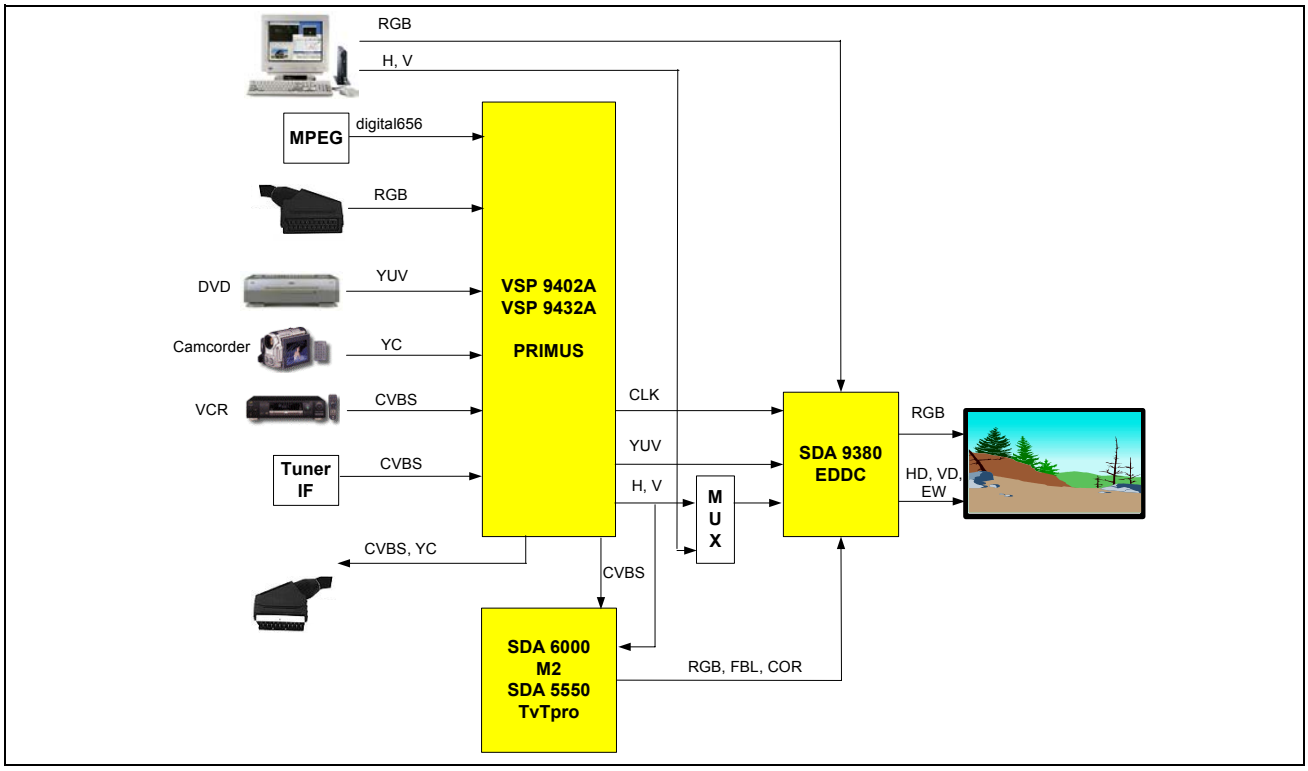


Figure 12-2 Application Overview with SDA9380

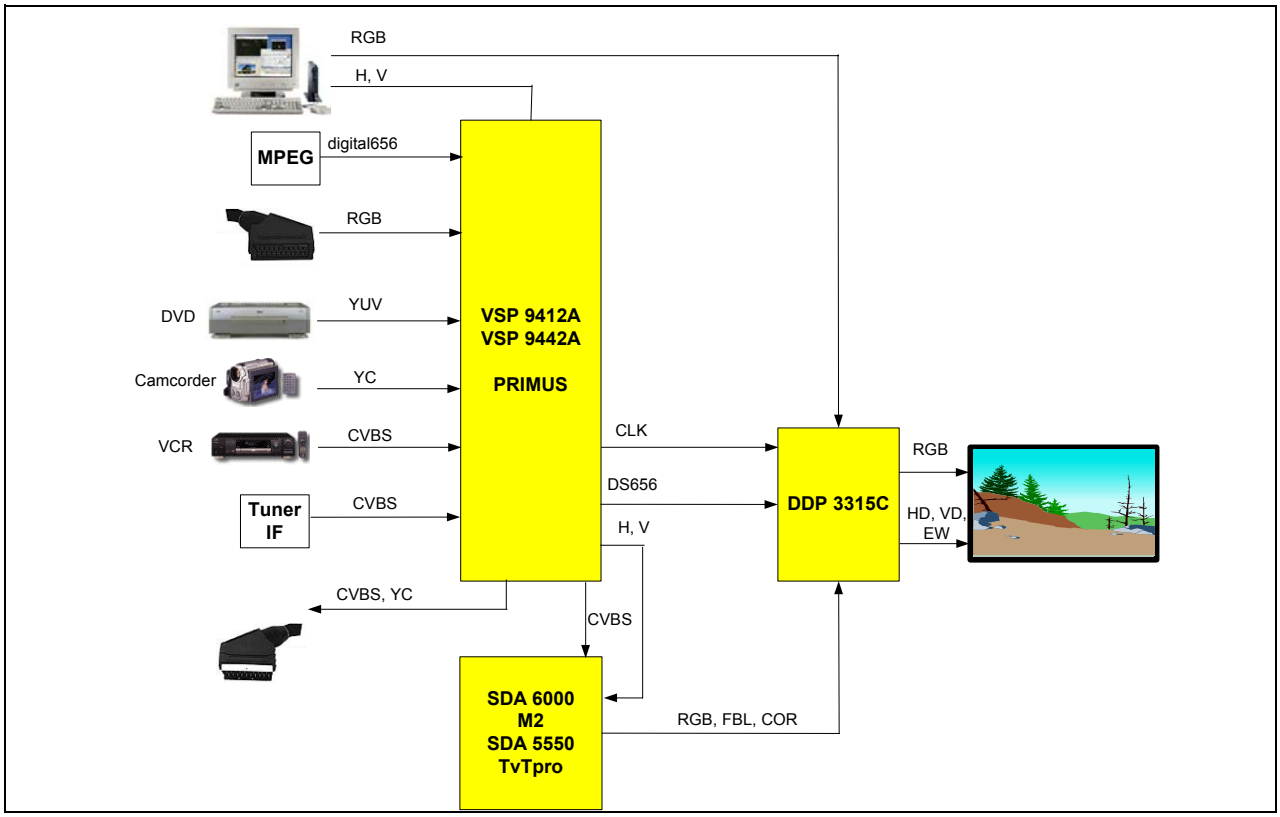


Figure 12-3 Application Overview with DDP 3315C

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