VPB261

H.261 EVALUATION BOARD

FEATURES

- Complete evaluation and prototyping system for GEC Plessey Semiconductors H.261 Video Compression/Decompression chipset.
- Fully software configurable IBM PC/XT/AT compatible expansion card
- RGB input and output at Rec. 601 resolution
- Optional gamma correction of input RGB data (VP510)
- Supports coding/decoding of CIF and QCIF images at data rates up to 2Mbits/s and frame rates up to 30Hz
- Three 8 bit video ADCs (GPS VP8708) provide 24 bit colour accuracy
- Triple 8 bit video DAC (GPS VP101) for RGB display
- All RAM requirements fully localised (DRAM & SRAM)
- Tristateable busses allow incremental CODEC evaluation

EVALUATION BOARD OVERVIEW

RGB format video is input to the board from a source which can be gen-locked to the composite sync signal provided by the VP520 video filter in the decode path (figure 1).

RGB data is sampled at the system clock frequency (27MHz) using an individual VP8708 for each of the RED, GREEN and BLUE channels. The data is colour space converted, filtered and coded to H.261 specification and passed to the transmission channel. The transmission channel is normally a simple link to the decoder section of the board, however this can be intercepted and output to another evaluation board, a network/ISDN Terminal Adaptor or a different H.261 decoder if desired. It is also possible to input H.261 data from another system and decode and display using the VPB261.

There is also the option of alternative video I/O formats via two headers on the PCB.

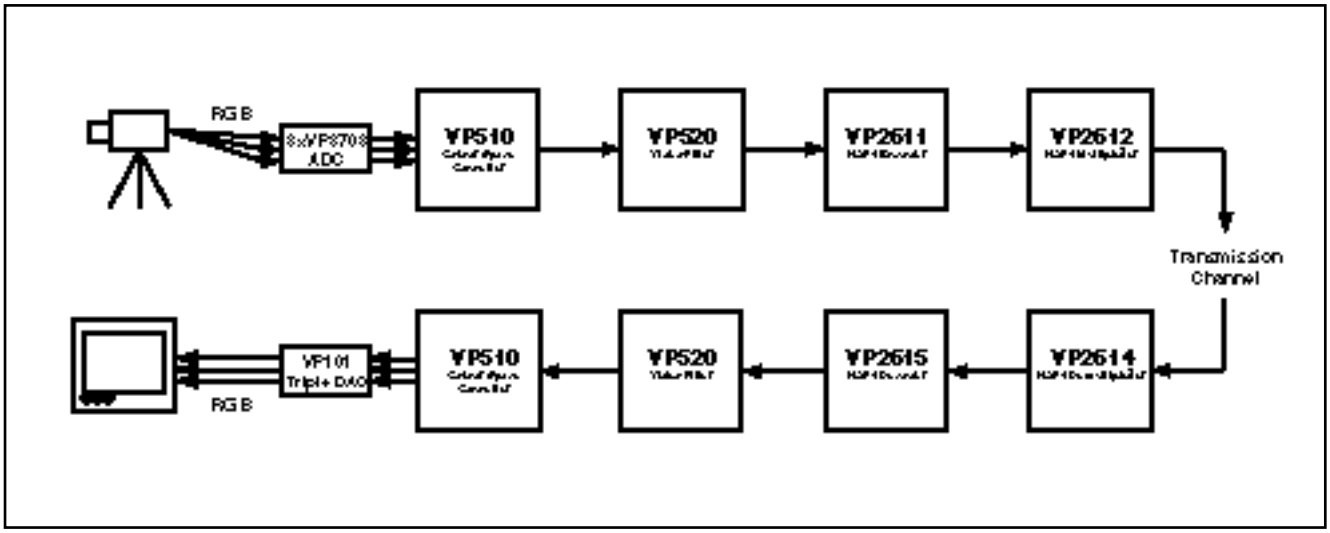


Fig.1 Block Diagram of The Evaluation Board

SOFTWARE

The software provided with the board allows the user to set up each device in all modes to allow for maximum board flexibility. The coefficients and setups in the VP510s and VP520s are fully programmable via the software, as are the setups in the VP2611, VP2612, VP2614 and VP2615.

The software runs under Microsoft Windows 3.1 and allows the user to access the internal registers of each chip.

PC BUS INTERFACE

The board interfaces to the PC over a standard IBM XT 8 bit interface. There is an individual address register on the board, which is written to whenever any of the devices are to be addressed. This register should contain the address internal to the device that is being written to / read from. The actual data is then transferred to/from the device on the board by addressing that device in the PC I/O map. This means that whenever data is to be passed to / from a device on the board it requires two PC operations, the first always being a write. (Except in the cases of the VP2611 and VP2615 where four PC operations will be completed due to the individual addressing strategy of these devices, see the datasheets for each of these devices for more information.)

An example of some code showing this is given in Fig.2.

Here, two aliases for the addresses in I/O space of the address register (311 hex) and the VP520 in the decoder side (31E hex) have been set up. In the code section, two registers internal to the VP520 have been programmed: the register in location C, the blanked screen Y value, and the register in location D, the blanked screen U value have been programmed with 64 and 20 hex respectively. (See VP520 data sheet for more information on these registers.)

The third part of the code section shows a read function from status register B in the VP2614. (First of all the address in the device is loaded into the address register, and then the value of the register is read from the device.)

The board is also supplied with some simple source code examples.

TRISTATE CONTROL

The board allows back to back coding/decoding in each successive stage of the system. This allows incremental evaluation of the coding process (see figure 3).

The tri-stating on the board is controlled by writing to another register, the board control register. This register provides the control for the tristate buffers and also controls the bit rate of the transmission channel. The first three bits of the lower nibble of this register are used for the tristate control, and one of the following values MUST be written to the nibble:

0 = 510 - 510
1 = 510 - 520 - 520 - 510
3 = 510 - 520 - 2611 - 2615 - 520 - 510
7 = Full H.261 encode / decode
{anything else = undefined operation}

SERIAL BIT RATE CONTROL

The serial bit rate is controlled by writing to the upper nibble of the board control register. The clock generated by the on board oscillator is on the encode side of the board. That is, if the user wishes to inject H.261 data from an external source via connector P2, the appropriate control lines should be asserted and jumpers JP2 to JP6 removed. (It is possible, however, to crudely run the decoder by providing a clock and H.261 data only, leaving the line controls connected to the on-board encoder.)

The table below shows the bit rate for each value written to the upper nibble of the board control register. Note this nibble MUST be programmed with one of the following values:

2 = 2.048 Mbits/s	3 = 1.024 Mbits/s
4 = 512 kbits/s	5 = 256 kbits/s
6 = 128 kbits/s	7 = 64 kbits/s

{anything else = undefined operation}

BUFFER CONTROL

When the buffer control option is selected, the buffer read and write pointers of the VP2612 are monitored to obtain a fullness value. This value is used to determine the quantisation of the encoder. If the buffer fullness reaches a certain threshold level the next frame is skipped. There is a linear relationship linking the fullness and bitrate parameters to quantiser and threshold levels - the threshold may also be adjusted via the software controls.

```
/* alias section */
addr_reg  = $311;    /* These are the addresses of the   */
VP2614    = $31C;    /* devices in the PC I/O memory map */
VP520_dec = $31E;

/* code section */
     port[addr_reg]  := $C;
     port[VP520_dec] := $64;

     port[addr_reg]  := $D;
     port[VP520_dec] := $20;

     port[addr_reg]  := $1;
     status_1        := port[VP2614];
```

Fig.2 Example of code

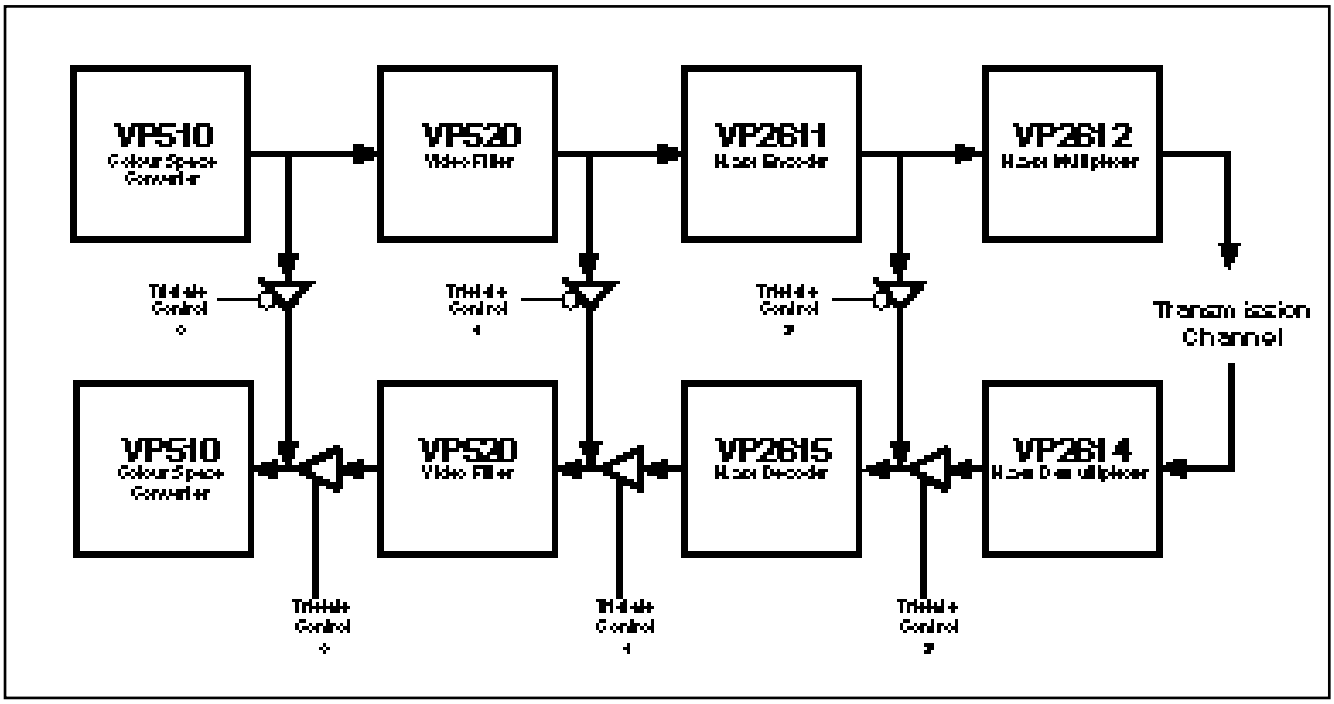


Fig.3 Tristate Connecting for incremental evaluation

COMPONENT SUMMARY

VP8708 Video ADC
A 30MHz analog video interface which includes a video amplifier with clamp and gain control and an internal voltage reference. The output of the video amplifier is externally connected to an anti-aliasing filter (3dB point approx. 6.75MHz) and then re-input to the device for final analog to eight bit digital conversion.

VP101 Triple 8 Bit CMOS Video DAC
A 30MHz or 50MHz device which uses video control inputs (BLANK, SYNC and REF WHITE) to provide appropriate levels required for standard video signals.

VP510 Bidirectional Colour Space Converter
The VP510 converts three channels of RGB data into two channels of decimated luminance and chrominance data. Each channel has its own lookup table, loaded via the software and used for gamma correction and/or ranging. There are two of these devices on board: one to convert RGB to Y-UV (in the encode path) and one to convert Y-UV to RGB (in the decode path). The direction of data flow in the device is set in the control word.

VP520 PAL/NTSC to CIF/QCIF Converter
The VP520 converts between CCIR601 resolution raster scan Y-UV data and H.261 format CIF/QCIF macroblocks. The VP520 supports both PAL and NTSC formats. All on board vertical and horizontal FIR filter coefficients are fully programmable (via software).

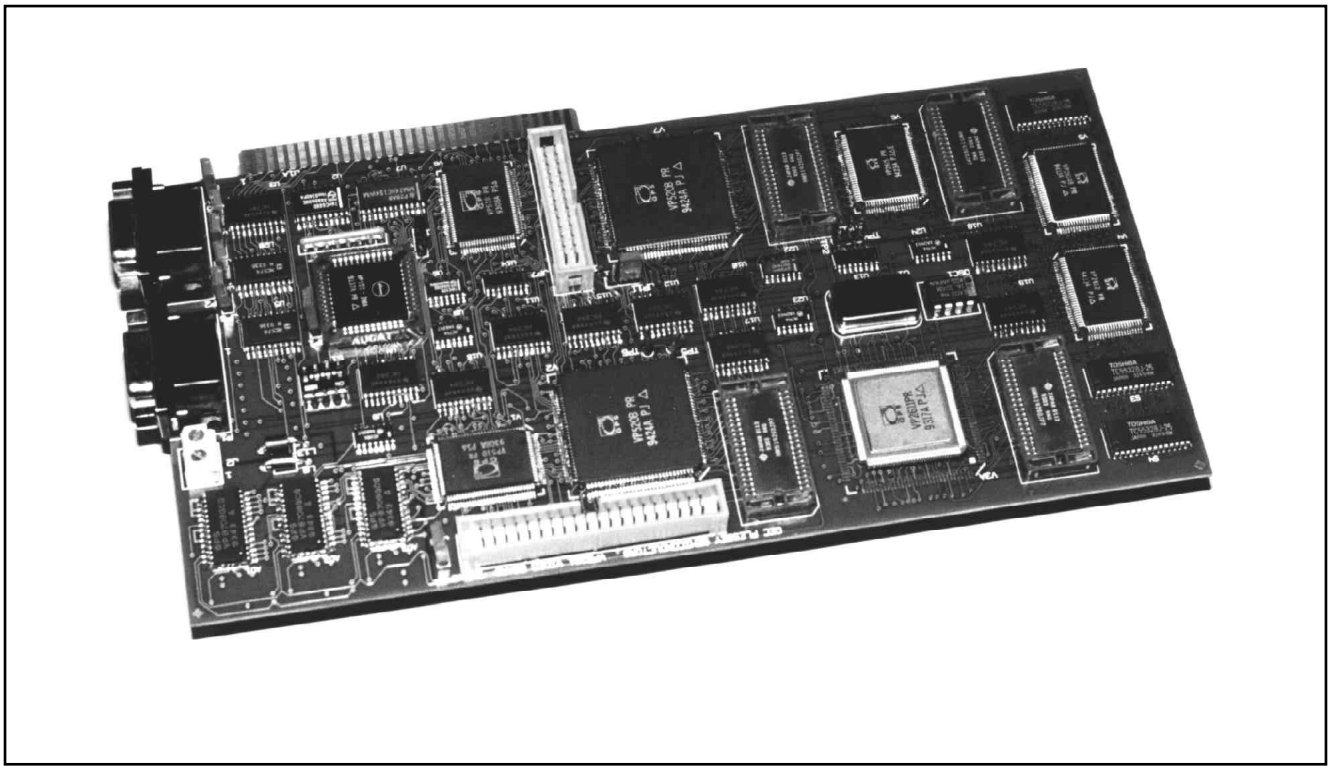
VP2611 H.261 Encoder
This device performs DCT, quantisation and run length coding of the input macroblocks. Optional quantisation weighting tables may also be programmed via the software interface. With a 27 MHz clock the device will accept data produced to full CIF resolution up to 30Hz frame rate. The VP2611 also implements motion estimation within a search window of +/- 7 pixels.

VP2612 Video Multiplexer
The VP2612 will convert run length coded data from the VP2611 encoder into an H.261 compatible bitstream. The serial port outputs the bitstream in frames containing header information and a BCH(511,493) cyclic redundancy code for error detection/correction.

VP2614 Video Demultiplexer
The device will extract error corrected parameters and run length coded DCT coefficients from an H.261 bitstream. It outputs data in the format required by the VP2615.

VP2615 H.261 Decoder
The VP2615 will take run length coded coefficients which have been error corrected and Huffman decoded, and output Y-UV data in macroblock format at CIF/QCIF resolutions.

VPB261



ORDERING INFORMATION

VPB261/--/APPL H.261 Evaluation Board

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