GEC PLESSEY
SEMICONDUCTORS

JULY 1995
PRELIMINARY INFORMATION
DS4076 - 1.3

VP551

NTSC/PAL DIGITAL VIDEO ENCODER

The VP551 converts digital Y, Cr, Cb, data into analog NTSC/PAL composite video and S-video signals. The outputs are capable of driving doubly terminated 75 ohm loads with standard video levels.

The device accepts data inputs complying with CCIR Recommendation 601 and 656, which are time multiplexed on an 8 bit bus at 27MHz. It is formatted as Cb, Y, Cr, Y (i.e. 4:2:2). The video blanking and sync information from REC 656 is included in the data stream when the VP551 is working in slave mode.

Its output pixel rate is 27MHz and the input pixel rate is half this frequency, i.e. 13.5MHz.

All necessary synchronisation signals are generated internally when the device is operating in master mode. Digital horizontal and vertical sync outputs are available for use by the host system.

The rise and fall times of sync, burst envelope and video blanking are internally controlled to be within composite video specifications.

Two digital to analog converters (DACs) are used to convert the digital luminance and chrominance data into analog signals. The inverted composite video signal is generated by summing the complementary current outputs of each DAC. An internally generated reference voltage provides the biasing for the DACs.

FEATURES

- Converts Y, Cr, Cb data to analog composite video and S-video
- Supports CCIR recommendations 601 and 656
- All digital video encoding
- Selectable master/slave mode for sync signals
- Switchable chrominance bandwidth
- Switchable pedestal with gain compensation
- SMPTE 170M NTSC or CCIR 624 PAL compatible outputs
- GENLOCK mode
- I^2C bus serial microprocessor interface
- 64 PQFP package

APPLICATIONS

- Digital Cable TV
- Digital Satellite TV
- Multi-media
- Video games
- Karaoke
- Digital VCRs

ORDERING INFORMATION

VP551/CG/GP1R

Notes: Prior to completion of full device characterisation, pre-preproduction parts will be designated VP551/PR/GP1R.

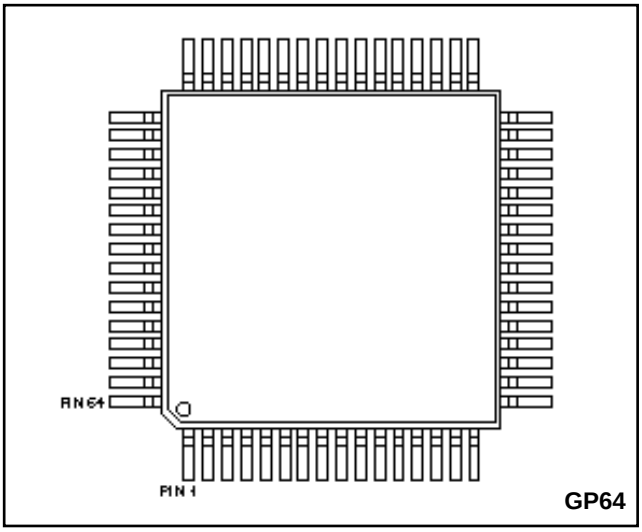


Fig.1 Pin connections (top view)

PIN	FUNCTION	PIN	FUNCTION
1	VDD	33	VDD
2	GND	34	RESET
3	D0 (VS O/P)	35	REFSQ
4	D1 (HS O/P)	36	GND
5	D2 (FC0 O/P)	37	VDD
6	D3 (FC1 O/P)	38	GND
7	D4 (FC2 O/P)	39	PD7
8	D5	40	PD6
9	D6 (SCSYNC I/P)	41	PD5
10	D7 (PALID I/P)	42	PD4
11	GND	43	PD3
12	VDD	44	PD2
13	GND	45	PD1
14	GND	46	PD0
15	PXCK	47	GND
16	VDD	48	VDD
17	CLAMP	49	AGND
18	COMPSYNC	50	VREF
19	GND	51	LUMAGAIN
20	VDD	52	LUMACOMP
21	TDO	53	AVDD
22	TDI	54	LUMAOUT
23	TMS	55	AGND
24	TCK	56	COMPOUT
25	GND	57	AGND
26	SA1	58	CHROMAOUT
27	SA2	59	AVDD
28	SCL	60	CHROMACOMP
29	VDD	61	CHROMAGAIN
30	SDA	62	AVDD
31	GND	63	AVDD
32	VDD	64	N/C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated): As specified in Recommended Operating Conditions

DC CHARACTERISTICS

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Units
Digital Inputs TTL compatible (except SDA, SCL)						
Input high voltage		VIN	2.0			V
Input low voltage		VIL			0.8	V
Digital Inputs SDA, SCL						
Input high voltage		VIH	0.7 VDD			V
Input low voltage		VIL			0.3 VDD	V
Input high current	VIN = VDD	IIH			10	µA
Input low current	VIN = VSS	IIL			-10	µA
Digital Outputs CMOS compatible						
Output high voltage	IOH = -1mA	VOH	3.7			V
Output low voltage	IOL = +4mA	VOL			0.4	V
Digital Output SDA						
Output low voltage	IOL = +6mA	VOL			0.6	V

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated): As specified in Recommended Operating Conditions

DC CHARACTERISTICS DACs

Parameter	Symbol	Min.	Typ.	Max.	Units
Accuracy (each DAC)					
Integral linearity error	INL			±1.5	LSB
Diffential linearity error	DNL			±1	LSB
Grey scale error				±5	% grey scale
Monotonicity			guaranteed		
Luminance video output current					
White level relative to black level (NTSC-USA)		16.74	17.6	18.46	mA
Black level relative to blank level (NTSC-USA)		0.95	1.44	1.90	mA
Black level relative to sync level (NTSC-USA)		6.3	7.63	8.96	mA
LSB size			69		µA
Chrominance video output current					
Black level (NTSC-USA)		13.51	14.23	14.95	mA
Peak chroma level relative to black level (NTSC-USA) (corresponding to 100% saturated red)		±10.12	±11.12	±12.12	mA
Peak burst level relative to black level (NTSC-USA)		±3.46	±3.81	±4.16	mA
Analog video output compliance	VAVOC	-0.3		1.6	V
Internal reference voltage	VREF	0.95	1.00	1.05	V
Internal reference voltage output impedance			TBD		Ω

ABSOLUTE MAXIMUM RATINGS

Supply voltage	VDD, AVDD	-0·3 to 7·0V
Voltage on any non power pin		-0·3 to VDD+0·3V
Ambient operating temperature		0 to 70°C
Storage temperature		-55°C to 125°C

Note: Stresses exceeding these listed under Absolute Maximum Ratings may induce failure. Exposure to Absolute Maximum Ratings for extended periods may reduce reliability. Functionality at or above these conditions is not implied.

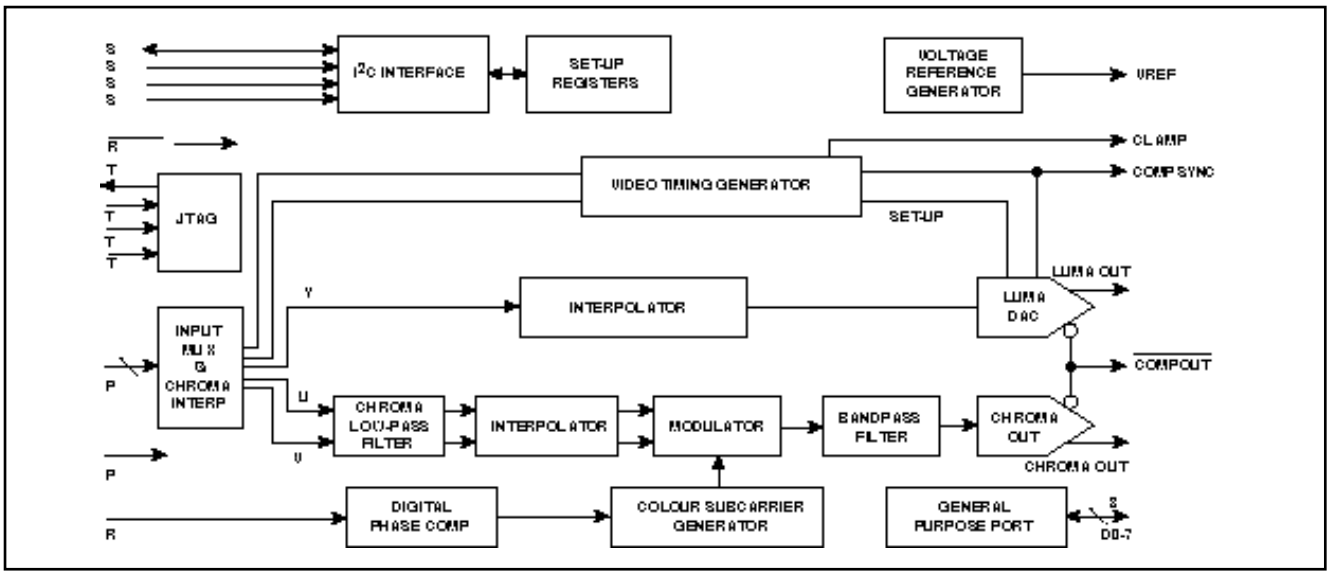


Fig.2 Functional block diagram

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Units
Power supply voltage	VDD, AVDD	4.75	5.00	5.25	V
Power supply current (including analog outputs)	IDD		150		mA
Input clock frequency	PXCK		27.00		MHz
SCL clock frequency	fscl			500	kHz
Analog video output load			37.5		Ω
Luma gain resistor (NTSC pedestal on)			736		Ω
Luma gain resistor (NTSC pedestal off)			731		Ω
Chroma gain resistor (NTSC pedestal on)			428		Ω
Chroma gain resistor (NTSC pedestal off)			458		Ω
Luma gain resistor (PAL)			734		Ω
Chroma gain resistor (PAL)			443		Ω
Ambient operating temperature		0		70	°C

ESD COMPLIANCE

Pins	Test	Test Levels	Notes
All pins	Human body model	2kV on 100pF through 1k5Ω	Meets Mil-Std-883 Class 2
All pins	Machine model	200V on 200pF through 0Ω & 500nH	

VIDEO CHARACTERISTICS

Parameter	Symbol	Min.	Typ.	Max.	Units
Luminance bandwidth			4.0		MHz
Chrominance bandwidth (Extended B/w mode)			1.3		MHz
Chrominance bandwidth (Reduced B/w mode)			650		kHz
Burst frequency (NTSC)			3.57954545		MHz
Burst frequency (PAL-B,G,H,I)			4.43361875		MHz
Burst frequency (PAL-M)			3.57561189		MHz
Burst frequency (PAL-N Argentina)			3.58205625		MHz
Burst cycles (NTSC and PAL-B,G,H,I,M,N)			10		Fsc cycles
Burst envelope rise / fall time			1.5		Fsc cycles
Analog video sync rise / fall time			90		ns
Analog video blank rise / fall time			160		ns
Differential gain			1.5		% pk-pk
Differential phase			1.0		°pk-pk
Signal to noise ratio (unmodulated ramp)			60		dB
Chroma AM signal to noise ratio (100% red field)			58		dB
Chroma PM signal to noise ratio (100% red field)			56		dB
Hue accuracy				2.5	%
Colour saturation accuracy				2.5	%
Residual sub carrier			-60		dB
Luminance / chrominance delay			0		ns

PIN DESCRIPTIONS

Pin Name	Pin No.	Description
PD0-7	39 - 46	8 Bit Pixel Data inputs clocked by PXCK. PD0 is the least significant bit, corresponding to Pin 46. These pins are internally pulled low.
D0-7	3 - 10	8 Bit General Purpose Port input/output. D0 is the least significant bit, corresponding to Pin 3. These pins are internally pulled low.
PXCK	15	27MHz Pixel Clock input. The VP551 internally divides PXCK by two to provide the pixel clock.
CLAMP	17	The CLAMP output signal is synchronised to COMPSYNC output and indicates the position of the BURST pulse, (lines 10-263 and 273-525 for NTSC and PAL-M; lines 6-310 and 319-623 for PAL-B,G,I,N(Argentina)).
COMPSYNC	18	Composite sync pulse output. This is an active low output signal.
TDO	21	JTAG Data scan output port. NOT AVAILABLE ON PROTOTYPE DEVICE.
TDI	22	JTAG Data scan input port. NOT AVAILABLE ON PROTOTYPE DEVICE.
TMS	23	JTAG Scan select input. NOT AVAILABLE ON PROTOTYPE DEVICE.
TCK	24	JTAG Scan clock input. NOT AVAILABLE ON PROTOTYPE DEVICE.
SA1	26	Slave address select.
SA2	27	Slave address select.
SCL	28	Standard I^2C bus serial clock input.
SDA	30	Standard I^2C bus serial data input/output.
$\overline{\text{RESET}}$	34	Master reset. This is an asynchronous active low input signal and must be asserted for a minimum of 200ns in order to reset the VP551.
REFSQ	35	Reference square wave input used only during Genlock mode.
VREF	50	Voltage reference output. This output is nominally 1·0V and should be decoupled with a 100nF capacitor to GND.
LUMA GAIN	51	Luminance full scale current control. A resistor connected between this pin and GND sets the magnitude of the luminance video output current. An internal loop amplifier controls a reference current flowing through this resistor so that the voltage across it is equal to the Vref voltage. This reference current has a weighting equal to 16 LSB's.
LUMACOMP	52	Luma DAC compensation. A 100nF ceramic capacitor must be connected between pin 52 and pin 53.
LUMAOUT	54	Luminance, inverted composite and chrominance video signal outputs. These are high
$\overline{\text{COMPOUT}}$	56	impedance current source outputs. A DC path to GND must exist from each of these pins.
CHROMAOUT	58	
CHROMA-COMP	60	Chroma DAC compensation. A 100nF ceramic capacitor must be connected between pin 60 and pin 59.
CHROMA GAIN	61	Chrominance full scale current control. As with the LUMAGAIN pin, a resistor between this pin and GND controls the magnitude of the chrominance video signal. An internal loop amplifier adjusts a reference current flowing through this resistor so that the voltage across it is equal to the Vref voltage. This reference current has a weighting equal to 16 LSB's.
VDD	1, 12, 16, 20, 29, 32, 33, 37, 48	Positive supply input. All VDD pins must be connected.
AVDD	53, 59 62, 63	Analog positive supply input. All AVDD pins must be connected.
GND	2, 11, 13, 14, 19, 25, 31, 36, 38, 47	Negative supply input. All GND pins must be connected.
AGND	49, 55, 57	Negative supply input. All AGND pins must be connected.

All other pins are N/C and should not be connected.

REGISTERS MAP

See Register Details for further explanations.

ADDRESS hex	REGISTER NAME	7	6	5	4	3	2	1	0	R/W	DEFAULT hex
	BAR	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	W	
00	PART ID2	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	R	
01	PART ID1	ID0F	ID0E	ID0D	ID0C	ID0B	ID0A	ID09	ID08	R	
02	PART ID0	ID07	ID06	ID05	ID04	ID03	ID02	ID01	ID00	R	
03	REV ID	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0	R	02
04	GCR	-	-	YCDELAY	RAMPEN	-	-	VFS1	VFS0	R/W	00
05	VOCR	-	CLAMPDIS	CHRBW	SYNCDIS	BURDIS	LUMDIS	CHRDIS	PEDEN	R/W	00
06	HANC	-	-	DFI2	DFI1	DFI0	Reserved	Reserved	ACTREN	*	00
07	ANCID	AN7	AN6	AN5	AN4	AN3	AN2	AN1	PARITY	R/W	00
08	SC_ADJ	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	R/W	97
09	FREQ2	FR17	FR16	FR15	FR14	FR13	FR12	FR11	FR10	R/W	87
0A	FREQ1	FR0F	FR0E	FR0D	FR0C	FR0B	FR0A	FR09	FR08	R/W	C1
0B	FREQ0	FR07	FR06	FR05	FR04	FR03	FR02	FR01	FR00	R/W	F1
0C	SCHPHM	-	-	-	-	-	-	-	SCH8	R/W	00
0D	SCHPHL	SCH7	SCH6	SCH5	SCH4	SCH3	SCH2	SCH1	SCH0	R/W	00
0E to 1F	Reserved										
20	GPPCTL	CTL7	CTL6	CTL5	CTL4	CTL3	CTL2	CTL1	CTL0	W	FF
21	GPPRD	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	R	-
22	GPPWR	WR7	WR6	WR5	WR4	WR3	WR2	WR1	WR0	W	00
23 to FE	Reserved										
FF	GPSCTL	FSC4SEL	Reserved	GENLKEN	NOLOCK	PALIDEN	TSURST	CHRMCLIP	TRSEL	R/W	00

Table.1 Register map

NOTE * For register HANC, bits 3, 4 and 5 are read only. Bits 1 and 2 are reserved.

Standard	Lines/ field	Field freq. HZ	Number of pixels/line at 27MHz	Horizontal freq. kHz. f_H	Subcarrier freq. kHz. f_{SC}	f_{SC}/f_H	SC_ADJ register hex	FREQ2-0 registers hex
NTSC (default)	525	59.94	1716	15.734266	3.57954545	(455/2)	xx	87 C1 F1
PAL-B, G, H, I	625	50	1728	15.625000	4.43361875	(1135/4+1/625)	9C	A8 26 2B
PAL-M	525	59.94	1716	15.734266	3.57561189	(909/4)	xx	87 9B C0
PAL-N (Argentina)	625	50	1728	15.625000	3.58205625	(917/4+1/625)	57	87 DA 51

Table.2 Line, field and subcarrier standards and register settings

xx = don't care.

The calculation of the FREQ register value is according to the following formula:-

$$FREQ = (2^{26} \times f_{SC}/f_H) / (\text{number of pixels/line}) \quad \text{hex}$$

Both NTSC and PAL-M values are rounded UP from the decimal number. PAL-B, G, H, I and N (Argentina) are rounded DOWN. The SC_ADJ value is derived from the adjustment needed to be added after 8 fields to ensure accuracy of the Subcarrier frequency. Note the SC_ADJ value of 9C required for PAL-B, G, H, I, is different to the default state of the register.

REGISTER DETAILS

BAR **Base register**
RA7-0 Register address.

PART ID 2-0 **Part number**
ID17-00 Chip part identification (ID) number.

REV ID **Revision number**
REV7-0 Chip revision ID number.

GCR **Global Control**
YCDELAY Luma to Chroma delay.
High = 37ns luma delay, this may be used to compensate for group delay in external filters.
Low = normal operation (default).

RAMPEN Modulated ramp enable.
High = ramp output for differential phase and gain measurements. A 27MHz clock must be applied to PXCK pin.
Low = normal operation (default).

VFS1-0 Video format select

VFS1	VFS0	
0	0	NTSC (default)
0	1	PAL-B,G,H,I,N(Argentina)
1	0	PAL-M
1	1	Reserved

VOCR **Video Output Control**
CLAMPDIS High = Clamp signal disable
Low = normal operation with clamp signal enabled (default).

CHRBW Chroma bandwidth select.
High = ±1·3MHz.
Low = ±650kHz (default)

SYNCDIS High = Sync disable (in composite video signal). COMPSYNC is not affected.
Low = normal operation with sync enabled (default).

BURDIS High = Chroma burst disable.
Low = normal operation, with burst enabled (default).

LUMDIS High = Luma input disable - force black level with synchronisation pulses maintained.
Low = normal operation, with Luma input enabled (default).

CHRDIS High = Chroma input disable - force monochrome.
Low = normal operation, with Chroma input enabled (default).

PEDEN High = Pedestal (set-up) enable a 7·5 IRE pedestal on lines 23-262 and 286-525. Valid for NTSC/PAL-M only
Low = normal operation, with pedestal disabled on all lines (default).

HANC **Horizontal Ancillary Data Control**
DFI2-0(read only) Digital Field Identification, 000=Field1
ANCTREN Ancillary timing reference enable. When High use FIELD COUNT from ancillary data stream. When low, data is ignored.

ANCID **Ancillary data ID**
AN7-1 Ancillary data ID
AN0 Parity bit (odd)
Only ancillary data in REC 656 data stream with the same ID as this byte will be decoded by the VP551 to produce H and V synchronisation and FIELD COUNT.

SC_ADJ **Sub Carrier Adjust**
SC7-0 Sub carrier frequency seed value, see table 2.

FREQ2-0 **Sub carrier frequency**
FR17-00 24 bit Sub carrier frequency programmed via I^2C bus, see table 2. FREQ2 is the most significant byte (MSB).

SCHPHM-L **Sub carrier phase offset**
SCH9-0 9 bit Sub carrier phase relative to the 50% point of the leading edge of the horizontal part of composite sync. SCHPHM bit 0 is the MSB. The nominal value is zero. This register is used to compensate for delays external to the VP551.

GPPCTL **General purpose port control**
CTL7-0 Each bit controls port direction
Low = output High = input

GPPRD **General purpose port read data**
RD7-0 I^2C bus read from general purpose port (only INPUTS defined in GPPCTL)

GPPWR **General purpose port write data**
WR7-0 I^2C bus write to general purpose port (only OUTPUTS defined in GPPCTL)

GPSCTL **GPS Control**
FSC4SEL When high, REFSQ = 4xFSC and GPP bit D6 is forced to become an input for a SCSYNC signal (high = reset), which provides a synchronous phase reset for FSC divider. Low = normal operation with REFSQ = 1xFSC. (default).

RESERVED Must be set low.

GENLKEN High = enable Genlock to REFSQ signal input.
Low = internal subcarrier generation (default).

NOLOCK	Genlock status bit (read only) Low = Genlocked. High = cannot lock to REFSQ. This bit is cleared by reading and set again if lock cannot be attained.
PALIDEN	High = enable external PAL ID phase control and GPP bit D7 is forced to become an input for PAL ID switch signal, (GPP bit D7 - Low = +135°, High = -135°). Low = normal operation, internal PAL ID phase switch is used (default).
TSURST	High = chip soft reset. Registers are NOT reset to default values. Low = normal operation (default).
CHRMCLIP	High = enable clipping of chroma data when luma goes below black level and is clipped. Low = no chroma clipping (default).
TRSEL	High = master mode, GPP bits D0 - 4 are forced to become a video timing port with VS, HS and FIELD outputs. Low = slave mode, timing from REC656.

I²C BUS CONTROL INTERFACE

I²C bus address

A6	A5	A4	A3	A2	A1	A0	R/ $\overline{W}$
0	0	0	1	1	SA2	SA1	X

The serial microprocessor interface is via the bi-directional port consisting of a data (SDA) and a clock (SCL) line. It is compatible to the Philips I²C bus standard (Jan. 1992 publication number 9398 393 40011). The interface is a slave transmitter - receiver with a sub-address capability. All communication is controlled by the microprocessor. The SCL line is input only. The most significant bit (MSB) is sent first. Data must be stable during SCL high periods.

A bus free state is indicated by both SDA and SCL lines being high. START of transmission is indicated by SDA being pulled low while SCL is high. The end of transmission, referred to as a STOP, is indicated by SDA going from low to high while SCL is high. The STOP state can be omitted if a repeated START is sent after the acknowledge bit. The reading device acknowledges each byte by pulling the SDA line low on the ninth clock pulse, after which the SDA line is released to allow the transmitting device access to the bus.

The device address can be partially programmed by the setting of the pins SA1 and SA2. This allows the device to respond to one of four addresses, providing for system flexibility. The I²C bus address is seven bits long with the last bit indicating read / write for subsequent bytes.

The first data byte sent after the device address, is the sub-address - BAR (base address register). The next byte will be written to the register addressed by BAR and subsequent bytes to the succeeding registers. The BAR maintains its data after a STOP signal.

NTSC/PAL Video Standards

Both NTSC (4-field, 525 lines) and PAL (8-field, 625 lines) video standards are supported by the VP551. All raster synchronisation, colour sub-carrier and burst characteristics are adapted to the standard selected. The VP551 generates outputs which follow the requirements of SMPTE 170M and CCIR 624 for PAL signals.

The device supports the following:
NTSC,
PAL B, G, H, I, N (Argentina) and M.

Video Timing - Slave sync mode

The VP551 has an internal timing generator which produces video timing signals appropriate to the mode of operation. In the default (power up) slave mode, all timing signals are derived from the input clock, PXCK, which must be derived from a crystal controlled oscillator. Input pixel data is latched on the rising edge of the PXCK clock.

The video timing generator produces the internal blanking and burst gate pulses, together with the composite sync output signal, using timing data (TRS codes) from the Ancillary data stream in the REC656 input signal, (when TRSEL (bit 0 of GPSCTL register) is set low).

Video Timing - Master sync mode

When TRSEL (bit 0 of GPSCTL register) is set high, the VP551 operates in a MASTER sync mode, all REC656 timing reference codes are ignored and GPP bits D0 - 4 become a video timing port with VS, HS and FIELD outputs. The PXCK signal is, however, still used to generate all internal clocks. When TRSEL is set high, the direction setting of bits 4 -0 of the GPPCTL register is ignored.

Video Blanking

The VP551 automatically performs standard composite video blanking. Lines 1-9, 264-272 inclusive, as well as the last half of line 263 are blanked in NTSC mode. In PAL mode, lines 1-5, 311-318, 624-625 inclusive, as well as the last half of line 623 are blanked.

The V bit within REC656 defines the video blanking when TRSEL (bit 0 of GPSCTL register) is set low. When in MASTER mode with TRSEL set high the video encoder is still enabled. Therefore if these lines are required to be blank they must have no video signal input.

Interpolator

The luminance and chrominance data are separately passed through interpolating filters to produce output sampling rates double that of the incoming pixel rate. This reduces the sinx/x distortion that is inherent in the digital to analog converters and also simplifies the analog reconstruction filter requirements.

Digital to Analog Converters

The VP551 contained two digital to analog converters which produce the analog video signals. The DACs use a current steering architecture in which bit currents are routed to one of two outputs; thus the DAC has true and complementary outputs. The use of identical current sources and current steering their outputs means that monotonicity is guaranteed.

An on-chip voltage reference of 1.0V (typ.) provides the necessary biasing. However, the VP551 may be used in applications where an external 1V reference is provided on the VREF pin, to adjust the video levels. In this case, the external reference should be temperature compensated and provide a low impedance output.

The full-scale output currents of the DACs is set by external resistors between the LUMAGAIN, CHROMAGAIN and GND pins. An on-chip loop amplifier stabilises the full-scale output current against temperature and power supply variations.

By summing the complementary current outputs of the two DACs, an inverted composite video signal is obtained. Note that this signal has a DC offset. The analog outputs of the VP551 are capable of directly driving a 37.5Ω co-axial cable.

DC Gain Adjust

The gains of the luma and chroma DACs are independently adjustable.

For the correct DAC gains in the NTSC pedestal on mode, the LUMAGAIN resistance should be 736Ω. The CHROMAGAIN resistance should be 428Ω for the proper corresponding chroma amplitude (including sinx/x compensation).

For the correct DAC gains in the PAL mode, the LUMAGAIN resistance should be 734Ω. The CHROMAGAIN resistance should be 443Ω for the proper corresponding chroma amplitude (including sinx/x compensation).

Luminance, Chrominance and Composite Video Outputs

The Luminance video output (LUMAOUT pin 54) drives a 37.5Ω load at 1.0V, sync tip to peak white. It contains only the luminance content of the image plus the composite sync pulses. In the NTSC mode, a set-up level (pedestal) offset can be added during the active video portion of the raster. The pedestal is programmed by PEDEN bit in VOCR register.

The Chrominance video output (CHROMAOUT pin 58) drives a 37.5Ω load at levels proportional in amplitude to the luma output (40 IRE pk-pk burst). This output has a fixed offset current which will produce approximately a 0.5V DC bias across the 37.5Ω load. Burst is injected with the appropriate timing relative to the luma signal.

In applications requiring only a true composite output, the lumaout and chromaout (pins 54 and 58) can be connected together and fed to a single output reconstruction filter (fig.3).

Luma, Chroma and true Composite video signals may be obtained simultaneously through the use of an external inverting video amplifier with the inverted composite video output ($\overline{\text{COMPOUT}}$ pin 56).

The inverted composite video output has a fixed DC offset. The sync tip is the most positive voltage and is approximately 1·5V with a 37.5Ω load.

Genlock using REFSQ input.

The VP551 can be Genlocked to another video source by setting GENLKEN high (in GPSCTL register) and feeding a phase coherent sub carrier frequency signal into REFSQ. Under normal circumstances, REFSQ will be the same frequency as the sub carrier. But by setting FSC4SEL high (in GPSCTL register), a 4 x sub carrier frequency signal may be input to REFSQ. In this case, the Genlock circuit can be reset to the required phase of REFSQ, by supplying a pulse to SCSYNC (pin 9). The frequency of SCSYNC can be at sub carrier frequency, but once per line, or once per field could be adequate, depending on the application.

Genlock in PAL mode.

When in Genlock mode with GENLKEN set high (in GPSCTL register), the VP551 requires a PAL phase identification signal, to define the correct phase on every line. This is supplied to PALID input (pin 10), High = -135° and low = +135°. The signal is asynchronous and should be changed before the sub carrier burst signal. PALID input is enabled by setting PALIDEN high (in GPSCTL register).

Master Reset

The VP551 must be initialised with the $\overline{\text{RESET}}$ pin 34. This is an asynchronous active low signal and must be active for a minimum of 200ns in order for the VP551 to be reset. The device resets to line 64, start of horizontal sync (i.e. line blanking active). There is no on-chip power on reset circuitry.

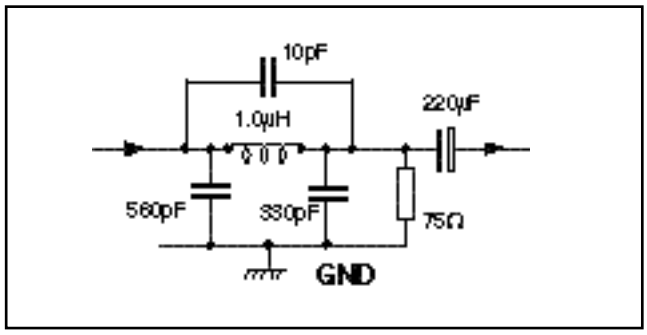


Fig.3 Output reconstruction filter

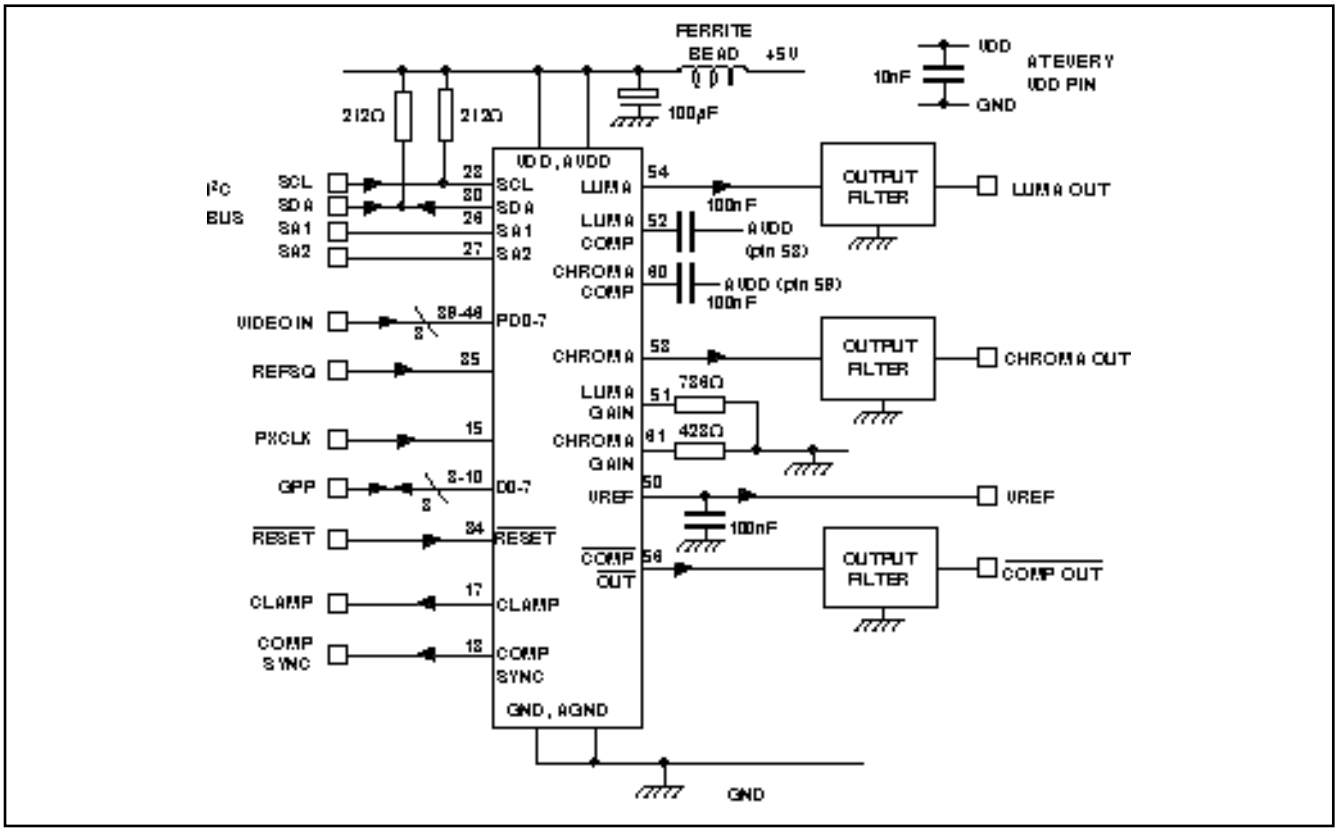


Fig.4 Typical NTSC application diagram, SLAVE mode. (Output filter - see Fig.3)

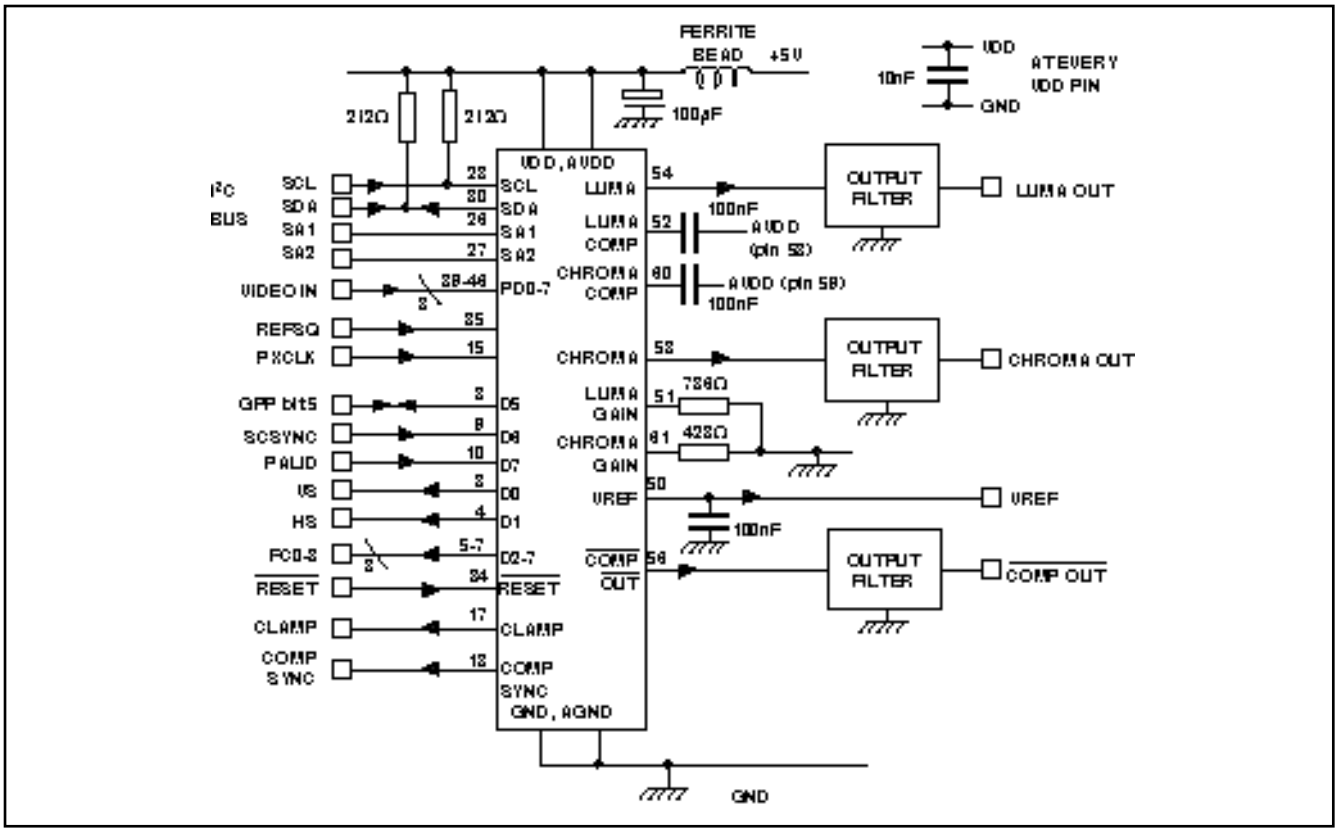
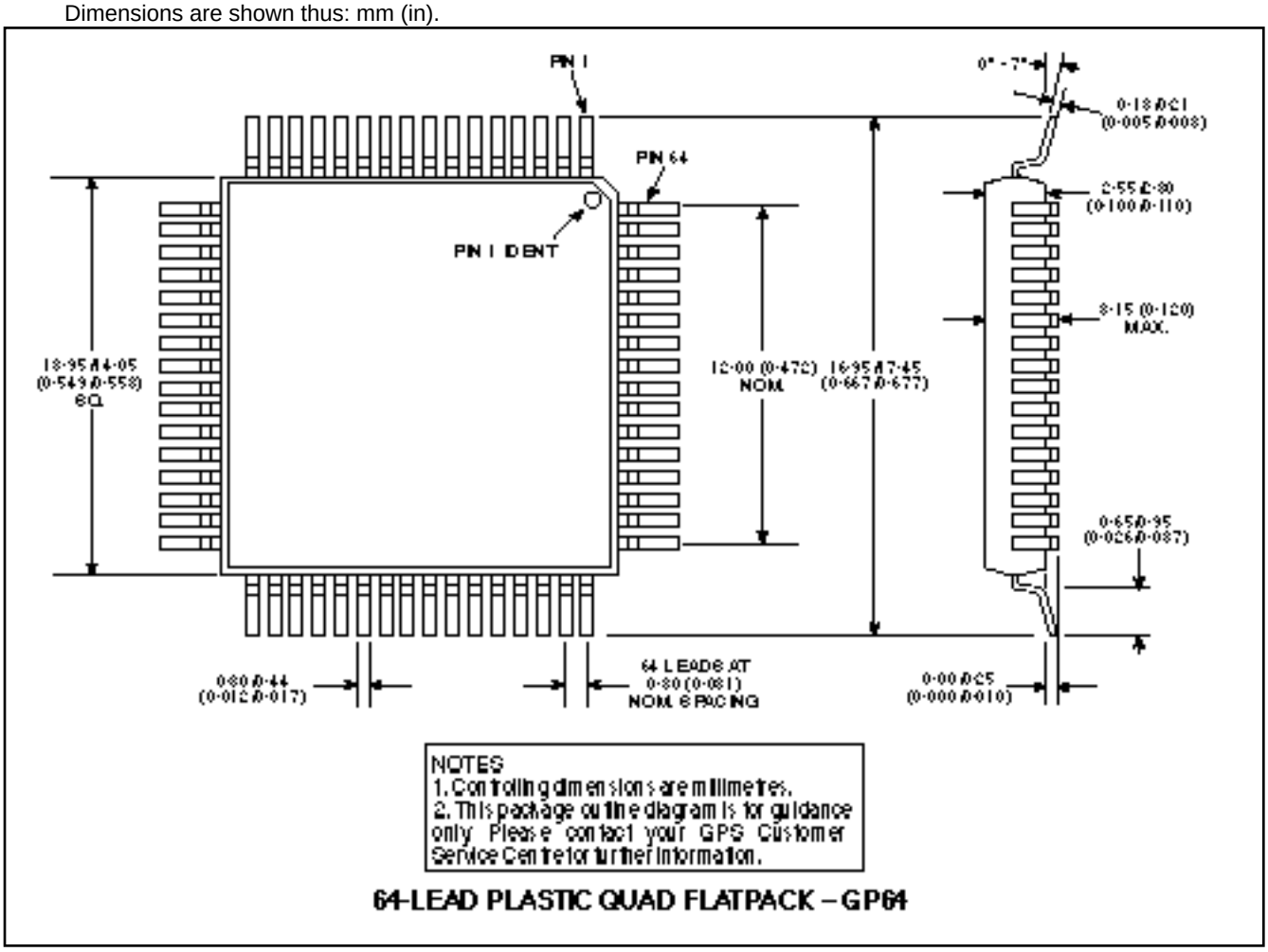


Fig.5 Typical NTSC application diagram, MASTER mode. (Output filter - see Fig.3)

PACKAGE DETAILS

Dimensions are shown thus: mm (in).



64-LEAD PLASTIC QUAD FLATPACK – GP64

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