



VNN7NV04 / VNS7NV04 VND7NV04 / VND7NV04-1

“OMNIFET II”: FULLY AUTOPROTECTED POWER MOSFET

| TYPE | R _{DS(on)} | I _{lim} | V _{clamp} |
|------------|---------------------|------------------|--------------------|
| VNN7NV04 | | | |
| VNS7NV04 | 60 mΩ | 6 A | 40 V |
| VND7NV04 | | | |
| VND7NV04-1 | | | |

- LINEAR CURRENT LIMITATION
- THERMAL SHUT DOWN
- SHORT CIRCUIT PROTECTION
- INTEGRATED CLAMP
- LOW CURRENT DRAWN FROM INPUT PIN
- DIAGNOSTIC FEEDBACK THROUGH INPUT PIN
- ESD PROTECTION
- DIRECT ACCESS TO THE GATE OF THE POWER MOSFET (ANALOG DRIVING)
- COMPATIBLE WITH STANDARD POWER MOSFET

DESCRIPTION

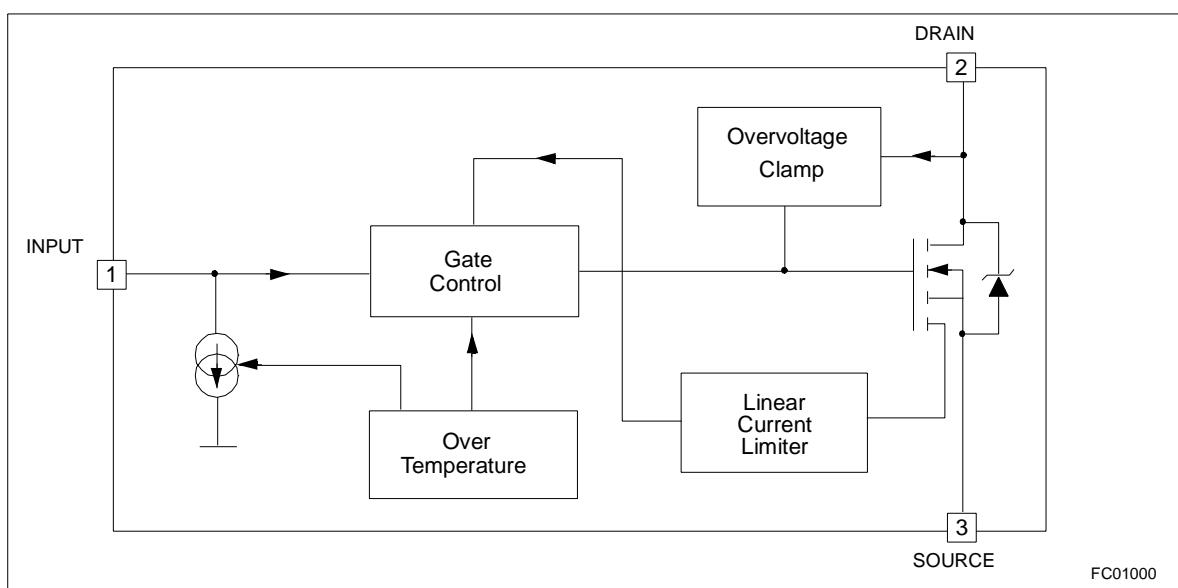
The VNN7NV04, VNS7NV04, VND7NV04 VND7NV04-1, are monolithic devices designed in STMicroelectronics VIPower M0-3 Technology, intended for replacement of standard Power

| PACKAGE | TUBE | T&R |
|---------------|------------|--------------|
| SOT-223 | VNN7NV04 | VNN7NV0413TR |
| SO-8 | VNS7NV04 | VNS7NV0413TR |
| TO-252 (DPAK) | VND7NV04 | VND7NV0413TR |
| TO-251 (IPAK) | VND7NV04-1 | - |

MOSFETS from DC up to 50KHz applications. Built in thermal shutdown, linear current limitation and overvoltage clamp protects the chip in harsh environments.

Fault feedback can be detected by monitoring the voltage at the input pin.

BLOCK DIAGRAM

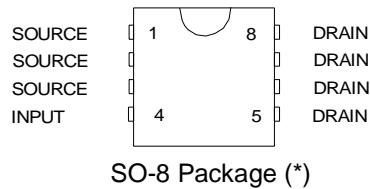


VNN7NV04 / VNS7NV04 / VND7NV04 / VND7NV04-1

ABSOLUTE MAXIMUM RATING

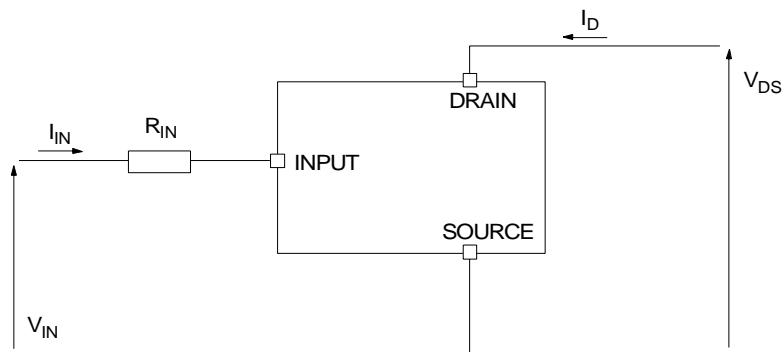
| Symbol | Parameter | Value | | | Unit |
|---------------|--|--------------------|------|-----------|------------|
| | | SOT-223 | SO-8 | DPAK/IPAK | |
| V_{DS} | Drain-source Voltage ($V_{IN}=0V$) | Internally Clamped | | | V |
| V_{IN} | Input Voltage | Internally Clamped | | | V |
| I_{IN} | Input Current | +/-20 | | | mA |
| $R_{IN\ MIN}$ | Minimum Input Series Impedance | 150 | | | Ω |
| I_D | Drain Current | Internally Limited | | | A |
| I_R | Reverse DC Output Current | -10.5 | | | A |
| V_{ESD1} | Electrostatic Discharge ($R=1.5K\Omega$, $C=100pF$) | 4000 | | | V |
| V_{ESD2} | Electrostatic Discharge on output pin only ($R=330\Omega$, $C=150pF$) | 16500 | | | V |
| P_{tot} | Total Dissipation at $T_c=25^\circ C$ | 7 | 4.6 | 60 | W |
| E_{MAX} | Maximum Switching Energy ($L=0.7mH$; $R_L=0\Omega$; $V_{bat}=13.5V$; $T_{jstart}=150^\circ C$; $I_L=9A$) | 40 | | 40 | mJ |
| E_{MAX} | Maximum Switching Energy ($L=0.6mH$; $R_L=0\Omega$; $V_{bat}=13.5V$; $T_{jstart}=150^\circ C$; $I_L=9A$) | | 37 | | mJ |
| T_j | Operating Junction Temperature | Internally limited | | | $^\circ C$ |
| T_c | Case Operating Temperature | Internally limited | | | $^\circ C$ |
| T_{stg} | Storage Temperature | -55 to 150 | | | $^\circ C$ |

CONNECTION DIAGRAM (TOP VIEW)



(*) For the pins configuration related to SOT-223, DPAK, IPAK see outlines at page 1.

CURRENT AND VOLTAGE CONVENTIONS



THERMAL DATA

| Symbol | Parameter | Value | | | | Unit |
|----------------|---|---------|--------|--------|------|------|
| | | SOT-223 | SO-8 | DPAK | IPAK | |
| $R_{thj-case}$ | Thermal Resistance Junction-case MAX | 18 | | 2.1 | 2.1 | °C/W |
| $R_{thj-lead}$ | Thermal Resistance Junction-lead MAX | | 27 | | | °C/W |
| $R_{thj-amb}$ | Thermal Resistance Junction-ambient MAX | 96 (*) | 90 (*) | 65 (*) | 102 | °C/W |

(*) When mounted on a standard single-sided FR4 board with 0.5cm^2 of Cu (at least $35\ \mu\text{m}$ thick) connected to all DRAIN pins.

ELECTRICAL CHARACTERISTICS (-40°C < T_j < 150°C, unless otherwise specified)

OFF

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|-------------|---|--|-----------|-----|-----------|---------------|
| V_{CLAMP} | Drain-source Clamp Voltage | $V_{IN}=0\text{V}; I_D=3.5\text{A}$ | 40 | 45 | 55 | V |
| V_{CLTH} | Drain-source Clamp Threshold Voltage | $V_{IN}=0\text{V}; I_D=2\text{mA}$ | 36 | | | V |
| V_{INTH} | Input Threshold Voltage | $V_{DS}=V_{IN}; I_D=1\text{mA}$ | 0.5 | | 2.5 | V |
| I_{ISS} | Supply Current from Input Pin | $V_{DS}=0\text{V}; V_{IN}=5\text{V}$ | | 100 | 150 | μA |
| V_{INCL} | Input-Source Clamp Voltage | $I_{IN}=1\text{mA}$ $I_{IN}=-1\text{mA}$ | 6 -1.0 | 6.8 | 8 -0.3 | V |
| I_{DSS} | Zero Input Voltage Drain Current ($V_{IN}=0\text{V}$) | $V_{DS}=13\text{V}; V_{IN}=0\text{V}; T_j=25^\circ\text{C}$ $V_{DS}=25\text{V}; V_{IN}=0\text{V}$ | | | 30 75 | μA |

ON

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|--------------|-----------------------------------|--|-----|-----|-----------|------------------|
| $R_{DS(on)}$ | Static Drain-source On Resistance | $V_{IN}=5\text{V}; I_D=3.5\text{A}; T_j=25^\circ\text{C}$ $V_{IN}=5\text{V}; I_D=3.5\text{A}$ | | | 60 120 | $\text{m}\Omega$ |

VNN7NV04 / VNS7NV04 / VND7NV04 / VND7NV04-1

ELECTRICAL CHARACTERISTICS (continued) ($T_j=25^\circ\text{C}$, unless otherwise specified)

DYNAMIC

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|--------------|--------------------------|--|-----|-----|-----|-------------|
| g_{fs} (*) | Forward Transconductance | $V_{DD}=13\text{V}$; $I_D=3.5\text{A}$ | | 9 | | s |
| C_{OSS} | Output Capacitance | $V_{DS}=13\text{V}$; $f=1\text{MHz}$; $V_{IN}=0\text{V}$ | | 220 | | pF |

SWITCHING

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|----------------|-----------------------|---|-----|------|------|------------------------|
| $t_{d(on)}$ | Turn-on Delay Time | $V_{DD}=15\text{V}$; $I_D=3.5\text{A}$ $V_{gen}=5\text{V}$; $R_{gen}=R_{IN \text{ MIN}}=150\Omega$ (see figure 1) | | 100 | 300 | ns |
| t_r | Rise Time | | | 470 | 1500 | ns |
| $t_{d(off)}$ | Turn-off Delay Time | | | 500 | 1500 | ns |
| t_f | Fall Time | | | 350 | 1000 | ns |
| $t_{d(on)}$ | Turn-on Delay Time | $V_{DD}=15\text{V}$; $I_D=3.5\text{A}$ $V_{gen}=5\text{V}$; $R_{gen}=2.2\text{K}\Omega$ (see figure 1) | | 0.75 | 2.3 | μs |
| t_r | Rise Time | | | 4.6 | 14.0 | μs |
| $t_{d(off)}$ | Turn-off Delay Time | | | 5.4 | 16.0 | μs |
| t_f | Fall Time | | | 3.6 | 11.0 | μs |
| $(dl/dt)_{on}$ | Turn-on Current Slope | $V_{DD}=15\text{V}$; $I_D=3.5\text{A}$ $V_{gen}=5\text{V}$; $R_{gen}=R_{IN \text{ MIN}}=150\Omega$ | | 6.5 | | $\text{A}/\mu\text{s}$ |
| Q_i | Total Input Charge | $V_{DD}=12\text{V}$; $I_D=3.5\text{A}$; $V_{IN}=5\text{V}$ $I_{gen}=2.13\text{mA}$ (see figure 5) | | 18 | | nC |

SOURCE DRAIN DIODE

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|--------------|--------------------------|---|-----|------|-----|---------------|
| V_{SD} (*) | Forward On Voltage | $I_{SD}=3.5\text{A}$; $V_{IN}=0\text{V}$ | | 0.8 | | V |
| t_{rr} | Reverse Recovery Time | $I_{SD}=3.5\text{A}$; $dl/dt=20\text{A}/\mu\text{s}$ | | 220 | | ns |
| Q_{rr} | Reverse Recovery Charge | $V_{DD}=30\text{V}$; $L=200\mu\text{H}$ | | 0.28 | | μC |
| I_{RRM} | Reverse Recovery Current | (see test circuit, figure 2) | | 2.5 | | A |

PROTECTIONS (-40°C < T_j < 150°C, unless otherwise specified)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|------------|-------------------------------|---|-----|-----|-----|------------------|
| I_{lim} | Drain Current Limit | $V_{IN}=5\text{V}$; $V_{DS}=13\text{V}$ | 6 | 9 | 12 | A |
| t_{dlim} | Step Response Current Limit | $V_{IN}=5\text{V}$; $V_{DS}=13\text{V}$ | | 4.0 | | μs |
| T_{jsh} | Overtemperature Shutdown | | 150 | 175 | 200 | $^\circ\text{C}$ |
| T_{jrs} | Overtemperature Reset | | 135 | | | $^\circ\text{C}$ |
| I_{gf} | Fault Sink Current | $V_{IN}=5\text{V}$; $V_{DS}=13\text{V}$; $T_j=T_{jsh}$ starting $T_j=25^\circ\text{C}$; $V_{DD}=24\text{V}$ | | 15 | | mA |
| E_{as} | Single Pulse Avalanche Energy | $V_{IN}=5\text{V}$; $R_{gen}=R_{IN \text{ MIN}}=150\Omega$; $L=24\text{mH}$ (see figures 3 & 4) | 200 | | | mJ |

(*) Pulsed: Pulse duration = 300μs, duty cycle 1.5%

PROTECTION FEATURES

During normal operation, the INPUT pin is electrically connected to the gate of the internal power MOSFET through a low impedance path.

The device then behaves like a standard power MOSFET and can be used as a switch from DC to 50KHz. The only difference from the user's standpoint is that a small DC current I_{ISS} (typ. 100 μ A) flows into the INPUT pin in order to supply the internal circuitry.

The device integrates:

- OVERVOLTAGE CLAMP PROTECTION: internally set at 45V, along with the rugged avalanche characteristics of the Power MOSFET stage give this device unrivalled ruggedness and energy handling capability. This feature is mainly important when driving inductive loads.

- LINEAR CURRENT LIMITER CIRCUIT: limits the drain current I_D to I_{lim} whatever the INPUT pin voltage. When the current limiter is active, the device operates in the linear region, so power dissipation may exceed the capability of the heatsink. Both case and junction temperatures increase, and if this phase lasts long enough, junction temperature may reach the overtemperature threshold T_{jsh} .

- OVERTEMPERRATURE AND SHORT CIRCUIT PROTECTION: these are based on sensing the chip temperature and are not dependent on the input voltage. The location of the sensing element on the chip in the power stage area ensures fast, accurate detection of the junction temperature. Overtemperature cut-out occurs in the range 150 to 190 °C, a typical value being 170 °C. The device is automatically restarted when the chip temperature falls of about 15°C below shut-down temperature.

- STATUS FEEDBACK: in the case of an overtemperature fault condition ($T_j > T_{jsh}$), the device tries to sink a diagnostic current I_{gf} through the INPUT pin in order to indicate fault condition. If driven from a low impedance source, this current may be used in order to warn the control circuit of a device shutdown. If the drive impedance is high enough so that the INPUT pin driver is not able to supply the current I_{gf} , the INPUT pin will fall to 0V. **This will not however affect the device operation: no requirement is put on the current capability of the INPUT pin driver except to be able to supply the normal operation drive current I_{ISS} .**

Additional features of this device are ESD protection according to the Human Body model and the ability to be driven from a TTL Logic circuit.

VNN7NV04 / VNS7NV04 / VND7NV04 / VND7NV04-1

Figure 1: Switching Time Test Circuit for Resistive Load

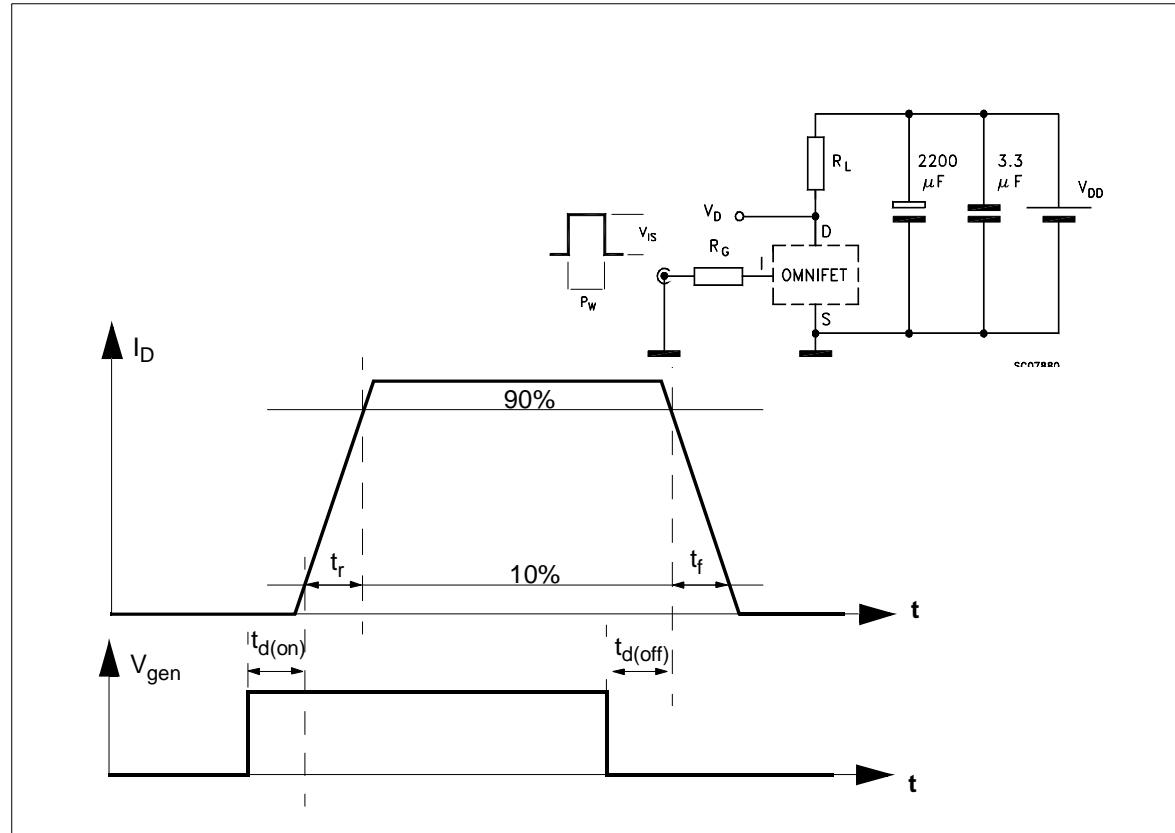
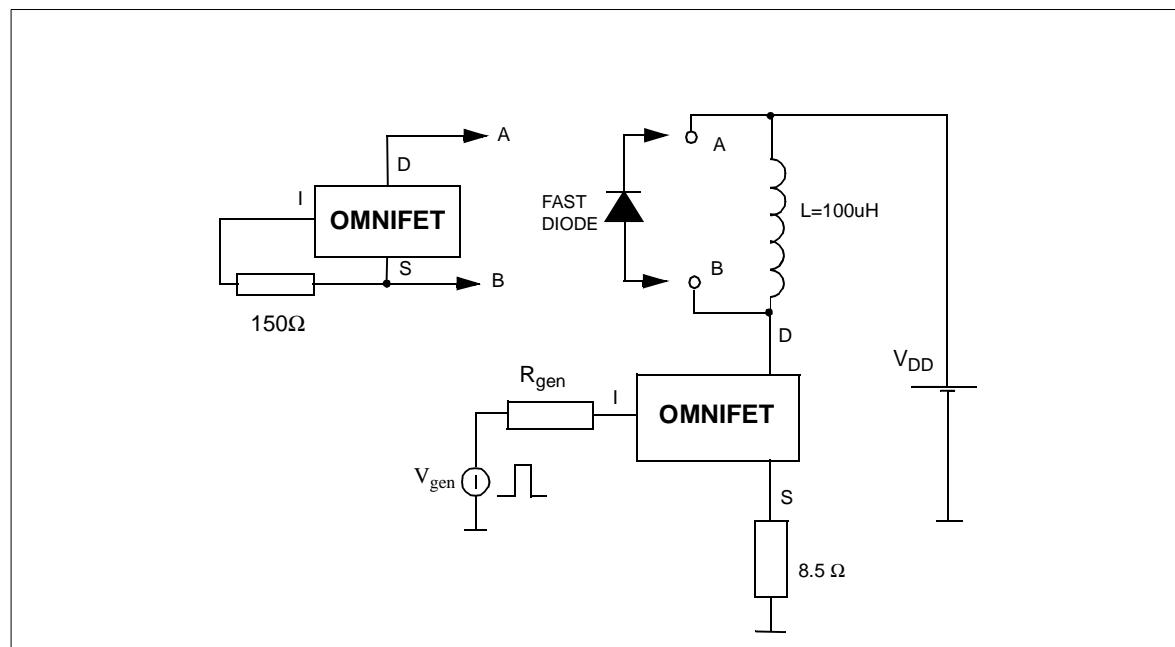


Figure 2: Test Circuit for Diode Recovery Times



VNN7NV04 / VNS7NV04 / VND7NV04 / VND7NV04-1

Figure 3: Unclamped Inductive Load Test Circuits

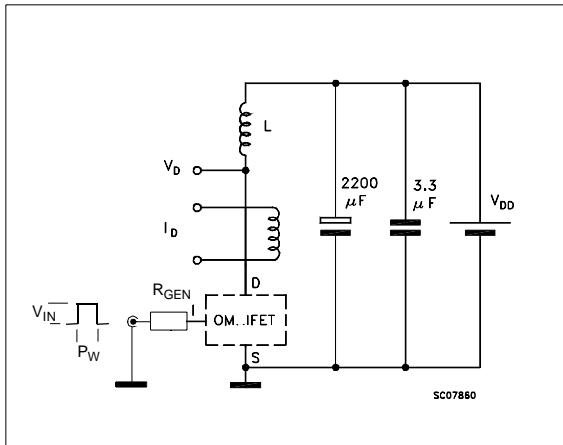


Figure 4: Unclamped Inductive Waveforms

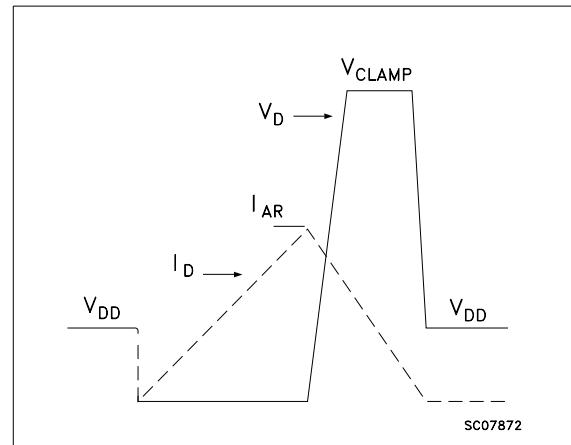
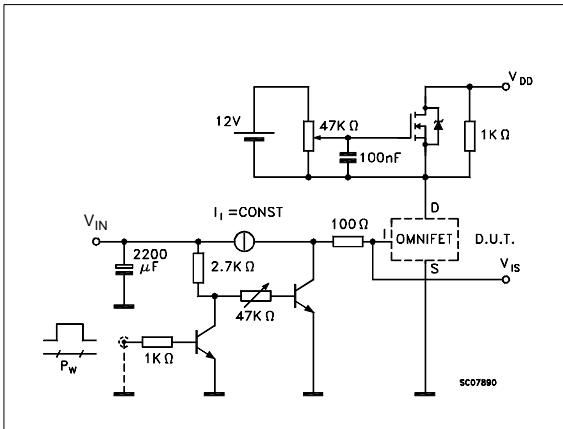
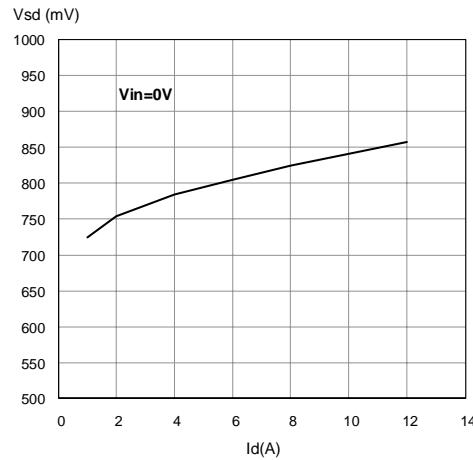


Figure 5: Input Charge Test Circuit

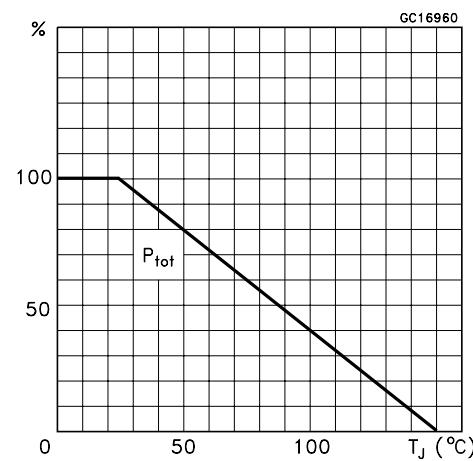


VNN7NV04 / VNS7NV04 / VND7NV04 / VND7NV04-1

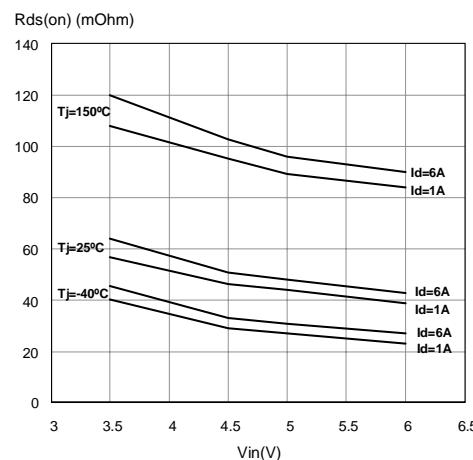
Source-Drain Diode Forward Characteristics



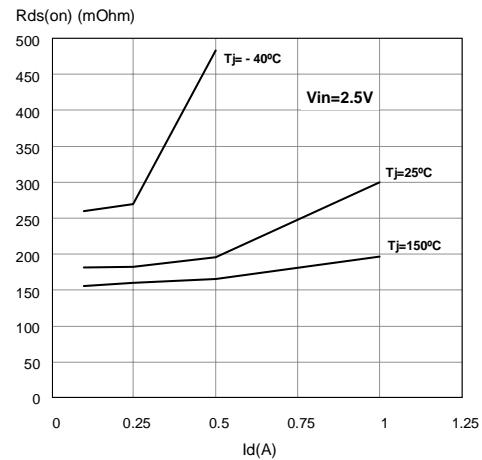
Derating Curve



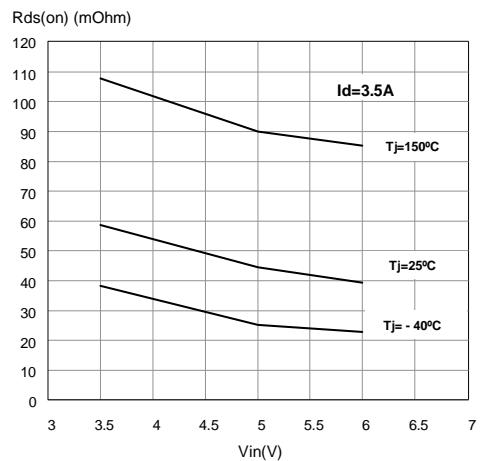
Static Drain-Source On resistance Vs. Input Voltage



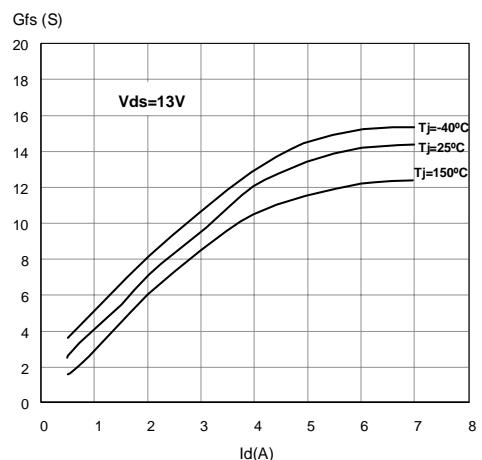
Static Drain Source On Resistance



Static Drain-Source On resistance Vs. Input Voltage

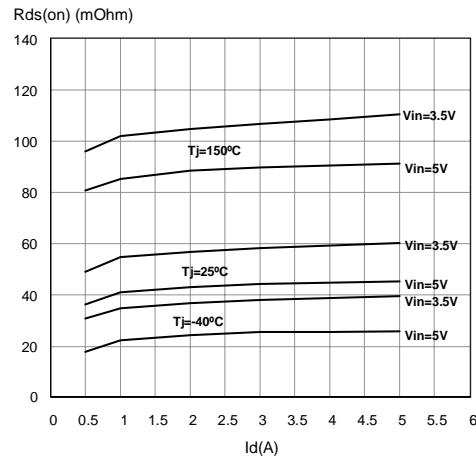


Transconductance

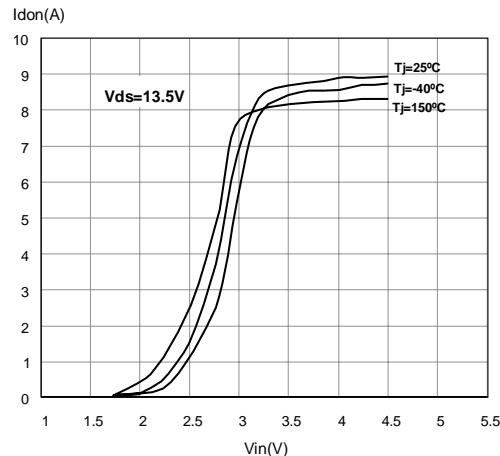


VNN7NV04 / VNS7NV04 / VND7NV04 / VND7NV04-1

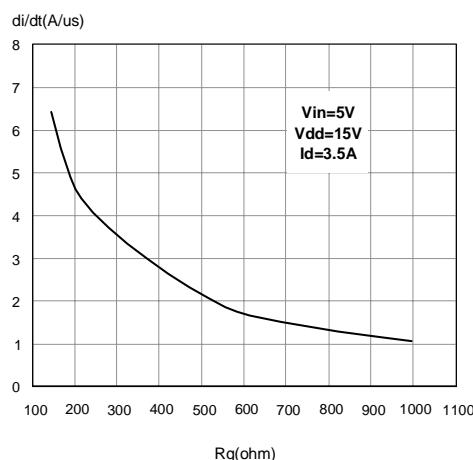
Static Drain-Source On Resistance Vs. Id



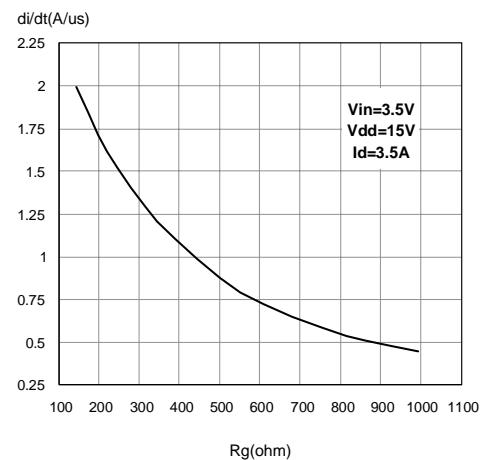
Transfer Characteristics



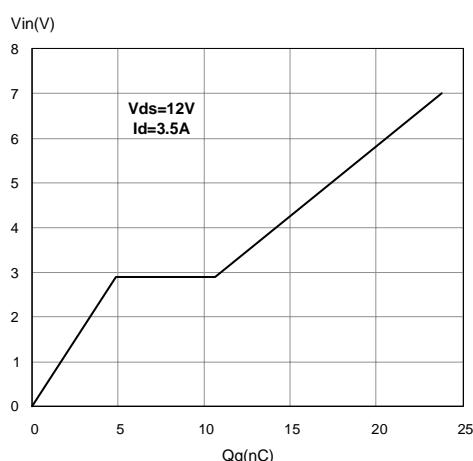
Turn On Current Slope



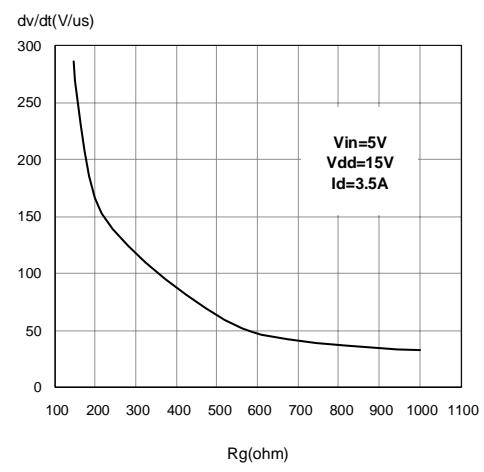
Turn On Current Slope



Input Voltage Vs. Input Charge

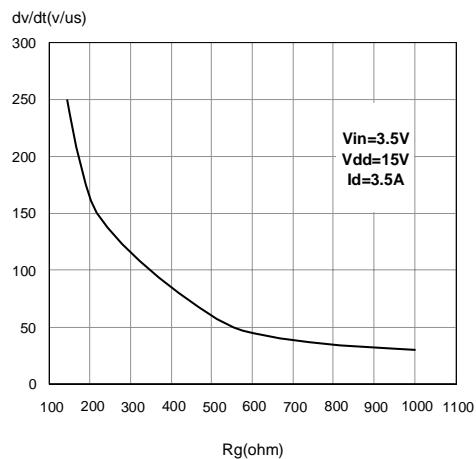


Turn off drain source voltage slope

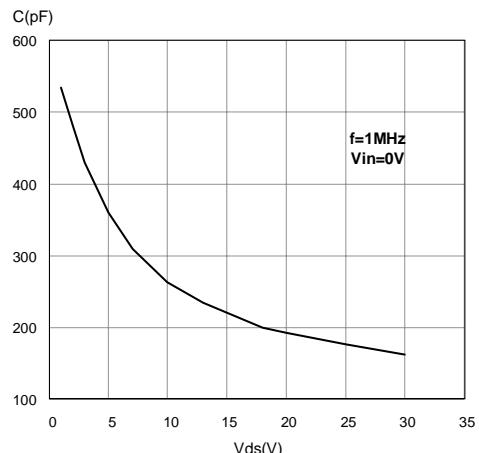


VNN7NV04 / VNS7NV04 / VND7NV04 / VND7NV04-1

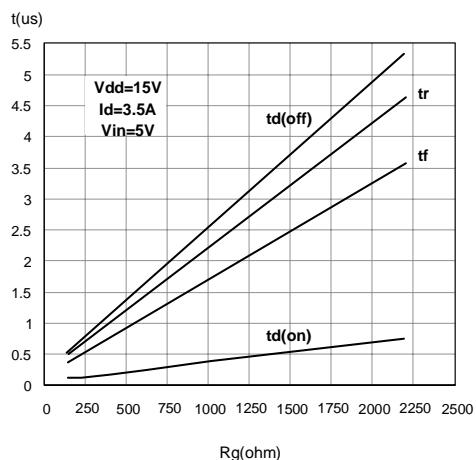
Turn Off Drain-Source Voltage Slope



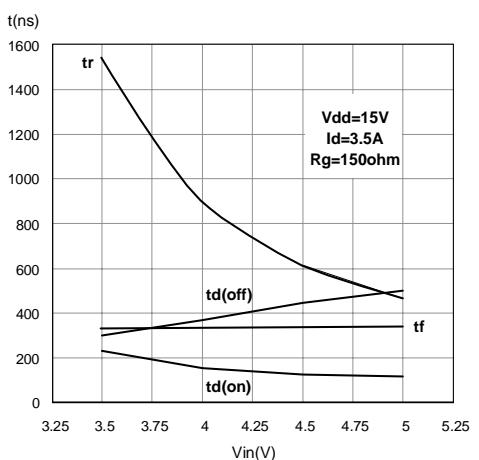
Capacitance Variations



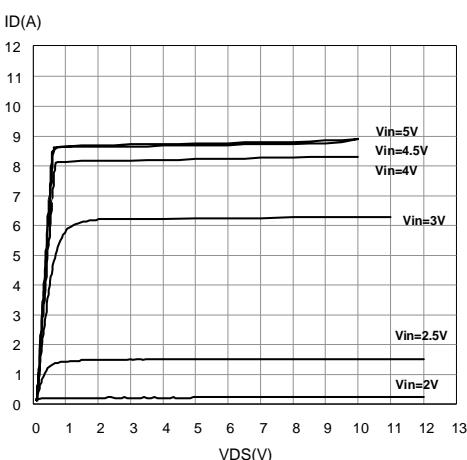
Switching Time Resistive Load



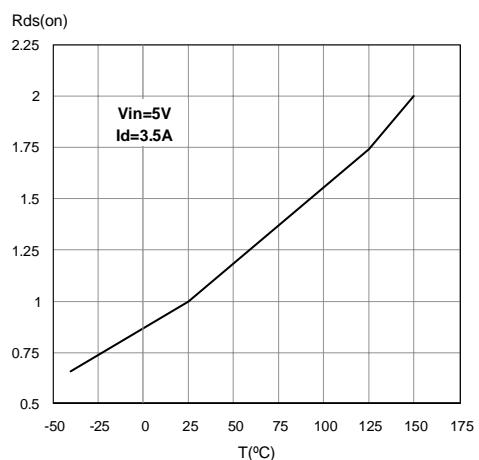
Switching Time Resistive Load



Output Characteristics

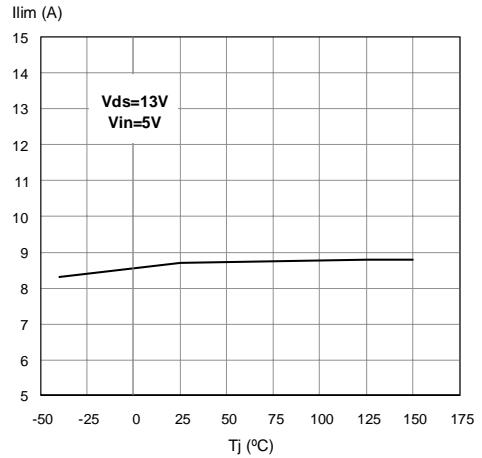
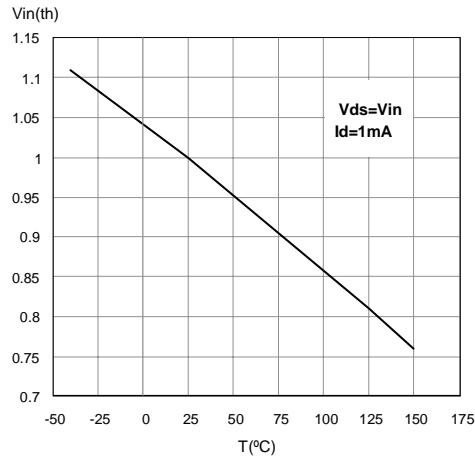


Normalized On Resistance Vs. Temperature

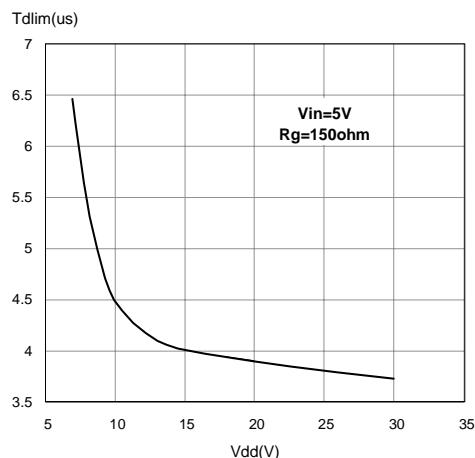


VNN7NV04 / VNS7NV04 / VND7NV04 / VND7NV04-1

Normalized Input Threshold Voltage Vs. Current Limit Vs. Junction Temperature

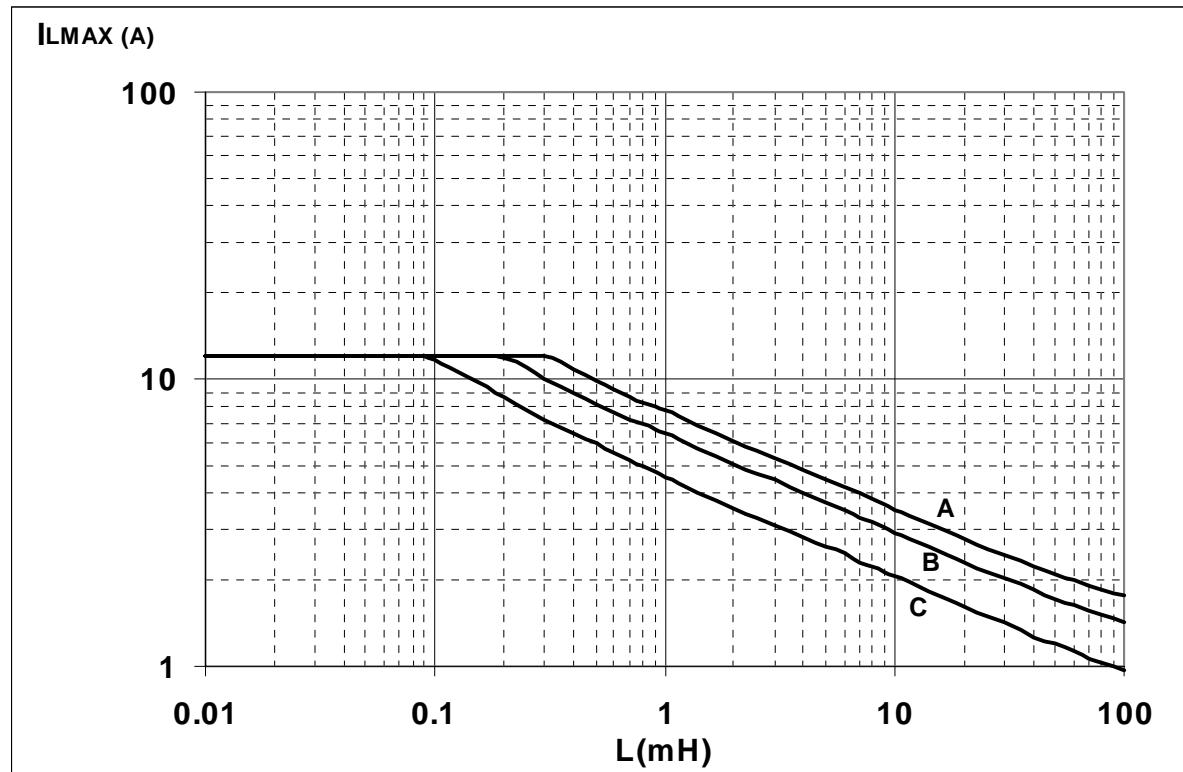


Step Response Current Limit



VNN7NV04 / VNS7NV04 / VND7NV04 / VND7NV04-1

SO-8 Maximum turn off current versus load inductance



A = Single Pulse at $T_{j\text{start}}=150^\circ\text{C}$

B= Repetitive pulse at $T_{j\text{start}}=100^\circ\text{C}$

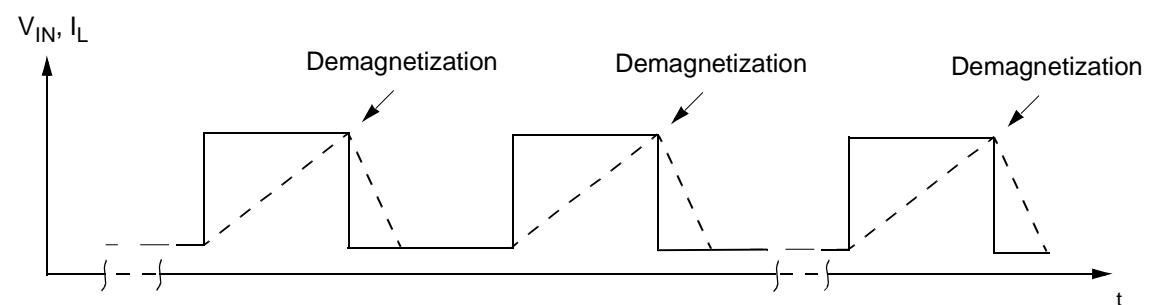
C= Repetitive Pulse at $T_{j\text{start}}=125^\circ\text{C}$

Conditions:

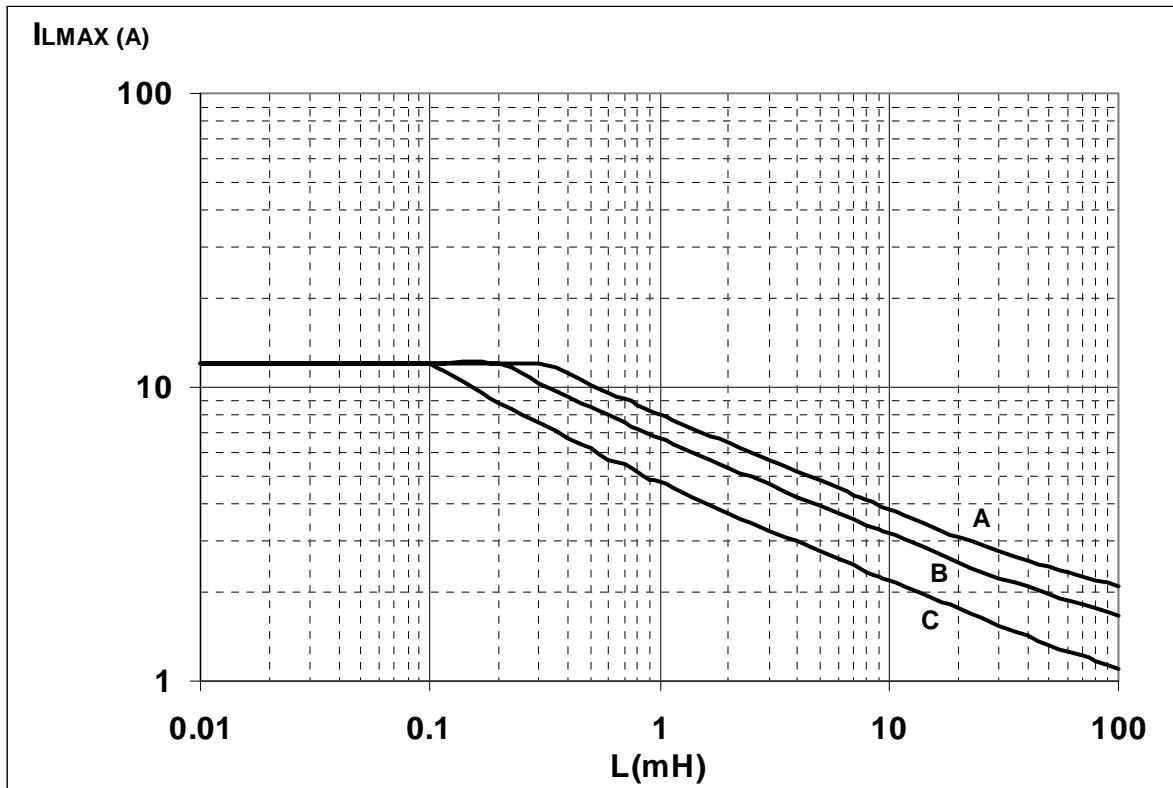
$V_{CC}=13.5\text{V}$

Values are generated with $R_L=0\Omega$

In case of repetitive pulses, $T_{j\text{start}}$ (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.



DPAK Maximum turn off current versus load inductance



A = Single Pulse at $T_{j\text{start}}=150^\circ\text{C}$

B= Repetitive pulse at $T_{j\text{start}}=100^\circ\text{C}$

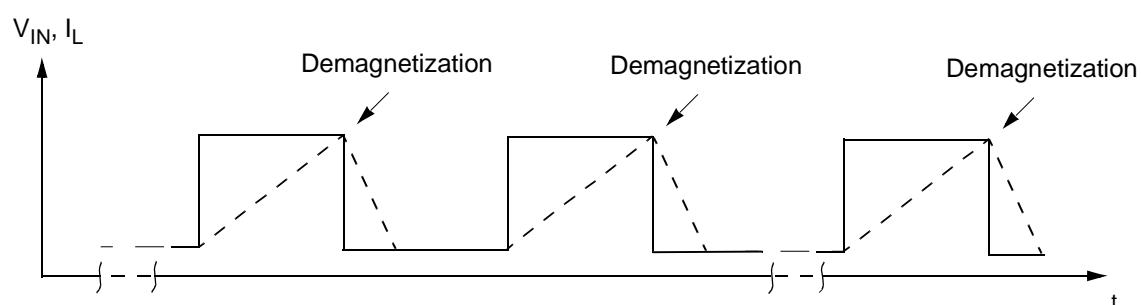
C= Repetitive Pulse at $T_{j\text{start}}=125^\circ\text{C}$

Conditions:

$V_{CC}=13.5\text{V}$

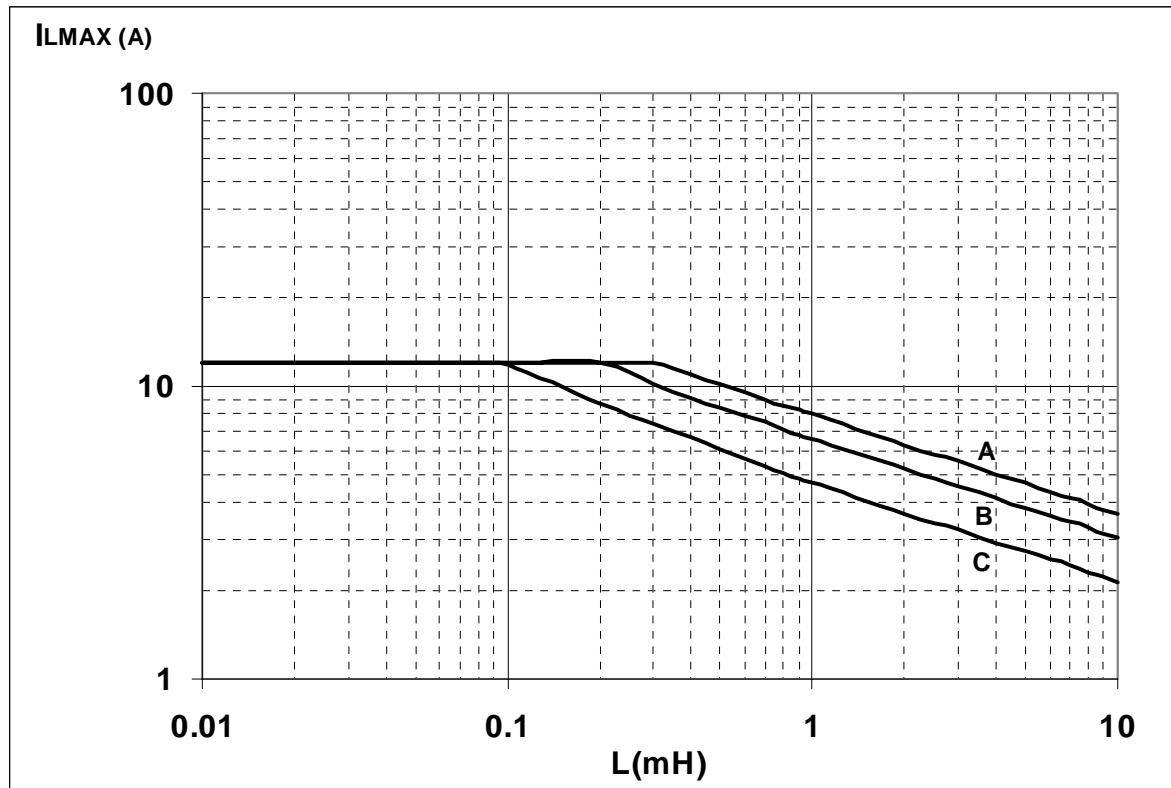
Values are generated with $R_L=0\Omega$

In case of repetitive pulses, $T_{j\text{start}}$ (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.



VNN7NV04 / VNS7NV04 / VND7NV04 / VND7NV04-1

SOT-223 Maximum turn off current versus load inductance



A = Single Pulse at $T_{jstart}=150^{\circ}\text{C}$

B= Repetitive pulse at $T_{jstart}=100^{\circ}\text{C}$

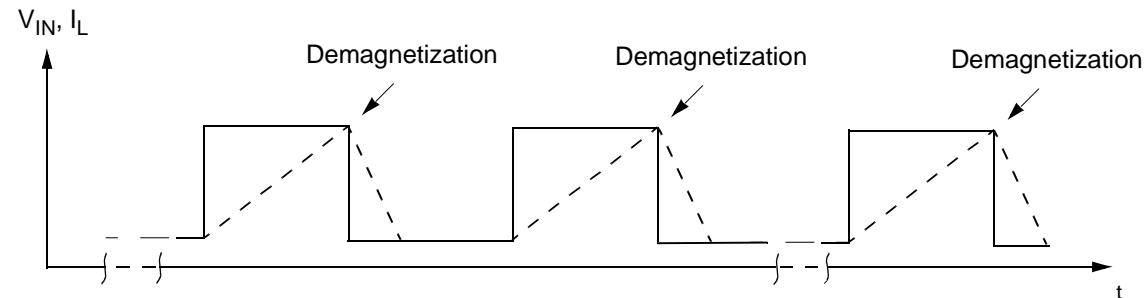
C= Repetitive Pulse at $T_{jstart}=125^{\circ}\text{C}$

Conditions:

$V_{CC}=13.5\text{V}$

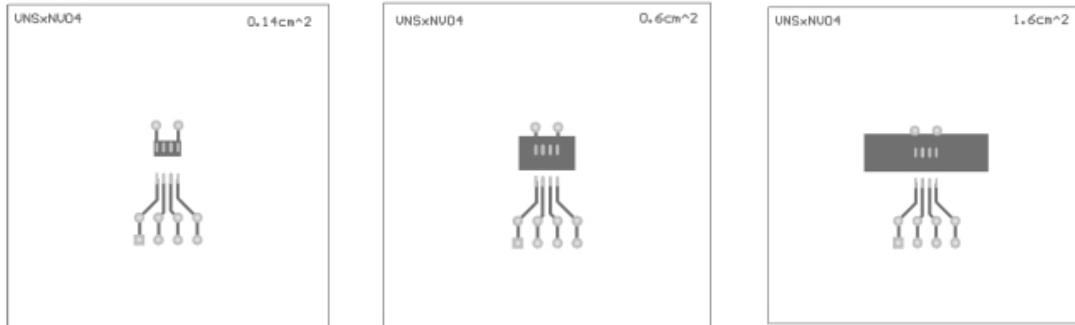
Values are generated with $R_L=0\Omega$

In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.



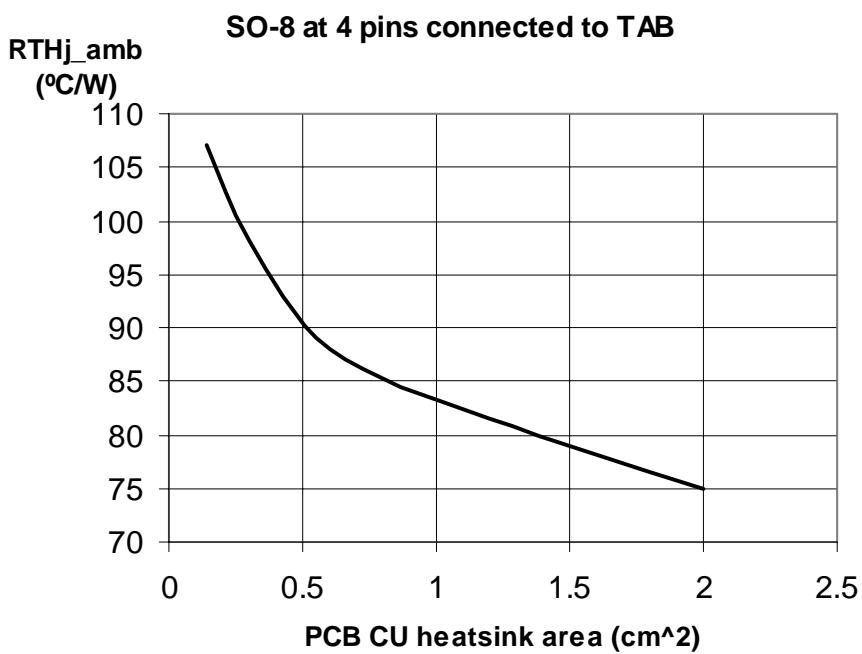
SO-8 THERMAL DATA

SO-8 PC Board



Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area= 58mm x 58mm, PCB thickness=2mm, Cu thickness=35 μ m, Copper areas: 0.14cm 2 , 0.6cm 2 , 1.6cm 2).

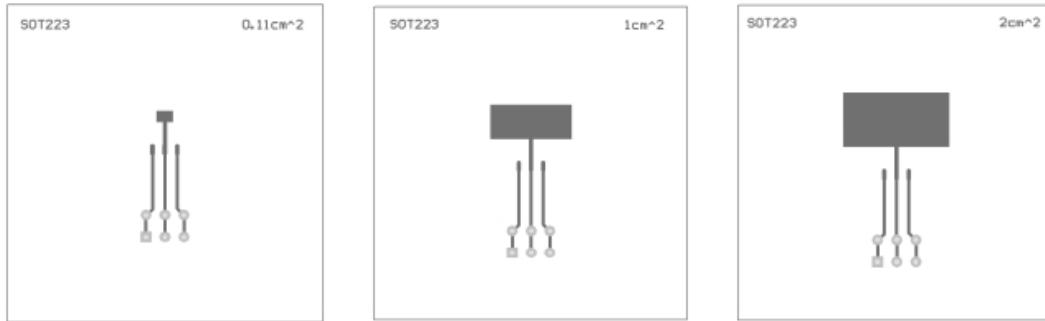
R_{thj_amb} Vs PCB copper area in open box free air condition



VNN7NV04 / VNS7NV04 / VND7NV04 / VND7NV04-1

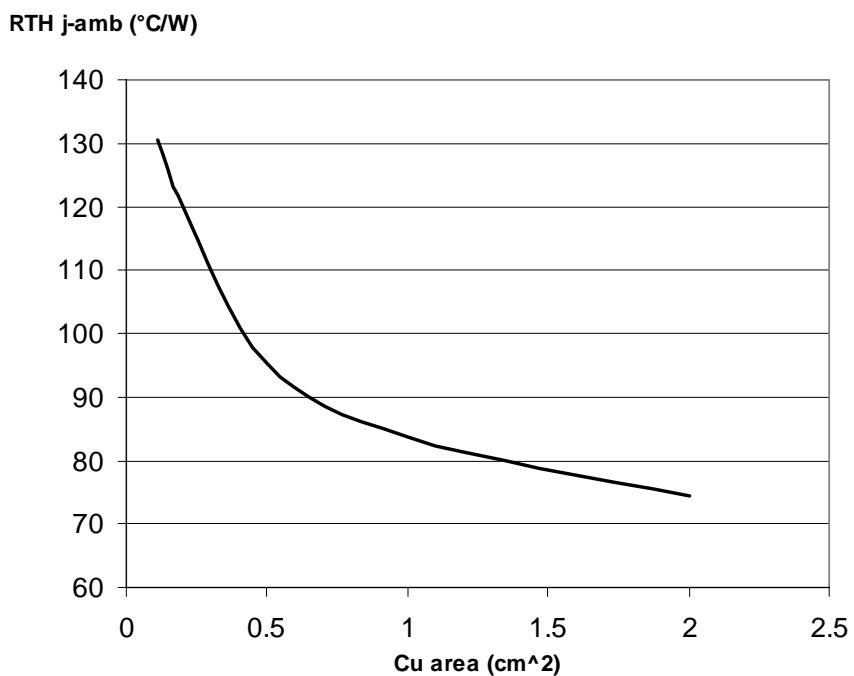
SOT-223 THERMAL DATA

SOT-223 PC Board



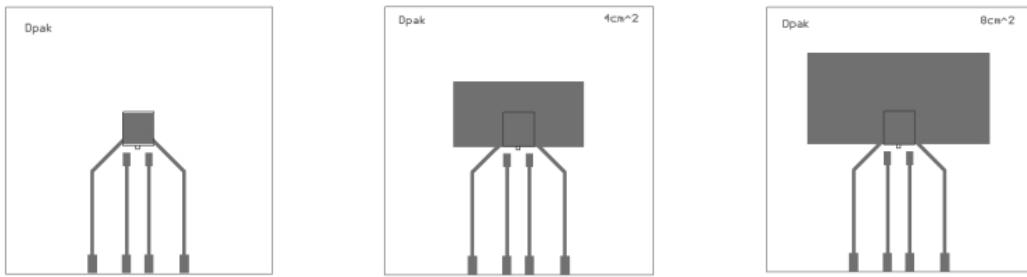
Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area= 58mm x 58mm, PCB thickness=2mm, Cu thickness=35μm, Copper areas: 0.11cm², 1cm², 2cm²).

$R_{thj-amb}$ Vs PCB copper area in open box free air condition



DPAK THERMAL DATA

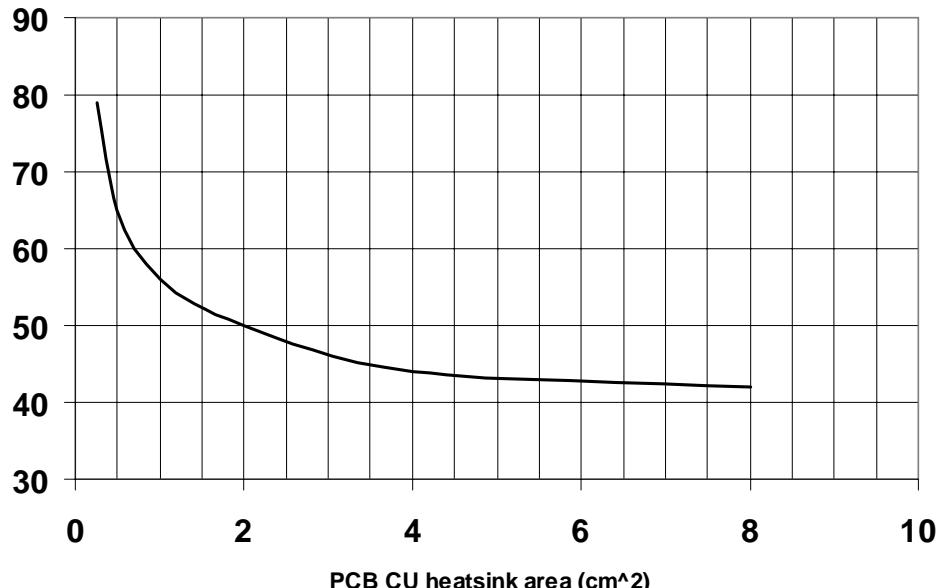
DPAK PC Board



Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area= 60mm x 60mm, PCB thickness=2mm, Cu thickness=35μm, Copper areas: from minimum pad lay-out to 8cm²).

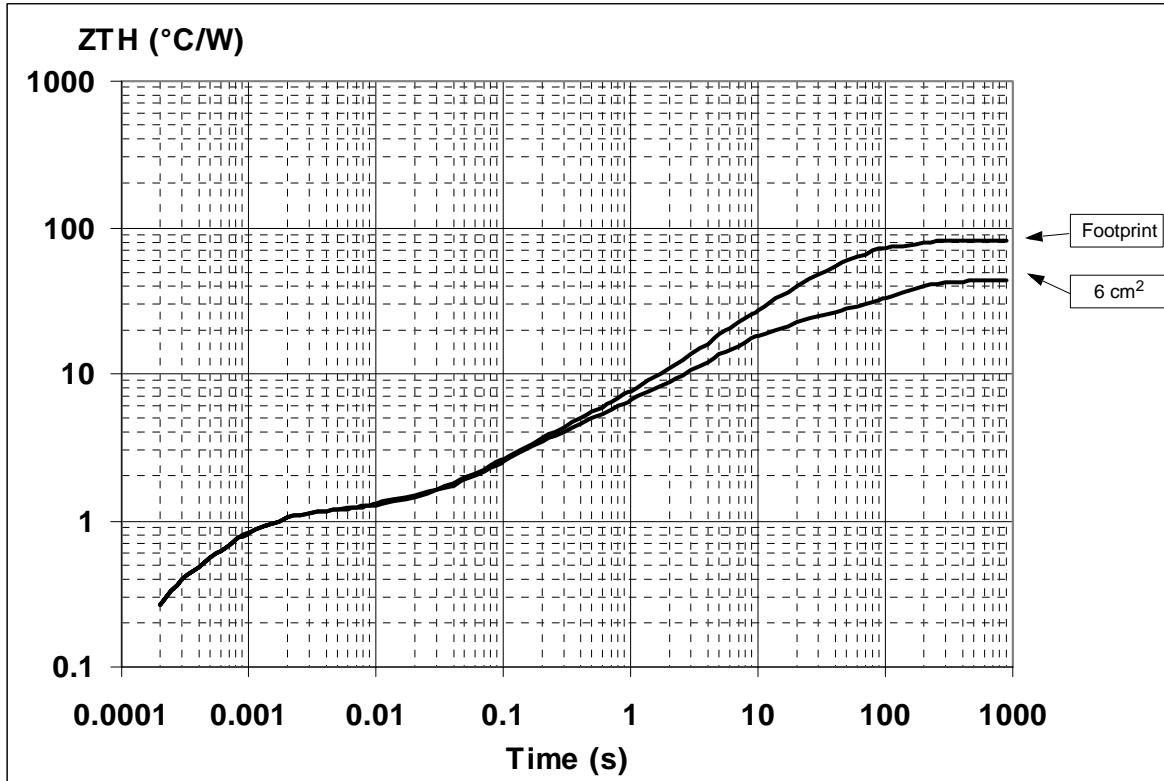
$R_{th,j-amb}$ Vs PCB copper area in open box free air condition

R_{TH,j_amb} (°C/W)

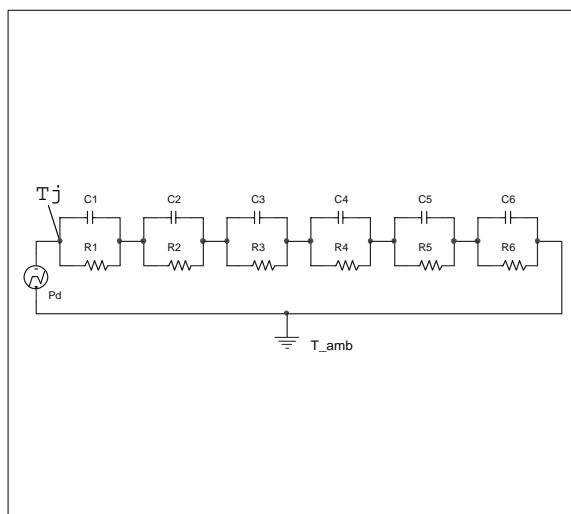


VNN7NV04 / VNS7NV04 / VND7NV04 / VND7NV04-1

DPAK Thermal Impedance Junction Ambient Single Pulse



Thermal fitting model of an OMNIFET II in DPAK



Pulse calculation formula

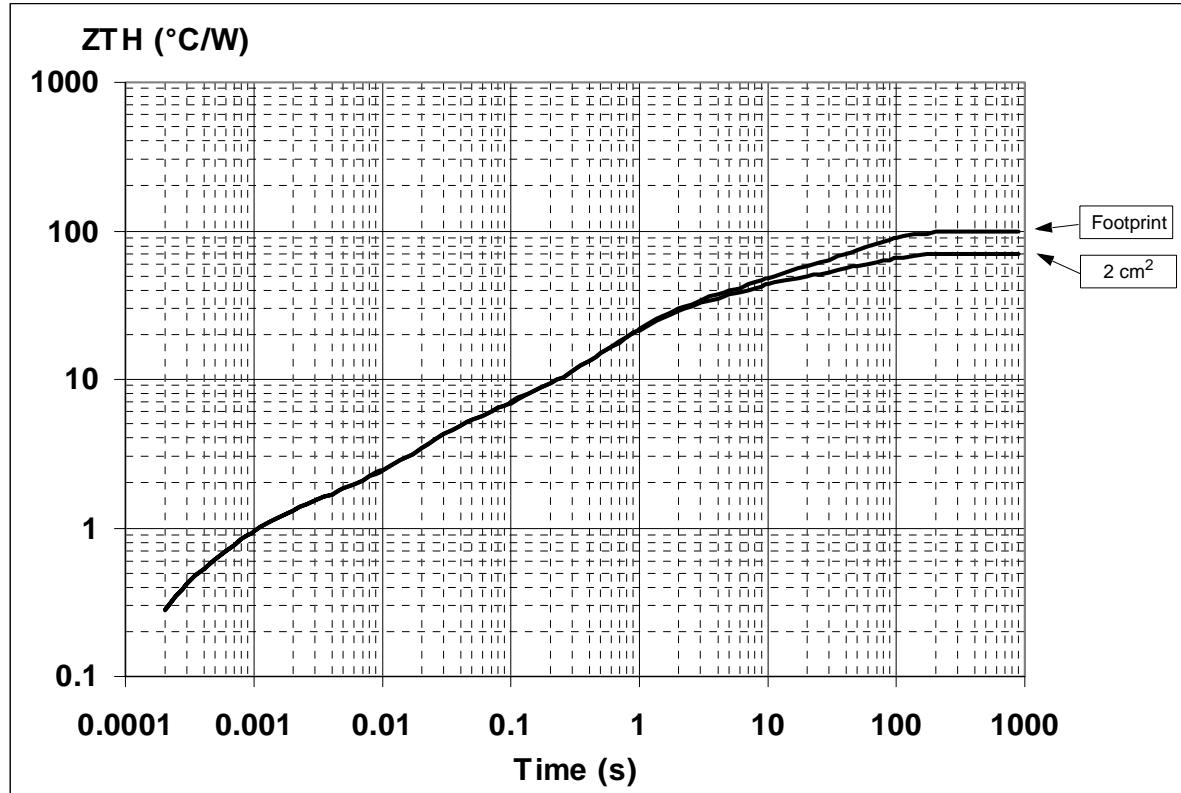
$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

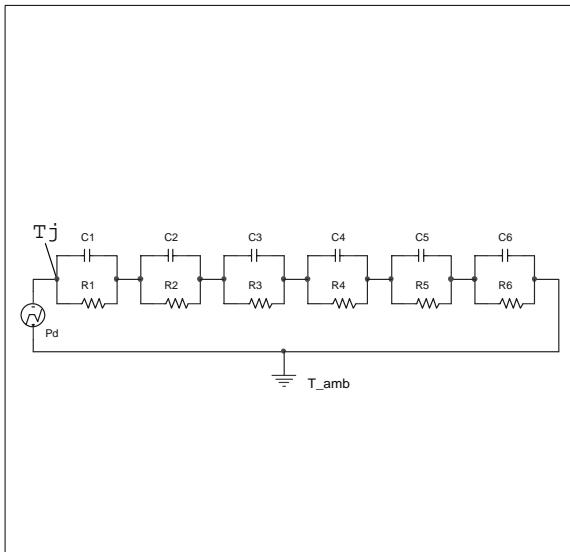
Thermal Parameter

| Area/island (cm^2) | Footprint | 6 |
|---|-----------|----|
| R_1 ($^{\circ}\text{C}/\text{W}$) | 0.1 | |
| R_2 ($^{\circ}\text{C}/\text{W}$) | 0.35 | |
| R_3 ($^{\circ}\text{C}/\text{W}$) | 1.20 | |
| R_4 ($^{\circ}\text{C}/\text{W}$) | 2 | |
| R_5 ($^{\circ}\text{C}/\text{W}$) | 15 | |
| R_6 ($^{\circ}\text{C}/\text{W}$) | 61 | 24 |
| C_1 ($\text{W.s}/^{\circ}\text{C}$) | 0.0006 | |
| C_2 ($\text{W.s}/^{\circ}\text{C}$) | 0.0021 | |
| C_3 ($\text{W.s}/^{\circ}\text{C}$) | 0.05 | |
| C_4 ($\text{W.s}/^{\circ}\text{C}$) | 0.3 | |
| C_5 ($\text{W.s}/^{\circ}\text{C}$) | 0.45 | |
| C_6 ($\text{W.s}/^{\circ}\text{C}$) | 0.8 | 5 |

SO-8 Thermal Impedance Junction Ambient Single Pulse



Thermal fitting model of an OMNIFET II in SO-8



Pulse calculation formula

$$Z_{\text{TH}\delta} = R_{\text{TH}} \cdot \delta + Z_{\text{THtp}}(1 - \delta)$$

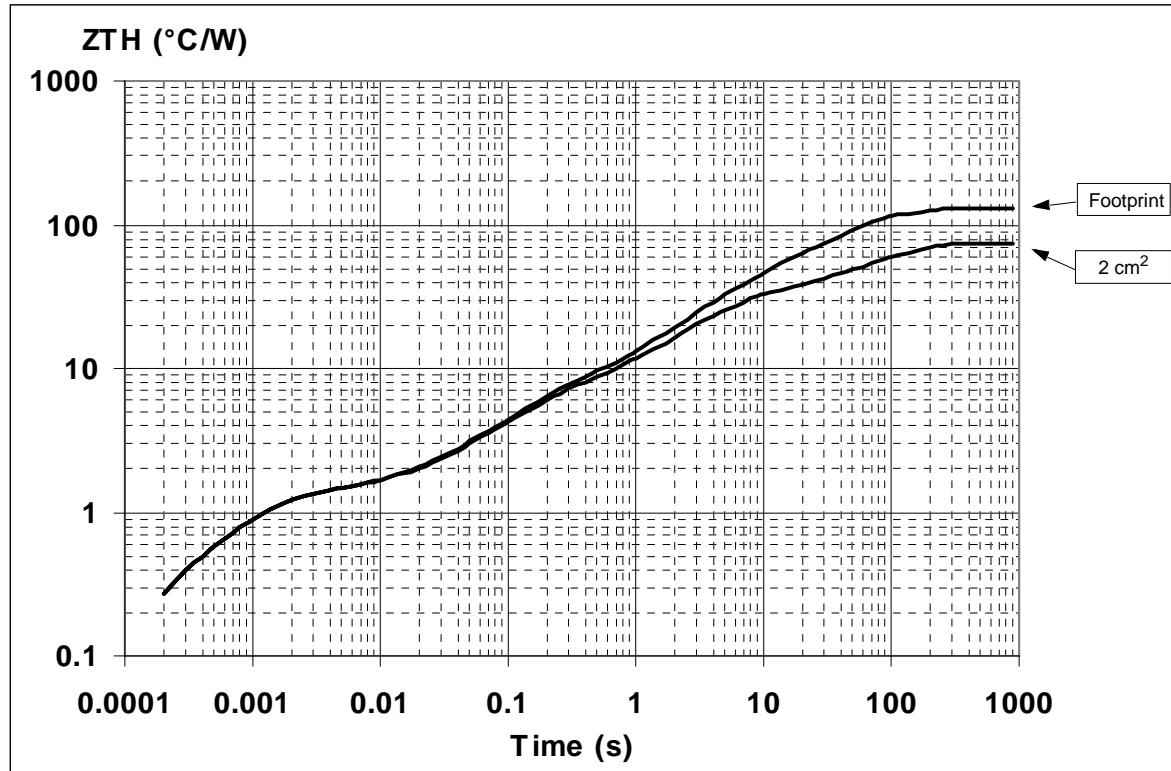
where $\delta = t_p/T$

Thermal Parameter

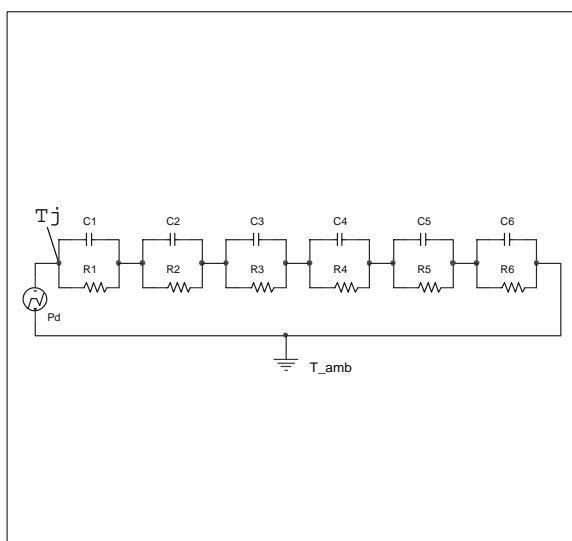
| Area/island (cm^2) | Footprint | 2 |
|--------------------------------------|-----------|----|
| R1 ($^{\circ}\text{C}/\text{W}$) | 0.2 | |
| R2 ($^{\circ}\text{C}/\text{W}$) | 0.9 | |
| R3 ($^{\circ}\text{C}/\text{W}$) | 3.5 | |
| R4 ($^{\circ}\text{C}/\text{W}$) | 21 | |
| R5 ($^{\circ}\text{C}/\text{W}$) | 16 | |
| R6 ($^{\circ}\text{C}/\text{W}$) | 58 | 28 |
| C1 ($\text{W.s}/^{\circ}\text{C}$) | 3.00E-04 | |
| C2 ($\text{W.s}/^{\circ}\text{C}$) | 9.00E-04 | |
| C3 ($\text{W.s}/^{\circ}\text{C}$) | 7.50E-03 | |
| C4 ($\text{W.s}/^{\circ}\text{C}$) | 0.045 | |
| C5 ($\text{W.s}/^{\circ}\text{C}$) | 0.35 | |
| C6 ($\text{W.s}/^{\circ}\text{C}$) | 1.05 | 2 |

VNN7NV04 / VNS7NV04 / VND7NV04 / VND7NV04-1

SOT-223 Thermal Impedance Junction Ambient Single Pulse



Thermal fitting model of an OMNIFET II in SOT-223



Pulse calculation formula

$$Z_{\text{TH}\delta} = R_{\text{TH}} \cdot \delta + Z_{\text{THtp}}(1 - \delta)$$

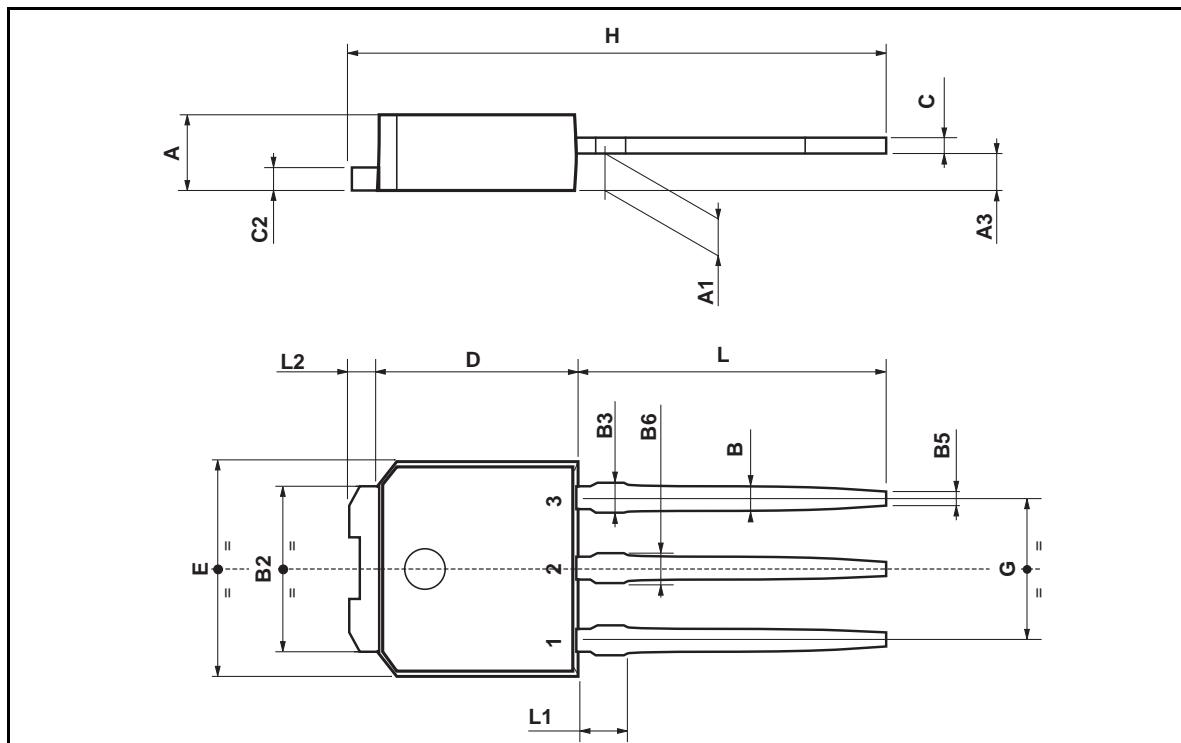
where $\delta = t_p/T$

Thermal Parameter

| Area/island (cm^2) | Footprint | 2 |
|---|-----------|----|
| R1 ($^{\circ}\text{C}/\text{W}$) | 0.2 | |
| R2 ($^{\circ}\text{C}/\text{W}$) | 1.1 | |
| R3 ($^{\circ}\text{C}/\text{W}$) | 4.5 | |
| R4 ($^{\circ}\text{C}/\text{W}$) | 24 | |
| R5 ($^{\circ}\text{C}/\text{W}$) | 0.1 | |
| R6 ($^{\circ}\text{C}/\text{W}$) | 100 | 45 |
| C1 ($\text{W} \cdot \text{s}/^{\circ}\text{C}$) | 3.00E-04 | |
| C2 ($\text{W} \cdot \text{s}/^{\circ}\text{C}$) | 9.00E-04 | |
| C3 ($\text{W} \cdot \text{s}/^{\circ}\text{C}$) | 3.00E-02 | |
| C4 ($\text{W} \cdot \text{s}/^{\circ}\text{C}$) | 0.16 | |
| C5 ($\text{W} \cdot \text{s}/^{\circ}\text{C}$) | 1000 | |
| C6 ($\text{W} \cdot \text{s}/^{\circ}\text{C}$) | 0.5 | 2 |

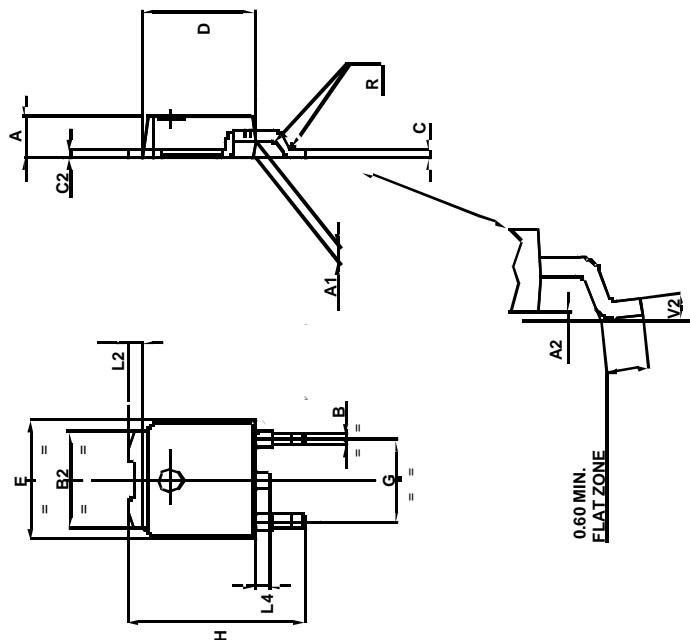
TO-251 (IPAK) MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|------|------|-----|------|-------|-------|-------|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | 2.2 | | 2.4 | 0.086 | | 0.094 |
| A1 | 0.9 | | 1.1 | 0.035 | | 0.043 |
| A3 | 0.7 | | 1.3 | 0.027 | | 0.051 |
| B | 0.64 | | 0.9 | 0.025 | | 0.031 |
| B2 | 5.2 | | 5.4 | 0.204 | | 0.212 |
| B3 | | | 0.85 | | | 0.033 |
| B5 | | 0.3 | | | 0.012 | |
| B6 | | | 0.95 | | | 0.037 |
| C | 0.45 | | 0.6 | 0.017 | | 0.023 |
| C2 | 0.48 | | 0.6 | 0.019 | | 0.023 |
| D | 6 | | 6.2 | 0.236 | | 0.244 |
| E | 6.4 | | 6.6 | 0.252 | | 0.260 |
| G | 4.4 | | 4.6 | 0.173 | | 0.181 |
| H | 15.9 | | 16.3 | 0.626 | | 0.641 |
| L | 9 | | 9.4 | 0.354 | | 0.370 |
| L1 | 0.8 | | 1.2 | 0.031 | | 0.047 |
| L2 | | 0.8 | 1 | | 0.031 | 0.039 |



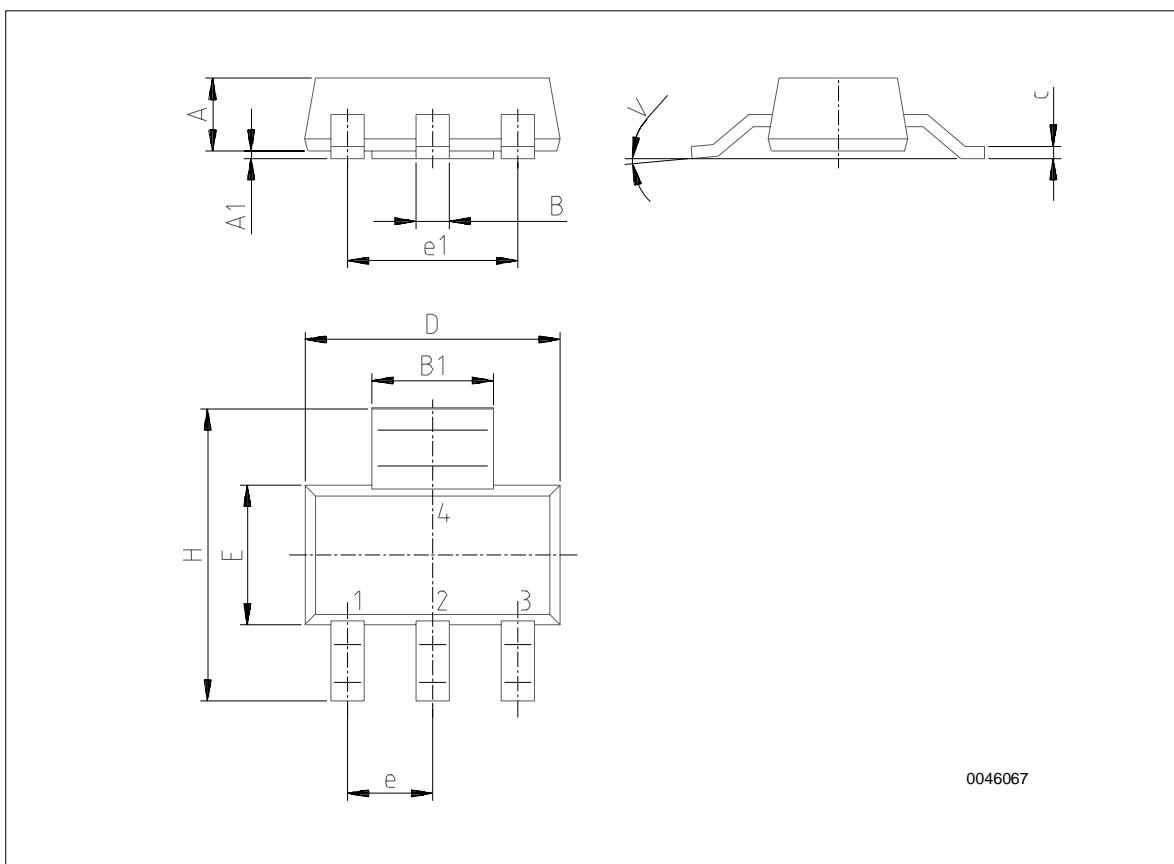
TO-252 (DPAK) MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|------|------|-----|------|-------|-------|-------|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | 2.2 | | 2.4 | 0.086 | | 0.094 |
| A1 | 0.9 | | 1.1 | 0.035 | | 0.043 |
| A2 | 0.03 | | 0.23 | 0.001 | | 0.009 |
| B | 0.64 | | 0.9 | 0.025 | | 0.035 |
| B2 | 5.2 | | 5.4 | 0.204 | | 0.212 |
| C | 0.45 | | 0.6 | 0.017 | | 0.023 |
| C2 | 0.48 | | 0.6 | 0.019 | | 0.023 |
| D | 6 | | 6.2 | 0.236 | | 0.244 |
| E | 6.4 | | 6.6 | 0.252 | | 0.260 |
| G | 4.4 | | 4.6 | 0.173 | | 0.181 |
| H | 9.35 | | 10.1 | 0.368 | | 0.397 |
| L2 | | 0.8 | | | 0.031 | |
| L4 | 0.6 | | 1 | 0.023 | | 0.039 |
| R | | 0.2 | | | 0.008 | |
| V2 | 0° | 8° | | 0° | 8° | |



SOT-223 MECHANICAL DATA

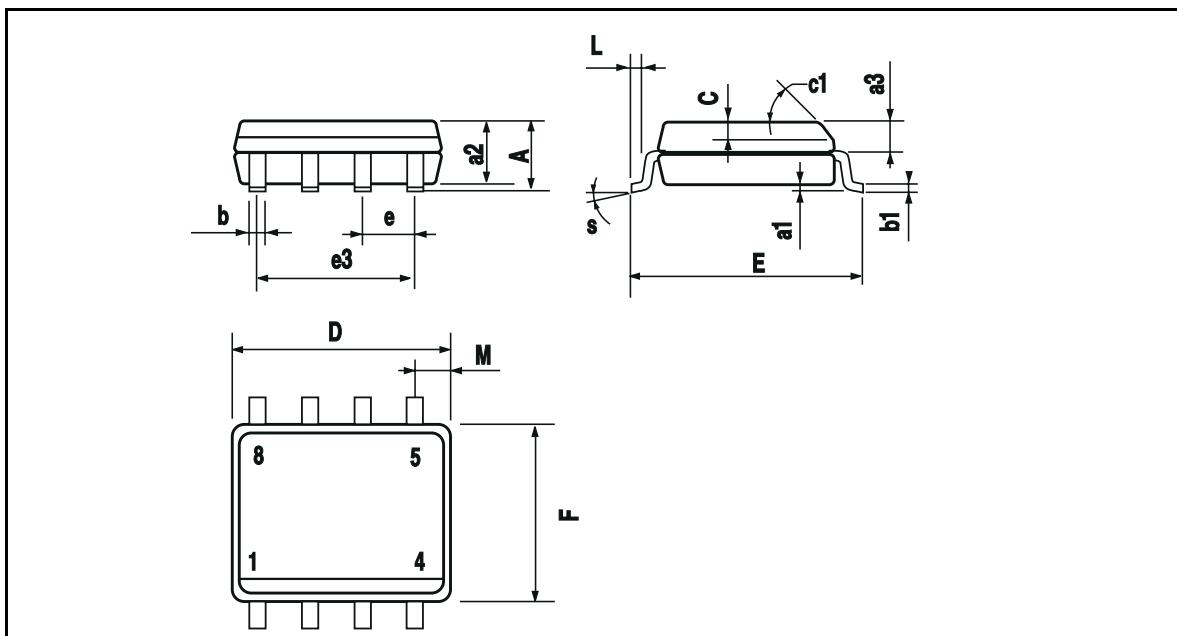
| DIM. | mm. | | | inch | | |
|------|----------|------|------|--------|-------|-------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | | 1.8 | | | 0.071 |
| B | 0.6 | 0.7 | 0.85 | 0.024 | 0.027 | 0.033 |
| B1 | 2.9 | 3 | 3.15 | 0.114 | 0.118 | 0.124 |
| c | 0.24 | 0.26 | 0.35 | 0.009 | 0.01 | 0.014 |
| D | 6.3 | 6.5 | 6.7 | 0.248 | 0.256 | 0.264 |
| e | | 2.3 | | | 0.09 | |
| e1 | | 4.6 | | | 0.181 | |
| E | 3.3 | 3.5 | 3.7 | 0.13 | 0.138 | 0.146 |
| H | 6.7 | 7 | 7.3 | 0.264 | 0.276 | 0.287 |
| V | 10 (max) | | | | | |
| A1 | 0.02 | | 0.1 | 0.0008 | | 0.004 |



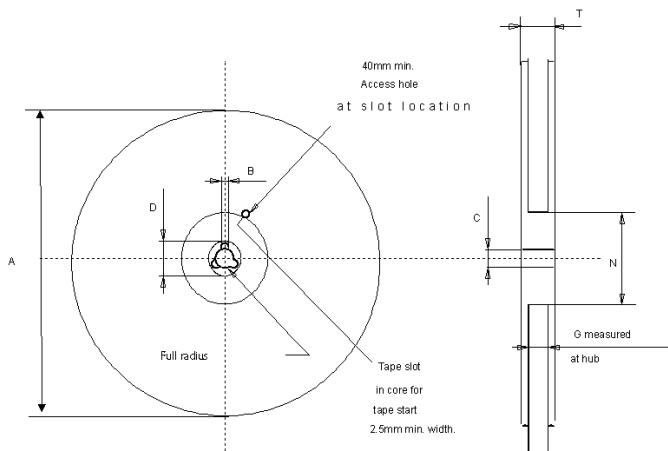
VNN7NV04 / VNS7NV04 / VND7NV04 / VND7NV04-1

SO-8 MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|------|-----------|------|------|-------|-------|-------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | | 1.75 | | | 0.068 |
| a1 | 0.1 | | 0.25 | 0.003 | | 0.009 |
| a2 | | | 1.65 | | | 0.064 |
| a3 | 0.65 | | 0.85 | 0.025 | | 0.033 |
| b | 0.35 | | 0.48 | 0.013 | | 0.018 |
| b1 | 0.19 | | 0.25 | 0.007 | | 0.010 |
| C | 0.25 | | 0.5 | 0.010 | | 0.019 |
| c1 | 45 (typ.) | | | | | |
| D | 4.8 | | 5.0 | 0.188 | | 0.196 |
| E | 5.8 | | 6.2 | 0.228 | | 0.244 |
| e | | 1.27 | | | 0.050 | |
| e3 | | 3.81 | | | 0.150 | |
| F | 3.8 | | 4.0 | 0.14 | | 0.157 |
| L | 0.4 | | 1.27 | 0.015 | | 0.050 |
| M | | | 0.6 | | | 0.023 |
| F | 8 (max.) | | | | | |



SOT-223 TAPE AND REEL SHIPMENT (suffix "13TR")



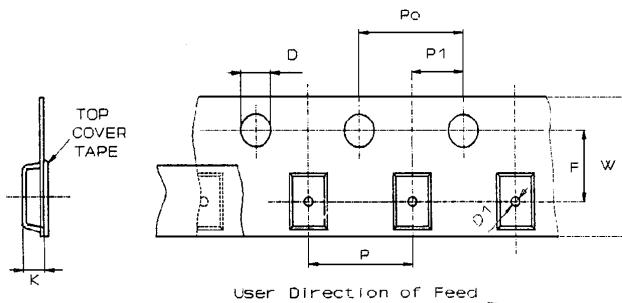
REEL DIMENSIONS

| | |
|---------------------------------|------|
| Base Q.ty | 1000 |
| Bulk Q.ty | 1000 |
| A (max) | 330 |
| B (min) | 1.5 |
| C (± 0.2) | 13 |
| F | 20.2 |
| G (+ 2 / -0) | 12.4 |
| N (min) | 60 |
| T (max) | 18.4 |

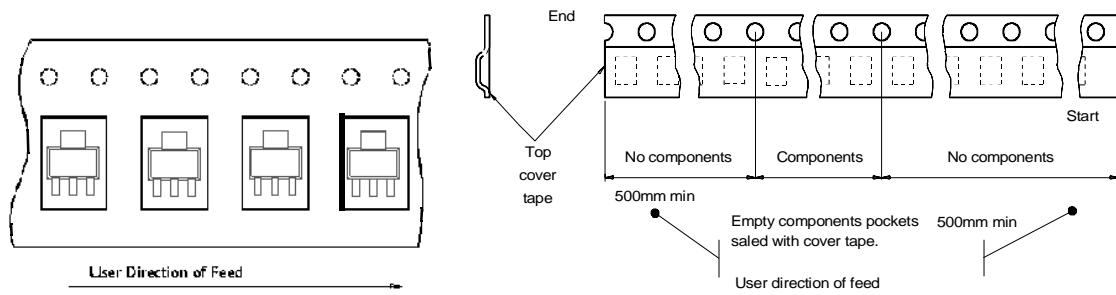
TAPE DIMENSIONS

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

| | | |
|--------------------------|------------------------------------|-----|
| Tape width | W | 12 |
| Tape Hole Spacing | P0 (± 0.1) | 4 |
| Component Spacing | P | 8 |
| Hole Diameter | D ($\pm 0.1/-0$) | 1.5 |
| Hole Diameter | D1 (min) | 1.5 |
| Hole Position | F (± 0.05) | 5.5 |
| Compartment Depth | K (max) | 4.5 |
| Hole Spacing | P1 (± 0.1) | 2 |

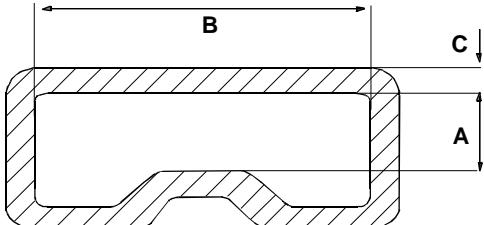


All dimensions are in mm.



VNN7NV04 / VNS7NV04 / VND7NV04 / VND7NV04-1

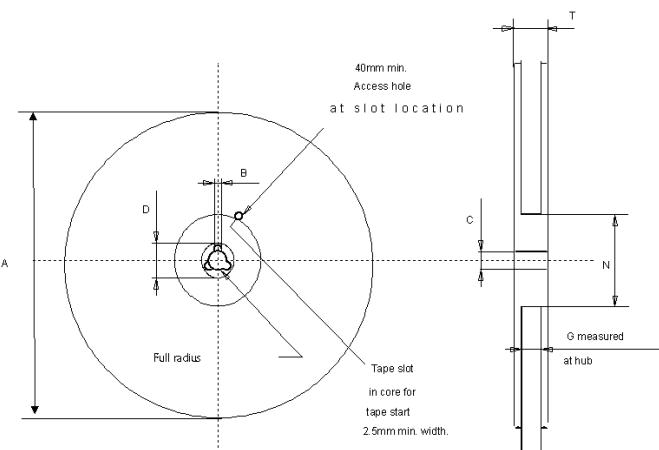
SO-8 TUBE SHIPMENT (no suffix)



| | |
|---|------|
| Base Q.ty | 100 |
| Bulk Q.ty | 2000 |
| Tube length (± 0.5) | 532 |
| A | 3.2 |
| B | 6 |
| C (± 0.1) | 0.6 |

All dimensions are in mm.

TAPE AND REEL SHIPMENT (suffix "13TR")



| REEL DIMENSIONS | |
|---------------------------------|------|
| Base Q.ty | 2500 |
| Bulk Q.ty | 2500 |
| A (max) | 330 |
| B (min) | 1.5 |
| C (± 0.2) | 13 |
| F | 20.2 |
| G (+ 2 / -0) | 12.4 |
| N (min) | 60 |
| T (max) | 18.4 |

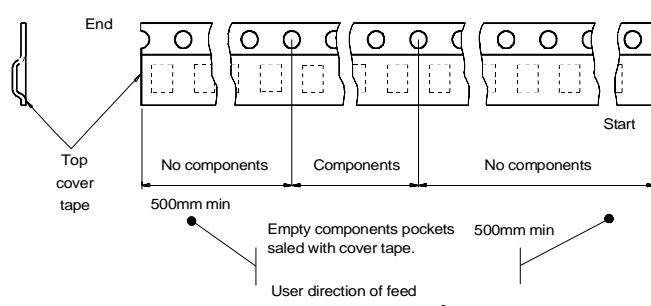
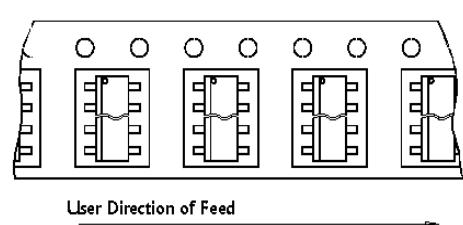
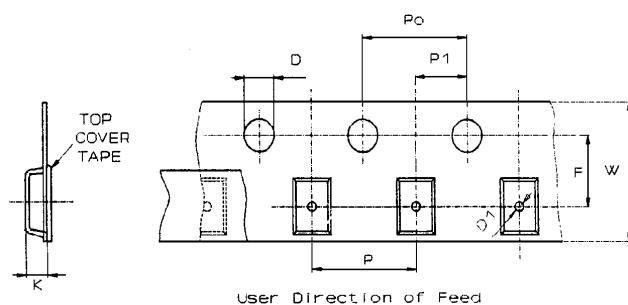
All dimensions are in mm.

TAPE DIMENSIONS

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

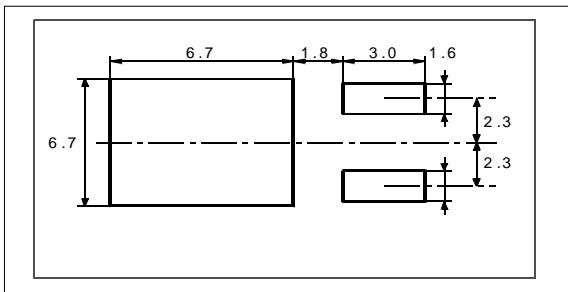
| | | |
|--------------------------|------------------------------------|-----|
| Tape width | W | 12 |
| Tape Hole Spacing | P0 (± 0.1) | 4 |
| Component Spacing | P | 8 |
| Hole Diameter | D ($\pm 0.1/-0$) | 1.5 |
| Hole Diameter | D1 (min) | 1.5 |
| Hole Position | F (± 0.05) | 5.5 |
| Compartment Depth | K (max) | 4.5 |
| Hole Spacing | P1 (± 0.1) | 2 |

All dimensions are in mm.



VNN7NV04 / VNS7NV04 / VND7NV04 / VND7NV04-1

DPAK FOOTPRINT

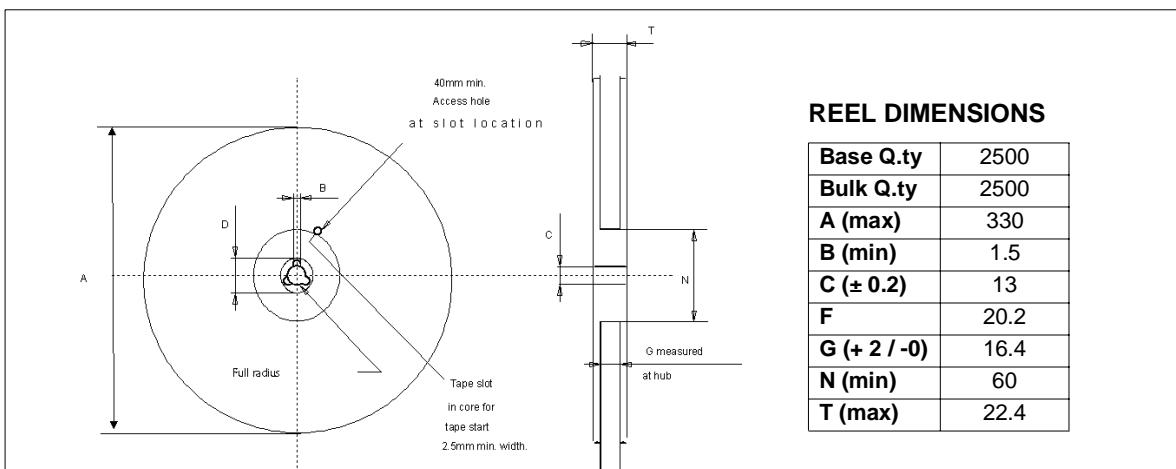


TUBE SHIPMENT (no suffix)

| | |
|---|------|
| Base Q.ty | 75 |
| Bulk Q.ty | 3000 |
| Tube length (± 0.5) | 532 |
| A | 6 |
| B | 21.3 |
| C (± 0.1) | 0.6 |

All dimensions are in mm.

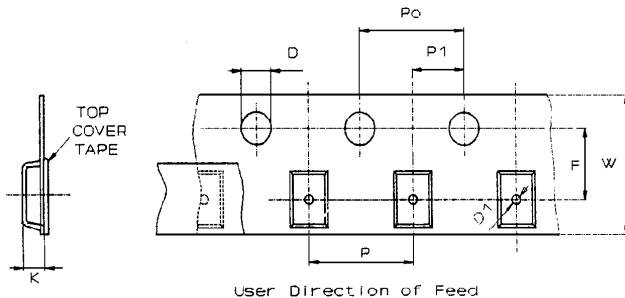
TAPE AND REEL SHIPMENT (suffix "13TR")



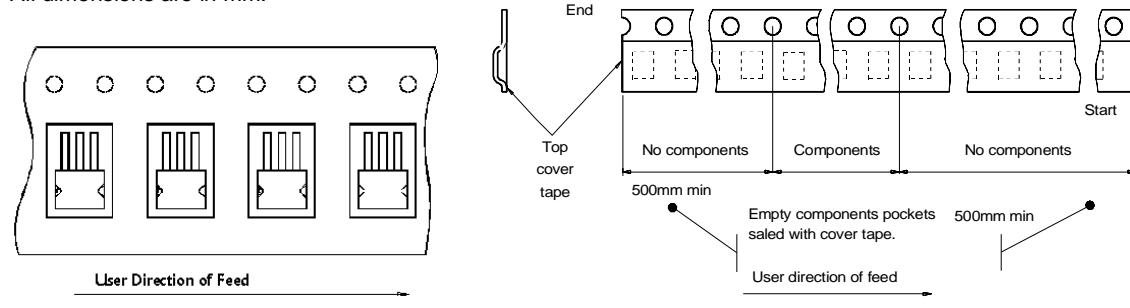
TAPE DIMENSIONS

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

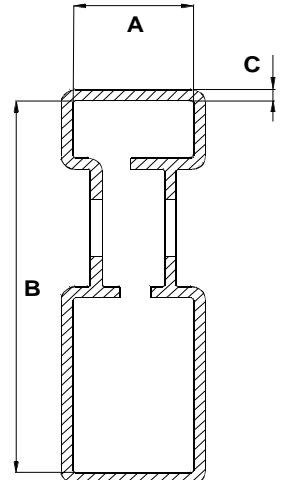
| | | |
|--------------------------|------------------------------------|-----|
| Tape width | W | 16 |
| Tape Hole Spacing | P0 (± 0.1) | 4 |
| Component Spacing | P | 8 |
| Hole Diameter | D ($\pm 0.1/-0$) | 1.5 |
| Hole Diameter | D1 (min) | 1.5 |
| Hole Position | F (± 0.05) | 7.5 |
| Compartment Depth | K (max) | 6.5 |
| Hole Spacing | P1 (± 0.1) | 2 |



All dimensions are in mm.



VNN7NV04 / VNS7NV04 / VND7NV04 / VND7NV04-1



IPAK TUBE SHIPMENT (no suffix)

| | |
|---|------|
| Base Q.ty | 75 |
| Bulk Q.ty | 3000 |
| Tube length (± 0.5) | 532 |
| A | 6 |
| B | 21.3 |
| C (± 0.1) | 0.6 |

All dimensions are in mm.

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a trademark of STMicroelectronics

© 2003 STMicroelectronics - Printed in ITALY- All Rights Reserved.

STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia -
Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - U.S.A.

<http://www.st.com>