

**VN771K**

QUAD SMART POWER SOLID STATE RELAY FOR COMPLETE H BRIDGE CONFIGURATIONS

TYPE	R _{DS(on)}	I _{OUT}	V _{CC}
VN771K	95 mΩ (*)	9A (**)	36V

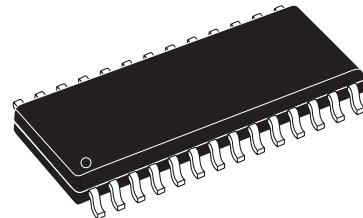
(*) Total resistance of one side in bridge configuration

(**) Typical current limitation value

- SUITED AS LOW VOLTAGE BRIDGE
- LINEAR CURRENT LIMITATION
- VERY LOW STAND-BY POWER DISSIPATION
- SHORT CIRCUIT PROTECTED
- STATUS FLAG DIAGNOSTIC (OPEN DRAIN)
- INTEGRATED CLAMPING CIRCUITS
- UNDERVOLTAGE PROTECTION
- ESD PROTECTION

DESCRIPTION

The VN771K is a device formed by three monolithic chips housed in a standard SO-28 package: a double high side and two low side switches. Both the double high side and low side switches are made using STMicroelectronics VIPower™ M0-3 Technology. This device is suitable to drive a DC motor in a bridge configuration as well as to be used as a quad switch for any low voltage application. The dual high side switches have built-in thermal shutdown



ORDER CODES		
PACKAGE	TUBE	T&R
SO-28	VN771K	VN771K13TR

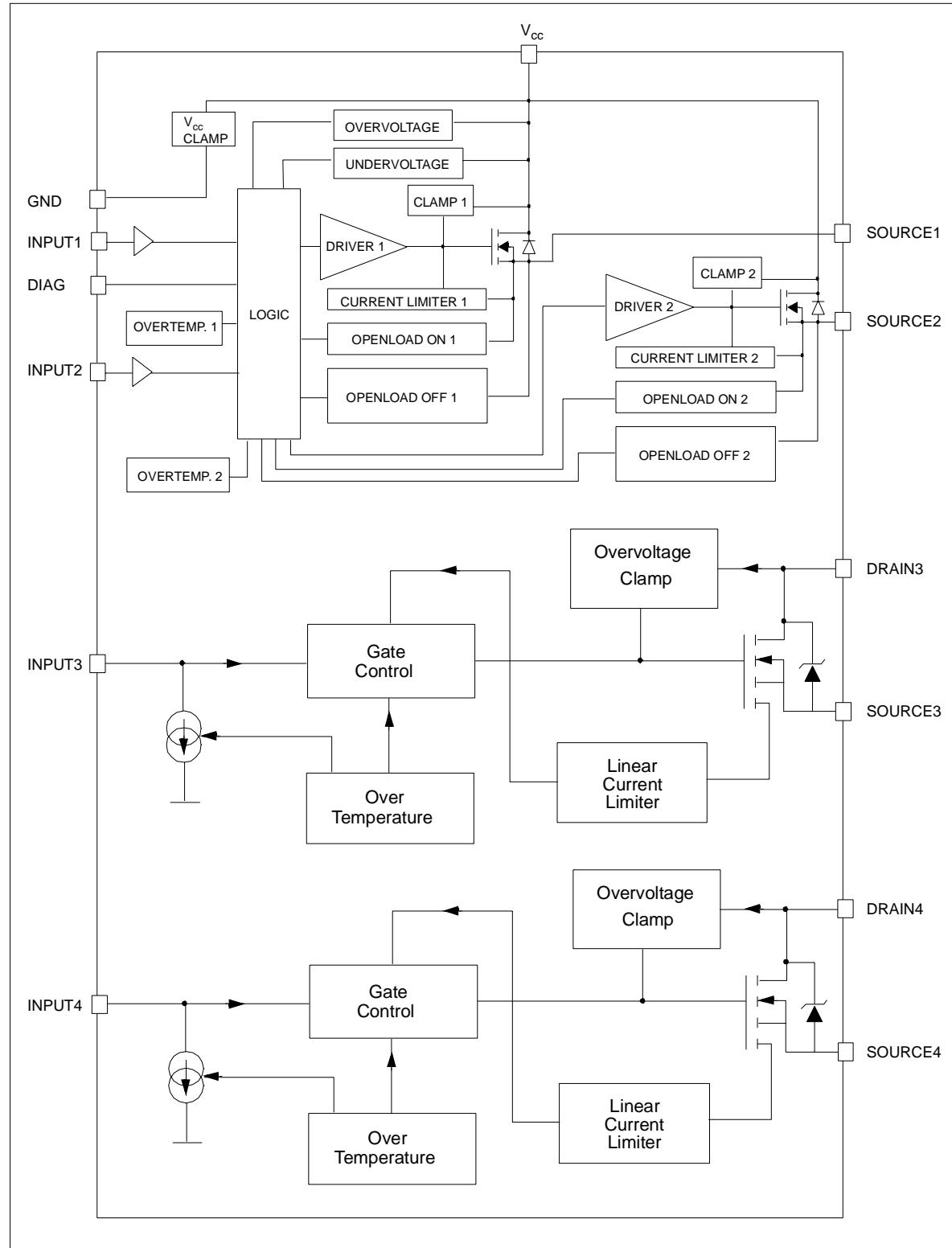
to protect the chips from overtemperature and current limiter blocks to protect the device from short circuit. Status output is provided to indicate open load in off and on state and overtemperature. The low side switches are two OMNIFET II types (fully autoproTECTED Power MOSFET in VIPower™ technology). They have built-in thermal shutdown, linear current limitation and overvoltage clamping. Fault feedback for thermal intervention can be detected by monitoring the voltage at the input pin.

PIN FUNCTION

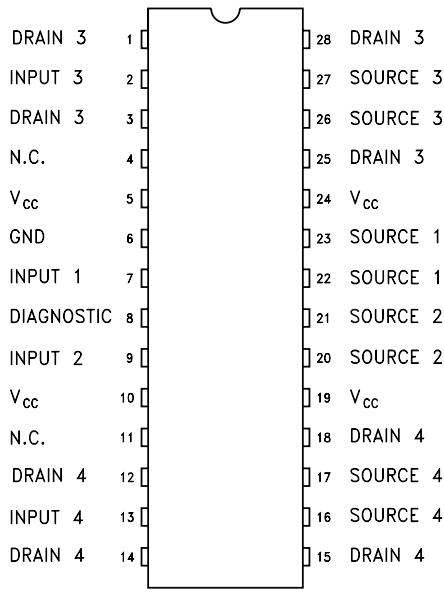
No	NAME	FUNCTION
1, 3, 25, 28	DRAIN 3	Drain of Switch 3 (low-side switch)
2	INPUT 3	Input of Switch 3 (low-side switch)
4, 11	N.C.	Not Connected
5, 10, 19, 24	V _{CC}	Drain of Switches 1 and 2 (high-side switches) and Power Supply Voltage
6	GND	Ground of Switches 1 and 2 (high-side switches)
7	INPUT 1	Input of Switch 1 (high-side switches)
8	DIAGNOSTIC	Diagnostic of Switches 1 and 2 (high-side switches)
9	INPUT 2	Input of Switch 2 (high-side switch)
12, 14, 15, 18	DRAIN 4	Drain of switch 4 (low-side switch)
13	INPUT 4	Input of Switch 4 (low-side switch)
16, 17	SOURCE 4	Source of Switch 4 (low-side switch)
20, 21	SOURCE 2	Source of Switch 2 (high-side switch)
22, 23	SOURCE 1	Source of Switch 1 (high-side switch)
26, 27	SOURCE 3	Source of Switch 3 (low-side switch)

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BLOCK DIAGRAM



CONNECTION DIAGRAM



THERMAL DATA

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal Resistance Junction-case (High-side switch)	MAX	°C/W
R _{thj-case}	Thermal Resistance Junction-case (Low-side switch)	MAX	°C/W
R _{thj-amb}	Thermal Resistance Junction-ambient	MAX	°C/W

ABSOLUTE MAXIMUM RATING

DUAL HIGH SIDE SWITCH

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	41	V
- V _{CC}	Reverse DC Supply Voltage	- 0.3	V
- I _{GND}	DC Reverse Ground Pin Current	- 200	mA
I _{OUT}	DC Output Current	Internally Limited	A
- I _{OUT}	Reverse DC Output Current	- 6	A
I _{IN}	DC Input Current	+/- 10	mA
I _{STAT}	DC Status Current	+/- 10	mA
V _{ESD}	Electrostatic Discharge (Human Body Model: R=1.5KΩ; C=100pF)		
	- INPUT	4000	V
	- STATUS	4000	V
	- OUTPUT	5000	V
- V _{CC}		5000	V
P _{tot}	Power Dissipation T _c =25°C	6	W
T _j	Junction Operating Temperature	Internally Limited	°C
T _c	Case Operating Temperature	- 40 to 150	°C
T _{stg}	Storage Temperature	- 55 to 150	°C

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ABSOLUTE MAXIMUM RATING (continued)

LOW SIDE SWITCH

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage ($V_{IN}=0V$)	Internally Clamped	V
V_{IN}	Input Voltage	Internally Clamped	V
I_{IN}	Input Current	+/-20	mA
$R_{IN\ MIN}$	Minimum Input Series Impedance	10	Ω
I_D	Drain Current	Internally Limited	A
I_R	Reverse DC Output Current	-15	A
V_{ESD1}	Electrostatic Discharge ($R=1.5K\Omega$, $C=100pF$)	4000	V
V_{ESD2}	Electrostatic Discharge on output pin only ($R=330\Omega$, $C=150pF$)	16500	V
P_{tot}	Total Dissipation at $T_c=25^\circ C$	6	W
T_j	Operating Junction Temperature	Internally limited	$^\circ C$
T_c	Case Operating Temperature	Internally limited	$^\circ C$
T_{stg}	Storage Temperature	-55 to 150	$^\circ C$

ELECTRICAL CHARACTERISTICS FOR DUAL HIGH SIDE SWITCH

($8V < V_{CC} < 36V$; $-40^\circ C < T_j < 150^\circ C$, unless otherwise specified)

POWER OUTPUTS (Per each channel)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{CC\ (*)}$	Operating Supply Voltage		5.5	13	36	V
$V_{USD\ (*)}$	Undervoltage Shut-down		3	4	5.5	V
$V_{OV\ (*)}$	Ovvoltage Shut-down		36			V
R_{ON}	On State Resistance	$I_{OUT}=2A$; $T_j=25^\circ C$ $I_{OUT}=2A$; $V_{CC}>8V$			60 120	$m\Omega$ $m\Omega$
$I_S\ (*)$	Supply Current	Off State; $V_{CC}=13V$; $V_{IN}=V_{OUT}=0V$ Off State; $V_{CC}=13V$; $T_j=25^\circ C$; $V_{IN}=V_{OUT}=0V$ On State; $V_{CC}=13V$		12 12 5	40 25 7	μA μA mA
$I_{L(off1)}$	Off State Output Current	$V_{IN}=V_{OUT}=0V$; $V_{CC}=36V$; $T_j=125^\circ C$	0		50	μA
$I_{L(off2)}$	Off State Output Current	$V_{IN}=0V$; $V_{OUT}=3.5V$	-75		0	μA
$I_{L(off3)}$	Off State Output Current	$V_{IN}=V_{OUT}=0V$; $V_{CC}=13V$; $T_j=125^\circ C$			5	μA
$I_{L(off4)}$	Off State Output Current	$V_{IN}=V_{OUT}=0V$; $V_{CC}=13V$; $T_j=25^\circ C$			3	μA

SWITCHING (Per each channel) ($V_{CC}=13V$)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on Delay Time	$R_L=6.5\Omega$ from V_{IN} rising edge to $V_{OUT}=1.3V$		30		μs
$t_{d(off)}$	Turn-off Delay Time	$R_L=6.5\Omega$ from V_{IN} falling edge to $V_{OUT}=11.7V$		30		μs
$dV_{OUT}/dt_{(on)}$	Turn-on Voltage Slope	$R_L=6.5\Omega$ from $V_{OUT}=1.3V$ to $V_{OUT}=10.4V$		See relative diagram		$V/\mu s$
$dV_{OUT}/dt_{(off)}$	Turn-off Voltage Slope	$R_L=6.5\Omega$ from $V_{OUT}=11.7V$ to $V_{OUT}=1.3V$		See relative diagram		$V/\mu s$

(*) Per device

ELECTRICAL CHARACTERISTICS FOR DUAL HIGH SIDE SWITCH (continued)
LOGIC INPUT (Per each channel)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IL}	Input Low Level				1.25	V
I_{IL}	Low Level Input Current	$V_{IN} = 1.25V$	1			μA
V_{IH}	Input High Level		3.25			V
I_{IH}	High Level Input Current	$V_{IN} = 3.25V$			10	μA
$V_{I(hyst)}$	Input Hysteresis Voltage		0.5			V
V_{ICL}	Input Clamp Voltage	$I_{IN} = 1mA$ $I_{IN} = -1mA$	6	6.8 -0.7	8	V V

STATUS PIN (Per each channel)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{STAT}	Status Low Output Voltage	$I_{STAT} = 1.6 mA$			0.5	V
I_{LSTAT}	Status Leakage Current	Normal Operation; $V_{STAT} = 5V$			10	μA
C_{STAT}	Status Pin Input Capacitance	Normal Operation; $V_{STAT} = 5V$			100	pF
V_{SCL}	Status Clamp Voltage	$I_{STAT} = 1mA$ $I_{STAT} = -1mA$	6	6.8 -0.7	8	V V

PROTECTIONS (Per each channel)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
T_{TSD}	Shut-down Temperature		150	175	200	°C
T_R	Reset Temperature		135			°C
T_{hyst}	Thermal Hysteresis		7	15		°C
t_{SDL}	Status Delay in Overload Conditions	$T_j > T_{TSD}$			20	μs
I_{lim}	Current limitation	$T_j = 125^\circ C$ $5.5V < V_{CC} < 36V$	6 8.5	9	15 15 15	A A A
V_{demag}	Turn-off Output Clamp Voltage	$I_{OUT} = 2A$; $L = 6mH$	V_{CC-41}	V_{CC-48}	V_{CC-55}	V

OPENLOAD DETECTION (Per each channel)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{OL}	Openload ON State Detection Threshold	$V_{IN} = 5V$	50	100	200	mA
$t_{DOL(on)}$	Openload ON State Detection Delay	$I_{OUT} = 0A$			200	μs
V_{OL}	Openload OFF State Voltage Detection Threshold	$V_{IN} = 0V$	1.5	2.5	3.5	V
$T_{DOL(off)}$	Openload Detection Delay at Turn Off				1000	μs

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ELECTRICAL CHARACTERISTICS FOR LOW SIDE SWITCHES

(-40°C < T_j < 150°C, unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V _{CLAMP}	Drain-source Clamp Voltage	V _{IN} =0V; I _D =7A	40	45	55	V
V _{CLTH}	Drain-source Clamp Threshold Voltage	V _{IN} =0V; I _D =2mA	36			V
V _{INTH}	Input Threshold Voltage	V _{DS} =V _{IN} ; I _D =1mA	0.5		2.5	V
I _{ISS}	Supply Current from Input Pin	V _{DS} =0V; V _{IN} =5V		100	150	µA
V _{INCL}	Input-Source Clamp Voltage	I _{IN} =1mA I _{IN} =-1mA	6 -1.0	6.8	8 -0.3	V
I _{DSS}	Zero Input Voltage Drain Current (V _{IN} =0V)	V _{DS} =13V; V _{IN} =0V; T _j =25°C V _{DS} =25V; V _{IN} =0V			30 75	µA

ON

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
R _{DS(on)}	Static Drain-source On Resistance	V _{IN} =5V; I _D =7A; T _j =25°C V _{IN} =5V; I _D =7A			35 70	mΩ

(T_j=25°C, unless otherwise specified)

DYNAMIC

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
g _{fs} (*)	Forward Transconductance	V _{DD} =13V; I _D =7A		18		S
C _{OSS}	Output Capacitance	V _{DS} =13V; f=1MHz; V _{IN} =0V		400		pF

SWITCHING

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t _{d(on)}	Turn-on Delay Time	V _{DD} =15V; I _D =7A V _{gen} =5V; R _{gen} =R _{IN MIN} =10Ω		80	250	ns
t _r	Rise Time			350	1000	ns
t _{d(off)}	Turn-off Delay Time			450	1350	ns
t _f	Fall Time			150	500	ns
t _{d(on)}	Turn-on Delay Time	V _{DD} =15V; I _D =7A V _{gen} =5V; R _{gen} =2.2KΩ		1.5	4.5	µs
t _r	Rise Time			9.7	30.0	µs
t _{d(off)}	Turn-off Delay Time			9	25.0	µs
t _f	Fall Time			10.2	30.0	µs
(di/dt) _{on}	Turn-on Current Slope	V _{DD} =15V; I _D =7A V _{gen} =5V; R _{gen} =R _{IN MIN} =10Ω		16		A/µs
Q _i	Total Input Charge	V _{DD} =12V; I _D =7A; V _{IN} =5V; I _{gen} =2.13mA		36.8		nC

ELECTRICAL CHARACTERISTICS FOR LOW SIDE SWITCHES (continued)
SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{SD} (*)	Forward On Voltage	$I_{SD} = 7A; V_{IN}=0V$		0.8		V
t_{rr}	Reverse Recovery Time			300		ns
Q_{rr}	Reverse Recovery Charge	$I_{SD}=7A; di/dt=40A/\mu s$		0.8		μC
I_{RRM}	Reverse Recovery Current	$V_{DD}=30V; L=200\mu H$		5		A

PROTECTIONS (-40°C < T_j < 150°C, unless otherwise specified)

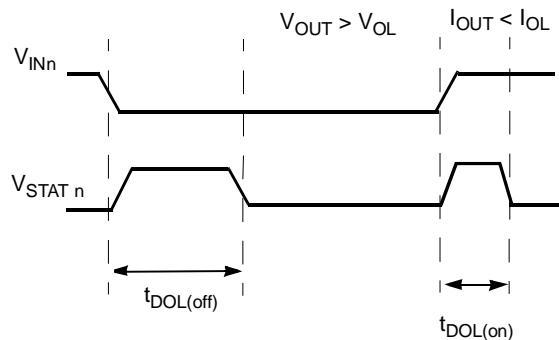
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{lim}	Drain Current Limit	$V_{IN}=5V; V_{DS}=13V$ $V_{IN}=5V; V_{DS}=13V; T_j=125^\circ C$	12 15	18 24	24 24	A A
t_{dlim}	Step Response Current Limit	$V_{IN}=5V; V_{DS}=13V$		45		μs
T_{jsh}	Overtemperature Shutdown		150	175		$^\circ C$
T_{irs}	Overtemperature Reset		135			$^\circ C$
I_{gf}	Fault Sink Current	$V_{IN}=5V; V_{DS}=13V; T_j=T_{jsh}$	10	15	20	mA
E_{as}	Single Pulse Avalanche Energy	starting $T_j=25^\circ C; V_{DD}=24V$ $V_{IN}=5V; R_{gen}=R_{IN\ MIN}=10\Omega; L=24mH$	400			mJ

(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

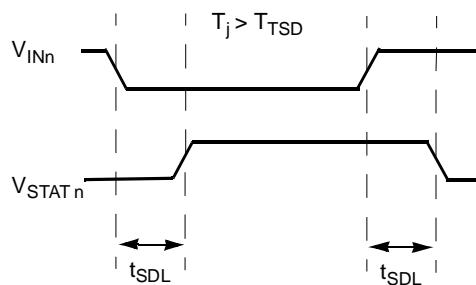
VN771K

DUAL HIGH-SIDE SWITCH

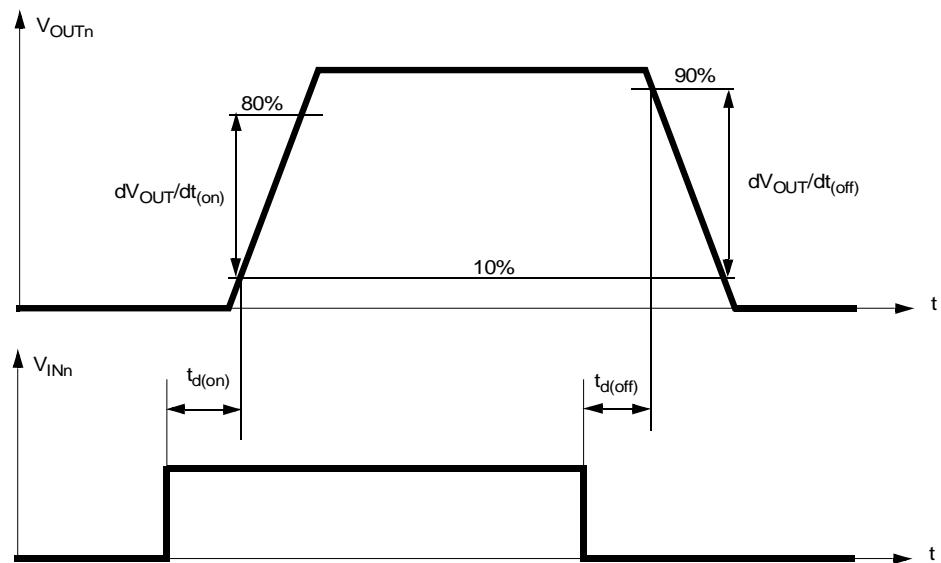
OPEN LOAD STATUS TIMING (with external pull-up)



OVER TEMP STATUS TIMING

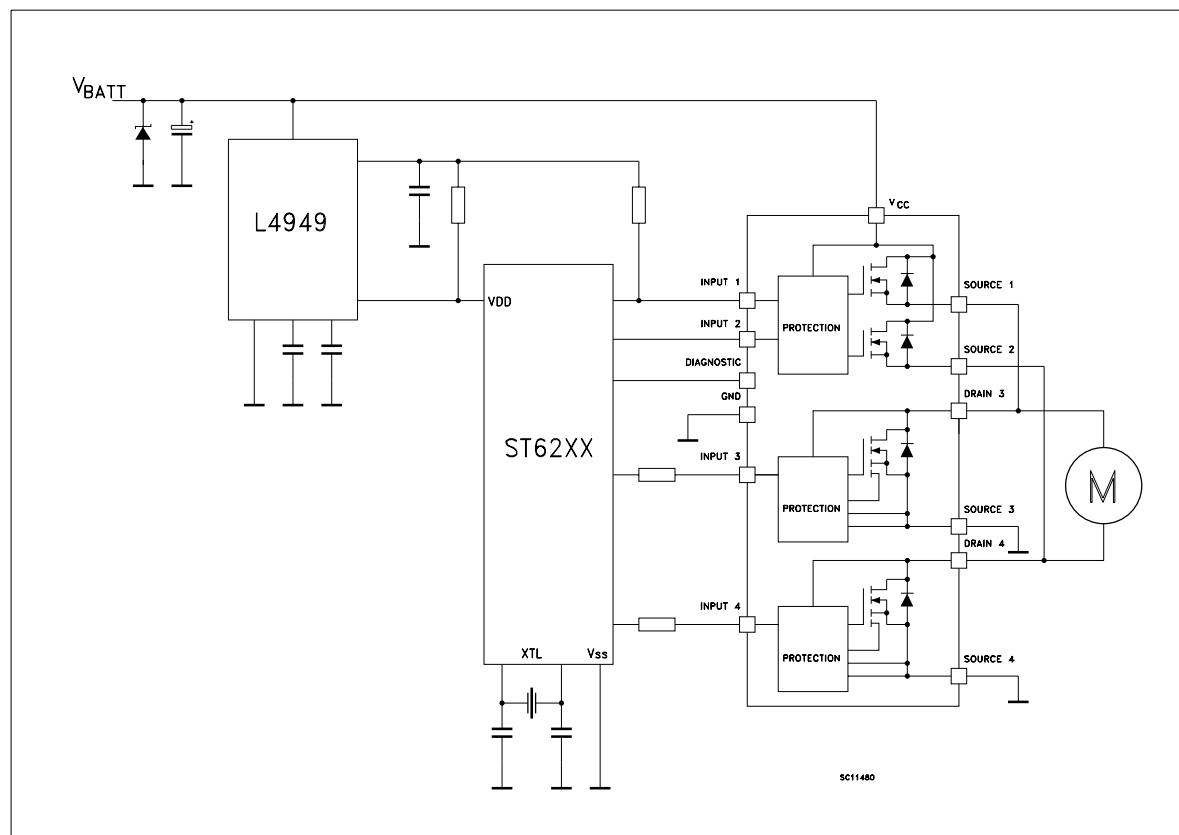


SWITCHING TIME WAVEFORMS



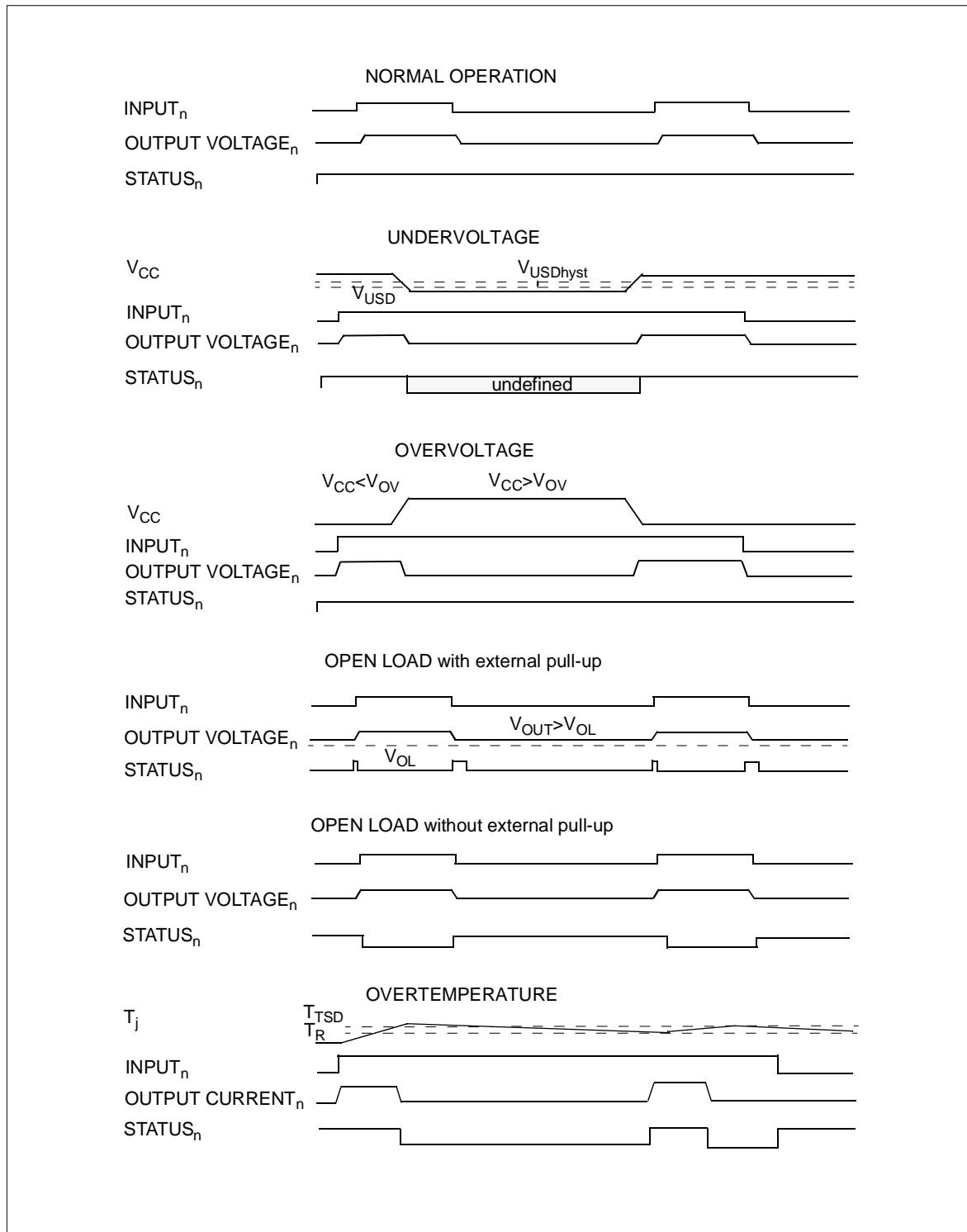
TRUTH TABLE

CONDITIONS	INPUT	OUTPUT	STATUS
Normal Operation	L H	L H	H H
Current Limitation	L H H	L X X	H $(T_j < T_{TSD})$ H $(T_j > T_{TSD})$ L
Overttemperature	L H	L L	H L
Undervoltage	L H	L L	X X
Ovvoltage	L H	L L	H H
Output Voltage $> V_{OL}$	L H	H H	L H
Output Current $< I_{OL}$	L H	L H	H L

TYPICAL APPLICATION DIAGRAM

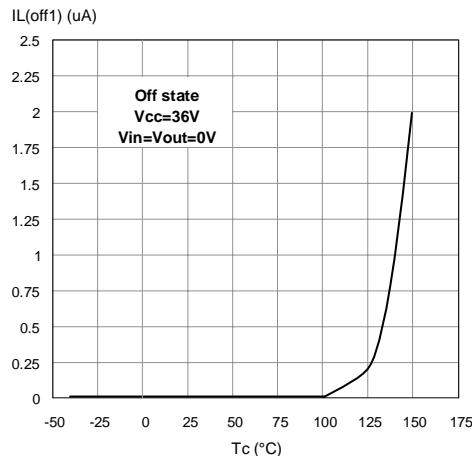
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Figure 1: Waveforms

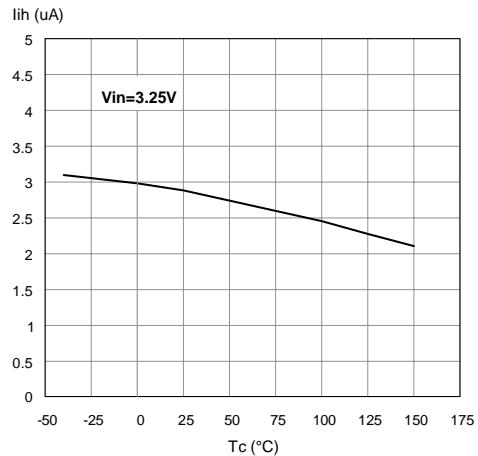


ELECTRICAL CHARACTERIZATION FOR DUAL HIGH SIDE SWITCH

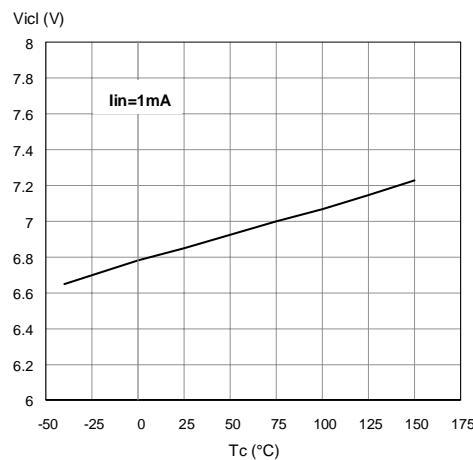
Off State Output Current



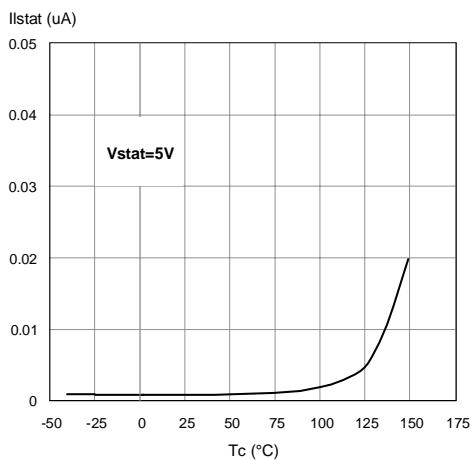
High Level Input Current



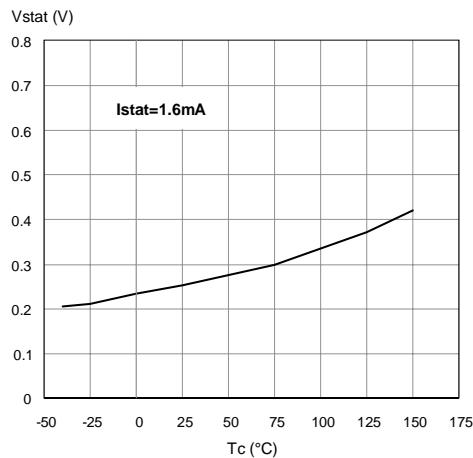
Input Clamp Voltage



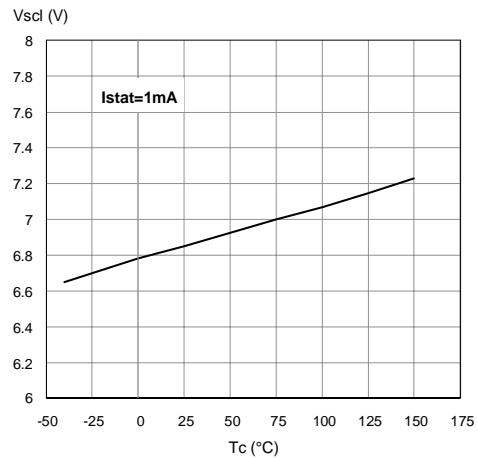
Status Leakage Current



Status Low Output Voltage



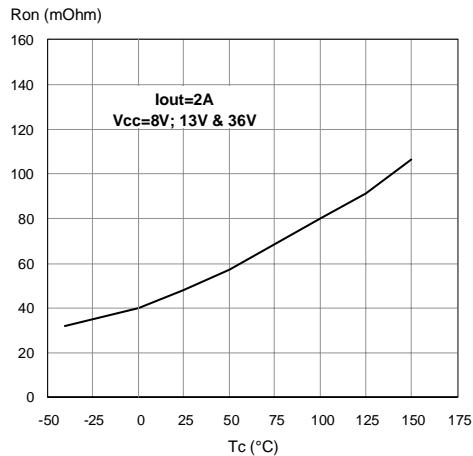
Status Clamp Voltage



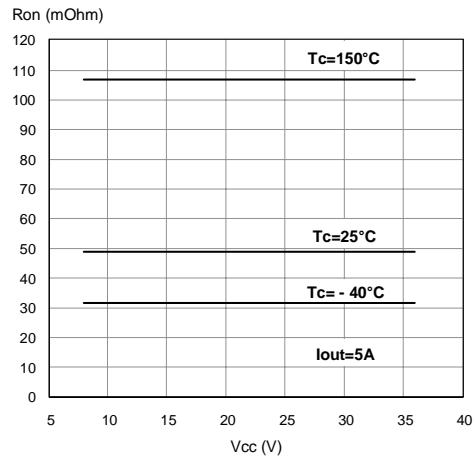
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ELECTRICAL CHARACTERIZATION FOR DUAL HIGH SIDE SWITCH (continued)

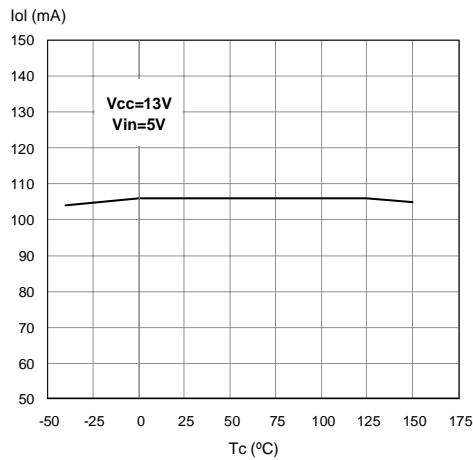
On State Resistance Vs T_{case}



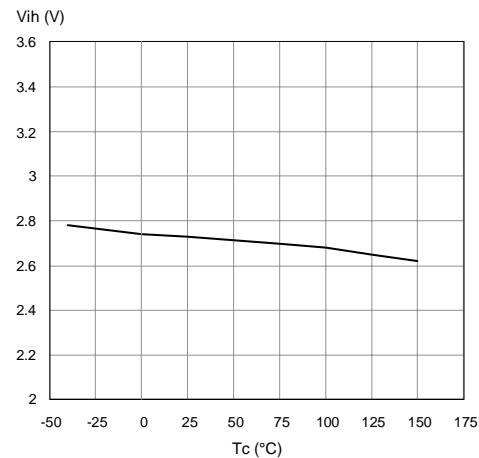
On State Resistance Vs V_{cc}



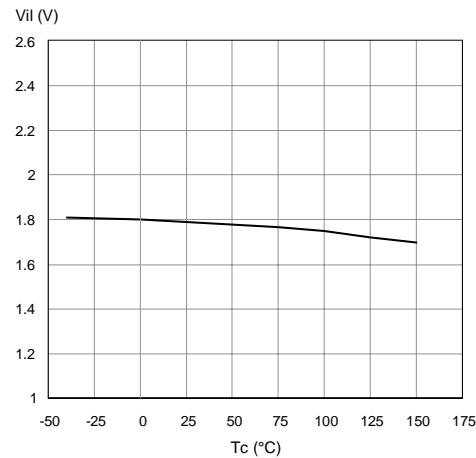
Openload On State Detection Threshold



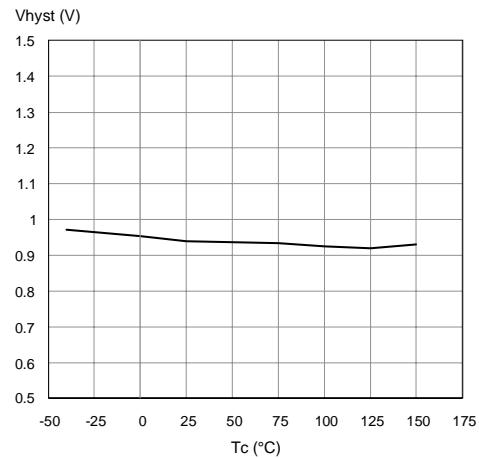
Input High Level



Input Low Level



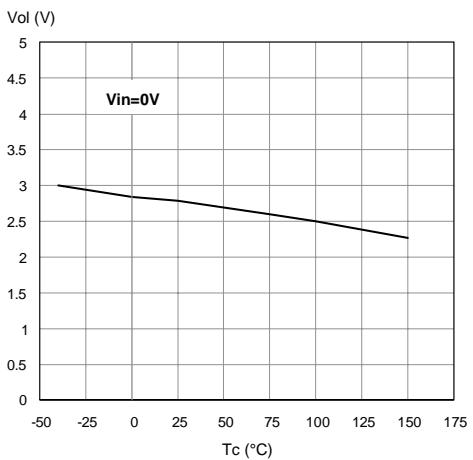
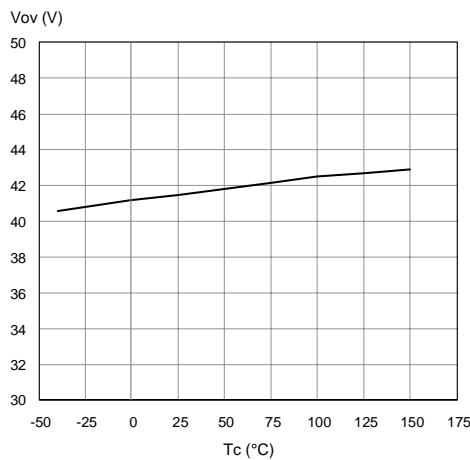
Input Hysteresis Voltage



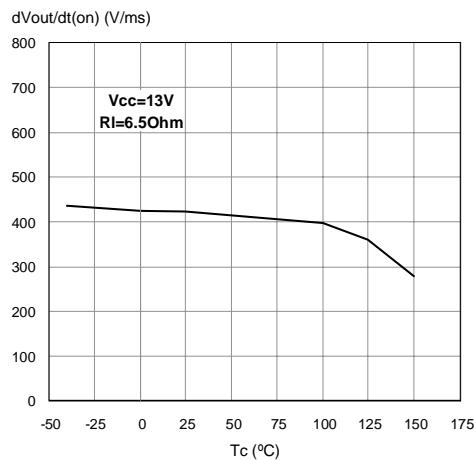
ELECTRICAL CHARACTERIZATION FOR DUAL HIGH SIDE SWITCH (continued)

Overvoltage Shutdown

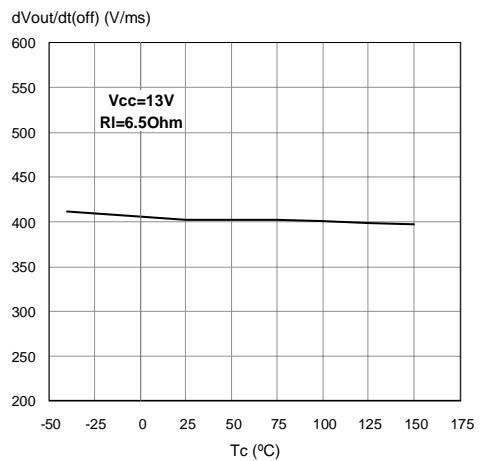
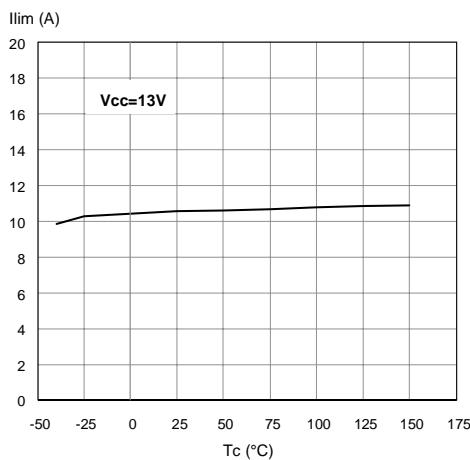
Openload Off State Voltage Detection Threshold



Turn-on Voltage Slope



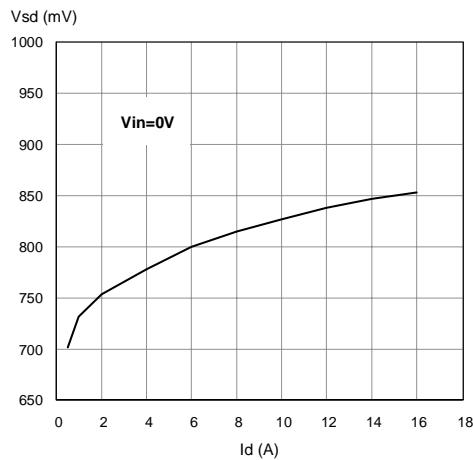
Turn-off Voltage Slope


 I_{LIM} Vs T_{case}


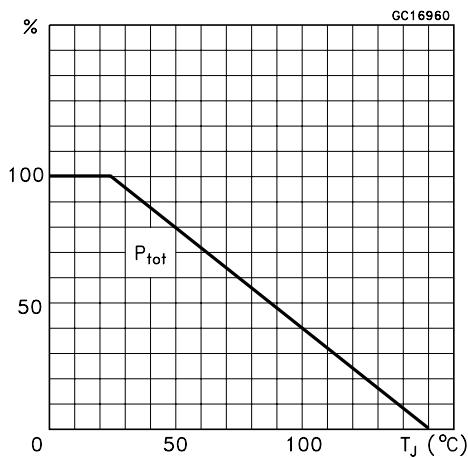
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ELECTRICAL CHARACTERIZATION FOR LOW SIDE SWITCHES

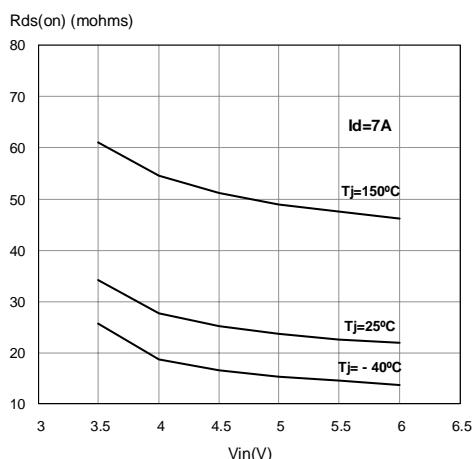
Source-Drain Diode Forward Characteristics



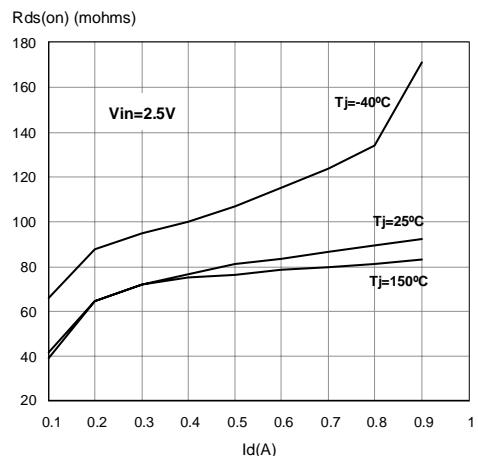
Derating Curve



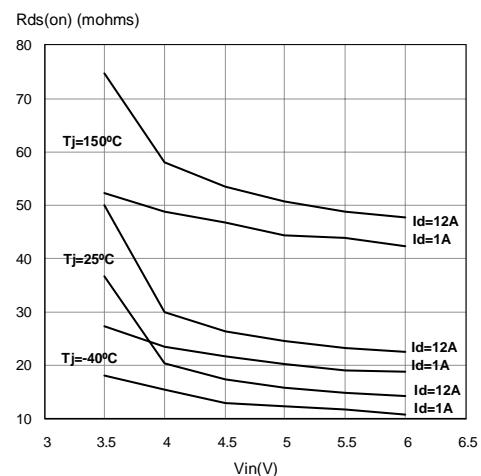
Static Drain-Source On resistance Vs. Input Voltage



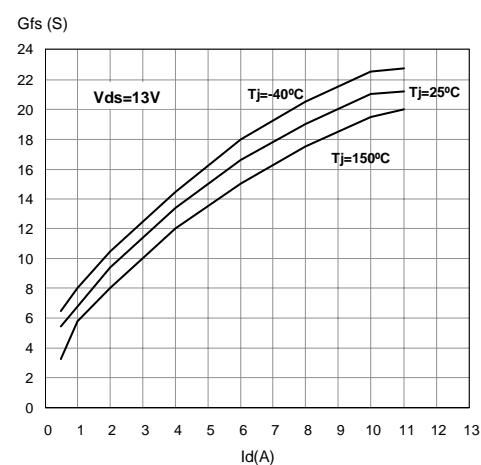
Static Drain Source On Resistance



Static Drain-Source On resistance Vs. Input Voltage

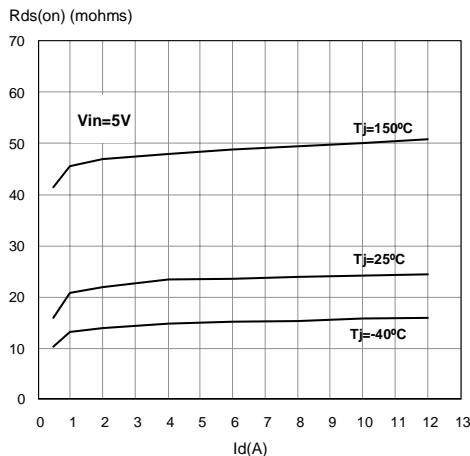


Transconductance

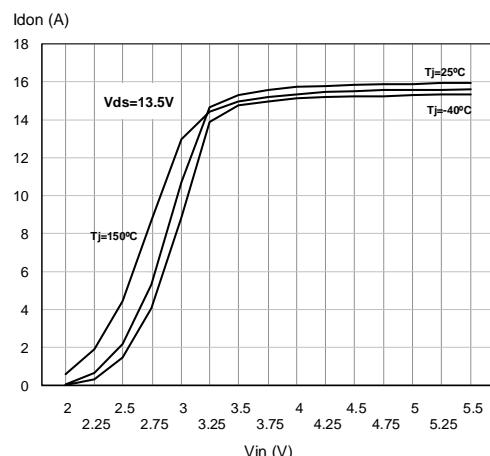


ELECTRICAL CHARACTERIZATION FOR LOW SIDE SWITCHES (continued)

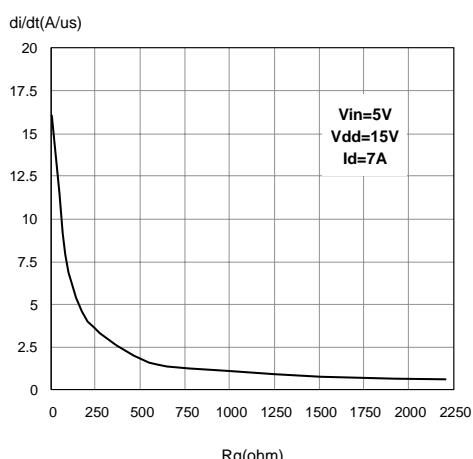
Static Drain-Source On Resistance Vs. Id



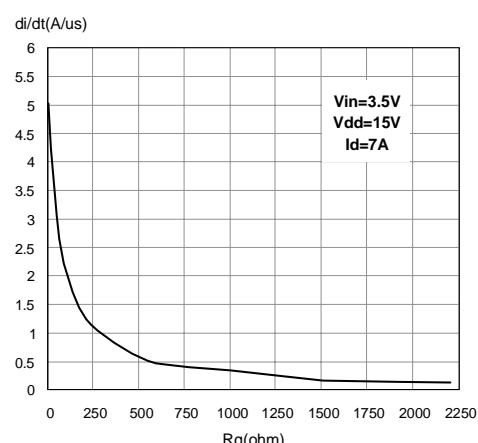
Transfer Characteristics



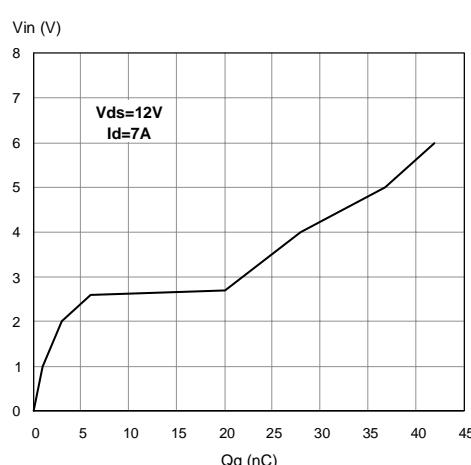
Turn On Current Slope



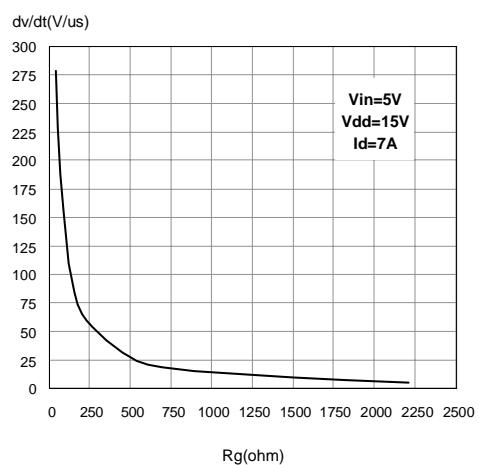
Turn On Current Slope



Input Voltage Vs. Input Charge



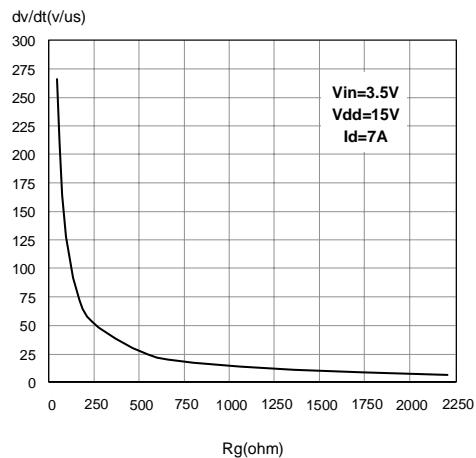
Turn off drain source voltage slope



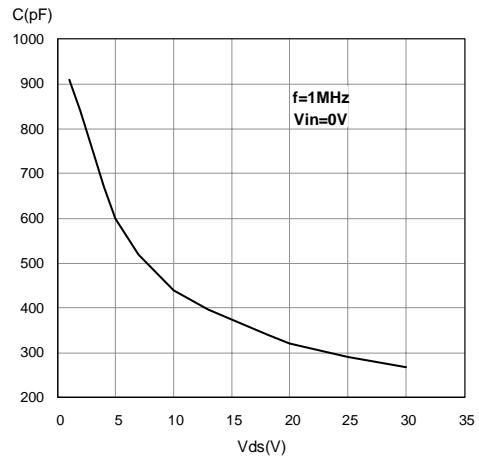
VN771K

ELECTRICAL CHARACTERIZATION FOR LOW SIDE SWITCHES (continued)

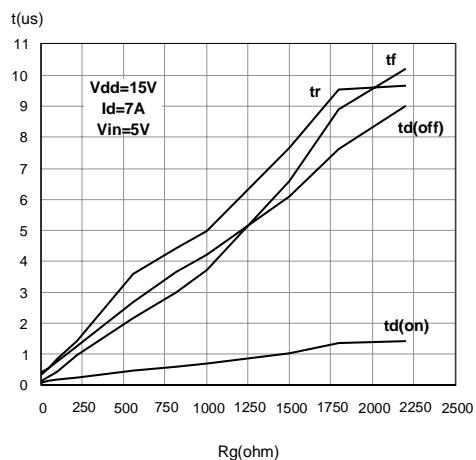
Turn Off Drain-Source Voltage Slope



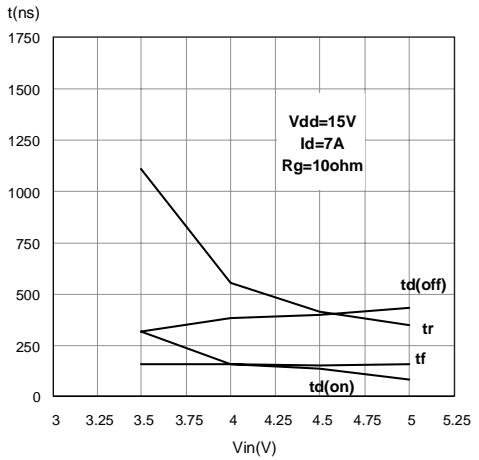
Capacitance Variations



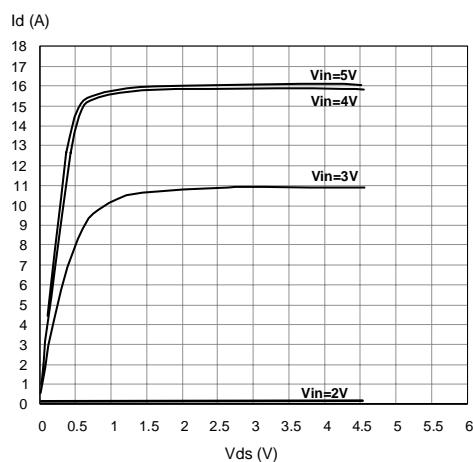
Switching Time Resistive Load



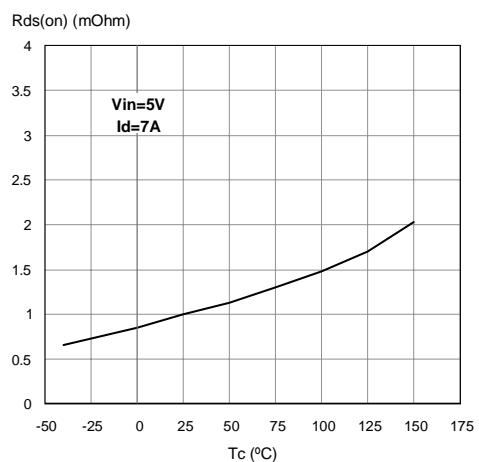
Switching Time Resistive Load



Output Characteristics

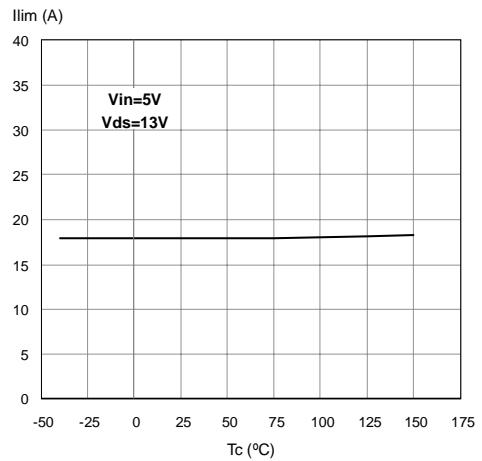
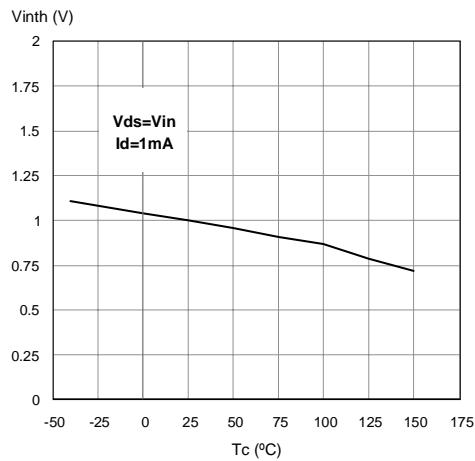
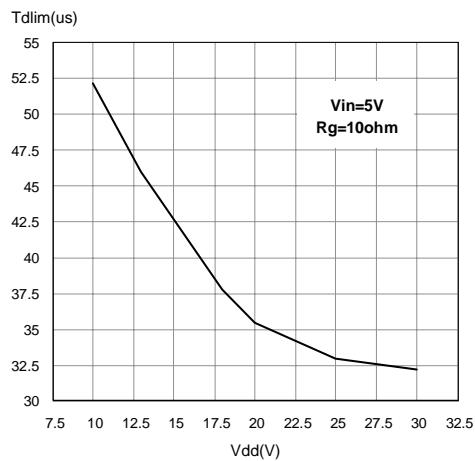


Normalized On Resistance Vs. Temperature



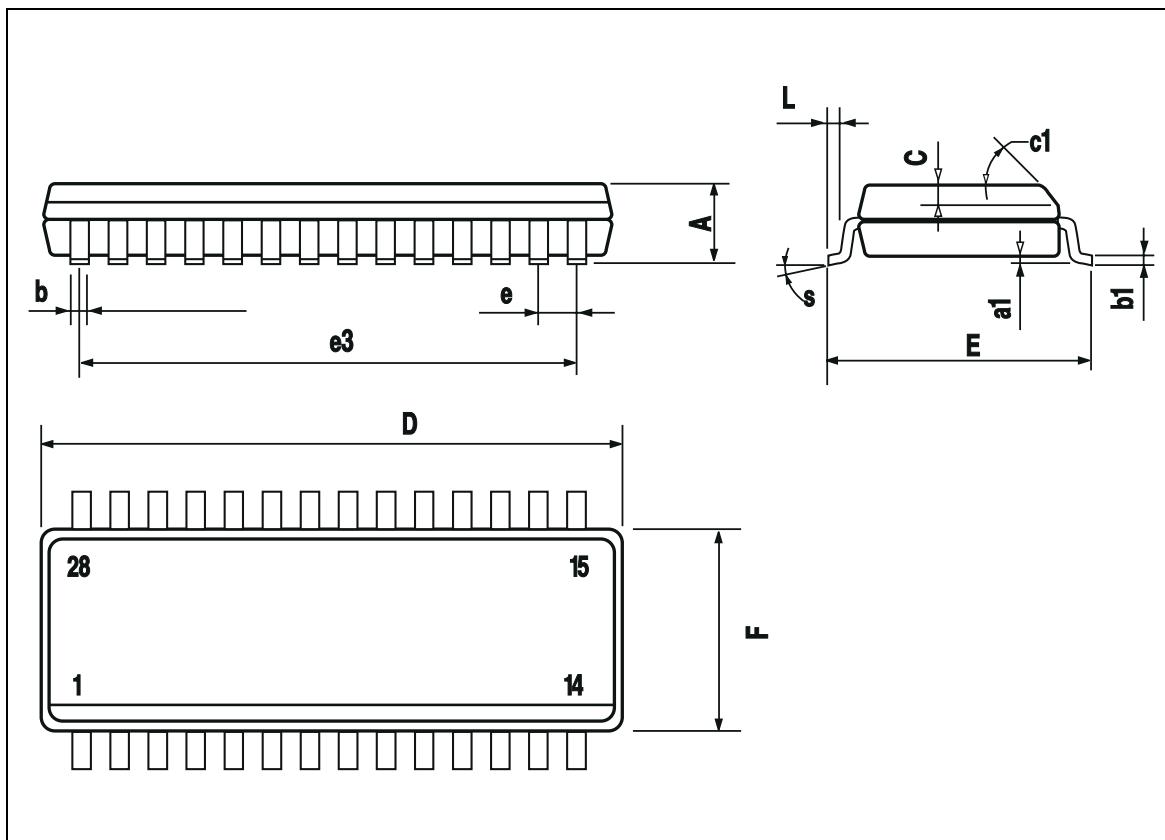
ELECTRICAL CHARACTERIZATION FOR LOW SIDE SWITCHES (continued)

Normalized Input Threshold Voltage Vs. Current Limit Vs. Junction Temperature
Temperature

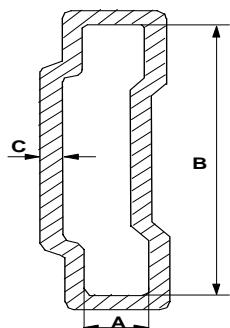
**Step Response Current Limit**

SO-28 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.10		0.30	0.004		0.012
b	0.35		0.49	0.013		0.019
b1	0.23		0.32	0.009		0.012
C		0.50			0.020	
c1	45 (typ.)					
D	17.7		18.1	0.697		0.713
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		16.51			0.650	
F	7.40		7.60	0.291		0.299
L	0.40		1.27	0.016		0.050
S	8 (max.)					



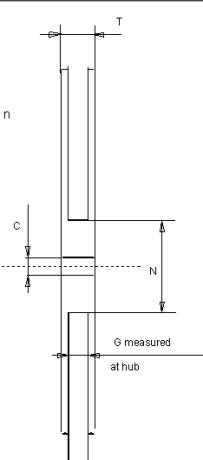
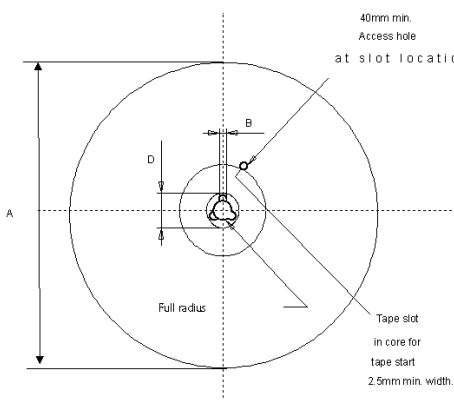
SO-28 TUBE SHIPMENT (no suffix)



Base Q.ty	28
Bulk Q.ty	700
Tube length (± 0.5)	532
A	3.5
B	13.8
C (± 0.1)	0.6

All dimensions are in mm.

TAPE AND REEL SHIPMENT (suffix "13TR")



REEL DIMENSIONS

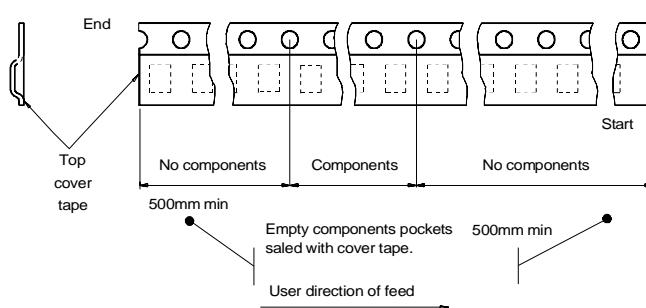
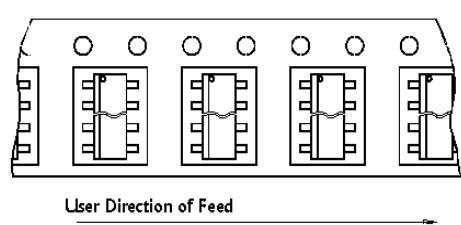
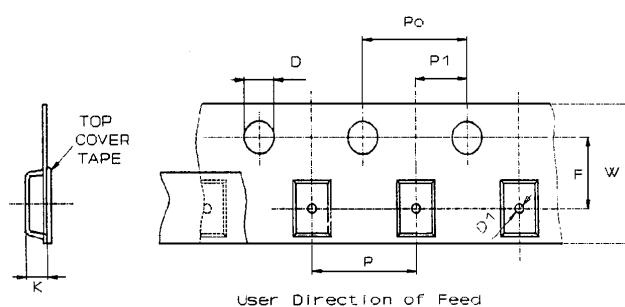
Base Q.ty	1000
Bulk Q.ty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	16.4
N (min)	60
T (max)	22.4

TAPE DIMENSIONS

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Tape width	W	16
Tape Hole Spacing	P0 (± 0.1)	4
Component Spacing	P	12
Hole Diameter	D ($\pm 0.1/-0$)	1.5
Hole Diameter	D1 (min)	1.5
Hole Position	F (± 0.05)	7.5
Compartment Depth	K (max)	6.5
Hole Spacing	P1 (± 0.1)	2

All dimensions are in mm.



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