Advance Information Supplement

Subject:	Additional Information for VDP 313xY
Data Sheet Concerned:	VDP 313xY 6251-519-1AI, Edition Feb. 24, 2000
Supplement:	No. 1/ 6251-519-1AIS
Edition:	Jan. 30, 2001

1. VDP 313xY-B2 — 14.11.2000

The VDP 313xY-B2 is hardware and software compatible to VDP 313xY-B1. Problems 5-10 have been corrected in this version.

1.1. New Features in Version B2:

Separate sync signals (HS/VS) can be output by switching the function of the CSY pin to horizontal sync output.

I²C Sub-address	Number of Bits	Mode	Function	Default	Name
h'10	8	w/r	Sync output bit[5:0] reserved (set to 0) bit[7:6] function of CSY pin 00 composite sync signal output 01 25 Hz output (field1/field2 signal) 10 horizontal sync signal output 11 1 MHz horizontal drive clock	0	CSYM

The INTLC pin can be forced to static high or low (depending on the defined INTLC inversion)

I²C Sub-address	Number of Bits	Mode	Function	Default	Name
h'9D	8	w/r	sync output control bit[0] invert INTLC bit[1] disable INTLC (tristateINTLC output) bit[2] invert VS bit[3] disable VS bit[4] disable CSY bit[5] force INTLC to polarity defined in 'INTLCINV'	0	SYCTRL INTLCINV INTLCDIS VSINV VSDIS CSYDIS INTLCFRC

The gain of the CR and CB components can be adjusted independently by enabling an additional attenuation of CR.

FP Sub-address	Function			Default	Name
h’17A	bit[10:0]	0..2047	CR-attenuation	1591	CR_ATT
	bit[11]	0/1	disable/enable CR-attenuation	0	CR_ATT_ENA

If not used, the second A/D converter for chrominance inputs can be disabled.

FP Sub-address	Function			Default	Name
h’39	bit[10:0]	0..2047	amplitude killer level (0:killer disabled)	25	KILVL
	bit[11]	0/1	disable/enable chroma ADC	0	

To allow the implementation of a peak white limiter as a function of the beamcurrent (with an external controller), the beamcurrent reduction value is averaged and stored in a new status register:

FP Sub-address	Function		Default	Name
h’60	bit[9:0]	latched multiplier for beamcurrent reduction	0	BCL_LAT

2. VDP 313xY-B1 05.06.2000

2.1. Differences between VDP 313xY-B1 and VDP 313xY-A0:

2.1.1. Horizontal Deflection

The new mode for horizontal deflection is now fully functional. From now on we recommend to use this new mode only (set I2C register h'10, bit[0] to 0!). The horizontal phase adjustment is different as in VDPB as the display timing is no longer coupled to the horizontal flyback (and PLL3) but derived directly from PLL2.

The new procedure for phase adjustment is as follows:

1. With HDRV the duration of the horizontal drive pulse has to be adjusted
2. With POFS2 the delay between input video and display timing (e.g. clamping pulse for analog RGB) has to be adjusted
3. With CSYDEL the delay between video and analog RGB (OSD) has to be adjusted.
4. With CSYDEL and HPOS the horizontal position of both, the digital and analog RGB signal (from SCART) relative to the clamping pulse has to be adjusted to the correct position, e.g. the pedestal of the generator signal.
5. With POFS3 the position of horizontal drive/flyback relative to RGB has to be adjusted
6. With NEWLIN the position of a scaled video picture can be adjusted (left, middle, center, etc; versions with panorama scaler only).
7. With HBST and HBSO, the start and stop values for the horizontal blanking have to be adjusted.

2.1.2. Chroma Format

The default chroma format has been adapted so that the selected format after reset is already correct. An additional initialization is no longer necessary. Leave bit[7:3] of h'14 to zero.

I²C Sub-address	Number of Bits	Mode	Function	Default	Name
h'14	8	w/r	luma/chroma matching delay		
			bit[2:0] –3...3 variable chroma delay	0	LDB
			bit[7:3] reserved, set to 0	0	

2.1.3. Black Level Expander

The stop position of the measurement window of the black level expander is now programmable also. It depends directly from the start position (symmetrical window) and the vertical standard. The vertical standard is selected with bit[8[of h'73.

I²C Sub-address	Number of Bits	Mode	Function	Default	Name
h'73	9	w v	black level expander measurement (not in version A0!)		BLE3
			bit[7:0] 0..255 vstart	15	BVST
			bit[8] 0/1 50/60 Hz measurement windowlength start line = vstart; stop line = 336/283 - vstart (or vertical sync)	0	BWL

2.1.4. CSY/VS/INTLC Output

The sync outputs can be disabled/inverted with the SYCTRL register.

I²C Sub-address	Number of Bits	Mode	Function		Default	Name
h'9D	8	w/r	sync output control		0	SYCTRL
			bit[0]	invert INTLC		INTLCINV
			bit[1]	disable INTLC (tristateINTLC output)		INTLCDIS
			bit[2]	invert VS		VSINV
			bit[3]	disable VS		VSDIS
			bit[4]	disable CSY		CSYDIS

2.1.5. Hardware ID

The definition of the following register is new:

I²C Sub-address	Number of Bits	Mode	Function		Default	Name
h'9F	16	r	Hardware version number (not in version A0)		read only	HWID
			bit[7:0]	hardware id (A3 =h'13, B1 = h'21 a.s.o.)		
			bit[15:8]	product code VDP 31xx Y (e.g. h'32 for VDP 3132 Y)		

2.2. Remaining Problems of VDP 313xY-B1 07.06.2000

No.	Problem	Description	Comment	OK
5.	Sync slicer	performance of vertical sync slicer not sufficient	firmware redesign B2	B2
6.	TINT phase	TINT phase inverted in YCrCb mode (NTSC only).	hardware redesign B2 workaround: check version and invert TINT value for B1	B2
7.	CSY output	delay with register CSYDEL not yet available; position shifted by 1/2 line	will be corrected in B2	B2
8.	no HOUT during reset	HOUT disabled during reset	will be corrected in B2	B2
9.	Scaler bypass after reset	sometimes, the IC comes up with enabled scaler bypass	will be corrected in B2	B2
10.	no luma lowpass filter	luma lowpass filter is disabled	will be corrected in B2	B2

3. VDP 313xY-A0 02.05.2000

3.1. Differences between VDP 313xY-A0 and VDP 31xxB

3.1.1. Features

– YCrCb input added

– automatic standard recognition added

– detection of Macrovision signals added

– angle and bow correction added

– no digital RGB interface for TPU 3050

– no standby mode and CLK5 output

3.1.2. Pinning

– CLK5 and VSTBY replaced by Cb and Cr/CIN2 inputs

– PR0 replaced by VSUPD

– PR1/2 replaced by PORT0/1

– HCS and FSY no longer multiplexe with PORT0/1

– GNDV replaced by VERTQ

– 3.3 V digital supply voltage (VSUPD)

3.1.3. Controlling

The I^2C addresses of the following registers have been changed:

New I^2C Sub-address	Old I^2C Sub-address	Function	Default	Name
SCAN VELOCITY MODULATION				
h'5A	h'62	video mode coefficients		
		bit[5:0] gain1	60	SVG1
		bit[8:6] differentiator delay 1 (0 = filter off, 1...6 = delay)	4	SVD1
h'56	h'5E	text mode coefficients		
		bit[5:0] gain 2	60	SVG2
		bit[8:6] differentiator delay 2 (0 = filter off, 1...6 = delay)	4	SVD2
h'52	h'5A	limiter		
		bit[6:0] limit value	100	SVLIM
		bit[8:5] not used, set to "0"	0	
h'4E	h'56	delay and coring		
		bit[3:0] adjustable delay, in 1/2 display clock steps,	7	SVDEL
		bit[7:4] coring value	0	SVCOR
		bit[8] not used, set to "0"		

New I²C Sub-address	Old I²C Sub-address	Function	Default	Name
DISPLAY CONTROLS & CHROMINANCE IMPROVEMENT				
h'4A	h'52	cutoff Red	0	CR
h'46	h'4E	cutoff Green	0	CG
h'42	h'4A	cutoff Blue	0	CB
h'5E	h'66	digital transient improvement		
		bit[3:0] 0..15 coring value	1	DTICO
		bit[7:4] 0..15 DTI gain	5	DTIGA
		bit[8] 0/1 narrow/wide bandwidth mode	1	DTIMO
HORIZONTAL DEFLECTION				
h'6E	h'7A	adjustable delay of PLL2, clamping, and blanking (relative to front sync); adjust clamping pulse for analog RGB input bit[8:0] –256..+255 ± 8 µs	–141	POFS2
h'72	h'76	adjustable delay of flyback, main sync, csync and analog RGB (relative to PLL2); adjust horizontal drive or csync bit[8:0] –256..+255 ± 8 µs	0	POFS3
		PLL2/3 filter coefficients, 1of5 bit code (n+ set bit number)		
h'62	h'6A	bit[5:0] proportional coefficient PLL3, 2^{-n-1}	2	PKP3
h'66	h'6E	bit[5:0] proportional coefficient PLL2, 2^{-n-1}	1	PKP2
h'6A	h'72	bit[5:0] integral coefficient PLL2, 2^{-n-5}	2	PKI2

The definition of the following register has been changed or is new:

I²C Sub-address	Number of Bits	Mode	Function	Default	Name
h'14	8	w/r	luma/chroma matching delay		
			bit[2:0] -3...3 variable chroma delay	0	LDB
			bit[7:3] reserved, set to 0	0	
h'73	9	w v	black level expander measurement (not in version A0!)		BLE3
			bit[7:0] 0..255 vstart	15	BVST
			bit[8] 0/1 50/60 Hz measurement windowlength	0	BWL
			start line = vstart; stop line = 336/283 – vstart (or vertical sync)		
h'76	9	w v	linear term of angle & bow correction bit[8:0] –256..+255 ± 500 ns	0	ANGLE
h'7a	9	w v	quadratic term of angle & bow correction bit[8:0] –256..+255 ± 500 ns	0	BOW
h'6e	9	w v	adjustable delay of PLL2, clamping, and blanking (relative to front sync) bit[8:0] –256..+255 ± 8 µs	–141	POFS2
h'72	9	w v	adjustable delay of horizontal drive & flyback (relative to PLL2) bit[8:0] –256..+255 ± 8 µs	0	POFS3

I²C Sub-address	Number of Bits	Mode	Function	Default	Name
h'7e	9	w v	adjustable delay of main sync (relative to PLL2) adjust horizontal position for digital picture bit[8:0] 20 steps =1 µs	120	HPOS
h'9e	8	w/r	delay of CSY output (relative to PLL2) bit[7:0] –128..127 ± 8 µs	0	CSYDEL

FP Sub-address	Function	Default	Name
h'148	Enable automatic standard recognition (ASR) bit[0] 0/1 PAL B,G,H,I (50 Hz) 4.433618 bit[1] 0/1 NTSC M (60 Hz) 3.579545 bit[2] 0/1 SECAM (50 Hz) 4.286 bit[3] 0/1 NTSC44 (60 Hz) 4.433618 bit[4] 0/1 PAL M (60 Hz) 3.575611 bit[5] 0/1 PAL N (50 Hz) 3.582056 bit[6] 0/1 PAL 60 (60 Hz) 4.433618 bit[10:7] reserved set to 0 bit[11] 1 reset status information 'switch' in asr_status (cleared automatically) 0: disable recognition; 1: enable recognition Note: For correct operation don't change FP reg. 20h and 21h, while ASR is enabled!	0	ASR_ENA
h'14E	Status of automatic standard recognition bit[0] 1 error of the vertical standard (neither 50 nor 60 Hz) bit[1] 1 detected standard is disabled bit[2] 1 search active bit[3] 1 search terminated, but failed bit[4] 1 no color found bit[5] 1 standard has been switched (since last reset of this flag with bit[11] of asr_enable) bit[4:0] 00000 all ok 00001 search not started, because vwin error detected (no input or SECAM L) 00010 search not started, because detected vert. standard not enabled 0x1x0 search started and still active 01x00 search failed (found standard not correct) 01x10 search failed, (detected color standard not enabled) 10000 no color found (monochrome input or switch betw. CVBS/SVHS necessary)	0	ASR_STATUS VWINERR DISABLED BUSY FAILED NOCOLOR SWITCH

FP Sub-address	Function	Default	Name
h'2F	YC_RC_B mode control register bit[6:0] reserved (set to 0) bit[7] 1 ADC over-/underflow (has to be reset after read if used) bit[8] 0 disable YC_RC_B 1 enable YC_RC_B bit[9] ADC range 0 nominal input amplitude (±350 mV) 1 extented input amplitude (±500 mV) bit[11:10] reserved (set to 0) Note: Activate the YC_RC_B mode by - enabling YC_RC_B - selecting simple PAL or NTSC M, svhs=1, comb=0 in the std register - setting cbw=2 in the insel register	0	YCRCB
h'30	Saturation control bit[11:0] 0...4094 (2070 corresponds to 100% saturation) 4095 disabled (test mode only)	2070	ACC_SAT
h'B5	crystal oscillator line-locked mode, autolock feature. If autolock is enabled, crystal oscillator locking is started automatically. bit[11:0] threshold; 0: autolock off	400	AUTOLOCK
h'14	input noise level	read only	NOISE
h'36	measured burst amplitude	read only	BAMPL
h'170	status of macrovision detection bit[0] AGC pulse detected bit[1] pseudo sync detected	read only	MCV_STATUS
h'171	bit[11:0] first line of macrovision detection window	6	MCV_START
h'172	bit[11:0] last line of macrovision detection window	15	MCV_STOP

3.2. Remaining Problems for VDP 313xY-A0 24.02.2000

No.	Problem	Description	Comment	OK
1.	Clamping of Cr/Cb input	Wrong internal synchronization. Clamping depends on result of hpll setup	hardware redesign B1 workaround (for evaluation only): perform several standard setups until clamping is ok (only for PAL; DVCO locked)	B1
2.	no VERTQ output	VERTQ output disabled	hardware redesign B1	B1
3.	Cr/Cb swap	swap of Cr/Cb in YCrCb mode (NTSC only)	hardware redesign B1	B1
4.	jitter in hor. deflection	wrong display clock shift; angle & bow not functional	hardware redesign B1 workaround: set h’10, bit[0] to 1 (old horizonatl deflection mode)	B1
5.	sync slicer	performance of vertical sync slicer not sufficient	firmware redesign B1	

4. Data Sheet Errata VDP 313xY (for Advance Information: Edition Aug. 15, 2000; 6251-519-1AI)

The definition of the following registers is missing or incorrect:

Default values of Table 2-4 on page 30 are defined as decimal values.

Table 2–4: I^2C control and status registers of the video frontend

I^2C Sub-address	Number of Bits	Mode	Function	Default	Name
Miscellaneous					
h'22	16	w/r	NEWLINE (available for versions with panorama scaler only): bit[10:0] NEWLINE register This register defines the readout start of the next line in respect to the value of the sync counter. bit[15:11] reserved (set to 0)	50	NEWLIN

Table 2–5: I^2C control and status registers of the video backend
(Registers are set to '0' at reset, default values are recommendations)

I^2C Sub-address	Number of Bits	Mode	Function	Default	Name
Luminance Channel					
h'73	9	w v	black level expander measurement bit[7:0] 0..255 vstart bit[8] 0/1 50/60 Hz measurement windowlength start line = vstart stop line = 336/283 – vstart (or vertical sync)	 15 0	BLE3 BVST BWL
Horizontal Deflection and Timing					
h'76	9	w v	linear term of angle & bow correction bit[8:0] –256..+255 (± 500 ns)	0	ANGLE
h'7A	9	w v	quadratic term of angle & bow correction bit[8:0] –256..+255 (± 500 ns)	0	BOW
h'6E	9	w v	adjustable delay of PLL2, clamping, and blanking (relative to front sync) bit[8:0] –256..+255 (± 8 µs)	–141	POFS2
h'72	9	w v	adjustable delay of horizontal drive & flyback (relative to PLL2) bit[8:0] –256..+255 (± 8 µs)	0	POFS3

Table 2–5: I²C control and status registers of the video backend
(Registers are set to '0' at reset, default values are recommendations)

I²C Sub-address	Number of Bits	Mode	Function	Default	Name
h'9D	8	w/r	sync output control bit[0] invert INTLC bit[1] disable INTLC (tristateINTLC output) bit[2] invert VS bit[3] disable VS bit[4] disable CSY bit[5] force INTLC to polarity defined in 'INTLCINV'	0	SYCTRL INTLCINV INTLCDIS VSINV VSDIS CSYDIS INTLCFRC
Hardware ID					
h'1F	8	w/r	bit[2:0] reserved, set to zero bit[3] 1 tristate CLK20 bit[4] 1 force CLK20 to low bit[5] 1 force CLK20 to high bit[7:6] reserved		CLK20

Table 2–6: Control Registers of the Fast Processor for control of the video frontend functions
–default values are initializied at reset

FP Sub-address	Function			Default	Name
Comb Filter					
h'27	comb filter control register				CMB_UC
	bit[0]	0	comb coefficients are calculated for luma/chroma	0	CC
		1	comb coefficients for luma are used for luma and chroma		
	bit[1]	0	luma comb strength depends on signal amplitude	0	DAA
		1	luma comb strength is independent of amplitude		
	bit[2]	0	reduced comb booster	1	KB
		1	max comb booster		
	bit[4:3]	0..3	comb strength for chroma signal	3	KC
	bit[6:5]	0..3	comb strength for luma signal	2	KY
	bit[11:7]	0..31	overall limitation of the calculated comb coefficients	0	CLIM
		0	no limitation		
		31	max limitation (1/2)		

Table 2–6: Control Registers of the Fast Processor for control of the video frontend functions
–default values are initializied at reset

FP Sub-address	Function	Default	Name
Standard Selection			
h'2F	YC_RC_B mode control register bit[6:0] reserved (set to 0) bit[7] 1 clipping due to ADC over-/underflow (has to be reset after read if used) bit[8] 0 disable YC_RC_B 1 enable YC_RC_B bit[9] ADC range 0 nominal input amplitude (±350 mV) 1 extented input amplitude (±500 mV) bit[11:10] reserved (set to 0) Note: Activate the YC_RC_B mode by - enabling YC_RC_B - selecting simple PAL or NTSC M, svhs=1, comb=0 in the std register - setting cbw=2 in the insel register	0	YCRCB ADCCLIP YCRCB_EN ADCR

Table 2–8: Control registers of the Fast Processor for control of the video backend functions
–default values are initializied at reset

FP Sub-address	Function	Default	Name
FP Display Control Register, Deflection			
h'10F	EHT compensation east/west gain coefficient –512...511 (sign extension to 12 bit)	0	EHTEW