SIEMENS

V23809-E1-E30
8B/10B V23809-E1-E40
1300 nm ESCON® Parallel Transceiver

Preliminary Data Sheet

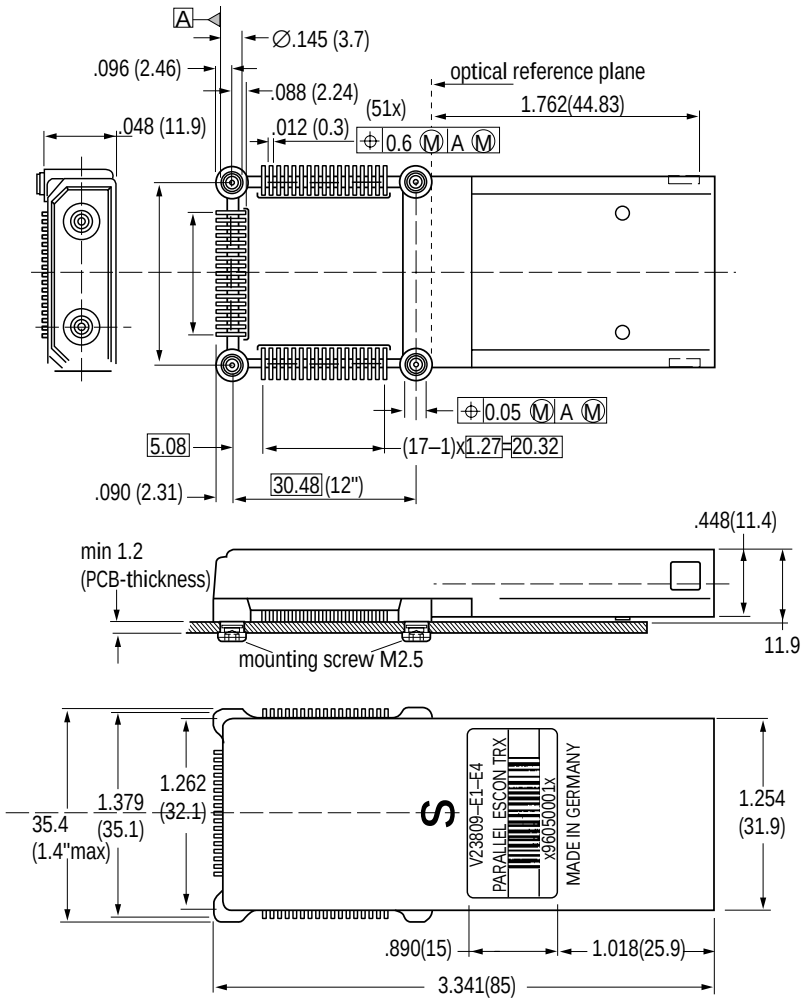
FEATURES

- **Complies with ESCON and SBCON standards**
- **Fully compatible with parallel transceiver V23806-A6-X1**
- **Transceiver includes clock recovery module, P-S /S-P and ESCON/SBCON receptacle**
- **Optional 8B/10B coder/decoder function (E40 only)**
- **SMT component for easy mounting on surface mount PC boards**
- **Transceiver mates keyed ESCON/ SBCON connector**
- **Data rates for ESCON/SBCON applications from 100 to 200 MBaud**
- **Data rates for individual applications from 100 to 300 MBaud**
- **Transmission distance of 3 km and more**
- **Single power supply of 3.0 V to 5.5 V (E40 only)**
- **Extremely low power consumption <2 W at 3.3 V (E40 only)**
- **All inputs and outputs TTL compatible**
- **Excellent EMI performance**
- **System optimized for 62.5 and 50 µm graded index fiber**
- **0.7" spacing between optical interface of transmitter and receiver**
- **Low profile for high slot density**

APPLICATIONS

- **ESCON architecture**
- **High speed computer links**
- **Local area networks**
- **High definition/digital television**
- **Switching systems**
- **Control systems**
- **FC transceiver version with SC duplex shell planned**

Dimensions in inches (mm)



Maximum Ratings (Absolute maximum stress)

Exceeding any one of these values may destroy the device immediately. However, the electro-optical characteristics described in the following tables are only valid for use under the recommended operating conditions.

Power Dissipation (PD)..... 2 W
Supply voltage (V_{CC}–V_{EE}) ..... –0.5 V to7 V
Maximum Inqut Voltage (V_{IN}) ..... V_{EE} to V_{CC}
Operating Case Temperature (Tcase).....–25 to 85°C
Humidity/Temperature Test Condition (R_H) ..... 85/85 %/°C
Lifetest Condition (Tamb/life).....115/1000°C/h
Soldering Conditions Temp/Time (T_{sold}) .....260/10°C/s
ESD Resistance (all pins to V_{EE}, Human Body) (ESD) .....1.5 kV
Output Current (I_o)..... 50 mA

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DESCRIPTION

The Siemens ESCON/SBCON optical devices, along with the ESCON/SBCON optical duplex connector, are best suited for high speed fiber optic duplex transmission systems operating at a wavelength of 1300 nm. The system is fully compatible with the IBM ESCON standard and the upcoming SBCON of ANSI. It includes a transmitter and a receiver as well as the clock recovery function and the serial/parallel interfaces. In addition, an 8 B/10 B coder-decoder function can be used optionally.

The ESCON Parallel Transceiver is designed for data rates of up to 300 MBaud. A non-dissipative plastic receptacle matches the ESCON duplex connector.

The inputs/outputs are TTL compatible and the unit operates on a single power supply from 3.0 to 5.5 V.

The optical interface of transmitter and receiver have standard 0.7” spacing. Receptacle and connector have been keyed in order to prevent reverse insertion of the connector into the receptacle. After proper insertion the connector is securely held by a snap-in lock mechanism.

The transmitter converts parallel electrical TTL input signals into an optical serial signal at data rates of between 100 and 300 MBaud. The receiver performs clock recovery on the incoming data stream and converts data to a parallel output.

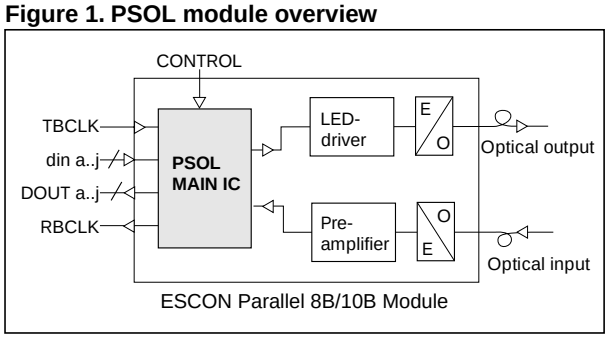
New Built-in Functions (E40 only)

The ESCON Parallel Transceiver 8B/10B contains an encoder/decoder unit, a serial/parallel converter part, a synthesizer/clock recovery PLL section, and a TTL input and a PECL output interface, as well as the serial electro-optical converting function.

The data from the parallel TTL input interface are converted to a serial bitstream feeding an LED driver. The differential receiver signal is converted to parallel data words at the TTL output.

This transceiver meets the requirements for the IBM ESCON® standard.

Figure 1. PSOL module overview



ESCON Parallel 8B/10B Module

The transceiver can be operated in two modes:

a) FSOL mode: conversion of 10 bit electrical data words to a serial bitstream and conversion of a serial bitstream to 10 bit-wide electrical data words.

In this mode the transceiver can be used as a plug-in replacement for the Parallel Transceiver V23806-A6-X1.

b) PSOL mode: conversion of 8 bit electrical data words to a serial optical bitstream using an 8B/10B encoder for optical data transmission and conversion of a serial bitstream to 10 bit-wide electrical data words using a 10B/8B decoder.

Switching between the two modes is done by applying Vcc or GND to the $\overline{\text{FSOL}}$/PSOL pins respectively.

Figure 2. Functionality: PSOL main IC in FSOL mode

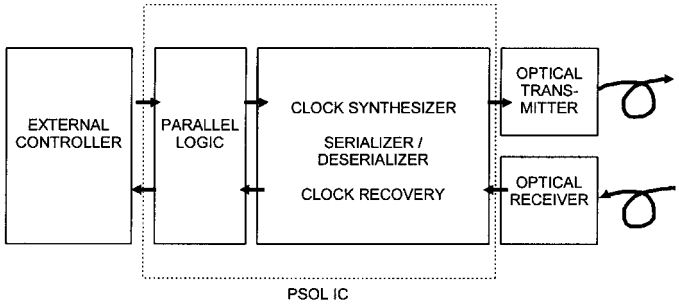
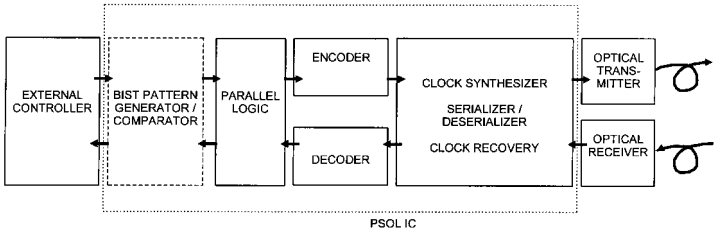


Figure 3. Functionality: PSOL main IC in PSOL mode



Recommended Operating Conditions

Parameter	Sym.	Min	Max	Units
Operating Ambient Temperature	T_C	0	70	°C
Power Supply Voltage	$V_{CC}–V_{EE}$	3	5.5	V
Supply Current 3.3 V	I_{CC}		300	mA
Supply Current 5 V			400	
Data Input High Voltage	V_{IH}	2	V_{CC}	V
Data Input Low Voltage	V_{IL}	V_{ee}	0.8	
Input Data Rise/Fall, 10–90%	t_R, t_F	0.4	1.3	ns
Output Current High	I_o		–0.4	mA
Output Current Low	I_{CC2}		4	

Transmitter Electro-Optical Characteristics
(Values in parentheses are for 300 MBd)

Transmitter	Sym.	Min.	Typ.	Max.	Units
Data Rate	DR	100		200 (320)	MBaud
Supply Current 3.3 V(1)	I_{CC}			200	mA
Supply Current 5 V(1)				300	
Launched Power (Ave.) BOL into 62.5µm Fiber (2, 3, 4)	P_O	–21 (–22)	–16.5	–14	dBm
Launched Power (Ave.) EOL into 62.5µm Fiber (2, 3. 4. 7)		–22 (–23)			

Transmitter	Sym.	Min.	Typ.	Max.	Units
Center Wavelength(5, 6)	l_C	1285		1355	nm
Spectral Width (FWHM)(6)	σλ			160	
Temperature Coefficient, Optical Optput Power	TCp			0.03	dB/°C
Output Rise/Fall Time, 20–80%(6)	t_R, t_F		1	1.7 (2)	ns
Deterministic Jitter(8)	J_d		0.6	0.8	
Random Jitter(9)	J_r			0.06	
Extinction Ratio (dynamic)(10)	ER		–16	–13	dB

Notes

1. Transmitter operating at 200 MBaud and 50% duty cycle.
2. Measured at the end of 1 meter fiber, cladding modes removed at a data rate of between 50 and 200 MBaud, 50% duty cycle.
3. Po [dBm]=10 log (Po/1 mW)
4. Po (BOL) >–20dBm and Po (EOL) >–21.5 dBm at T_{case}=60°C.
5. Measured at T_{case}=60°C
6. Full width, half magnitude of peak wavelength: special relationship between λc, dλ, tr/tf according to FC-PH Rev 4.3 Paragraph 6.3.2. and Fig.26. Spectral width must be considered.
7. Over 10^5 hours lifetime at T_{amb}=35°C
8. Deterministic Jitter, measured at 200 MBaud with Jitter Test Pattern shown in Figure 5. In the Test Pattern are five positive and five negative transitions. Measure the time of the 50% crossing of all 10 transitions. The time of each crossing is then compared to the mean expected time of the crossing. The DJ is the range of the timing variations.
9. RMS value measured with 1010 pattern at 200 Mbaud. Peak-to-peak value is determined as RMS multiplied by 14 for BER 1E-12.
10. Extinction ratio is the logarithmic measure of the optical power in the OFF state (POFF) to twice the average power (P0):
    ER=10 log [(2xP0)/POFF]; optical power measured in mW or
    ER=ΩP0+3dBΩ–POFF; optical power measured in dBm

Receiver Electro-Optical Characteristics

(Values in parentheses are for 300 MBd)

Receiver	Sym.	Min.	Typ.	Max.	Units
Data Rate	Dr	100		200 (300)	MBaud
Supply Current (1)	I_{CC}			100	mA
Sensitivity (Average Power)BOL(2, 3, 4)	P_{IN}	–32.5 (–29)	–35.5		dBm
Sensitivity (Average Power) EOL(2, 3, 4, 5)		–32 (–28.5)	–35		
Saturation (Average Power)	P_{SAT}	–14			
Signal Detect Assert Level(6)	P_{SDA}	–44.5		–36,0	
Signal Detect Deassert Level(6)	P_{SDD}	–45		–37.5	
Signal Detect Hysteresis	P_{SDA}–P_{SDD}	0.5	1.5	3	dB
Signal Detect Reaction Time	SDreac	3		500	µs

Receiver	Sym.	Min.	Typ.	Max.	Units
Signal Detect Hysteresis	P_{SDA}–P_{SDD}	0.5	1.5	3	dB
Signal Detect Reaction Time	SDreac	3		500	µs
Max. Deterministic Jitter Optical Input(7, 9)	J_d			0.19	% of Unit Intervals
Max. Random Jitter RMS Optical Input(8, 9)	J_r			0.09	

Notes

1. For V_{CC}–V_{EE} (min, max). 50% duty cycle.
2. Measured at the end of 1 meter fiber, cladding modes removed at a data rate of between 50 and 200 MBaud, 50% duty cycle.
3. Po [dBm]=10 log (Po [mW])
4. Measured at BER=1E-12, 200 MBaud transmission rate and 50% duty cycle 2^7-1 PRBS pattern; center wavelength between 1200nm and 1500 nm, fiber type 62.5/125 µm/0.29 NA or 50/125 µm/0.2 NA; input optical rise and fall times are 1.2 ns and 1.5 ns (20% - 80%) respectively.
5. Over 10^5 hours lifetime at T_{amb}=35°C
6. Indicates the presence or absence of optical power at the receiver input. Signal detect at logic “high“ when asserted. All powers are average power levels. Pattern 2^7-1 at 200 MBaud.
7. Deterministic Jitter measured at 200 MBaud with Jitter Test Pattern shown in Figure 5. In the test pattern are five positive and five negative transitions. Measure the time of the 50% crossing of all 10 transitions. The time of each crossing is then compared to the mean expected time of the crossing. The DJ is the range of the timing variations.
8. To convert from specified RMS value to peak-to-peak value (at BER 1E-12) multiply value by 14.
9. Jitter at optical input. Jitter magnitudes above specified level may increase the bit error rate.

Transceiver Pin Description 10 Bit Interface: FSOL Mode

In this mode the transceiver is compatible with the former version, V23806-A6-X1

Pin#	Pin Name	Level/Logic	Description
1, 6, 9, 26, 43, 45, 48, 51	Vee	Power Supply	Ground attached to the case
2	Vcc PRE		Preamplifier positive power supply
3	SIGDET	TTL out	Signal detected
4	LOCKREF	TTL in	Control input for RX PLL
5	SYNCEN		Control of byte alignment operation
7,8	VccFAST	Power Supply	Bipolar IC positive power supply
10 to 19	Dout a to j	TTL out	Data output parallel 10 channels
20	RBCLK	TTL out	Read byte clock
21	PAROUT		Parity bit out
22	BSYNC		Byte synchronization operation
23	PARERR	TTL out	Parity bit error

Pin#	Pin Name	Level/Logic	Description
24,25	VccSLOW	Power Supply	Logic positive power supply
27	Loopsel a	TTL in	Test loop select
28	Loopsel b		
29	RESREC		Receiver reset
30	RESFF		Reset all flip-flops
31	TBCLK		Transmit byte clock
32	PARIN		Parity bit in
33 to 42	Din j to a		Data input parallel 10 channels
44	TESTCLK		Test clock. In test mode this clock is the bit clock
46	TESTMOD		If this signal is low TESTCLK is used
47	TXOFF		Transceiver off when logical high
49,50	Vcc DRI	Power Supply	LED driver positive power supply

Transceiver Pin Description 8 Bit interface: PSOL Mode (E40 only)

Pin#	Pin Name	Level/ Logic	Description
1, 6, 26, 43, 45, 48, 51	Vee	Power Supply	Ground attached to the case
2	Vcc PRE		Preamplifier positive power supply
3	SIGDET	TTL out	Signal detected
4	$\overline{R}$		Read pulse for external FIFOs
5	SYNCEN	TTL in	Control of byte alignment operation
7,8	VccFAST	Power Supply	Positive power supply of the bipolar IC
9	$\overline{PSOL1}$/ PSOL2	TTL in	Mode select for PSOL Mode 1 or Mode 2
10	RK	TTL out	Receiver special character flag
11 to 18	Dout A to H		Decoded data output parallel 8 channels
19	RCV		Receiver code violation
20	RBCLK		Read byte clock
21	PAROUT		Parity bit out
22	$\overline{W}$		Write pulse for external FIFOs
23	PARERR		Parity bit error
24, 25	VccSLOW	Power Supply	Logic positive power supply

Pin#	Pin Name	Level/ Logic	Description
27	Loopsel a	TTL in	Test loop select
28	Loopsel b		
29	$\overline{EPI}$		Enable parallel input
30	$\overline{ENPI}$		Enable next parallel input
31	TBCLK		Transmit byte clock
32	PARIN		Parity bit in
33	TCV		Transmitter code violation
34 to 41	Din H to A		Uncoded data input parallel 8 channels
42	TK		Transmitter special character flag
44	$\overline{RAW}$/COD		Select Raw Mode/Coder Mode
46	$\overline{BIST}$		Enable built-in self test
47	TXOFF		Transceiver off when logical high
49, 50	Vcc DRI	Power Supply	LED driver positive power supply

Figure 4. Signal detect threshold and hysteresis

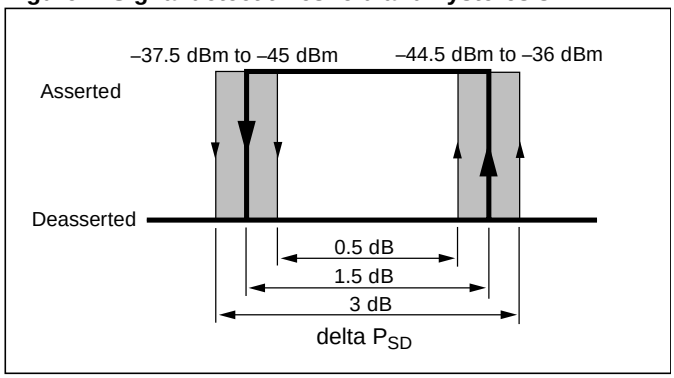
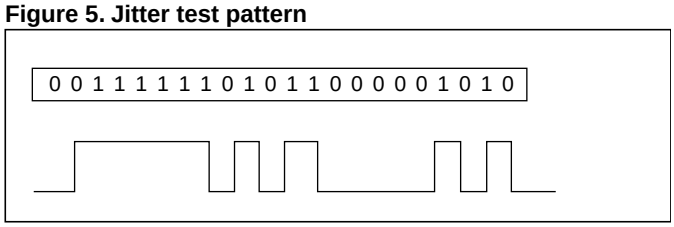
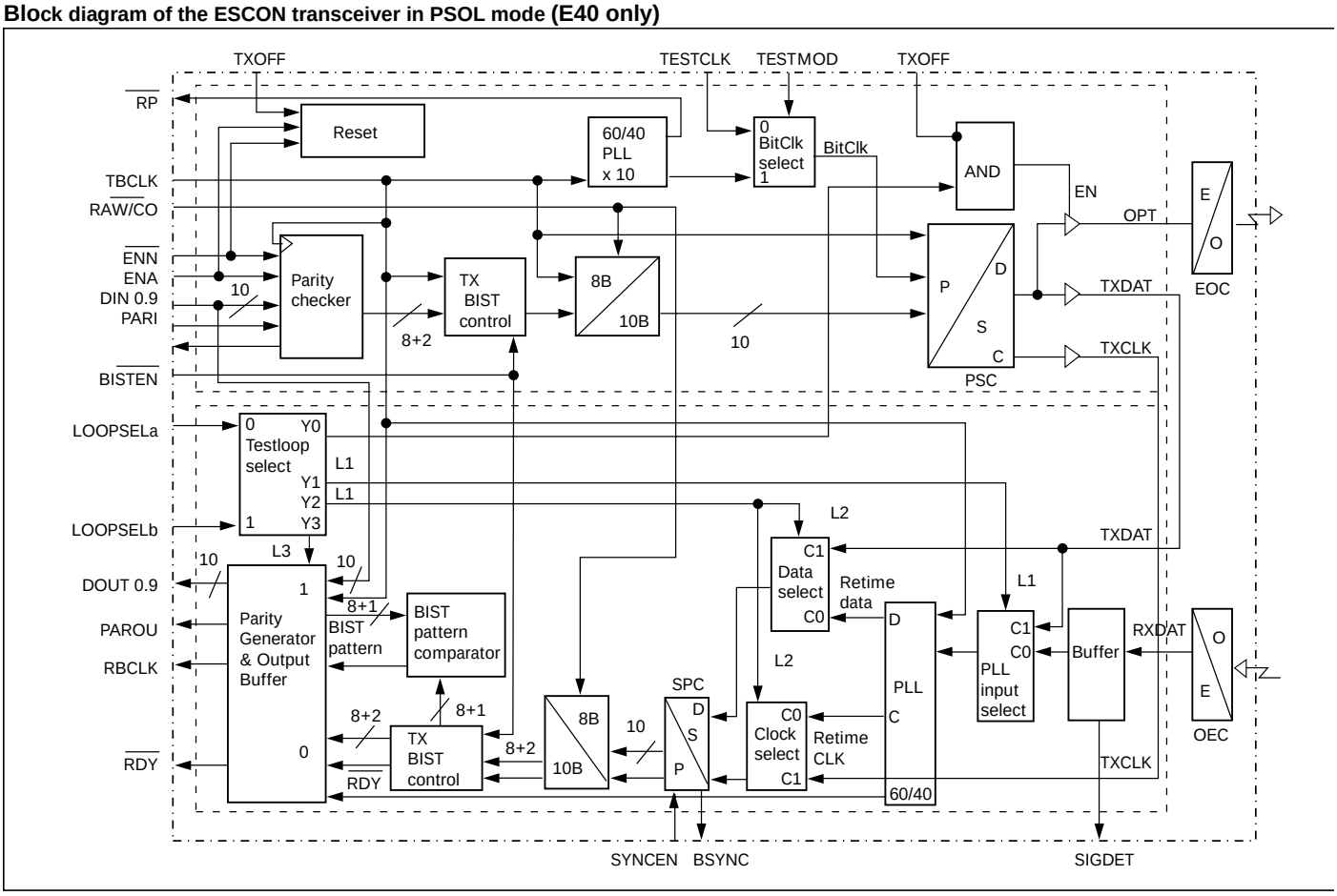


Figure 5. Jitter test pattern



Block diagram of the ESCON transceiver in PSOL mode (E40 only)



APPLICATION NOTE

Power Supply Filtering

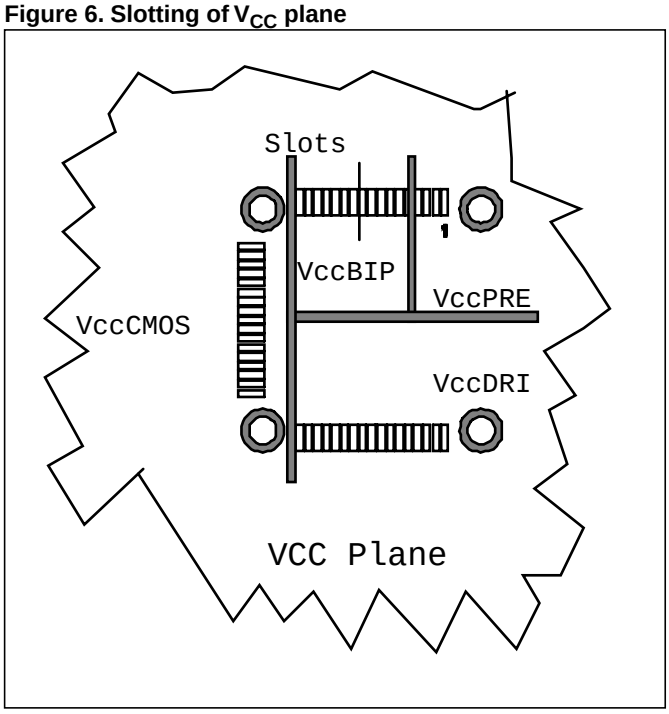
In most of the applications using ESCON 200 MBd Optical Transceivers, additional high speed circuits such as switching power supply, clock oscillator, or high speed multiplexer are present on the application board. These often create power supply noise at a high spectral bandwidth, caused by very fast transitions in today's chip technology.

The Siemens ESCON Transceiver Family provides superior EMI performance regarding emission and immission of radiation and provides immunity against conductive noise. Some basic recommendations are given in this document to ensure proper functionality in the field.

For proper operation the use of a multilayer board with ground and Vcc plane is strongly recommended. The Vcc plane should be slotted as shown in Figure 6 to avoid crosstalk between different circuitry inside the module. The metallized package is internally connected to the V_{EE}-pins of the module. Nevertheless the package must be connected externally to ground for best shielding characteristics. Ground contact should be made with the ground rings shown in Figure 6. Because of high switching currents at V_{CC}DRI, the use of an external 6.8 to 22 µF capacitor is recommended at V_{CC}DRI.

The observance of normal design rules for high speed digital systems is sufficient to ensure safe operation.

Figure 6. Slotting of V_{CC} plane



Note: Slots are non-copper areas inside the V_{CC} plane to avoid cross-current flow

Figure 7. Recommended footprint

The avoidance of any component or non-isolated structure, like tracks or vias, under the transceiver is strongly recommended.

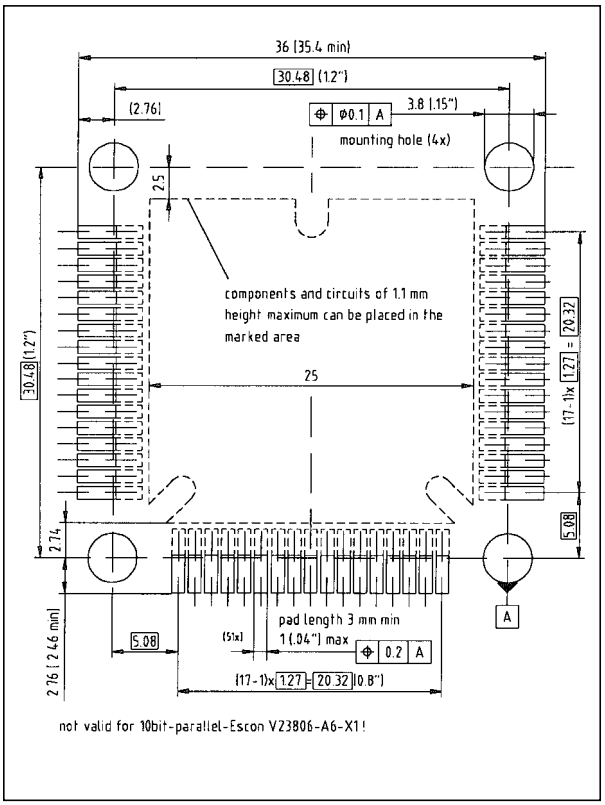


Figure 8. Power-on sequence in FSOL mode