GEC PLESSEY
SEMICONDUCTORS

JANUARY 1995

DS2468 -2.2

ULA DT & DV SERIES

HIGH PERFORMANCE MIXED DIGITAL/ANALOG ARRAY FAMILY

ULTRA HIGH SPEED DIGITAL ARRAYS WITH HIGH PERFORMANCE ANALOG

The DT/DV series of arrays are designed to provide cost effective single chip solutions to high speed combined digital and analog mixed signal systems.

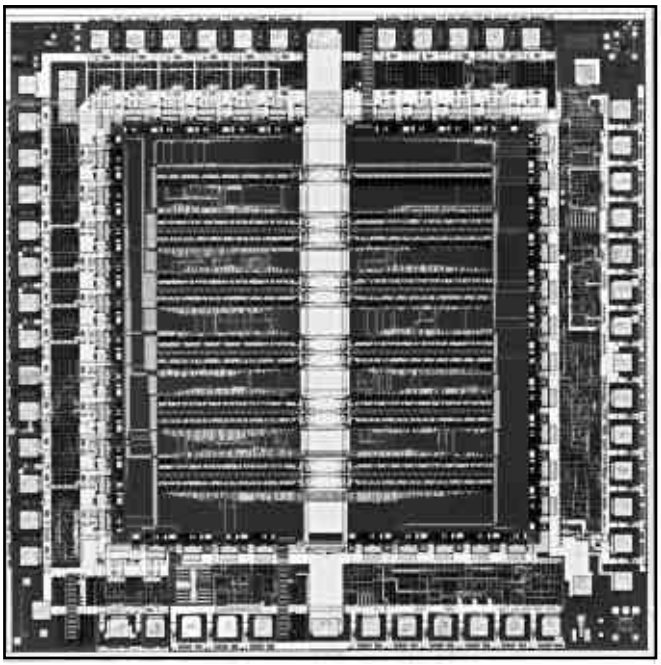

Fig. 1 A DT Series array

FEATURES

- Combines High Performance Digital and Analog
- System Speeds to 200MHz
- Full Design Support, Including:
  - Characterised digital and analog macros
  - Complete CAD suite
  - Silicon compilers
  - SPICE libraries
  - Comprehensive design element libraries
- Analog Features:
  - 200MHz analog capability
  - 43 transistors and 52 resistors per analog cell
  - Closely matched components (1%)
  - Low offsets (< 0·3mV)
  - Optimised for high speed/low power
  - Range of high performance characterised analog macros
  - Complex macros can use multiple cells
- Digital Features:
  - Gate delays to 500ps
  - Differential logic giving unprecedented speed/ power performance
  - Selective speeding-up option
  - Excellent gate delay with high loads
  - Toggle rates to 600MHz
- I/O Features:
  - Interfaces to TTL, CMOS and true ECL
  - 0V to 5V or ±5V operation
- Special Features:
  - Bandgap regulator
  - High current drive transistors (100mA per cell)
- Advanced 1·2 Micron Bipolar Process
- Wide Range of Package Styles
- Full Military Temperature Range

GENERAL DESCRIPTION

For many years, GEC Plessey Semiconductors ASIC products have been successfully fulfilling the requirements for single chip systems in silicon for lower frequency applications. The DT/DV series extends the benefits of mixed signal capability to systems operating at frequencies up to 200MHz. Integrating the complete system onto the chip saves space and assembly costs and greatly simplifies board design.

The DT/DV series arrays feature enhanced high performance mixed Analog and Digital capabilities. The analog cell components are optimised for good matching, low offset and high speed.

There is a high performance logic function core on each array which is supported by a family of Design Elements offering effective gate delays to below 0·5ns. These delays are virtually independent of fan-out, supply voltage and clock frequency.

The supporting libraries of both Analog and Digital Design Elements and Macro functions can be combined to obtain optimum results for a specific system.

The technology employs the 1·2 micron advanced complementary bipolar process (LG2 process), which is fully supported by the EDA environment built around the Cadence Analog Artist Design System and operates within the Cadence Design Framework architecture.

PRODUCT RANGE

The DT/DV array series product range is shown in Table 1, below. Actual cell utilisation can be up to 100% of the uncommitted gate count, depending on the circuit structure.

Detail	ULA Type							
	6DT 6DV	11DT 11DV	16DT 16DV	25DV	28DV	38DT 38DV	60DT 60DV	90DT 90DV
Matrix core cells(DT)[1]	252	440	676	1020	-	1596	2500	3762
Matrix core cells(DV)[1,2]	170	324	432	-	780	1080	1672	2550
Equivalent gate count	630	1100	1690	2250	2280	3990	6250	9405
Power pads	8	8	8	8	8	10	10	12
Analog cells (full)	26	40	48	68	68	76	94	120
Analog cells (half)	8	8	8	8	8	8	8	8
Bond pads	42	56	64	76	84	94	112	140

Table 1 Details of range of DT/DV series arrays

NOTES
1. A core matrix gate is defined as a 2-input 2-output RNOR gate. The dual output configuration of the RNOR gate allows for wire-OR, which significantly increases the effective gate count.
2, All DV core cells are for multi-level (3) differential logic macro implementation.

CHIP ARCHITECTURE

The chip architecture of the DT/DV series shown in Fig. 2 comprises an inner core of matrix cells for the digital circuitry. The outer ring of analog cells is used for realising the analog functions and for interfacing.

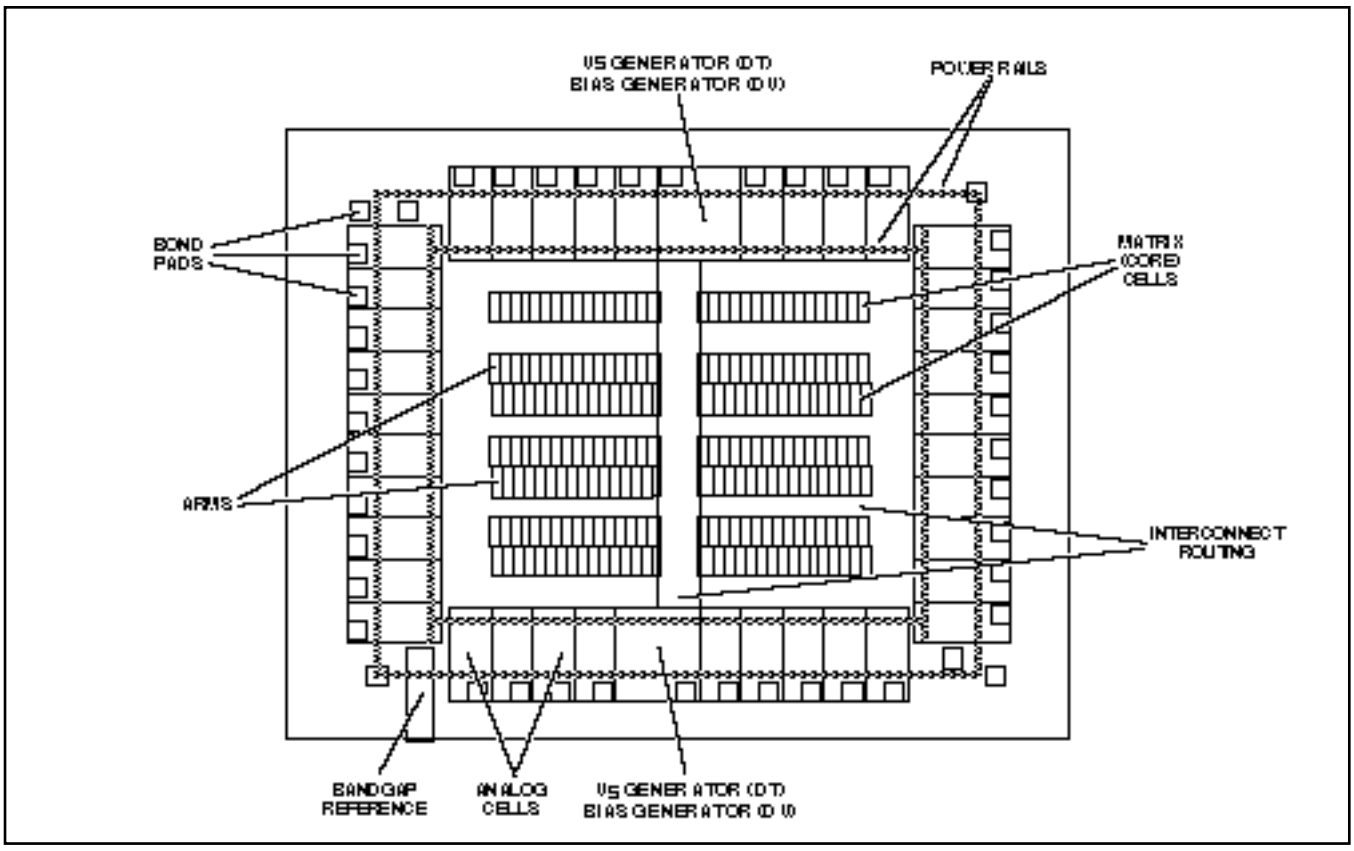

Fig. 2 Chip floorplan: symbolic representation

ANALOG CELLS

A most important aspect of the DT/DV series of mixed signal arrays is the range of circuit functions possible with the analog cells.

The high quality of the optimally matched components used in the cells, together with the comprehensive range of values, gives the DT/DV series the ability to implement high performance analog functions.

Each analog cell contains up to 43 transistors and 52 resistors, which can be interconnected to produce a wide variety of functions. Adjacent resistors in a cell are matched to within ±1% and similar transistors have matching V_{BE} values to within 300µV. These factors, together with the 6GHz f_T of the transistors, facilitate the high analog performance.

The analog cells also provide for the I/O buffering to interface to external circuitry and are therefore required to be robust and flexible. The inputs and outputs provide the designer with multiple interface options, can withstand electrostatic discharges and are not susceptible to latch-up (the process is inherently radiation-hard).

The cells can be configured to interface with all commonly used technologies such as TTL, CMOS and true ECL. The ready availability of TTL compatible outputs, with the associated source and sink currents and low $R_{CE\ (SAT)}$, means that high capacitive loads can be switched at speed without the need for additional buffering. Many of these functions are available as fully characterised macros.

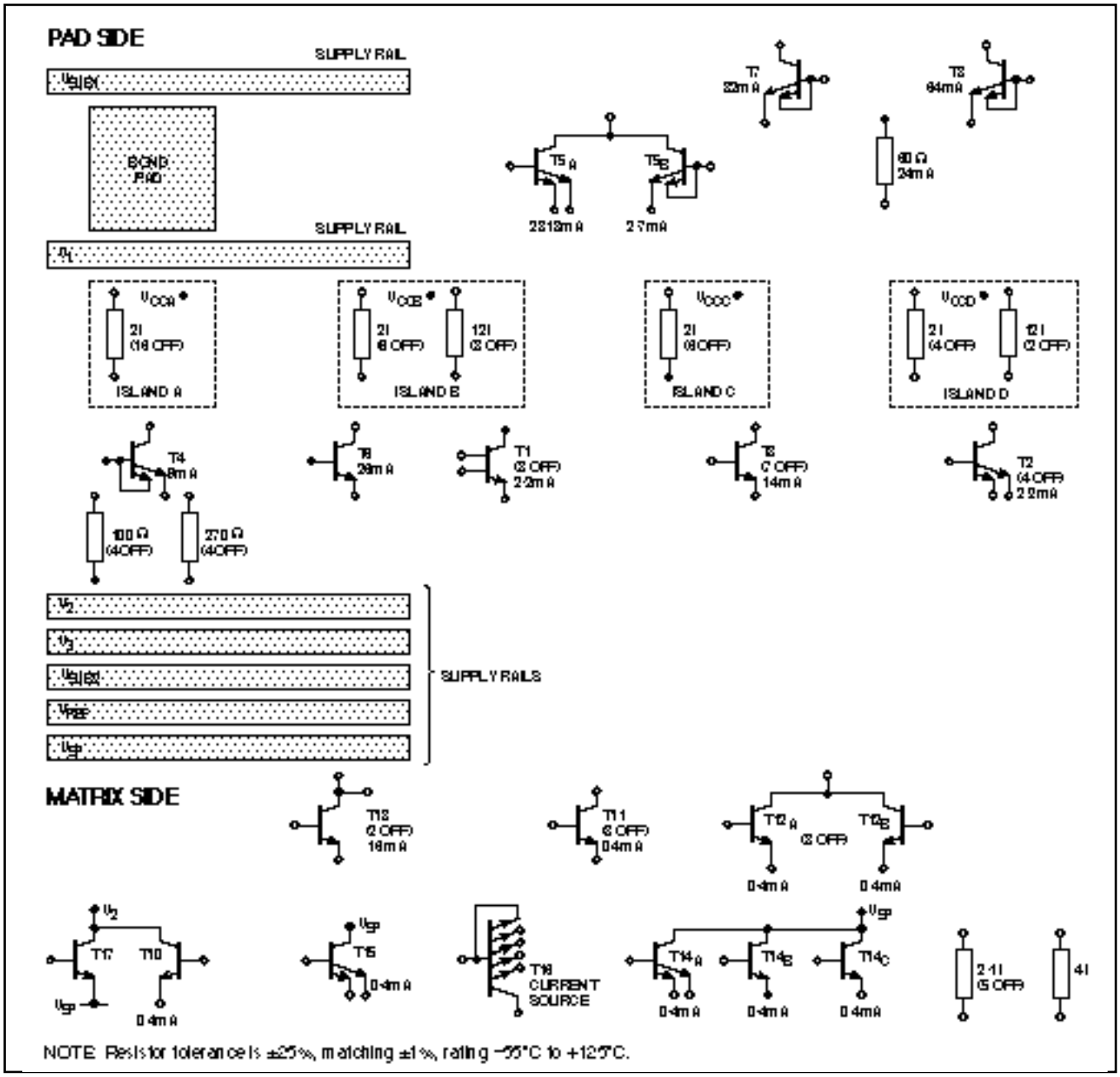

Fig. 3 DT series analog cell components

TYPICAL ANALOG PERFORMANCE CHARACTERISTICS

All parameters are for nominal V_{CC} = 5V at T_{AMB} = 25°C

Parameter	Component	Value	Units	Conditions
I_{CE}	T2	2·2	mA	
I_{CE}	T5	13·0	mA	
I_{CE}	T4	9·0	mA	
I_{CE}	T3	1·4	mA	
I_{CE}	T6	26·0	mA	
H_{FE} forward	T1	150		I_C = 100µA
H_{FE} inverse	T1	10		I_C = 100µA
V_{BE}	T1	0·775	V	I_C = 1mA
V_{BE} matching	T1	±300	µV	Between adjacent devices within one analog cell
f_T	T1	6000	MHz	I_C = 2mA
Resistor accuracy	All R	±25	%	
Resistor matching	R	±1	%	Adjacent resistors within one analog cell
Resistor voltage coefficient	R	1	%/V	

Table 2 Analog component characteristics

CORE CELLS FOR SYSTEM LOGIC

The core logic cell components can be configured into a range of logic gates and functions with differing complexities, functionality and speed/power attributes.

The core consists of rows of identical matrix cells, the rows being separated by routing channels for component or function interconnection. Power is distributed to each matrix cell by dedicated power rails between the rows of cells.

Each DT matrix cell is equivalent to two 2-input gates, comprising 8 transistors and 2 resistors. Gates with effective delays to below 0·5ns and 1·5ns clock to output flip-flops are features of the DT matrix capability. These delays are virtually independent of fan-out, supply voltage and clock frequency.

The DV series offers gates with effective delays to 200ps and flip-flops with clock to output delays of below 1ns.

Each matrix cell in the DT series can be connected to form two basic gate structures, NOR and RNOR and two special variants, PNOR and WNOR.

The basic low power NOR gate uses current mode logic (CML) and is used whenever propagation delay is not critical. Taking the NOR gate and adding an output buffer creates an RNOR gate using an identical number of matrix cells but giving significantly faster switching times. Moreover, the delay is virtually unaffected by output loading.

The PNOR gate has been designed to drive the very high fan-outs typically found on clock lines. Table 3a shows that even when driving 50 gates the delay is below 3ns.

Large wire-OR nets can be realised using WNOR gates to significantly reduce complexity and overall propagation delays.

Each cell in the DV series is designed for multi-level differential logic elements (to 3 levels). Differential logic automatically provides the true and inverse of every input and output, removing the need for inverters. The AND gate shown in Fig. 7 can become a NAND, OR or NOR simply by changing the input and output connections. The significance of eliminating inverters is that overall system speed can be increased for a given gate delay.

Matrix Performance

Table 3 refers to 2-input gates. Speed-up is achieved by the selective use of additional matrix cell components.

Within the DT/DV series of arrays there is a choice of speed/power options to suit the particular system requirements. the options available are shown in Table4.

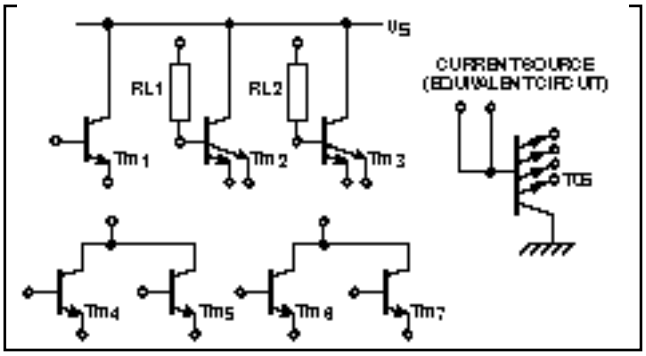

Fig. 4 DT core matrix cell content

Gate type	t_{PD} (ns)	I_G (µA) (average)	Comments
NOR	1·5	60	Fanout = 2
NOR	0·9	120	Speeded-up
RNOR	0·8	170	Buffered NOR gate, fanout = 2
RNOR	0·45	340	Speeded-up
PNOR	2·5	360	Fan out = 50
WNOR	3·5	120	Fan out = 20

Table 3 DTA gate performance

Series device type	Gate speed (ns)	
	Standard	Speeded-up
DT (emitter follower logic matrix)		
DTA option	0·8	0·45
DTB option	1·2	0·65
DTC option	2·4	1·35
Average gate I_{CC} at 1ns = 48µA at high speed		
DT (3-level differential logic matrix)		
DVA option	0·4	0·2
DVB option	1·0	0·5
Average gate I_{CC} at 200ps = 210µA at high speed		

Table 4 Speed/power options

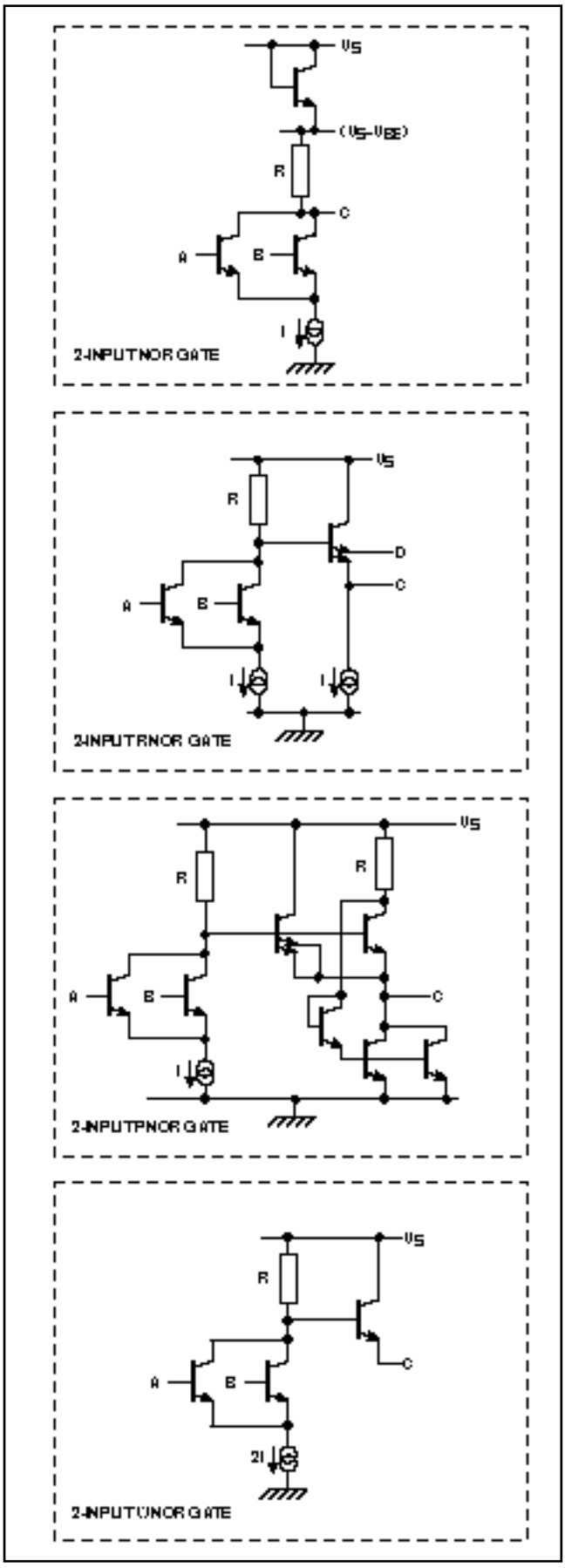

Fig. 5 DT logic gate schematic

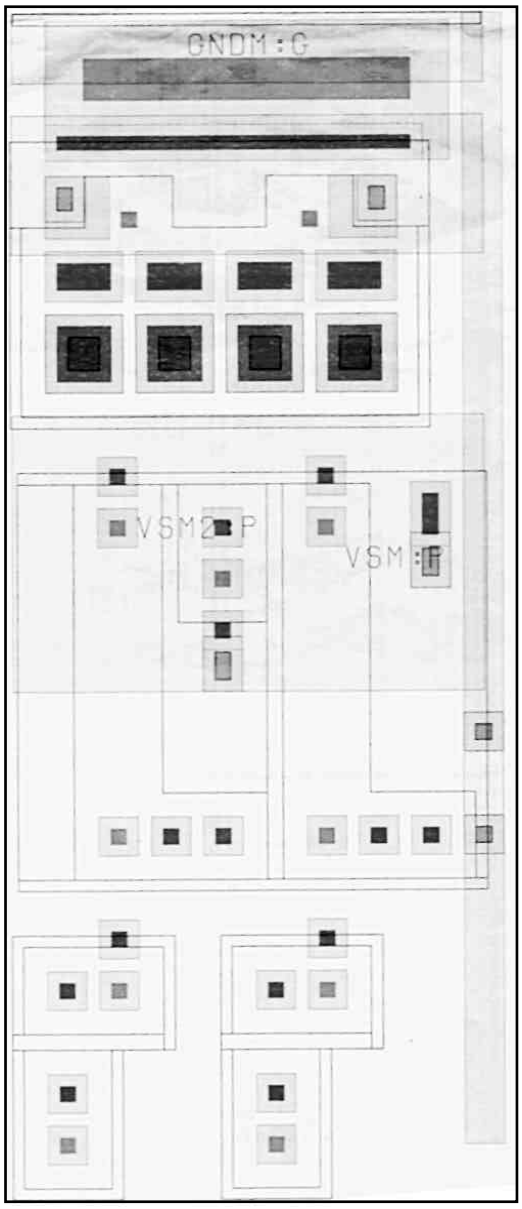

Fig. 6 DT matrix cell layout

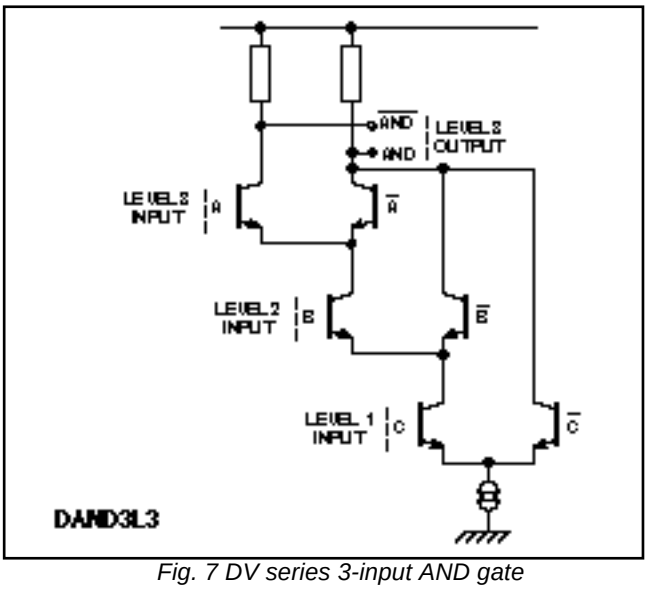

Fig. 7 DV series 3-input AND gate

DIFFERENTIAL LOGIC

'Differential logic' is a radical approach to logic function design. It can provide an order of magnitude improvement in speed-power product, ensuring that system power levels are kept to a minimum. It achieves a two to four times improvement in speed, with the added advantage that the standard D-type flip-flop clock to output delay is less than two equivalent gate delays.

Differential logic is based on steering current through a logic tree by means of differential pairs of transistors stacked across the supply. Many complex functions can be achieved using this technique. It eliminates the need to generate and distribute accurate temperature compensated voltage references.

A differential pair of transistors also has an extremely linear and sharp transfer characteristic, allowing the use of logic swings as low as 100mV, with excellent discrimination between logic levels.

Differential logic functions are configured from matrix components and offer sub-nanosecond equivalent delays at frugal power levels (see Table 5). Here, complete functions such as D-types are built up as ready-defined macros as shown in Fig. 8. As an illustration of the performance benefits, consider a 2-level D-type which offers a clock to output delay of 1·45ns. This performance is equivalent to a gate delay of 500ps and, moreover,the differential logic element consumes only one third the power of a conventional implementation using gates.

In asynchronous systems, the susceptibility to data errors is a major consideration. Data errors occur when latches are clocked at or near a change of input data state, which leads to 'metastability errors'. The differential logic macros include 'metastability hardened' elements offering improved data error rates for high speed asynchronous systems.

Differential Logic Performance

The figures given in Table 5 relate to a 2-level differential logic D-type with reset (Macro DF2DT1SRL1). The clock input and Q output are level 1, and the data input is on level 2, as shown in Fig. 8.

Parameter	Value
$t_{PD(0)}$ CLOCK to QL1	1·45ns
$t_{PD(1)}$ CLOCK to QL1	1·45ns
$t_{PD(0)}$ RESET to QL1	1·5ns
$t_{PD(1)}$ SET to QL1	1·5ns
$t_{SET\ UP(0)}$ Data input	0·9ns
$t_{SET\ UP(1)}$ Data input	0·9ns
$t_{HOLD(0)}$ Data input	0ns
$t_{HOLD(1)}$ Data input	0ns
I_G (average)	540µA

Table 5 Differential logic performance

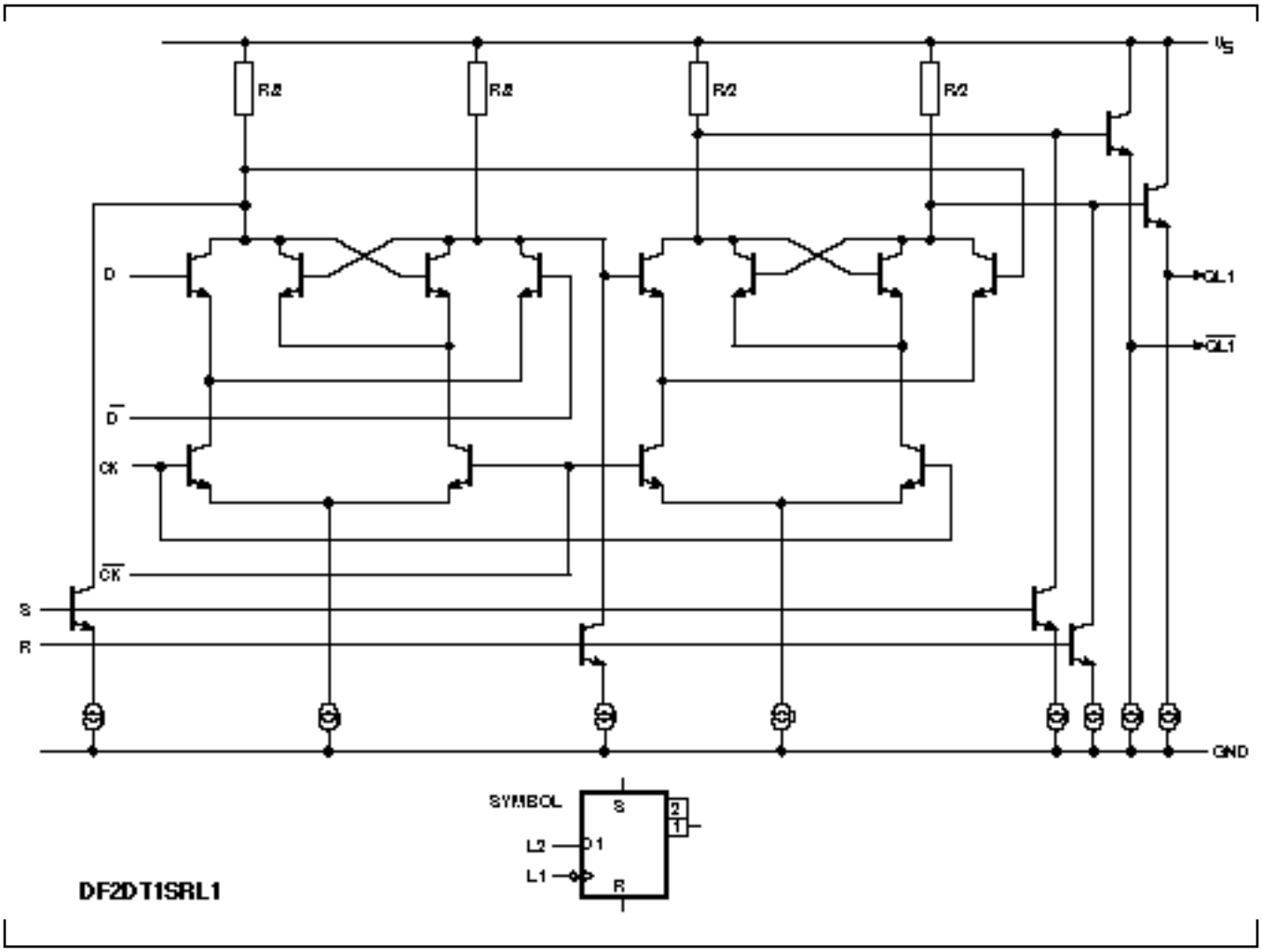

Fig. 8 Schematic of DT series differential logic D-type flip-flop (2-level)

CHARACTERISTICS

All DT/DV series ULAs are designed to operate with supplies of 0V to 5V or ±5V (true ECL) and over the full temperature range of −55°C to +125°C , therefore embracing all the various military, industrial and commercial temperature ranges.

ABSOLUTE MAXIMUM RATINGS

Operation at Absolute Maximum Ratings is not implied. Exposure to stresses greature than those listed may affect reliability and could cause permanent damage to the device.

Supply voltage V_{CC}	−0.5V to +7.0V
Input voltage V_{IN} (at V_{CC} = 5V)	−0.5V to +5.5V
Operating temperature range T_{AMB}	−55°C to +125°C
Storage temperature range T_{STG}	−65°C to +150°C

DC CHARACTERISTICS

All parameters are for nominal V_{CC} = 5V and V_{EE} = −5V (where applicable) over the temperature range. T_{AMB} = 0°C to +70°C unless otherwise specified.

Characteristic	Macro type	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage, V_{CC}		4·75	5·0	5·25	V	Commercial/industrial
		4·5	5·0	5·5	V	Military
High level input voltage, V_{IH}	DT/DV2 & 502	2·0		5·5	V	High performance TTL input buffer
	DT/DV6		4·1		V	ECL input
	DT/DV506		−0·9		V	ECL input
Low level input voltage, V_{IL}	DT/DV2 & 502	0		0·8	V	High performance TTL input buffer
	DT/DV6		3·3		V	ECL input
	DT/DV506		−1·7		V	ECL input
High level input current, I_{IH}	DT/DV2 & 502	0		20	µA	High performance TTL input buffer (V_{IH}=V_{CC})
	DT/DV6		40		µA	ECL input (V_{IH} = V_{CC})
	DT/DV506		40		µA	ECL input (V_{IH} = 0V)
Low level input current, I_{IL}	DT/DV2 & 502			−0·4	mA	High performance TTL input buffer (V_{IL}=0·8V)
	DT/DV6 & 506		20		µA	ECL input
High level output voltage, V_{OH}	DT/DV31 & 531	2·4			V	Totem pole output (I_O = I_{OH} max.)
	DT/DV32 & 532	2·4	3·4		V	Tristate output (I_O = I_{OH} max.)
	DT/DV51		V_{CC}−1·0		V	ECL output (I_O = I_{OH} max.)
	DT/DV551		−1·0		V	ECL output (I_O = I_{OH} max.)
Low level output voltage, V_{OL}	DT/DV31 & 531			0·5	V	Totem pole output (I_O = I_{OL} max.)
	DT/DV32 & 532			0·5	V	Tristate output (I_O = I_{OL} max.)
	DT/DV51		V_{CC}−1·8		V	ECL output (I_O = I_{OL} max.)
	DT/DV551		−1·8		V	ECL output (I_O = I_{OL} max.)
High level output current, I_{OH}	DT/DV31 & 531			−400	µA	Totem pole output
	DT/DV32 & 532			−400	µA	Tristate output at V_{OH} min.
Low level output current, I_{OL}	DT/DV31 & 531			8	mA	Totem pole output (V_{OL} = 0·5V)
	DT/DV32 & 532			8	mA	Tristate output (V_{OL} = 0·5V)
	DT/DV38 & 538			8	mA	Open collector (V_{OL} = 0·5V)
	DT/DV46			64	mA	Tristate output (V_{OL} = 0·5V)
Output leakage current, I_{OZ}	DT/DV32 & 532			±10	µA	Tristate
	DT/DV38 & 538			10	µA	Open collector (V_{OH} = V_{CC})

AC CHARACTERISTICS

The DT/DV process LG2 technology library contains all the timing information for each cell in the design library. This information is accessible to the simulator, which calculates propagation delays for all signal paths in the circuit design. The EDA simulator can automatically derate timings according to various factors, such as:

Supply voltage variation (from 5V)
Chip temperature
Processing tolerance
Gate fan-out
Input transition time
Input signal polarity
Interconnection wiring

For initial assessments of feasibility, worst case estimations can be done in the following manner, at 25°C and 5V nominal. Similar calculations may be applied for any voltage and temperature relevant to the application. An additional safety factor of ±5% may be applied for conservative design.

- For temperature, a derating multiplier, K_T, of 0·3% per °C should be used.
- For supply voltage derating a factor, K_V, of −20% per volt should be used (this also includes capacitance, f_T and logic changes).
- For manufacturing variation, K_P, the tolerance is ±25%

The maximum variation on typical delays over the commercial grade product at 4·75V and T_{AMB} = +70°C (assuming a junction temperature of +90°C) will be:

$$t_{PD\ (max.)} = K_P \times K_V \times K_T \times t_{PD\ (typ.)}$$
$$= 1{\cdot}25 \times [1 + (5{\cdot}0 - 4{\cdot}75)0{\cdot}20] \times [1 + (90 - 25)0{\cdot}003] \times t_{PD}$$
$$= 1{\cdot}25 \times (1 + 0{\cdot}05) \times (1 + 0{\cdot}195) \times t_{PD\ (typ.)}$$
$$= 1{\cdot}25 \times (1{\cdot}05) \times (1{\cdot}195) \times t_{PD\ (typ.)}$$
$$= 1{\cdot}57 \times t_{PD\ (typ.)}$$

By similar calculation, the minimum delay, $t_{PD\ (min.)}$, at 5·25V and 0°C will be:

$$t_{PD\ (min.)} = 0{\cdot}65 \times 0{\cdot}95 \times 0{\cdot}92 \times t_{PD\ (typ.)}$$
$$= 0{\cdot}56 \times t_{PD\ (typ.)}$$

DESIGN SUPPORT AND INTERFACES

The Electronic Design Automation (EDA) Environment

GPS has built its ASIC design environment around Cadence's Analog Artist Design System, a leading analog EDA system for analog and mixed signal ICs. This analog design system, along with a GPS proprietary automatic place and routing software are integrated within the Cadence Design Framework architecture. It was developed in parallel with the latest ULA family to ensure complete compatibility between the design environment and the chip hardware.

Design Entry

Mixed signal designs can be described in a behavioural format using analog and digital hardware description languages or captured schematically at the component and macro level.

Circuit stimuli can be entered in behavioural formats or by conventional logic truth tables and from this, mixed signal test vectors can be generated.

This type of option provides versatile design entry which allows the designer the flexibility on design entry.

Design Interface

DT/DV series designs can be carried out either by GPS or the customer, using one of a number of customer entry levels, such as:

- The customer produces a verified breadboard and test schedule and GPS performs a turnkey design from this stage through to samples.
- The customer designs on her/his workstation using standard Design Elements and carries out functional and timing simulation.
- The customer designs using GPS Design Elements in a compatible Design Environment.

DESIGN ENVIRONMENT (See Fig. 9)

Electrical Rule Check

Electrical rule check ensures validity of the captured design by checking fan-in and fan-out and that the design technology rules are not violated.

Simulation

Component level simulation for analog and high performance circuits is performed with Cadence SPICE or Spectre – an advanced circuit simulator which provides extemely fast and accurate simulation for circuits with over 50,000 transistors. Logic simulation is undertaken with Verilog-XL using models from a proven logic macro library. Fault grading is available with Verifault.

Mixed mode simulation is used on designs containing analog and digital circuits. Verilog-XL and Cadence SPICE/ Spectre run concurrently to model the circuit. A mixture of behavioural, gate level and component level models can be used to realise the optimum run time and accuracy required.

Through the facilities of Dantes or TSSI, the simulation vectors can be edited and reviewed, then automatically translated into formats suitable for production test machines.

PHYSICAL ENVIRONMENT

Layout

The layout tools enable physical design of the entire mixed signal chip or customised analog cell to be constructed in several formats. Semi-Custom Arrays, Structured Arrays, Standard Cell and Full Custom. The Structured Arrays accomodate a mixture of formats, allowing Semi-Custom Arrays, Standard and Full Custom cells to be integrated on one chip.

Automatic place and routing of logic gates is performed using GPS proprietary tools. These tools allow for parameterised cells to be used to customise the delay paths within specific areas of the digital design, thereby giving the added flexibility in the speed/power option of logic functions within an ASIC design.

Track Load Extraction

Track load extraction maps the actual circuit layout onto the design database. This allows representative physical simulations to be implemented and the final circuit performance assessed.

Layout Verification and Design Rule Check

When the layout is complete it can be verified and checked against design rules using LVS and DRC decks to ensure precise 1:1 mapping of the circuit onto silicon.

Mask manufacture and wafer fabrication can then be undertaken.

DESIGN REVIEWS

Design reviews are an integral part of the support provided by GEC Plessey Semiconductors during the development of a Semi-Custom integrated circuit. These reviews are scheduled meetings between the customer's representative and the allocated project engineer. They ensure that all the correct design procedures have been observed to date and that the procedures and requirements for the next phase are fully understood.

A total of four design reviews are held prior to full production. These reviews are:

- **Design Review 1** – Initial concept and system specification.
- **Design Review 2** –On completion of design and simulation.
- **Design Review 3** – On completion of layout and post-layout simulation.
- **Design Review 4** – On supply of prototypes prior to approval for full production.

At the end of the design and layout phase and when Design Review 3 has been completed, GPS manufactures prototypes. The test program is generated as part of the design process and is used to test the prototypes. This program is extended, on approval of prototypes, for finished production product.

Spectre, Verilog-XL, Verifault and Dantes are trademarks of Cadence Design Sysyems Inc.

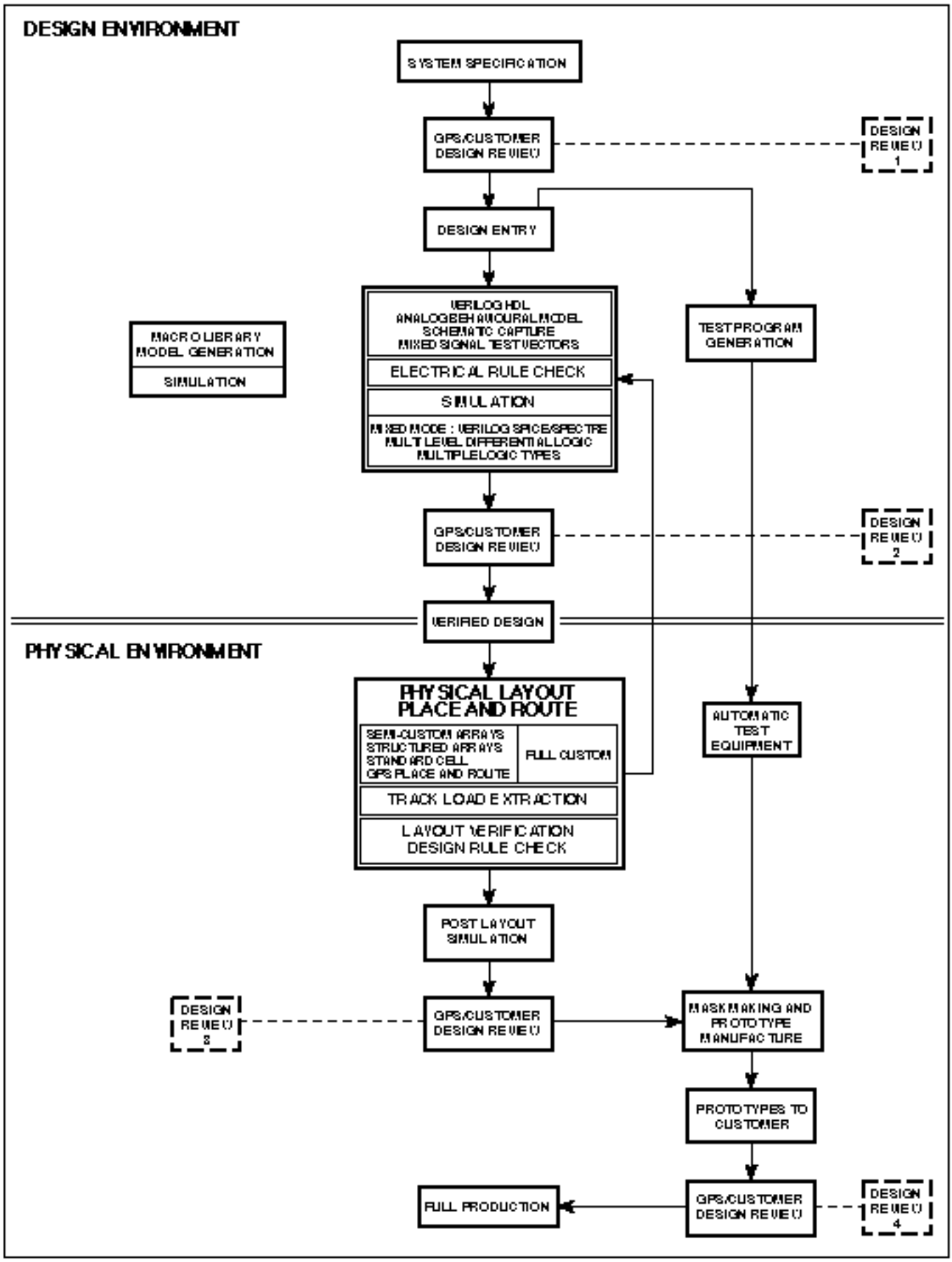

Fig. 9 The DT/DV series design route

SPECIAL ANALOG FUNCTIONS

Each DT/DV series array features a programmable bandgap reference and high current transistors as detailed in Table 6.

Parameter	Value	Units	Conditions
Bangap			
Voltage range (buffered output)	1·3-2·6	V	Mask programmed
Output voltage temperature coefficient	±100	ppm	V_{OUT} = 1·32V
High current transistors (on each peripheral cell)			
I_{OL} (32mA + 32mA + 32mA)	96	mA	V_{OUT} = 0·5V

Table 6 Special analog functions

Function	Number of peripheral cells	Number of pins
Amplifier	2	2
Comparator	2	2
Video amplifier	3	4
AGC amplifier	5	5
Zero crossing comparator	2	2
Hysteresis comparator (Schmitt trigger)	3	1
Precision monostable	2	2
VCO with fast lock	4	4

Table 7 Analog macro examples

SPECIAL FUNCTION MACRO LIBRARY

The list of circuits includes examples of the immense variety of circuit configurations that are possible and that have been produced as macros on DT/DV arrays. Examples of the analog capabilities are given in Table 7.

The special function library is being continually enlarged with many of the macros designed to solve the problems met in specific market sectors such as computer peripherals.

Some examples of macros and their performance characteristics, used and available from DT/DV integrations, can be seen in Fig. 10. Full details of all macros available, as listed in the cell library on the following pages, can be found in the DT/DV Design Manual and the DT/DV Macro Library documents.

The analog performance attainable by the DT/DV series is illustrated by an AGC amplifier from the macro library, shown in Fig. 10. The specification for this amplifier is given in Table 8.

Parameter	Value	Units
Differential input resistance	5·6	kΩ
Differential input bias current	5	µA
Differential input voltage range	30-400	mV
Max. Gain	80	V/V
Gain control range (min.)	18	dB
Gain controlactive voltage range	2·3-3·3	V
Gain input current	2	µA
3dB bandwidth	50	MHz
Max. output differential voltage swing	4	V
Output sink current	3	mA
Output resistance (max.)	20	Ω
Reference voltage V_{ACRF}	2·3-2·7	V

Table 8 AGC amplifier performance

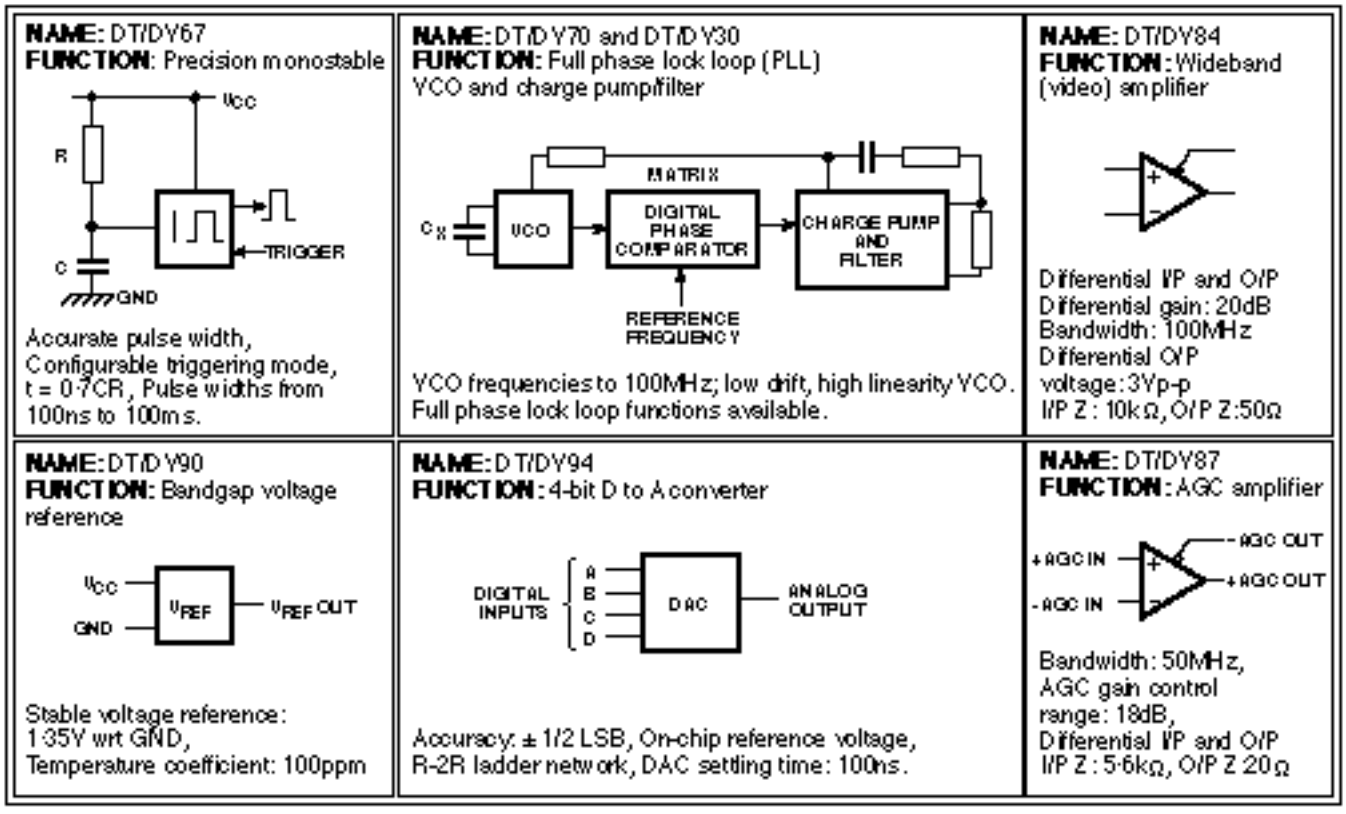

Fig. 10 Examples of DT/DV macro functions used in integrations

CELL LIBRARY

A most comprehensive cell library is available for the DT/DV series. The implementation of a cell has involved the silicon planning, design rule checking, automatic generation of a SPICE file for performance analysis, SPICE simulation and results extraction, generation of the EDA cell simulator and verification of the cell attributes for layout tools.

Analog and I/O Macros

The DT/DV series has been designed to give outstanding analog performance. The Analog Macro Library encompasses a comprehensive range of analog and I/O functions. These provide a rapid, proven and fully characterised solution to a wide range of circuit requirements. The library is constantly being expanded to include more functions.

Moreover, a new design can be readily created when the exact circuit function does not already exist in library or it is required to optimise the performance of an existing macro.

This can be completed by either GEC Plessey Semiconductors or the customer and proven using the comprehensive SPICE parameters available for the DT/DV series.

Input & Output Interface Function Macro Library

These macros provide interfacing to TTL, CMOS and true ECL technologies together with functions such as Schmitt trigger inputs. Also included within the library are macro variations such as ECL inputs with internal voltage reference levels or macros for use with an external source.

The 500 series macros are for use with ±5V supplies.

ANALOG MACRO LIBRARY

Monostables

DT/DV66	Simple RC monostable
DT/DV67	Precision RC monostable
DT/DV72	Voltage controlled monostable
DT/DV73	Narrow pulse monostable

Oscillators

DT/DV65	Simple RC oscillator
DT/DV68	Crystal oscillator
DT/DV69	Overtone crystal oscillator
DT/DV70	Voltage controlled oscillator
DT/DV71	Switched voltage controlled oscillator
DT/DV74	Precision RC oscillator

Comparators

DT/DV80	Fast voltage comparator
DT/DV81	Low power voltage comparator
DT/DV82	Low offset voltage comparator
DT/DV83	High impedance voltage comparator

Amplifiers

DT/DV84	Video amplifier
DT/DV85	Audio amplifier
DT/DV86	Filter amplifier
DT/DV87	AGC amplifier

References

DT/DV90	1·3V voltage reference
DT/DV91	2·6V voltage reference

Miscellaneous

DT/DV93	Differentiator
DT/DV94	4-bit D to A converter
DT/DV95	Fast flip-flop

I/O MACRO LIBRARY

Inputs

DT/DV2 & 502	TTL input
DT/DV4 & 504	Low power TTL input
DT/DV5 & 505	ECL input plus bias generator
DT/DV6 & 506	ECL input
DT/DV7	High impedance TTL input
DT/DV8 & 508	Differential ECL input
DT/DV10	Three state input
DT/DV62	Precision Schmitt trigger input
DT/DV63 & 563	Schmitt trigger input

Outputs

DT/DV30	Charge pump output
DT/DV31 & 531	TTL output
DT/DV32 & 532	Tristate output
DT/DV35 & 535	Low power TTL output
DT/DV37 & 537	Low power tristate output
DT/DV38 & 538	Open collector output
DT/DV39	Low power open collector output
DT/DV40 & 540	Open collector output with pull up
DT/DV41	Low power open collector O/P with pull up
DT/DV43	Open emitter output
DT/DV44	96mA open collector output
DT/DV45	32mA open collector output
DT/DV46	64mA tristate output
DT/DV47	32mA tristate output
DT/DV51 & 551	ECL output
DT/DV52 & 552	Differential ECL output

Input/Output

DT/DV33 & 533	Tristate output/TTL input
DT/DV34	Low power tristate output/low power TTL I/P
DT/DV36	Open collector output/TTL input

DT SERIES LOGIC CELL LIBRARY

The DT logic cell library contains a listing of all the types of Logic Design Elements available for the DT arrays. These are divided into four groups:

- **Logic Gates** – Basic logic primitives such as NOR gates, RNOR gates etc.
- **Logic Functions** – Flip-flops, Latches etc.
- **Differential Logic Elements** – High speed, low power logic gatesand functions.
- **Logic Macros** – Counters, adders, registers, decoders etc.

In this brief listing, only the minimum group of letters required to indicate the generic type of each element is given, with a number of examples to show how each element name is built up. For example, for the family of single input RNOR D-type the generic name is given as DT1. A full D-type flip-flop, that is, one with SET, RESET, Q output and $\overline{Q}$ output, is invoked by the name DT1SRQN. Any unwanted terminals are omitted from the name.

Logic Gates

1 to 8-input primitive gates.

NOR1	RNOR1	PNOR1
NOR2	RNOR2	PNOR2
NOR3	RNOR3	PNOR3
NOR4	RNOR4	PNOR4
NOR5	RNOR5	
NOR6	RNOR6	
NOR7	RNOR7	
NOR8	RNOR8	
WNOR1	FPNOR1	FWNOR1
WNOR2	FPNOR2	FWNOR2
	FPNOR3	FWNOR3
	FPNOR4	FWNOR4

DT SERIES LOGIC CELL LIBRARY (Continued)

Logic Functions

These are further divided into two groups of NOR and RNOR.

(a) NOR logic functions

The prefix 'C' indicates CML

CDT1	1-input D-type flip-flop
CDT2	2-input D-type flip-flop
CDT3	3-input D-type flip-flop
CDT4	4-input D-type flip-flop
CDST1	Special D-type flip-flop
CTT1	T-type flip-flop
CDL1	Level triggered data latch
CEQV	Equivalence gate
CEXOR	Exclusive OR gate
CNMONO	Negative edge triggered narrow pulse monostable
CPMONO	Positive edge triggered narrow pulse monostable

(b) RNOR logic functions

DT1	1-input D-type flip-flop
DT2	2-input D-type flip-flop
DT3	3-input D-type flip-flop
DT4	4-input D-type flip-flop
DST1	Special D-type flip-flop
DTA1	Alternative reset D-type flip-flop
TT1	T-type flip-flop
DL1	Level triggered data latch
REQV	Equivalence gate
REXOR	Exclusive-OR gate
NMONO	Negative edge triggered narrow pulse monostable
PMONO	Positive edge triggered narrow pulse monostable

Differential Logic Elements (2-Level)

DF2L1	CML to DCML, level 1 output
DF2L2	CML to DCML, level 2 output
DF2L12	CML to DCML, level 1 and 2 output
DF2ANDL1	2-input AND gate, level 1 output
DF2ANDL2	2-input AND gate, level 2 output
DF2ANDL12	2-input AND gate, level 1 and 2 output
DF2DL1L1	Data latch, level 1 output
DF2DL1L2	Data latch, level 2 output
DF2DL1L12	Data latch, level 1 and 2 output
DF2DT1L1	D-type flip-flop, level 1 output
DF2DT1L2	D-type flip-flop, level 2 output
DF2DT1L12	D-type flip-flop, level 1 and 2 output
DF2DT1RL1	D-type flip-flop with Reset, level 1 output
DF2DT1RL2	D-type flip-flop with Reset, level 2 output
DF2DT1RL12	D-type flip-flop with Reset, level 1 and 2 output
DF2DT1SRL1	D-type flip-flop with Set/Reset, level 1 output
DF2DT1SRL2	D-type flip-flop with Set/Reset, level 2 output
DF2DT1SRL12	D-type flip-flop with Set/Reset, level 1 and 2 output
DF2EXORL1	Exclusive-OR gate, level 1 output
DF2EXORL2	Exclusive-OR gate, level 2 output
DF2EXORL12	Exclusive-OR gate, level 1 and 2 output
DF2CMLT	DCML to CML, True output
DF2CMLW	DCML to CML, Wire-OR output
DF2CMLTW	DCML to CML, True and Wire-OR output
DF2SELL1	2-1 Selector, level 1 output
DF2SELL2	2-1 Selector, level 2 output
DF2SELL12	2-1 Selector, level 1 and 2 output
DF2DTS1RL1	Special D-type flip-flop, level 1 output
DF2DTS1RL2	Special D-type flip-flop, level 2 output
DF2DTS1RL12	Special D-type flip-flop, level 1 and 2 output
DF2LRL2	Level 1 to level 2
DF2DELL1	Delay, level 1 output
DF2DELL2	Delay, level 2 output
DF2LSL1	Level 2 to level 1
DF2DL1RL1	Data latch with Reset, level 1 output
DF2DL1RL2	Data latch with Reset, level 2 output
DF2DL1RL12	Data latch with Reset, level 1 and 2 output
DF2MDL1L2	Metastable resistant Latch, level 2 output
DF2MDL1RL2	Metastable resistant Latch with Reset, level 2 output
DF2ANDCML	2-input AND gate, CML output
DF2DL1CML	Data Latch, CML output
DF2DL1RCML	Data Latch with Reset, CML output
DF2DT1CML	D-type flip-flop, CML output
DF2DT1RCML	D-type flip-flop with Reset, CML output
DF2DT1SRCML	D-type flip-flop with Set/Reset, CML output
DF2DTS1RCML	Special D-type flip-flop, CML output
DF2EXORCML	Exclusive-OR gate, CML output
DF2SELCML	2-1Selector, CML output
DF2DELPER	Delay, level 2 output to peripheral
DF2ANDPER	2-input AND gate, level 2 output to peripheral
DF2DL1PER	Data Latch, level 2 output to peripheral
DF2DL1RPER	Data Latch with Reset, level 2 output to peripheral
DF2DT1PER	D-type flip-flop, level 2 output to peripheral
DF2DT1RPER	D-type flip-flop with Reset, level 2 output to peripheral
DF2DT1SRPER	D-type flip-flop with Set/Reset, level 2 output to peripheral
DF2DTS1RPER	Special D-type flip-flop, level 2 output to peripheral
DF2EXORPER	Exclusive-OR gate, level 2 output to peripheral
DF2SELPER	2-1Selector, level 2 output to peripheral
DF2LRPER	Level 1 to level 2 peripheral
DF2L2PER	CML to level 2 peripheral

Logic Macro Functions

The Logic Macro Function Library comprises a set of commonly used logic functions which can be used in conjunction with all other Logic Design elements or Logic Cells.

The same notation is used here as with the Logic Function Library in that each example is of the full element complete with SET and RESET where applicable. Functions which are available in both NOR and RNOR logic are prefixed (C).

(a) Gates

NAND2	2-input NAND gate
NAND3	3-input NAND gate
NAND4	4-input NAND gate
(C)OA22	2-input, 2-wide OR-NAND
(C)OA23	2-input, 3-wide OR-NAND
(C)OA24	2-input, 4-wide OR-NAND
(C)OA32	3-input, 2-wide OR-NAND
OA33	3-input, 3-wide OR-NAND
(C)OA34	3-input, 4-wide OR-NAND
(C)OA232	3, 3-input, 2-wide OR-NAND

(b) Flip-flops

(C)SR	S-R flip-flop
WDT	D-type flip-flop with wired-OR outputs, e.g. WDTSR
(C)MDT	D-type flip-flop with multiplexed data input, e.g. (C)MDTSR
(C)JK	J-K flip-flop, e.g. (C)JKSR
(C)JNK	JNK flip-flop, e.g. (C)JNKSR
(C)TE	Toggle enable D-type flip-flop, e.g. (C)TESR

(c) Multiplexers

(C)MPX2	2- to 1-line multiplexer
(C)MPX4	4- to 1-line multiplexer
(C)MPX8	8- to 1-line multiplexer
(C)MPX16	16- to 1-line multiplexer

(d) Data selectors

(C)DSL2	1- to 2-line data selector
(C)DSL4	1- to 4-line data selector
(C)DSL8	1- to 8-line data selector
(C)DSL16	1- to 16-line data selector

(e) Decoders

(C)DEC4	2- to 4-line decoder
(C)DEC8	3- to 8-line decoder
(C)DEC16	4- to 16-line decoder

(f) Comparators

(C)EQCOM4	4-bit equality comparator
(C)MCOM4	4-bit magnitude comparator

(g) Adders

(C)HA	Half adder
(C)GFA	Gated full adder

(h) Registers

(C)DR4	4-bit clocked data register, e.g. (C)DR4R
(C)DR6	6-bit clocked data register, e.g. (C)DR6R
(C)DR8	8-bit clocked data register, e.g. (C)DR8R
(C)TDL4	4-bit transparent data latch, e.g. (C)TDL4R
(C)TDL6	6-bit transparent data latch, e.g. (C)TDL6R
(C)TDL8	8-bit transparent data latch, e.g. (C)TDL8R

(i) Counters

(C)A4BRC	4-bit ripple counter, e.g. (C)A4BRC
(C)A6BRC	6-bit ripple counter, e.g. (C)A6BRC
(C)A8BRC	8-bit ripple counter, e.g. (C)A8BRC
(C)SD3C	Synchronous ÷ 3 counter, e.g. (C)SD3CR
(C)SD5C	Synchronous ÷ 5counter, e.g. (C)SD5CR
(C)AD6C	Asynchronous ÷ 6counter, e.g. (C)AD6CR
(C)AD7C	Asynchronous ÷ 7counter, e.g. (C)AD7CR

(j) Synchronous binary counters

(C)SBUC4	4-bit binary up counter, e.g. (C)SBUC4R
(C)SBDC4	4-bit binary down counter, e.g. (C)SBDC4R
(C)SBUDC4	4-bit binary up/down counter, e.g. (C)SBUDC4R
(C)SPBUC4	Presettable binary up counter
(C)SPBUC4RC	Presettable binary up counter with carry-out & reset
(C)SPBDC4	Presettable binary down counter
(C)SPBDC4SC	Presettable binary down counter with carry-out and set

(j) Synchronous decade counters

(C)SDUC4	4-bit decade up counter, e.g. (C)SDUC4R
(C)SDDC4	4-bit decade down counter, e.g. (C)SDDC4R
(C)SDUDC4	4-bit decade up/down counter, e.g. (C)SDUDC4R
(C)SPDUC4	Presettable decade up counter
(C)SPDUC4RC	Presettable decade up counter with carry-out & reset
(C)SPDDC4	Presettable decade down counter
(C)SPDDC4SC	Presettable decade down counter with carry-out& set

(k) Shift registers

(C)PISO	4-bit synchronous PISO, e.g. (C)PISOR

DV SERIES LOGIC CELL LIBRARY

The DV logic cell library contains a listing of the multi-level (3-level) Differential Logic Design Element Primitives which have been designed, captured and characterised for use in DV array designs.

Differential logic is explained briefly on page 6; it is an extension of ECL that seeks to maintain or improve on the advantages of ECL while eliminating some of the disadvantages. The basic gate is still based on the long-tailed pair and the steering of current to one of two complementary outputs and thus dispenses with the need for a voltage reference.

The use of complementary outputs dramatically increases noise immunity because any noise is experienced as a common-mode signal and is therefore rejected by the gate. This allows very low swings to be used (close to the theoretical limit of 100mV) while simultaneously achieving high noise immunity, higher speed (for the same gate current and process). Common-mode operation also gives excellent immunity to drops in the supply distribution system, crosstalk and temperature variations, while the sharp transfer characteristic of the differential pair gives excellent resistance to metastability.

Differential logic, like ECL, can be stacked to give many levels of switching in a tree structure. The large number of possible paths for the gate current to reach the output (all determined by logical states) means that very high complexity can be built into a single gate. This is limited by the available supply rail and the need for level shifters to interface signals.

A 3-level system has been chosen as the best compromise for this library. For most libraries the primitive logic function is a multi-input NAND or NOR gate, whereas a single gate using differential logic can be as complex as a 4:1 multiplexer or a transparent latch with reset. Many other examples of high functionality can be seen in this library.

A standard cell methodology was deliberately adopted to simultaneously maximise performance and minimise the area penalties for differential logic. A large library has been developed in order to offer maximum flexibility to the designer, thus minimising the task of physical implementation and easing the problems of using a new logic family.

Every module has been carefully optimised to minimise both area and critical-path delays. These two factors guarantee the designer maximum performance and allow her/him to adopt a high level design approach in the safe knowledge that system performance will not be compromised.

DV PRIMITIVES

Group 1. Functions with Outputs on Level 3 (Top Level) Only – Suffix L3

DBUF3L3	Level 3 buffer
DEOR22L3	2-input EXCLUSIVE-OR gate
DTTREL3	T-type flip-flop with reset and toggle enable
DLR1L3	Level regenerator 1
DEOR3L3	3-input EXCLUSIVE-OR gate
DDTSPL3	4-bit scan path register
DLR2L3	Level regenerator 2
DAOR31L3	3-input AND-OR gate 1
DEQG1L3	3-input 2-bit EQUALITY gate (with CASCADE input)
DAND2L3	2-input AND gate
DGT1L3	1-bit GREATER THAN element (with CASCADE input)
DOR2L3	2-input OR gate
DAORS5L3	5-input AND-OR select gate
DTTL3	T-type flip-flop
DAOR32L3	3-input AND-OR gate
DOR22L3	2-input OR gate 2
DOROS5L3	5-input OR-OR select gate
DFLADD1L3	1-bit full adder element
DOR3L3	3-input OR gate
DEQGL3	3-input 2-bit EQUALITY gate (with CASCADE input)
DLTCHL3	Transparent data latch
DOR4L3	4-input OR gate 1
D4TO1MLXL3	4 to 1 multiplexer
DDCDR3L3	3 to 8 decoder
DAND22L3	2-input AND gate 2
DXAND3L3	3-input EXCLUSIVE-OR-AND gate
DTCZ1L3	1-bit true/complement zero/one element
DAND3L3	3-input AND gate
DOAND31L3	3-input OR-AND gate 1
DCARRY1L3	1-bit (cascade) carry generator
DOAND31L3	3-input OR-AND gate 2
DHFADD1L3	1-bit half adder element
DAND42L3	4-input AND gate 2
DAORS3L3	3-input AND-OR select gate
DREFL3	Fixed level reference
DAND5L3	5-input AND gate
DAORS31L3	3-input AND-OR select gate
D2TO1MXLL3	2 to 1 multiplexer
DOR42L3	4-input OR gate 2
DLTCHRL3	Transparent latch with reset
DDCDR2L3	2 to 4 decoder
DAND4L3	4-input AND gate
DOR5L3	5-input OR gate
DDTL3	D-type flip-flop
DOEOR3L3	3-input OR-EXOR gate
DJKL3	*J-K type flip-flop*
DDTRL3	D-type flip-flop with reset
D1TO2DMXL3	1 to 2 demultiplexer
DJKRL3	J-K type flip-flop with reset
DTTEL3	T-type flip-flop with toggle enable
DEOR2L3	2-input EXCLUSIVE-OR gate
DTTRL3	T-type flip-flop with reset
D1TO4DMXL3	1 to 4 demultiplexer

DV PRIMITIVES (Continued)

Group 2. Functions with Outputs on Level 2 (Middle Level) Only – Suffix L2

DOAND22L2	2-input OR-AND gate 2
DOAND31L2	3-input OR-AND gate 1
DLTCHL2	Transparent data latch
DAOR31L2	3-input AND-OR gate 1
DOR22L2	2-input OR gate 2
DPWRDR42L2	Level 2 input power driver
DEOR22L2	2-input EXCLUSIVE-OR gate 2
D1TO2DMXL2	1 to 2 demultiplexer
DJKRL2	J-K type flip-flop with reset
DBUF2L2	Level 2 buffer
DOR5L2	5-input OR gate
D2TO1MXLL2	2 to 1 multiplexer
DOR4L2	4-input OR gate
DDTL2	D-type flip-flop
DTCZ1L2	1-bit true/complement zero/one element
DAND5L2	5-input AND gate
DAORS5L2	5-input AND-OR select gate
DAND4L2	4-input AND gate
DOEOR3L2	3-input OR-EXOR gate
DLS1L2	Level shifter 1
DOR42L2	4-input OR gate 2
DREFL2	Fixed level reference
DOR3L2	3-input OR gate
DTTREL2	T-type flip-flop with reset and toggle enable
DOR2L2	2-input OR gate
DOROS5L2	5-input OR-OR select gate
DAND42L2	4-input AND gate 2
DAORS3L2	3-input AND-OR select gate
DAND3L2	3-input AND gate
DOAND32L2	3-input OR-AND gate 2
DAND2L2	2-input AND gate
DAOR32L2	3-input AND-OR gate 2
DPWRDR43L2	Level 3 input power driver
DEOR3L2	3-input EXCLUSIVE-OR gate
DPWRDR41L2	Level 1 input power driver
DEOR2L2	2-input EXCLUSIVE-OR gate
D4TO1MLXL2	4 to 1 multiplexer
DJKL2	J-K type flip-flop
DTTL2	T-type flip-flop

Group 3. Functions with Outputs on Level 1 (Bottom Level) Only – Suffix L1

DAND2L1	2-input AND gate
DPWRDR43L1	Level 3 input power driver
DTCZ1L1	1-bit true/complement zero/one element
DREFL1	Fixed level reference
DOR2L1	2-input OR gate
DLS4L1	Level shifter 4
DPWRDR41L1	Level 1 input power driver
DBUF1L1	Level 1 buffer
DTTL1	T-type flip-flop
DAORS5L1	5-input AND-OR select gate
DOROS5L1	5-input OR-OR select gate
DOEOR3L1	3-input OR-EXOR gate
DOR4L1	4-input OR gate
DOR42L1	4-input OR gate 2
DPWRDR42L1	Level 2 input power driver
DLS2L1	Level shifter 2
DDTL1	D-type flip-flop
DJKRL1	J-K type flip-flop with reset
DEOR3L1	3-input EXCLUSIVE-OR gate
DJKL1	J-K type flip-flop
DAND4L1	4-input AND gate
DAND42L1	4-input AND gate 2

Group 4. Functions with Outputs on Levels 2 and 3 Suffix L23

DAND2L23	2-input AND gate
DLTCHL23	Transparent data latch
DOR5L23	5-input OR gate
DAND22L23	2-input AND gate 2
DJKL23	J-K type flip-flop
DOR2L23	2-input OR gate
DTTL23	T-type flip-flop
DEOR2L23	2-input EXCLUSIVE-OR gate
DTTREL23	T-type flip-flop with reset and toggle enable
DAND5L23	5-input AND gate
DREFL23	Fixed level reference
DOROS5L23	5-input OR-OR select gate
DOEOR3L23	3-input OR-EXOR gate
DOR4L23	4-input OR gate
DAND4L23	4-input AND gate
DDTL23	D-type flip-flop
DEOR3L23	3-input EXCLUSIVE-OR gate
DAND42L23	4-input AND gate 2
DTCZ1L23	1-bit true/complement zero/one element
DJKRL23	J-K type flip-flop with reset
DEOR22L23	2-input EXCLUSIVE-OR gate 2
DOR42L23	4-input OR gate 2
DOR22L23	2-input OR gate 2
D1TO2DMXL23	1 to 2 demultiplexer
DAORS5L23	5-input AND-OR select gate

Group 5. Functions with Outputs on Levels 1 and 3 Suffix L13

DEOR3L13	3-input EXCLUSIVE-OR gate
DDTL13	D-type flip-flop
DJKRL13	J-K type flip-flop with reset
DOR4L13	4-input OR gate
DAORS5L13	5-input AND-OR select gate
DREFL13	Fixed level reference
DAND42L13	4-input AND gate 2
DAND4L13	4-input AND gate
DOR42L13	4-input OR gate 2
DOROS5L13	5-input OR-OR select gate
DTTL13	T-type flip-flop
DJKL13	J-K type flip-flop
DOEOR3L13	3-input OR-EXOR gate
DTCZ1L13	1-bit true/complement zero/one element

Group 6. Functions with Outputs on Levels 1 and 2 Suffix L12

DLS3L12	Level shifter 3
DPWRDR42L12	Level 2 input power driver
DTTL12	T-type flip-flop
DDTL12	D-type flip-flop
DAORS5L12	5-input AND-OR select gate
DOROS5L12	5-input OR-OR select gate
DJKL12	J-K type flip-flop
DOR4L12	4-input OR gate
DOR42L12	4-input OR gate 2
DREFL12	Fixed level reference
DOEOR3L12	3-input OR-EXOR gate
DJKRL12	J-K type flip-flop with reset
DEOR3L12	3-input EXCLUSIVE-OR gate
DOR2L12	2-input OR gate
DAND4L12	4-input AND gate
DAND42L12	4-input AND gate 2
DPWRDR43L12	Level 3 input power driver
DPWRDR41L12	Level 1 input power driver
DTCZ1L12	1-bit true/complement zero/one element
DAND2L12	2-input AND gate

Group 7. Functions with Outputs on Levels 1, 2 and 3 Suffix L123

DOR42L123	4-input OR gate 2
DOROS5L123	5-input OR-OR select gate
DTTL123	T-type flip-flop
DAORS5L123	5-input AND-OR select gate
DREFL123	Fixed level reference
DAND2L123	2-input AND gate
DEOR3L123	3-input EXCLUSIVE-OR gate
DJKRL123	J-K type flip-flop with reset
DOR2L123	2-input OR gate
DJKL123	J-K type flip-flop
DOR4L123	4-input OR gate
DAND4L123	4-input AND gate
DAND42L123	4-input AND gate 2
DOEOR3L123	3-input OR-EXOR gate
DTCZ1L123	1-bit true/complement zero/one element
DDTL123	D-type flip-flop

DV COMPLEX MACROS

Using the above DX gate primitives, a range of more complex logic function macros has been developed. The range is constantly being extended to meet specific customer system design and performance requirements.

Examples of the types of functions that have already been developed are given below. It should be noted that this listing is not exhaustive; it is given here to demonstrate the capability of the DX cell library.

DUDCTRM	1-bit synchronous up/down counter module with count enable, parallel load and reset
DTM	Terminating module, generating final carry-out from module DLAC plus global carry-in
DSISOR4	4-bit serial-in/serial-out register with reset
DPISO4	4-bit parallel-in/serial-out register
DUDCT4	4-bit synchronous up/down counter with count enable and parallel load
DUCTR4	4-bit synchronous up counter with reset
DDCDR2	2 to 4-bit decoder (active low input)
D8TO1MX	8 to 1 multiplexer
DLTCH8	8-bit data latch
DLTCH16	16-bit data latch
DMCMP4	4-bit magnitude comparator (74L85 type) with cascade inputs
DADD8	8-bit adder with full look-ahead carry
DALU4	4-bit arithmetic logic unit (74181 type)
DSUM	2-bit sum module with look-ahead carry
DLAC	Look-ahead carry module, producing: carry, carry propagate and carry generate signals across two blocks
DSIPOR4	4-bit serial-in/parallel-out register with reset
DDTSP4	4-bit scan path register
DUDCTR4	4-bit synchronous up/down counter with count enable, parallel load and reset
DPAR9	9-bit parity generator (74180 type)
DDCDR4	3 to 8-bit decoder (active low output)
D1TO8DMX	1 to 8 demultiplexer
DLTCHR8	8-bit data latch with reset
DLTCHR16	16-bit data latch with reset
DADD4	4-bit adder with full look-ahead carry (7483 type)
DADD16	16-bit adder with full look-ahead carry

PACKAGING

A wide variety of ceramic and plastic package styles are available. Packages in clude dual-in-line, flatpacks, chip carriers, small outline (SO) packages and pin grid arrays.

The selection of a suitable package for a given application is determined by a number of factors:

- Number of input and output pins
- Number of power supply connections
- Application environment and temperature range
- Array die size relative to package island size
- Power dissipation
- Method of mounting package to PCB

Production quantities of the DT/DV series ULAs are available in industry-standard ceramic and plastic packages as shown below in Table 9. Prototype samples are normally supplied in ceramic only. Where plastic production packages are requested, ceramic prototypes will be supplied in the nearest equivalent and tested to the final test specification.

QUALITY AND RELIABILITY

At GEC Plessey Semiconductors, quality and reliability are built into the product by rigorous control of all processing operations and by minimising random uncontrolled effects in all manufacturing operations. Process management involves full documentation of all procedures, recording of batch-by-batch data, using traceability procedures and the provision of appropriate equipment and facilities to perform sample screens and conformance testing on finished product.

A common management system is used to control the manufacturing of GPS processes. All products benefit from the use of an integrated monitoring system throughout manufacturing, which leads to high quality standards for all technologies.

Further information is contained in the Quality Brochure, available from GEC Plessey Semiconductors Sales Offices.

Package code	Package type	Through board	Surface mount	Description
DC	DILMON	✓		Dual-in-line, multilayer ceramic. Brazed leads. Metal sealed lid.
DG	CERDIP	✓		Dual-in-line, ceramic body. Alloy leadframe. Glass sealed.
DP	PLASDIP	✓		Dual-in-line, plastic moulded. Copper or alloy leadframe.
AC	PGA	✓		Pin Grid Array, multilayer ceramic. Metal sealed lid.
MP	Small Outline		✓	Dual-in-line, plastic moulded. 'Gullwing' formed leads.
LC	LCC		✓	Leadless Chip Carrier, multilayer ceramic. Metal sealed lid.
HC	Leaded Chip Carrier		✓	Quad multilayer ceramic. Brazed 'J'-formed leads. Metal sealed lid.
GC	Leaded Chip Carrier		✓	Quad multilayer ceramic. Brazed 'Gullwing' leads. Metal sealed lid.
HG	Quad CERPAC		✓	Quad ceramic body. 'J'-formed leads. Glass sealed.
GG	Quad CERPAC		✓	Quad ceramic body. 'Gullwing'-formed leads. Glass sealed.
HP	PLCC		✓	Quad leaded plastic chip carrier. 'J'-formed leads.
GP	PQFP		✓	Quad plastic flatpack. 'Gullwing'-formed leads.

Table 9 Available package types

GEC PLESSEY
SEMICONDUCTORS

HEADQUARTERS OPERATIONS
GEC PLESSEY SEMICONDUCTORS
Cheney Manor, Swindon,
Wiltshire, United Kingdom SN2 2QW.
Tel: (01793) 518000
Fax: (01793) 518411

GEC PLESSEY SEMICONDUCTORS
P.O. Box 660017
1500 Green Hills Road,
Scotts Valley, California 95067-0017,
United States of America.
Tel: (408) 438 2900
Fax: (408) 438 5576

CUSTOMER SERVICE CENTRES
- **FRANCE & BENELUX** Les Ulis Cedex Tel: (1) 64 46 23 45 Fax: (1) 64 46 06 07
- **GERMANY** Munich Tel: (089) 3609 06-0 Fax: (089) 3609 06-55
- **ITALY** Milan Tel: (02) 66040867 Fax: (02) 66040993
- **JAPAN** Tokyo Tel: (03) 5276-5501 Fax: (03) 5276-5510
- **NORTH AMERICA** Scotts Valley, USA Tel: (408) 438 2900 Fax: (408) 438 7023
- **SOUTH EAST ASIA** Singapore Tel: (65) 3827708 Fax: (65) 3828872
- **SWEDEN** Stockholm, Tel: 46 8 702 97 70 Fax: 46 8 640 47 36
- **TAIWAN, ROC** Taipei, Tel: 886 2 5461260 Fax: 886 2 7190260
- **UK, EIRE, DENMARK, FINLAND & NORWAY**
  Swindon Tel: (01793) 518510 Fax: (01793) 518582

These are supported by Agents and Distributors in major countries worldwide.