ULA DA SERIES

ANALOG/DIGITAL MIXED SIGNAL ARRAY FAMILY

The ULA DA Series is a family of 8 arrays developed to provide single chip solutions to a wide variety of mixed analog/ digital applications. The customer design route is greatly simplified by the use of the PDM Design Modelling System, which enables the user to achieve maximum system integration rapidly with minimum system cost.

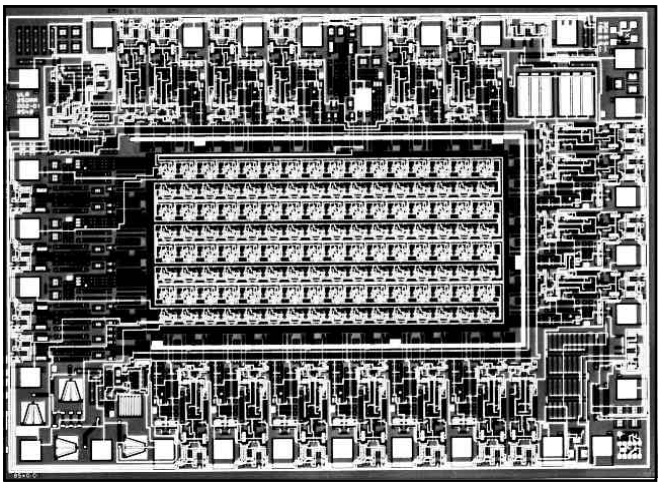


Fig. 1 A DA Series chip

FEATURES

- Combines Analog and Digital
- Comprehensive Analog Cells
- PNP and NPN Transistors
- Special Purpose Analog Cells
- High Current Drive: 120mA
- Auto Place and Route
- Sea of Gates Configuration
- Eight Array Types
- Operation from 1V to 18V
- Two Speed/Power Options
- Many Package Options
- Supports the PDM System
- Suitable for Customer Design

GENERAL DESCRIPTION

In addition to the features listed above, the DA Series has on-chip capacitors, matched resistors and low logic current. High performance analog circuits can be designed using NPNs with an f_T of 500MHz and PNPs of 300 MHz. The transistors are closely matched, with gains that are practically flat from below 10nA to above 10mA.

The chip architecture exploits the mixed signal performance by combining a central core of logic cells surrounded by analog cells to implement the required analog or digital I/O functions. The interface or analog cells contain 9 NPN and 4 PNP transistors, together with supporting resistors and bond pad capacitors. These components are used to implement the high performance analog and digital interface circuits required by the design. Up to 48mA can be driven by each analog cell. Special cells located in the corners of the chip include a bandgap reference (1·25V, low temperature coefficient), voltage regulator, low offset transistors, precision matched resistors, capacitors and high current transistors (120mA). Autorouted interconnection commits the components on the array to the specified design.

An extensive library of analog and digital macro functions supports the PDM design system. Digital macros range from simple inverters and gates to complex counters and shift registers. Users can build their own logic macros from the basic set. Amplifiers, comparators, oscillators and regulators – as well as more complex analog functions – exist as macros within the design software and as fully characterised physical macro parts. New macro functions are regularly added to the library and, if requested, special analog macros can be designed to supplement the library.

PRODUCT RANGE

The DA Series product range is shown below.

Array	Logic gates	Analog cells	Analog NPNs	Analog PNPs	Bond pads
2DA	20	6	110	50	18
8DA	80	10	146	66	22
18DA	176	14	182	82	26
25DA	256	18	218	98	30
35DA	352	22	254	114	34
50DA	512	24	272	122	36
90DA	924	32	344	154	44
150DA	1458	40	416	186	52

ABSOLUTE MAXIMUM ARRAY RATINGS

Parameter	Min.	Max.	Units
Supply voltage	−0·5	+20	V
Input voltage	−0·5	+18.0	V
Operating temperature range, T_{AMB}	−55	+125	°C
Storage temperature range, T_{STG}	−65	+150	°C

THE DA SERIES BIPOLAR TECHNOLOGY

The process technology used for the DA Series is the LD process, which is a variant of the basic Mixed Signal Bipolar VLSI process. The LD process maintains the high performance VLSI capability but includes vertical structure PNP transistors with an f_T of 300 MHz. The addition of these active components, along with the inherent features of high h_{FE} over a wide operating collector current range, low R_{SAT}, low offsets, low leakage, excellent speed/power product and high reliability makes the DA series eminently suitable for combined analog and digital functions for both commercial and military mixed signal applications.

TYPICAL ARRAY CHARACTERISTICS at T_{AMB} = 25°C

Parameter	Value	
	DA(A)	DA(B)
Gate supply current (Note 1)	10·5µA	2·0µA
Gate delay	60ns	430ns
Toggle frequency	3·3MHz	0·5MHz
Transistor pair base-emitter matching	<1mV	
Analog switch offset	<1mV	
Bandgap reference	1·25V	
Bandgap reference stability	50ppm/°C	
Voltage range:		
On-chip shunt regulator	1·0 to 2·5V	
On-chip series regulator	2·5 to 5·5V	
On-chip series regulator (using additional high voltage components)	5·5 to 18·0V	

NOTES
1. Matrix supply current = number of gates used x gate supply current.
2. Gate power and supply current based on 60% duty cycle.
3. Clock rate is based on critical (clock) path gate delay in an edge-triggered D-type flip-flop.

ANALOG TRANSISTOR CHARACTERISTICS

Typical values at T_{AMB} = 25°C (unless otherwise stated)

Characteristic	Symbol	Transistor size								Unit	Conditions
		PNP		NPN							
		1A	2A	1A	2A	4A	10A	16A	60A		
Current gain	h_{fe} forward	-	-	140	140	150	150	-	-		I_E = 1µA to 1mA
		-	-	-	-	-	-	120	120		I_E = 1µA to 100mA
		55	-	-	-	-	-	-	-		I_E = 1µA to 200µA
		-	55	-	-	-	-	-	-		I_E = 1µA to 400µA
Current gain	h_{fe} inverse	6·5	7	7	10	11	45	-	-		I_E = 1µA to 10mA
		-	-	-	-	-	-	70	15		I_E = 1µA to 100mA
Leakage current	I_{CBO}	0·01	0·01	0·01	0·01	0·01	0·01	0·01	0·05	nA	V_{CB} = 1V
Leakage current	I_{CEO}	0·5	0·5	0.5	0·5	0·5	0·5	0·5	25	nA	V_{CB} = 1V
Base emitter voltage	V_{BE}	670	652	654	616	598	594	582	548	mV	I_E = 10µA
V_{BE} matching between adjacent transistors		±1·5	±1	±1	±1	±0·5	±0·5	±0·5	±0·5	mV	I_E = 1µA, I_C = 10µA
Collector offset voltage	$V_{CE\ SAT}$	-	-	3·0	3·0	1·5	0·8	0·8	1·0	mV	I_B = 30µA, I_C = 10µA
V_{offset} matching/ adjacent pairs of transistors		-	-	50	50	10	10	10	50	µV	I_C = 0µA, I_B = 30µA
Collector saturation resistance	R_{SAT}	-	-	55	55	30	25	25	-	Ω	I_C = 1mA, I_B = 100µA
		-	-	-	-	-	-	-	3	Ω	I_C = 100mA, I_B = 10mA
	$V_{CBO\ (min)}$	8	8	8	18	18	8	8	18	V	
	$V_{EBO\ (min)}$	6·0	6·0	6·0	6·0	6·0	6·0	6·0	6·0	V	
	$V_{CEO\ (min)}$	8	8	4.5	4·5	4·5	4·5	4·5	4·5	V	
Collector slope resistance	R_C	25	25	20	20	20	20	20	20	kΩ /mA	
Collector current	$I_{C(max)}$	0.2	0.4	12	12	30	20	20	120	mA	T_{AMB} = 0°C to +70°C

DIFFUSED RESISTOR CHARACTERISTICS

T_{AMB} = 25°C

Characteristic	Cell type		
	Corner	Analog	
	All	Banks 9k	Others
Absolute tolerance	±25%	±25%	±30%
Voltage coefficient (typ.)	+0·5%/V	+0·5%/V	+1·5%/V
Temperature coefficient (typ.)	+0·2%/°C	+0·2%/°C	+0·25%/°C
Matching	±0·5%	±0·5%	±1%

METHODS OF POWERING THE ULA

Several methods are available for supplying power to the ULA. In general, any external supply can be used (from 1V to rectified mains) by suitable choice of a minimum of external components. The most commonly used supply is 5V and this is the recommended voltage for most applications.

The ULA operates directly from a 5V supply. Two other methods are shown below; these are from 18V and from rectified mains voltage. All the methods shown provide a temperature-compensated noise-free supply to the logic cells.

Method 1

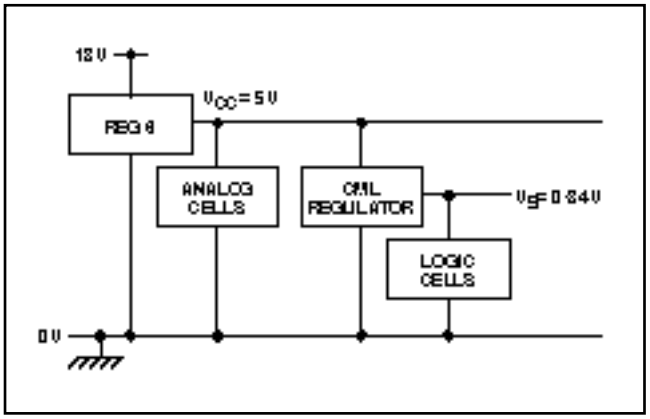


Fig. 2 18V supply, on-chip series voltage regulator

Fig. 2 shows one method of deriving the ULA V_{CC} of 5V from an external 18V supply. REG6 is a suitable series regulator macro. The supply to the matrix (V_S=0·84V) is fixed by theCML regulator on the chip.

Method 2

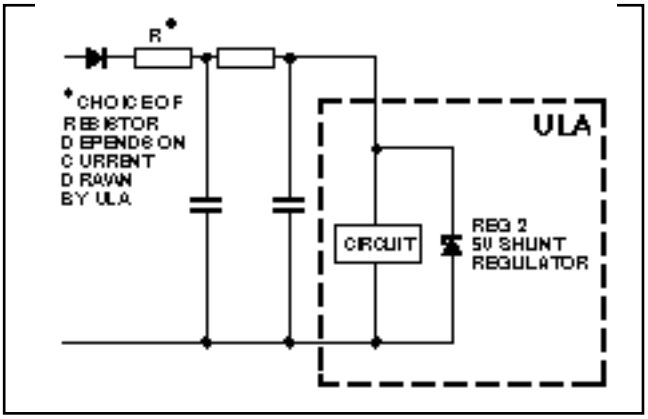


Fig. 3 Mains driven voltage regulator

By a suitable choice of an external resistor and a few other components, the ULA can be supplied from rectified mains voltage, as shown in Fig. 3. REG2 is a suitable 5V shunt regulator macro.

NOTE

Although the arrays will operate from supply voltages below 5V, the standard analog macros have been designed to operate at 5V nominal. For circuits requiring lower voltage operation, therefore, special non-standard macros will be required. In such cases, GPS should be consulted before commencing a design.

THE CHIP ARCHITECTURE

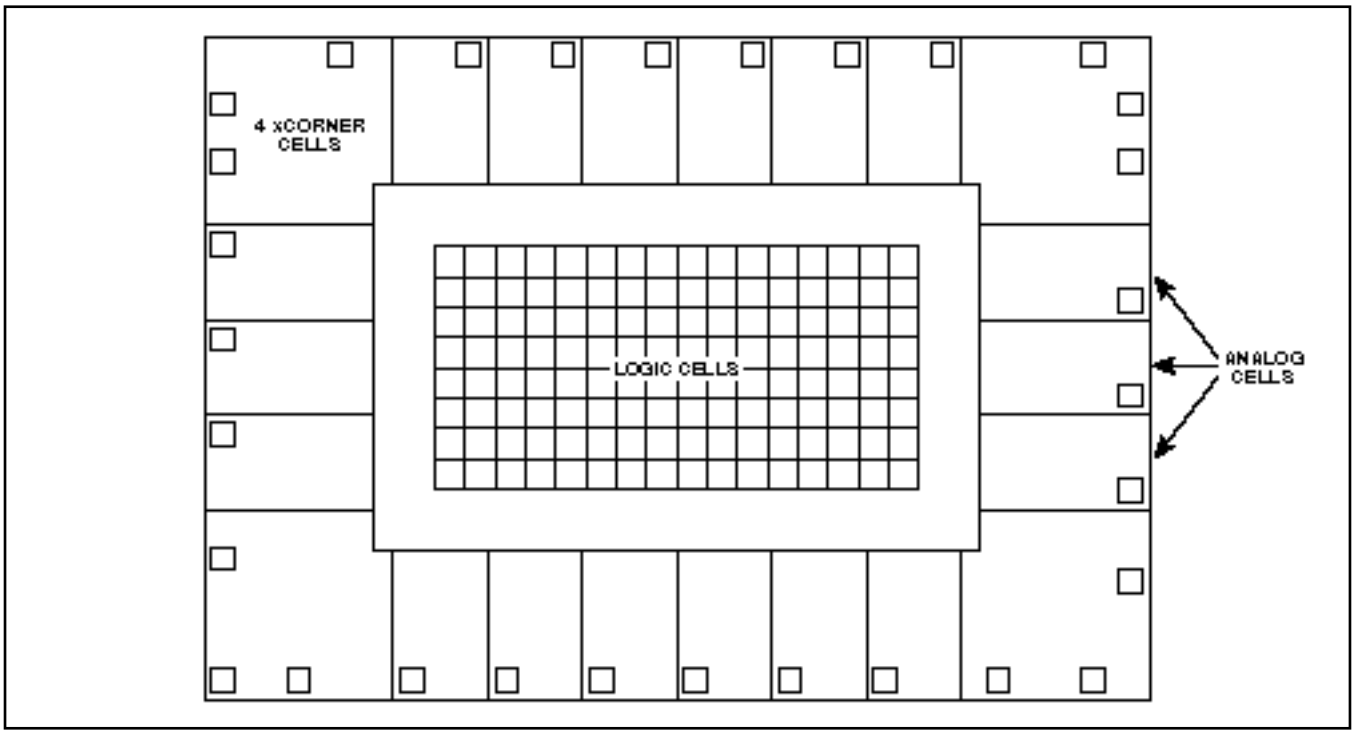


Fig. 4 DA Series chip architecture

ANALOG CELLS

These are used for the implementation of analog functions and I/O circuits. They are located around the periphery of each array.

CORNER CELLS

There are 4 corner cells, which contain a variety of specialised components to support analog and I/O functions.

LOGIC CELLS

These are used to implement the logic functions for the digital portion of the semi-custom design. They are contained within the central core of the chip in a matrix arrangement.

ANALOG CELL

This cell has been designed for the implementation of the majority of analog functions and is located around the periphery of the chip. The number per chip is dependent on the array size and ranges from 6 to 40.

Each analog cell contains an extensive range of components as illustrated in Fig. 5. The transistors have a high ß, which is flat over a wide range of currents, and are well matched to better than 1mV on V_{BE} and 15µV on V_{offset}. The resistors range in value from 800Ω to 80kΩ , with matching to within ±1% for the analog cells and ±0·5% for the resistor bank in the corner cell and with excellent voltage and temperature characteristics.

NOTE

Reference is made to 1A, 2A, 4A, and 10A transistors. These are area ratios; the basic area is 1A, so 4A is four times the basic area. In general, the greater the area the higher the current capability, the lower the offset and the better the V_{BE} matching.

Analog Cell Content

The analog cell contains the following components:

- 9 NPN transistors
- 4 PNP transistors
- 4 x 80kΩ resistors
- 4 x 40kΩ resistors
- 2 x 20kΩ resistors
- 8 x 9kΩ resistors
- 1 x 800Ω resistor
- 2 x Logic pull-up resistors
- 1 Bond pad (can be used as low value capacitor)

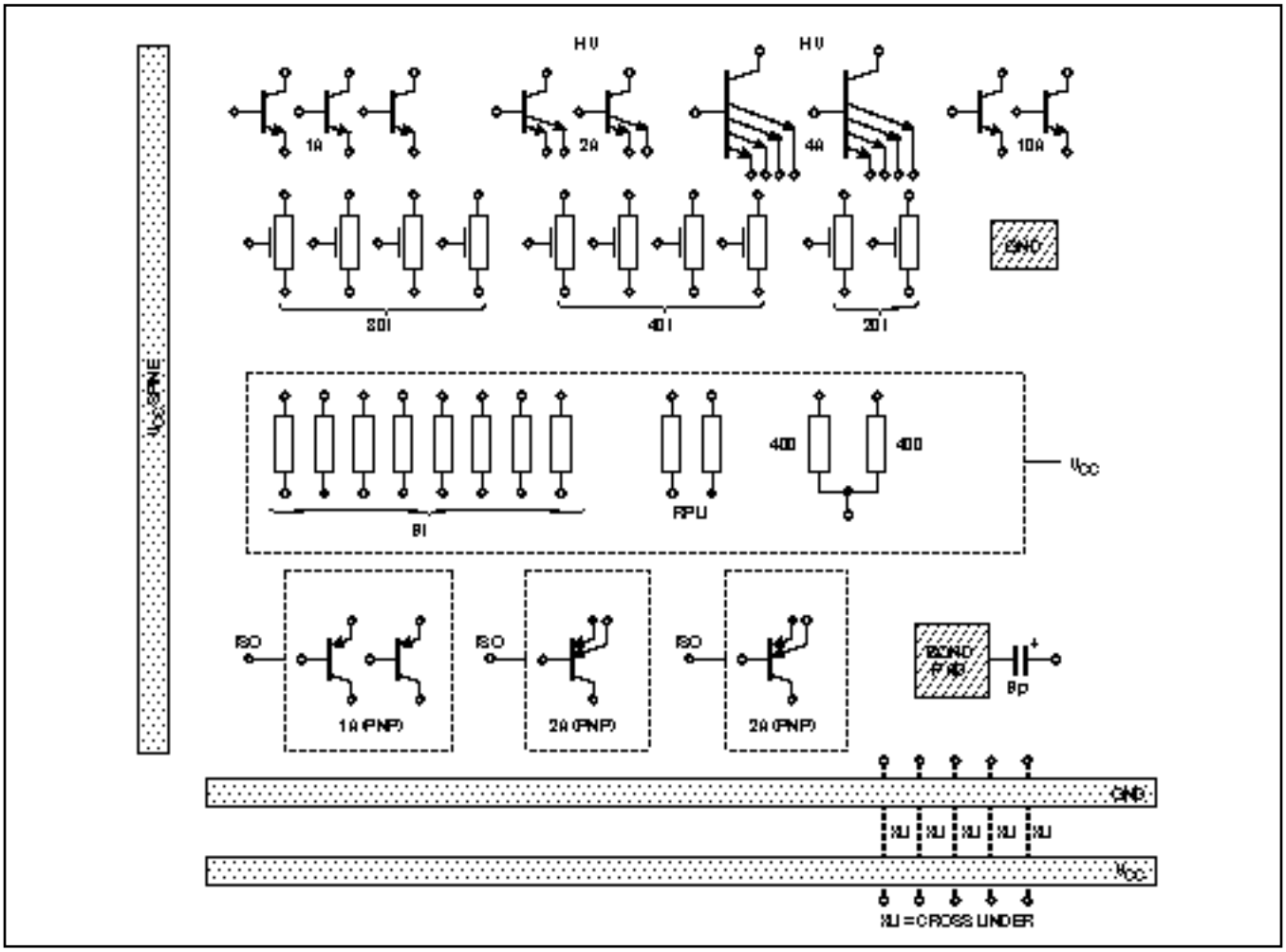


Fig. 5 DA Series analog cell content

CORNER CELL

Common to all the arrays in the ULA DA family are special cells distributed in the four corners of the chip. These include a bandgap reference, voltage regulator, high current transistors, compensation capacitors and banks of resistors. The cells serve to support the analog cells for analog circuit design and special I/O requirements.

Top Left Corner

- REGULATOR COMPONENTS
  - Bandgap core
  - Bandgap potential dividers
  - Level shift components
  - Pass elements
- 3 bond pads
- Half analog cell

The bandgap reference provides a stable reference voltage of nominally 1·25V, with a typical temperature coefficient of 50 ppm/°C. This reference is used as the basis of voltage regulators and references.

Top Right Corner

- 2 large area capacitors
- 3 low offset NPN transistors
- 4 10kΩ CT diffused resistors (high voltage)
- 3 200kΩ epitaxial resistors (high voltage)
- 4 2A PNP transistors (high voltage)
- 4 high voltage cross-unders
- 3 bond pads
- Half analog cell

The two diffused capacitors (nominally 35pF) can be used for compensation. They are both based on a transistor structure and can be configured as such if required.

Bottom Left Corner

- 4 60A power NPN transistors (high voltage)
- 3 power cross-unders (high voltage)
- 1 cross-under (high voltage)
- 4 25Ω isolation resistors (high voltage)
- 3 10kΩ CT diffused resisors (high voltage)
- 1 V_S regulator (for CML logic)
- 3 bond pads
- Half analog cell

The four transistors are particularly suitable for high current outputs, such as triac drivers, supplying up to 120mA each (over the temperature range 0°C to +70°C).

The V_S regulator provides a stable, noise-free voltage supply to the logic matrix, enabling the DA Series to be used in electrically noisy environments.

Bottom Right Corner

- 4 BANKS of 8:
  5kΩ diffused resistors in common isolation (high voltage)
- 3 low offset NPN transistors
- 4 200kΩ epitaxial transistors (high voltage)
- 4 2A PNP transistors (high voltage)
- 4 cross-unders (high voltage)
- 4 4A NPN transistors (high voltage)
- 3 bond pads
- Half analog cell

The diffused resistors in the four banks are matched to better than 0·5% and are useful for applications such as data conversion.

ANALOG MACROS

A range of macros has been developed to ease the design process and to support the use of a customer design route using the PDM system, described later.

Details of the extensive range of DA macros are presented in the Analog Cell Library section of the Mixed Signal ASIC Technical Handbook. A few examples are shown below.

Analog Macro and I/O Library

Low offset op-amps	RC oscillators	D-A converters
High gain op-amps	Crystal oscillators	A-D converters
PNP input op-amps	Monostables	Triac drivers
		Zero crossing switch
Low offset comparators	Schmitt triggers	LCD drivers
PNP input comparators	Switch-on reset circuits	LED drivers
	Analog switches	Photodiode amplifier
5V series regulator		Low voltage amplifiers
5V shunt regulator	Logic signal interfaces	VCOs
Battery low detector	High current outputs	Phase lock loop
2·5V reference		
1·25V reference		
Programmable reference		

Analog Macro Examples

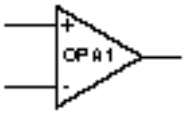
MACRO NAME
OPA1

FUNCTION
General purpose operational amplifier

BOND PAD REQUIREMENTS
1 for internal compensation
1 for each pin taken off the chip

PERIPHERAL CELL REQUIREMENTS
1 analog cell

SCHEMATIC SYMBOL



SPECIFICATION

Characteristic	Value			Unit	Conditions
	Min.	Typ.	Max.		
Supply voltage	4·5	5	5.5	V	
Supply current		150	280	µA	V_{CM} = 2·5V, V_{OUT} = 2V
Input offset voltage		±2	±10	mV	V_{CM} = 2·5V
Input bias current		10	50	nA	V_{CM} = 2·5V
Input common mode range	1		V_{CC}−1·3	V	
Common mode rejection ratio	60	70		dB	
Open loop gain		40		V/mV	V_{CM} = 2·5V, V_{OUT} = 2V, R_{LOAD} = 10kΩ
Open loop bandwidth		20		Hz	V_{CM} = 2·5V, V_{OUT} = 2V
Unity gain bandwidth		250		kHz	V_{CM} = 2·5V, V_{OUT} = 2V
Large signal bandwidth		60		kHz	V_{OUT} = 3V p-p
Slew rate		0·6		V/µs	
Output voltage range	0·2		V_{CC}−1·5	V	
Output source current		1		mA	
Output sink current	45	90		µA	
Short circuit output current		5	7	mA	

NOTE: Typical data quoted at V_{CC} = 5V and T_{AMB} = 25°C

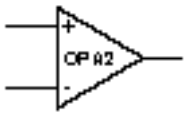
MACRO NAME
OPA2

FUNCTION
Low offset operational amplifier

BOND PAD REQUIREMENTS
1 for internal compensation
1 for each pin taken off the chip

PERIPHERAL CELL REQUIREMENTS
1 analog cell

SCHEMATIC SYMBOL



SPECIFICATION

Characteristic	Value			Unit	Conditions
	Min.	Typ.	Max.		
Supply voltage	4·5		5.5	V	
Supply current		135	280	µA	V_{CM} = 2·5V, V_{OUT} = 2V
Input offset voltage			±2·5	mV	V_{CM} = 2·5V
Input bias current			25	nA	V_{CM} = 2·5V
Input common mode range	0·8		V_{CC}−0·5	V	
Common mode rejection ratio				dB	
Open loop gain				V/mV	V_{CM} = 2·5V, V_{OUT} = 2V, R_{LOAD} = 10kΩ
Open loop bandwidth				Hz	V_{CM} = 2·5V, V_{OUT} = 2V
Unity gain bandwidth				kHz	V_{CM} = 2·5V, V_{OUT} = 2V
Large signal bandwidth				kHz	V_{OUT} = 3V p-p
Slew rate				V/µs	
Output voltage range	0·2		V_{CC}−1·5	V	
Output source current			1	mA	
Output sink current	45			µA	
Short circuit output current				mA	

NOTE: Typical data quoted at V_{CC} = 5V and T_{AMB} = 25°C

Analog Macro Examples (continued)

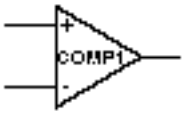
MACRO NAME
COMP1

FUNCTION
General purpose comparator

BOND PAD REQUIREMENTS
1 for each pin taken off the chip

PERIPHERAL CELL REQUIREMENTS
1 analog cell

SCHEMATIC SYMBOL



SPECIFICATION

Characteristic	Value			Unit	Conditions
	Min.	Typ.	Max.		
Supply voltage	4·5	5	5.5	V	
Supply current		105	200	µA	$V_{IN}+ = 3·5V$, $V_{IN}- = 1·5V$
Input offset voltage		2	5	mV	$V_{CM} = 2·5V$
Input bias current		75	300	nA	$V_{CM} = 2·5V$
Input common mode range	0·8		$V_{CC}-0·7$	V	
Voltage gain		8500		V/V	$V_{CM} = 2·5V$
t_{PLH}		1·1		µs	$V_{IN}- = 2·5V$ $V_{IN}+ = 2·4V \rightarrow 2·505V$
t_{PHL}		1		µs	$V_{IN}+ = 2·5V$ $V_{IN}- = 2·6V \rightarrow 2·495V$
t_{PLH}		0·2		µs	$V_{IN}+ = 2·5V$ $V_{IN}- = 1·5V \rightarrow 3·5V$
t_{PHL}		0·9		µs	$V_{IN}+ = 2·5V$ $V_{IN}- = 3·5V \rightarrow 1·5V$

ANALOG MACRO KIT PARTS

To accommodate the design route which employs the PDM system (described later), all analog macros are available as kit parts. Each is housed in an 18-pin DIL package containing a number of macros. As an example, the ADM005 kit part is illustrated opposite.

Absolute maximum Ratings

Supply voltage V_{CC}	+7·0V max. −0·5 min.
Input voltage V_{IN}	+5·5V max. −0·5V min.
Operating temperature	−55°C to +125°C
Storage temperature	−65°C to +150°C

ADMOO5 Kit Contains

- 2 x OPA2 Low offset operational amplifier
- 1 x OPA3 Low offset operational amplifier
- 1 x VF1 Voltage follower
- 1 x REF1 1·25V bandgap reference

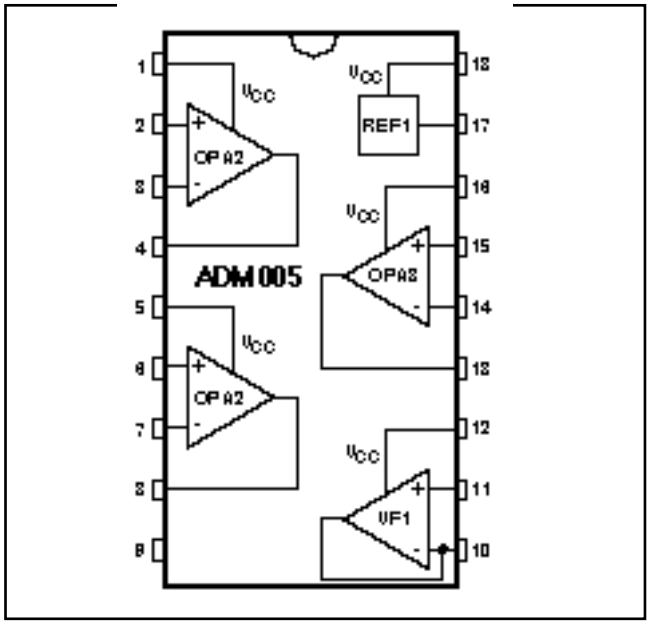


Fig. 6 analog macro kit part ADM005

LOGIC CELL

The logic cells located in the central matrix of the array are used to implement logic functions (gates, flip-flops, counters etc.). The logic cell (Fig. 7) has been optimised to allow compact logic structures, based on Current Mode Logic (CML), to be constructed.

CML operates by the switching of a current source. Typical circuit arrangements for the two basic gate types are shown in Fig. 8.

The current source is chosen so that $IR_L < 0{\cdot}5V_S$. The gate transistors do not saturate and so the additional gate delays associated with saturation effects are avoided. This, coupled with operation from a very low supply voltage (less than 1V), provides fast switching and reduced power consumption.

Additionally, two logic speed options area vailable: DA (A) and DA (B). Savings in supply current can be made by selecting the B option (nominal consumption per gate = 2µA) for those applications where clock frequency is less demanding.

All arrays use a logic swing of 280mV which results in a power-delay time product of 0·6pJ. The reduced noise margins associated with such a low logic swing (in comparison with TTL levels) are not detrimental because the noise on the internal logic supply (which is regulated) is reduced proportionally.

The internal V_S regulator is set to 0·84V (approx.). This is temperature compensated so that the logic swings from the gate outputs remain symmetrical about the gate input thresholds.

LOGIC DESIGN

The logic primitives that are used are NOR gates and inverters. All logic elements are made up of these two basic primitives. Each logic cell contains enough components for two 2-input NOR gates. It is a simple matter to configure a cell to form two inverters or one 3- or 4-input gate.

LOGIC MACRO FUNCTIONS

A unique metal pattern which converts a grouping of logic cell components into a logic element is known as a logic macro function. These predesigned circuits have been completely characterised and are accessible through a library similar to a catalogue covering standard TTL or CMOS logic families. The complexity of the elements ranges from a simple NOR gate to a complex 1-line to 16-line data selector.

The logic macro concept allows designers to work in a hierarchical fashion with large numbers of logic blocks of any level of complexity, while allowing flexibility of layout with a small number of standard elements.

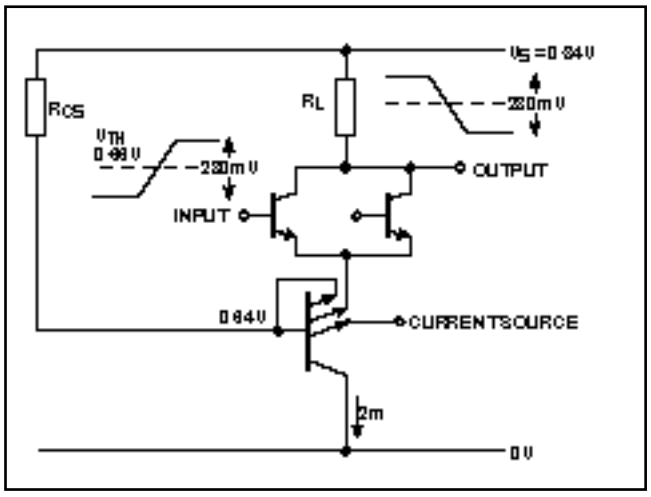


Fig. 7 Logic gate (1/2 cell)

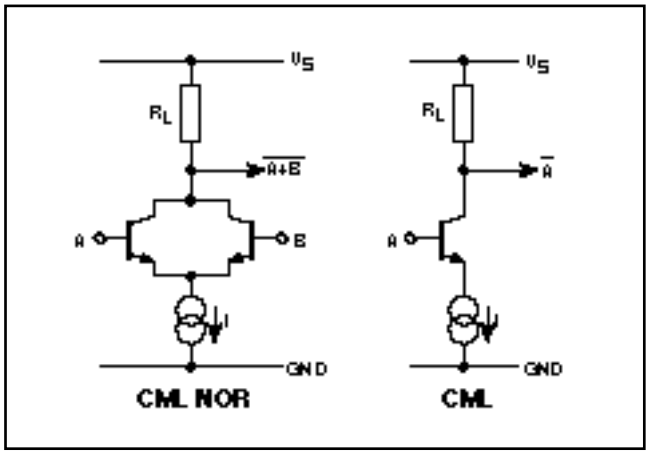


Fig. 8 NOR gate and inverter

Current Mode Logic Speed/Power Options		
Option	**Gate I_C (µA) Typ.**	**Gate speed (ns)**
DA(A)	10·5	60
DA(B)	2·0	430

DA SERIES LOGIC MACRO FUNCTIONS

Standard NOR gate
Buffered NOR gate
Hi-Drive NOR gate

1-Input D-types
Special D-types
T-types
Fast T-types
Data latches

Equivalence element
Exclusive-OR

S-R flip-flop
Negative edge-triggered narrow pulse monostable
Positive edge-triggered narrow pulse monostable
J-K flip-flop
J-K flip-flop with reset
J-K flip-flop with set
J-K flip-flop with set and reset
Toggle enable D-type
Toggle enable D-type with reset
Toggle enable D-type with set
Toggle enable D-type with set and reset

2-line to 1-line multiplexer
4-line to 1-line multiplexer
1-line to 2-line data selector
1-line to 4-line data selector
1-line to 8-line data selector
1-line to 16-line data selector
2-line to 4-line decoder
3-line to 8-line decoder
4-line to 16-line decoder
BCD to 7-segment decoder

4-bit equality comparator

4-bit clocked data register
4-bit clocked data register with reset

4-bit transparent data latch
4-bit transparent data latch with reset

4-bit ripple counter
4-bit ripple counter with reset
Divide by 3 counter
Divide by 3 counter with reset
Divide by 5 counter
Divide by 5 counter with reset
Divide by 6 counter
Divide by 6 counter with reset
Divide by 7 counter
Divide by 7 counter with reset
4-bit binary down counter
4-bit binary down counter with reset
4-bit binary up counter
4 bit binary up counter with reset
1 bit binary up-down counter (single cascadable bit)
1 bit binary up-down counter with reset (single cascadable bit)
4-bit binary up-down counter
4-bit binary up-down counter with reset
4-bit decade up counter
4-bit decade up counter with reset
4-bit decade down counter
4-bit decade down counter with reset

THE ULA DA SERIES DESIGN ROUTE

Introduction

The design route employs the PDM system, which is an advanced benchtop prototype modelling system for mixed signal semi-custom array design. It provides an excellent design route by allowing for a rapid design cycle, in-system verification and evaluation prior to committing to silicon.

System Overview

The hardware kit consists of a reconfigurable logic module, an analog design tablet, analog and logic macros and analog kit parts. This is used in conjunction with a computer hardware platform to provide the overall PDM system hardware.

The full circuit schematic, including external components, is entered using the schematic capture program. Analog and logic functions are selected from the macro library. The logic section of the design is down loaded via an RS232 link into the reconfigurable logic module. The logic module, which is now configured to replicate the logic section of the semi-custom design, is connected to the analog design tablet via a 48-channel ribbon cable onto which the physical analog macros (packaged as kit parts) and external components are connected.

Circuit Evaluation and Verification

Once connected to replicate the circuit to be integrated by the semi-custom product, the input and output signals and loads are attached to the design tablet. The PDM hardware is then an accurate model of the in-system ASIC.

Tests can be performed to verify the performance and validate the circuit. Any modifications and design revisions can be implemented quickly and a reiteration of evaluation, modification and verification can be performed before committing to silicon.

Committing to Silicon

When the design and evaluation process is completed an integrated package containing the captured verified system design, basic parametric test information and functional description is supplied to GPS for integration onto silicon. Samples of the defined ASIC are manufactured and functionally tested before shipping to the customer.

THE DESIGN PROCEDURE (see Fig. 9)

Introduction

The design route is split into three distinct areas:

- Circuit Design
- Prototype Modelling
- Physical Design

System Specification

Whether the DA Series forms the complete system, or is just a part of a larger system, a clear overall system specification is essential.

System Partitioning

The system is partitioned into sub-systems (where applicable). A sub-system can be a DA array, PROM, PLA, etc. The partitioning into individual sub-systems must ensure that the semi-custom device is not required to contain incompatible technology mixes or circuit configurations.

ULA DA Series Target Specification

At this point a target specification should be written detailing parameters that are strictly relevant to achieving the desired performance.

Circuit Design

Before proceeding to this point it is essential to become familiar with the capabilities of the ULA DA family and the PDM system. Support documents as listed below are supplied with the PDM kit.

- PDM User's manual
- DA Series Design Manual
- DA Series Analog Macro Library and Kit Parts
- DA Series Logic Macro Library

The system design is carried out on the computer system. The paper design is converted to a schematic format and captured by calling up suitable analog and logic macros from the library menus.

It is possible to include elements and components that are external to the ULA DA design, as part of the schematic capture. This useful feature means that the whole system can be recorded on one diagram if required.

Prototype Modelling

When the schematic capture is complete the netlist of the digital portion is down loaded to the logic module and is configured within the logic module. The analog section is built up using the analog macro kit parts on the design tablet and interfaced to the logic section, thereby creating a hardware replica of the design to be integrated.

Integration Package

Once the circuit has been fully evaluated, the circuit details are transferred to GPS on floppy disc or cartridge.

Physical Design

On receipt of the Design Integration Package, GPS carries out a design review. Part of this review is aimed at integrating as many of the gain/level setting resistors as possible so as to reduce both the pin count and the number of external components. Following this, the design is integrated on silicon and prototypes dispatched within 4-8 weeks.

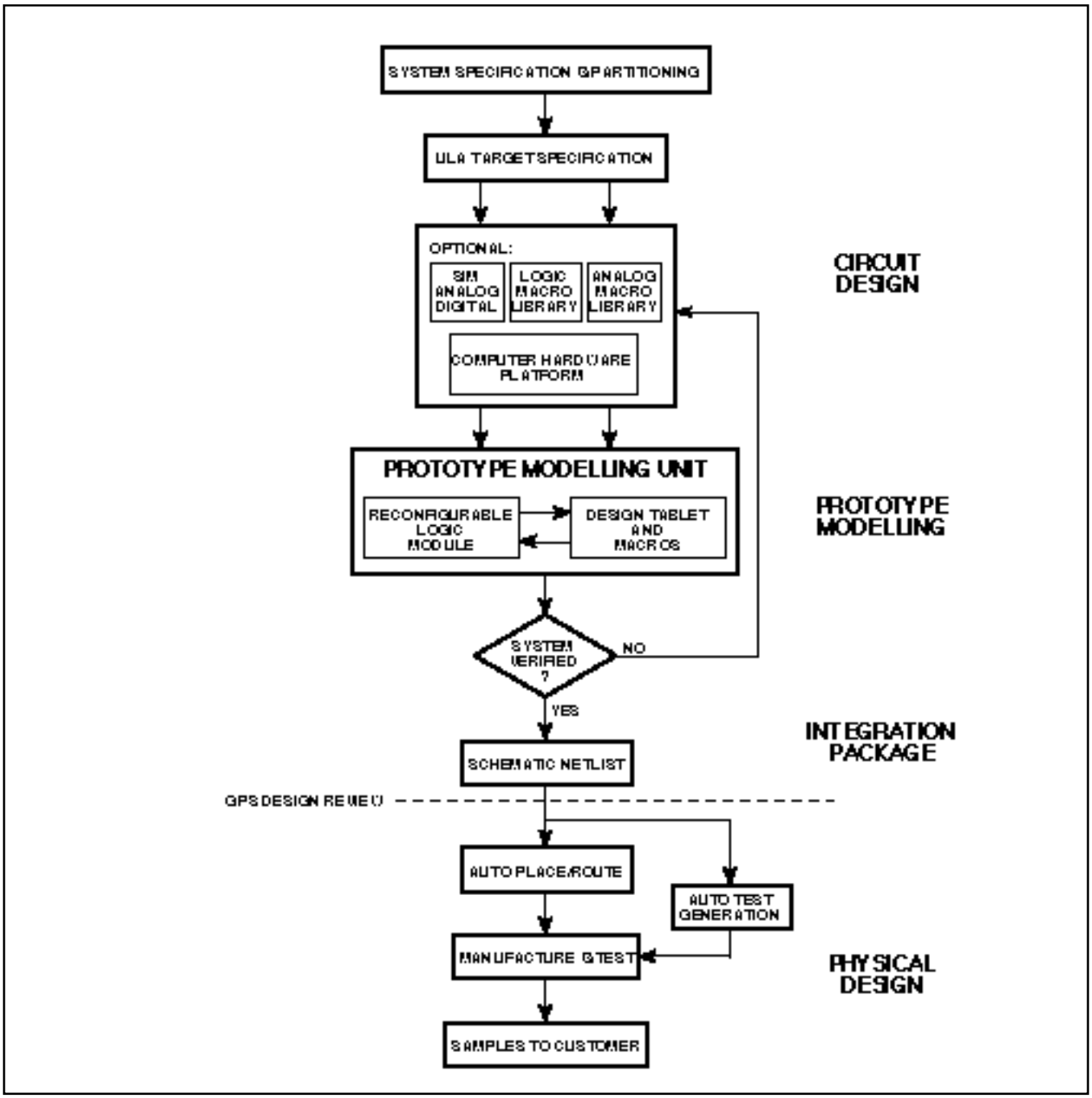


Fig. 9. PDM Design Modelling for mixed signal semi-custom

Minimum Computer Hardware Requirements

- IBM PC/AT compatible bus
  EGA graphics
  2 x RS232 port (1 for mouse)
  3-button mouse
  20 Mbyte hard disc
  5·25in. floppy (1·2 Mbyte)
  Operating system MS-DOS 3.0 onwards
  640 Kbyte RAM

PDM Kit Supplied by GPS

Hardware	Reconfigurable logic module	
	Analog tablet	
	Analog kit parts	
Optional	Basic transistor kit parts	
Software	Schematic capture	
	Logic mapping	Supplied on 5·25 or 3·5in floppy disc
	Analog and logic macro library	Supplied on 5·25 or 3·5in floppy disc
	Digital simulation	Supplied on 5·25 or 3·5in floppy disc
Optional support	Spice simulation	
Documentation	User's Manual	
	Analog Macro Library	
	Logic Macro Library	
	ULA DA Design Manual	

PACKAGING

A wide variety of ceramic and plastic package styles is available. Packages include dual-in-line, flatpacks, chip carriers, small outline (SO) packages and pin grid arrays.

The selection of a suitable package for a given application is determined by a number of factors:

- Number of input and output pins
- Number of power supply connections
- Application environment and temperature range
- Array die size relative to package island size
- Power dissipation
- Method of mounting package to PCB

Production quantities of the DA series arrays are available in industry-standard ceramic and plastic packages as shown below in Table 1. Prototype samples are normally supplied in ceramic only. Where plastic production packages are requested, ceramic prototypes will be supplied in the nearest equivalent and tested to the final test specification.

Packaging Options

The information given in Table 2 shows which array sizes will fit in which plastic packages and is intended only as a guide. Detailed package specifications are available from GPS Design Centres on request. Available packages are being continuously updated, so if a particular package is not listed, please enquire through your GPS Sales Representative.

Package code	Package type	Through board	Surface mount	Description
DC	DILMON	✓		Dual-in-line, multilayer ceramic. Brazed leads. Metal sealed lid.
DG	CERDIP	✓		Dual-in-line, ceramic body. Alloy leadframe. Glass sealed.
DP	PLASDIP	✓		Dual-in-line, plastic moulded. Copper or alloy leadframe.
AC	PGA	✓		Pin Grid Array, multilayer ceramic. Metal sealed lid.
MP	Small Outline		✓	Dual-in-line, plastic moulded. 'Gullwing' formed leads.
LC	LCC		✓	Leadless Chip Carrier, multilayer ceramic. Metal sealed lid.
HC	Leaded Chip Carrier		✓	Quad multilayer ceramic. Brazed 'J'-formed leads. Metal sealed lid.
GC	Leaded Chip Carrier		✓	Quad multilayer ceramic. Brazed 'Gullwing' leads. Metal sealed lid.
HG	Quad CERPAC		✓	Quad ceramic body. 'J'-formed leads. Glass sealed.
GG	Quad CERPAC		✓	Quad ceramic body. 'Gullwing'-formed leads. Glass sealed.
HP	PLCC		✓	Quad leaded plastic chip carrier. 'J'-formed leads.
GP	PQFP		✓	Quad plastic flatpack. 'Gullwing'-formed leads.

Table 1 Available package types

Package type	Leads	2DA	8DA	18DA	25DA	35DA	50DA	90DA	150DA
Plastic Dual In Line (DP)	8	·	·						
	14	·	·	·	·	·			
	16	·	·	·	·	·			
	18	·	·	·	·	·			
	20		·	·	·				
	22		·	·	·	·	·		
	24			·	·	·	·		
	28			·	·	·	·	·	
	40				·	·	·	·	·
	48					·	·	·	·
Quad PLLC, J-Form (HP)	28	·	·	·	·	·	·	·	·
	44				·	·	·	·	·
	52								·
Miniature Plastic DIL (Wide Body) (MP/W)	16	·	·	·					
	18	·	·	·	·	·	·		
	20		·	·					
	24		·	·	·				
	28		·	·	·	·			

Table 2 DA series plastic package options

QUALITY AND RELIABILITY

At GEC Plessey Semiconductors, quality and reliability are built into the product by rigorous control of all processing operations and by minimising random uncontrolled effects in all manufacturing operations. Process management involves full documentation of all procedures, recording of batch-by-batch data, using traceability procedures and the provision of appropriate equipment and facilities to perform sample screens and conformance testing on finished product.

A common management system is used to control the manufacturing of GPS processes. All products benefit from the use of an integrated monitoring system throughout manufacturing, which leads to high quality standards for all technologies.

Further information is contained in the Quality Brochure, available from GEC Plessey Semiconductors Sales Offices.

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