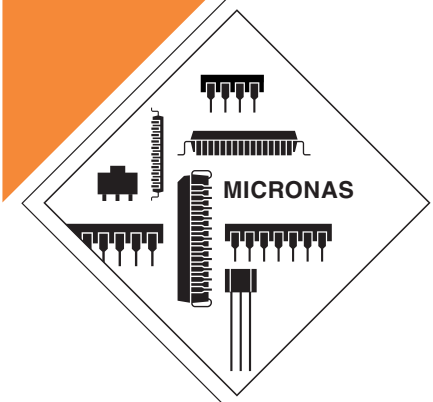

ADVANCE INFORMATION

UAC 3554B, UAC 3556B Universal Serial Bus (USB) Codecs

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MICRONAS

Contents

Page	Section	Title
4	**1.**	**Introduction**
4	1.1.	Features
6	**2.**	**Functional Description**
7	2.1.	General
7	2.2.	Hardware
7	2.2.1.	USB Interface
7	2.2.1.1.	Transceiver
7	2.2.1.2.	USB-Interface
7	2.2.2.	Audio Streaming Interface
7	2.2.3.	Generic USB Output
7	2.2.4.	Audio Control Interface
7	2.2.5.	I^2S Interface - Input/Output
7	2.2.6.	Power Supply
7	2.2.7.	Audio Processing Unit
8	2.3.	Analog Front-end and ADC
8	2.3.1.	Analog-to-Digital Converter
8	2.3.2.	Microphone and Line Input
8	2.3.3.	Analog Back-end
8	2.3.3.1.	Digital-to-Analog Converters
8	2.3.3.2.	Analog Filter
8	2.3.3.3.	Analog Volume
8	2.3.3.4.	Line-out/Headphone Amplifier
8	2.3.4.	General Purpose I/O
9	2.3.5.	Special I/O
9	2.3.5.1.	SOF (Start of Frame)
9	2.3.5.2.	SEN (Suspend Enable)
9	2.3.5.3.	SUSPEND
9	2.3.6.	Clock System
9	2.4.	Firmware
9	2.4.1.	USB Microcontroller Firmware
9	2.4.1.1.	Chapter 9 Functions
9	2.4.1.2.	Device and String Descriptor
9	2.4.1.3.	HID Report Descriptor
11	2.4.2.	Audio Processing Firmware
11	2.4.2.1.	Automatic Gain Control
11	2.4.2.2.	Quasi-Peak
11	2.4.2.3.	Bass Control
11	2.4.2.4.	Treble Control
12	2.4.2.5.	Parametric Equalizer
12	2.4.2.6.	Volume, Mute, and Balance Control
12	2.4.2.7.	Subwoofer Output and Bass Management
13	2.4.3.	Micronas Dynamic Bass (MDB)
13	2.4.3.1.	Dynamic Amplification
13	2.4.3.2.	Adding Harmonics

Contents, continued

Page	Section	Title
14	**3.**	**Specifications**
14	3.1.	Outline Dimensions
14	3.2.	Pin Connections and Short Descriptions
17	3.3.	Pin Descriptions
17	3.3.1.	Power Supply Pins
17	3.3.2.	Analog Audio Pins
18	3.3.3.	Interface Pins
18	3.3.4.	Other Pins
19	3.4.	Pin Configuration
20	3.5.	Pin Circuits
22	3.6.	Electrical Characteristics
22	3.6.1.	Absolute Maximum Ratings
23	3.6.2.	Recommended Operating Conditions
25	3.6.3.	Characteristics
31	**4.**	**UAC 3554B Applications**
31	4.1.	Recommended Low-Pass Filters for Analog Outputs
32	4.2.	Typical Application
34	**5.**	**Data Sheet History**

Universal Serial Bus (USB) Codecs

1. Introduction

The UAC 3554B is the base version of Micronas' new USB audio IC family. It contains the functionality of its predecessor – the Micronas USB Audio DAC UAC 3552A – plus an audio ADC, digital serial interfaces and an additional DAC channel for the subwoofer signal.

The high-performance audio ADC with direct microphone and line input makes the UAC 3554B the ideal solution for all kinds of USB codec applications. This includes the replacement of analog sound cards in PCs. Integrated headphone amplifiers allow direct headphone connection. Therefore, the IC can be employed as a single-chip headset solution without an extra power supply (bus-powered).

Apart from the standard audio processing such as volume, bass, and treble, the UAC 3554B offers a programmable 5-band parametric equalizer for correcting the frequency response of the applied speaker. Adjustable dynamic low-frequency processing for the subwoofer channel leads to a reduced number of external analog components. Internal sampling rate converters offer high flexibility in handling all sampling rates for USB upstream and downstream independently.

The codec functionality of the UAC 3554B is extended by additional interfaces, like I^2S, allowing all kinds of digital audio processing systems to be connected to the USB (e. g. Dolby Digital or MP3 decoding chips, such as DPL 4519G, MAS 3528E, or MAS 35x9F).

General-purpose inputs and outputs connect the UAC 3554B to peripheral hardware such as buttons, keyboards, LEDs etc. Via I^2C, more complex peripherals like LCD displays can be controlled; and the UAC 3554B itself can be remote-controlled via I^2C in non-USB environments.

All in all, the IC is designed as the ideal connecting matrix between USB, analog and digital audio input and output, home stereo, compressed audio, and all kinds of human interface devices. Many functions are adjustable to the customer's needs. Moreover, complete plug-in download functionality of the on-chip microcontroller turns the UAC 3554B into a customer-specific IC. Micronas supplies a standard ROM firmware based on the USB Composite Class, Audio Class, and HID Class.

Table 1–1: Members of the UAC 355xB Family

Version	Description
UAC 3556B	Universal Serial Bus (USB) Codec with standard ROM firmware and bootloader for 8-kByte firmware download
UAC 3554B	mask-programmed version

1.1. Features

- single-chip, USB specification 1.0/1.1 compliant, stereo audio A/D and D/A converter
- adaptive isochronous endpoints for downstream and upstream USB Audio
- supports 16-bit mono/stereo and 24-bit stereo for downstream (D/A converter)
- supports 8-bit mono and 16-bit mono/stereo, for upstream (A/D converter)
- generic ISO-downstream endpoint (Dolby Digital, MP3)
- USB programmable device and configuration descriptor
- bus-powered device
- remote wake-up
- 12 general-purpose I/O pins
- I^2S input/output interface
- independent adaptive sample rates of 6.4 to 48 kHz for USB upstream and downstream (enhanced full-duplex)
- audio baseband control: bass, treble, loudness, volume, balance, and mute
- dynamic bass boost
- digital speaker equalizer (5-band parametric equalizer)
- adjustable digital subwoofer filter
- THD better than 0.01% and SNR of typ. 96 dB for D/A converters
- THD better than 0.05% and SNR of typ. 92 dB for A/D converters
- integrated low-power stereo headphone amplifier
- subwoofer output
- I^2C interface (master/slave)
- downloadable plug-in code for the µController
- on-chip analog filters for out-of-band noise suppression

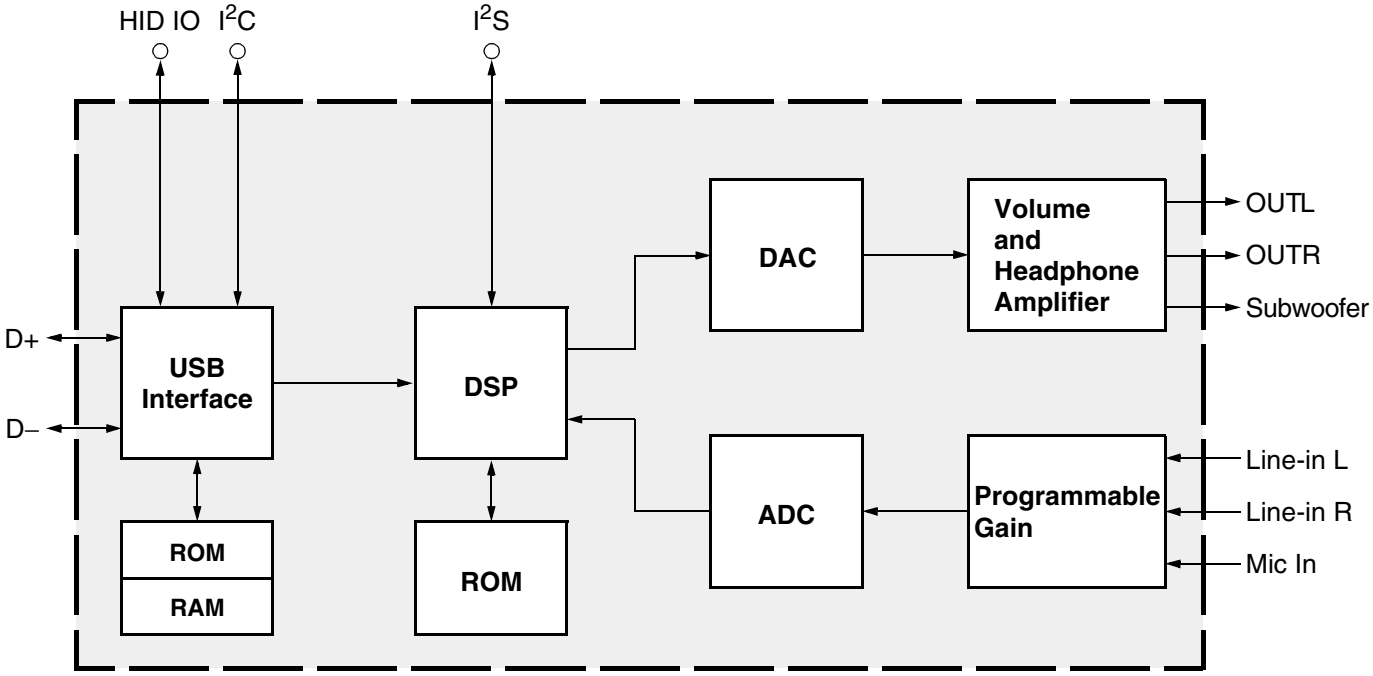

Fig. 1–1: Block diagram of the UAC 3554B

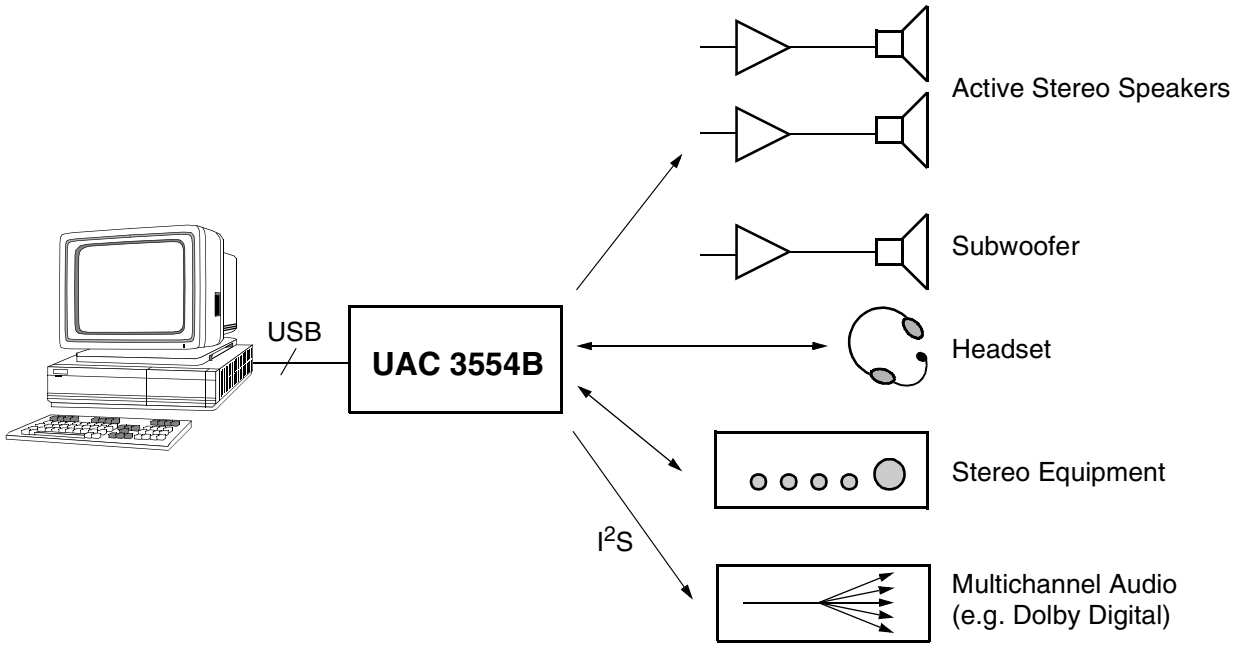

Fig. 1–2: System application diagram

2. Functional Description

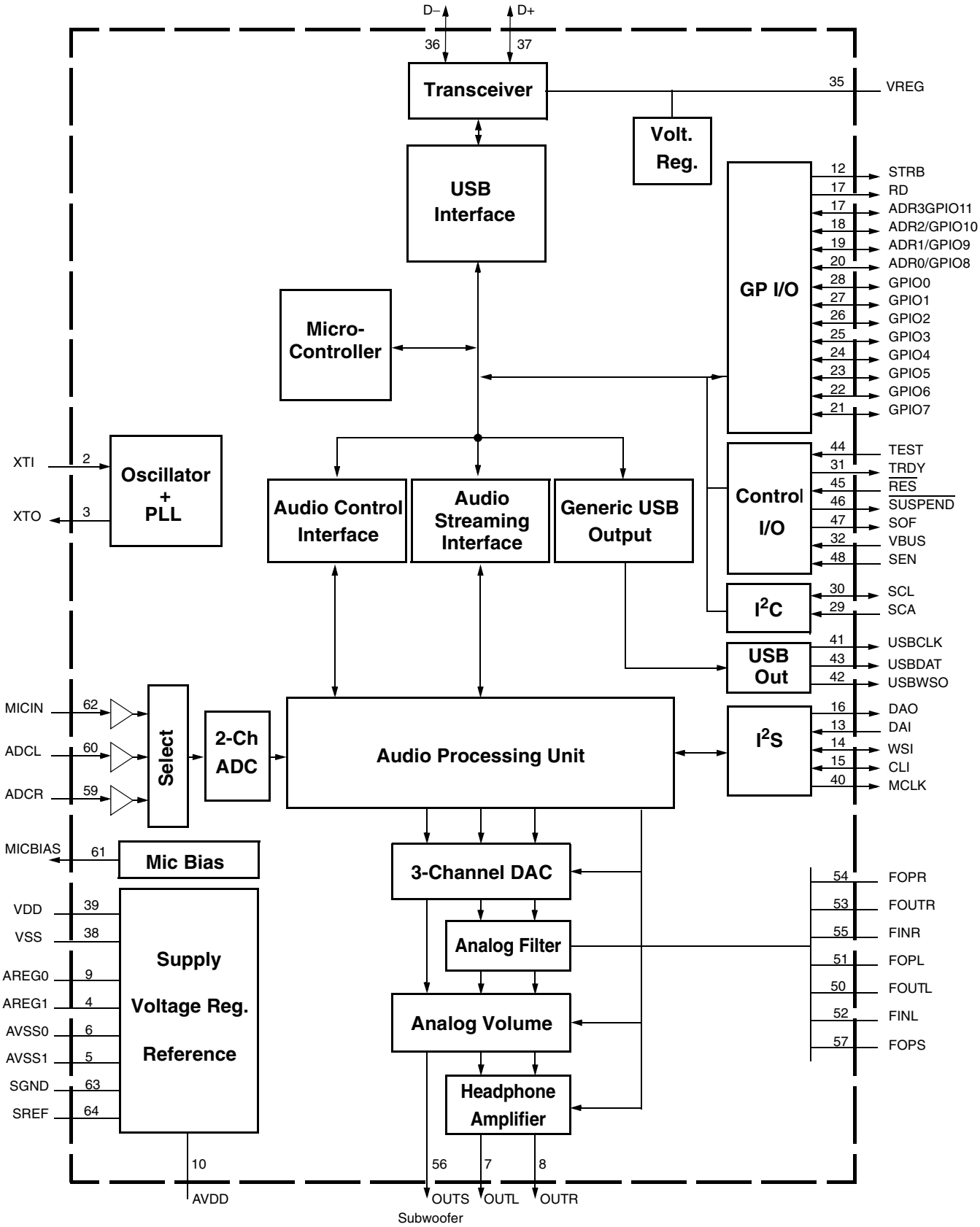

Fig. 2–1: Detailed block diagram of the UAC 3554B

2.1. General

The functionality of the UAC 3554B can be entirely controlled by any USB-operating system without any additional drivers.

However, the IC offers far more complexity if vendor-specific controlling or download code is used. With external I^2C controlling, the IC can even work as an audio codec in a non-USB environment.

The use of this extended functionality is not described in the standard data sheet and can be found in separate application notes.

2.2. Hardware

A detailed block diagram of the UAC 3554B is depicted in Fig. 2–1. The functions of the blocks are explained in the following sections.

2.2.1. USB Interface

2.2.1.1. Transceiver

The differential input transceiver is used to handle the USB data signal according to the full-speed (12 MB/s) USB driver characteristics (USB SPEC 1.1 - 7.1.4). This block is supplied by an internal voltage regulator. The internal pull-up resistor on the D+ line, indicating that the UAC 3554B is connected to the USB bus, can be switched on and off by firmware.

2.2.1.2. USB-Interface

The USB interface consists of a Serial Interface Engine (SIE) and a microcontroller. The SIE does all the low level USB-protocol handling, like NRZI coding, bit stuffing and CRC-computation. A receiver/transceiver logic handles the data traffic between the USB-data to and from the microcontroller memory. The microcontroller does the Chapter-9 processing and the decoding of class- and vendor-specific USB requests.

A part of the memory is reserved for download software. This allows adding extra functionality to the GPIO pins, like control of external components via USB. Downloading is handled by an extra driver which allows direct RAM/ROM access via USB or from an external I^2C EEPROM.

2.2.2. Audio Streaming Interface

The audio streaming interface directly connects the SIE to the DSP in order to transmit the digital audio data in both directions.

2.2.3. Generic USB Output

This interface provides a generic 'isochronous' downstream endpoint for sending audio signals to peripheral ICs like Micronas' Dolby Digital decoder MAS 3528E or to an MP3 decoder, e.g. the MAS 3507D or MAS 3509F. This works independently from the main downstream endpoint. The audio format on the USB-OUT pins is burst I^2S.

2.2.4. Audio Control Interface

The Audio Control Interface links the microcontroller to the DSP and is used to initialize the DSP and to transmit audio-related USB control data, like volume setting, tone control etc.

The Audio Control Interface supports full access to all DSP registers from the microcontroller and I^2C.

2.2.5. I^2S Interface - Input/Output

The I^2S output interface operates in master mode at a fixed sampling rate of 48 kHz. The master clock is programmable to 18.432 MHz and 24.576 MHz.

The I^2S input interface operates in slave mode at sample rates from 6.4kHz to 48kHz.

Both interfaces support standard and inverted word strobes.

2.2.6. Power Supply

The UAC 3554B has three on-chip-voltage-regulators providing the optimal supply voltage for the analog and digital sections, thus allowing to power the IC by the USB-Bus supply lines, as well, as from external supply. They also serve to reduce cross-talk and EMI.

For stable operation, all three regulators need an external capacitor connected from the output to ground.

If a higher output level is required, the IC can operate in 5-V modus. In this case, the IC is powered from an external 5-V supply: AVDD has to be connected to AREG0 and AREG1 and SREF must be switched to 5-V mode.

2.2.7. Audio Processing Unit

The audio processing unit is a powerful DSP core which allows baseband audio processing as well, as customized algorithms. For more details on the software see Section 2.4.2. “Audio Processing Firmware” on page 11.

2.3. Analog Front-end and ADC

2.3.1. Analog-to-Digital Converter

The A/D converter achieves a signal-to-noise ratio of 90 dB (typ.) and a bandwidth of 20 kHz (at f_s=48 kHz).

2.3.2. Microphone and Line Input

The input gain of the microphone input is programmable in the range of 0 dB to +22.5 dB.
The input gain for the line input is programmable in the range of −3 dB to 19.5 dB.

Switching between microphone and line input affects the left channel only. The right channel is always connected to the ADC.

The microphone bias is automatically switched on when the microphone input is selected.

2.3.3. Analog Back-end

The analog back-end comprises the stereo audio DAC, the subwoofer DAC, analog filters, input mixer, op amps for optimal external postfiltering, analog volume and mute, and the output amplifiers for stereo speakers plus subwoofer.

2.3.3.1. Digital-to-Analog Converters

Micronas' unique multibit sigma-delta DACs convert the audio data with high linearity and a superior S/N.

2.3.3.2. Analog Filter

This block contains the active components for the optional analog postfilters. It is recommended to use a second-order filter (see Section 4. "UAC 3554B Applications" on page 31) in order to attenuate the out-of-band noise caused by the sigma delta DACs.

2.3.3.3. Analog Volume

Volume control covers a range from 0 dB to −114 dB with 1 dB step size and additional mute position. It is split into a digital and an analog volume system. This ensures that the DAC performance parameters do not degrade at reduced volume settings.

2.3.3.4. Line-out/Headphone Amplifier

The line-out/headphone amplifier output is provided at the OUTL and OUTR pins connected either to stereo headphones or to the power amplifier within an USB speaker. The stereo headphones require external serial resistors in both channels. See Section 4. "UAC 3554B Applications" on page 31.

An extended output power range is possible if the application does not require stereo output. In this mode the two output pins operate in bridge mode with complementary signals. This mode is useful for mono headset applications.

2.3.4. General Purpose I/O

The Micronas firmware uses the GPIO pins to connect keys, which are related to the USB HID class or for vendor-specific control functions and LEDs in order to indicate on/off states for example. The standard configuration defines the GPIO0...GPIO3 as input pins for the audio control shown in Table 2–1.

Table 2–1: Standard Key Configuration

Pin	Function
GPIO0	Volume Up
GPIO1	Volume Down
GPIO2	MuteToggle
GPIO3	BassBoost Toggle

The keys are polled by the microcontroller and the corresponding key codes are transmitted to the host on request.

The output pins are not predefined and therefore not related to any USB functions. They can be set or reset by vendor-specific software or downloadable plug-in code.

The default HID functionality can be switched off and then the functions of the 12 GPIO pins can be defined by a vendor-specific driver or download code. Each pin can be configured as input or output pin with programmable pull-down resistor and low or high driving current.

2.3.5. Special I/O

2.3.5.1. SOF (Start of Frame)

The SOF pin provides a 1-ms signal which is synchronous to the USB 1-ms frame rate. It can be used for test purpose or as an USB-synchronous reference for vendor-specific external circuitry.

2.3.5.2. SEN (Suspend Enable)

This is a digital input that prevents the device from entering the low-power mode which can be requested by the host PC or by disconnecting the device from the USB. The SEN pin is also used as an input for the remote wake-up function.

SEN	
high	suspend enabled
low	suspend disabled

2.3.5.3. SUSPEND

The SUSPEND pin is a digital output pin that indicates the low-power mode. It can be used to power down external circuitry, like power amplifiers in an USB speaker.

Table 2–2: SUSPEND pin

SUSPEND	
high	normal power
low	low power

2.3.6. Clock System

The UAC 3554B requires a 12-MHz clock source, which is realized as an on-chip oscillator with external crystal. Also an external oscillator can be used. In this case, the clock has to be connected to XTI. The 12 MHz is the input clock for a PLL circuit which generates all clocks needed within the IC.

2.4. Firmware

The functionality of the UAC 3554B is mainly defined by firmware. The internal µ-controller handles the USB requests whereas the Audio Processing Unit processes the sound features.

2.4.1. USB Microcontroller Firmware

2.4.1.1. Chapter 9 Functions

The chapter 9 of the USB Spec 1.1 defines the USB device framework which is the middle layer of the USB protocol hierarchy (see USB Spec 1.1 page 175). It handles routing data between the bus interface and various endpoints. The endpoint is a source or sink for data within the device.

2.4.1.2. Device and String Descriptor

This is part of the firmware and provides manufacturer and product-related information to the host computer during the enumeration procedure. This comprises:

– vendor ID

– product ID

– device release number

– manufacturer string

– product string

– serial number string

These descriptors are stored in ROM. If any vendor-specific information is required here, an external I^2C-EEPROM can be used to store this data.

The UAC 3554B is shipped with the Micronas device descriptor and allows complete USB functionality.

2.4.1.3. HID Report Descriptor

The HID report descriptor defines the functionality of the GPIO Pins. The basic information here are the usage IDs for the key inputs.

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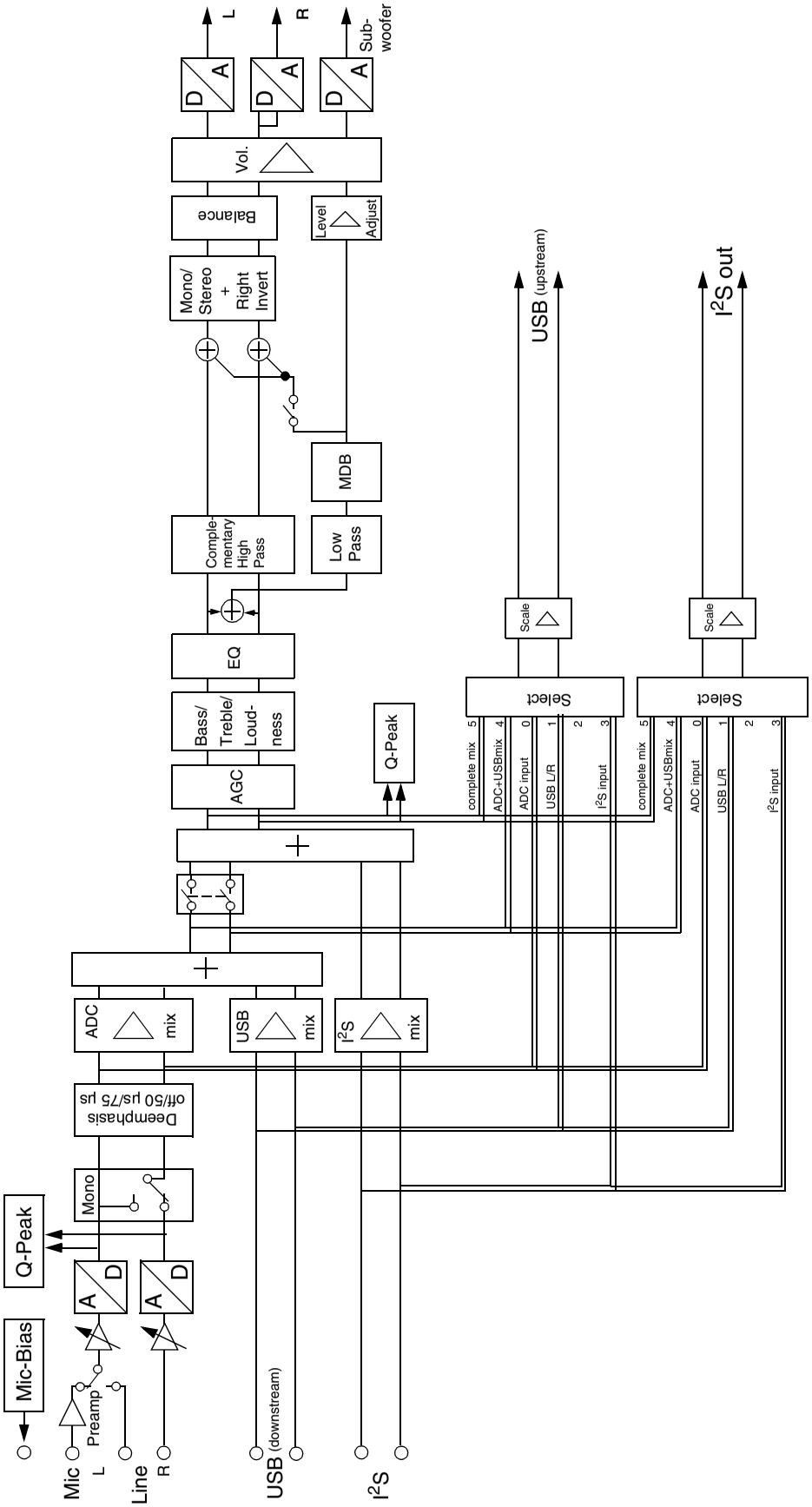

Fig. 2–2: Audio processing

2.4.2. Audio Processing Firmware

All audio processing is realized by DSP firmware. The audio building blocks can be split into USB-independent features such as parametric equalizer, I^2S I/O, and blocks which belong to USB feature units, mixer units, and selection units defined in the USB Device Class Definition for Audio Devices.

The USB unit provides basic manipulation of the incoming logical channels and can be controlled by the standard windows mixer tool or in a more efficient way by the Micronas mixer tool. The USB-independent features are predefined in the internal ROM, an external EEPROM or the host device driver.

The UAC 3554B supports two logical channels (i.e. left and right). Multichannel or surround systems, however, can also be realized using more than one UAC 3554B, because phase or delay distortion is eliminated in the device by locking the audio processing to the USB frame rate. An overview of the architecture is given in Fig. 2–2.

2.4.2.1. Automatic Gain Control

The Automatic Gain Control (AGC) is one of the building blocks of the feature unit (USB Device Class Definition for Audio Devices 1.0, page 39).

Different sound sources fairly often do not have the same volume level. The Automatic Gain Control solves this problem by equalizing the volume levels within a defined range. Below a threshold level the signals are not affected. The level-adjustment is performed with time constants in order to avoid short-time adjustments due to signal peaks.

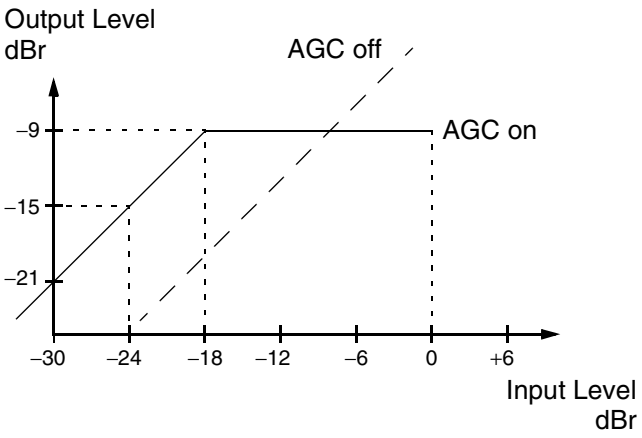

Fig. 2–3: Simplified AGC characteristics

Table 2–3: AGC parameters

Parameter	Settings	Default if enabled
Decay time	8 sec 4 sec 2 sec 20 ms	4 sec

2.4.2.2. Quasi-Peak

Two quasi-peak detectors are provided:

1. behind the ADCs. This allows the programming of an AGC in the µ-controller or a VU-meter on the host side.

2. in the DAC channel. This can be used e.g. for a VU-meter on the host side.

The feature is based on the following time constants:

attack time: 1.3 ms
decay time: 37 ms

2.4.2.3. Bass Control

The bass control provides gain or attenuation to frequency components below a corner frequency of 120 Hz. The bass control works identically on both channels in a range of −12 to +12 dB.

2.4.2.4. Treble Control

The treble control provides gain or attenuation to frequency components above a corner frequency of 6 kHz. The treble control works identically on both channels in a range of −12 to +12 dB.

2.4.2.5. Parametric Equalizer

The parametric equalizer is an audio feature that is not accessed via standard USB controls. It allows the compensation of the frequency response of a speaker. Alternatively, frequency responses can be set to suit individual tastes. The equalizer consists of 5 individually adjustable bands. The control parameters and the parameter range for each band is shown in Table 2–4.

Table 2–4: Equalizer parameters

Parameter	Min	Max
Center Frequency	50 Hz	15 kHz
Gain/Attenuation	–6 dB	+6 dB
Filter Quality (Q)	0.5	3

The adjustment of the equalizer is supported by an application program that allows to set up frequency responses and to download the corresponding filter coefficients into the UAC 3554B. When the frequency response matches the requirements, it can be programmed into the external EEPROM or can be set by a vendor specific device driver. The UAC 3554B is shipped with a flat frequency response.

2.4.2.6. Volume, Mute, and Balance Control

The volume control is partly realized in the analog back-end. This preserves high audio quality (SNR) at low volume settings because signal and noise are attenuated in the same way. This is not the case for pure digital volume control. The UAC 3554B uses digital volume control only for the fine tuning. The volume setting is smoothed by an internal ramping algorithm in order to avoid audible clicks during volume change. The splitting between analog and digital volume is handled by the UAC 3554B automatically.

The balance is implemented digitally by attenuating one channel.

The mute control is part of the volume system in the UAC 3554B. It functions simultaneously on both channels and can be switched on and off under USB control. Similar to the volume control, clicks are avoided by a ramping algorithm.

2.4.2.7. Subwoofer Output and Bass Management

The subwoofer signal is created by combining the left and the right channels directly behind the equalizer block using the formula (L+R)/2. Due to division by 2, the D/A converter will not be overloaded, even with full scale input signals. The subwoofer is filtered by a third-order low-pass filter with programmable corner frequency and programmable characteristic followed by a level adjustment. At the main channels a complementary high-pass filter can be switched on. Subwoofer and main output use the same volume.

Please note, that the predefined subwoofer parameters in the internal ROM are set in such a way, that the low frequencies of both channels are summed up and are distributed equally to left and right channel. This reduces the risk of overload of the speakers, but degrades the channel separation for low frequencies. Since the human perception cannot extract information about direction from low frequencies, this is no drawback. In addition this method allows a click-free enable and disable of the bass boost (MDB).

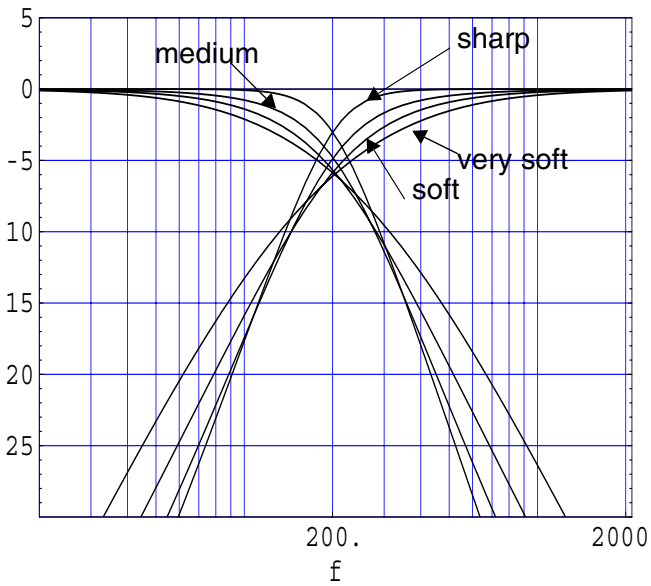

Fig. 2–4: Subwoofer characteristics (e.g. f_c = 200 Hz)

Table 2–5: Subwoofer parameters

Parameter	Settings/ Range	Default
Corner Freq.	50 ... 400 Hz	90 Hz
Characteristic	-sharp edge -medium edge -soft edge -very soft edge	sharp edge
Complementary High-Pass Filter for L/R channel	-L/R unfiltered -L/R high-pass filtered -Subw. added to high-pass filtered L/R	Subw. added to high-pass filtered L/R

Table 2–5: Subwoofer parameters, continued

Parameter	Settings/ Range	Default
Level Adjustment	–60 ... +12 dB (relative to main volume)	0 dB
Subw. DAC	-off -on	on

2.4.3. Micronas Dynamic Bass (MDB)

The **M**icronas **D**ynamic **B**ass algorithm (MDB) implements a sophisticated bass boost system, which extends the frequency range of loudspeakers or headphones.

The MDB is placed in the subwoofer path. For applications without a subwoofer, the enhanced bass signal can be added back onto the left/right channels. Micronas Dynamic Bass combines two effects: dynamic amplification and adding harmonics.

Several parameters allow tuning the characteristics of MDB according to the loudspeaker, the cabinet, and personal preferences. For more detailed information on how to set up MDB, Micronas will provide an appropriate Application Note.

Table 2–6: MDB parameters

Parameter	Range	Default if disabled	Default if enabled
Effect Strength	off ... max	off	medium
Harmonic Content	0 .. 100%	0%	50%
Center Frequency	20 ... 300 Hz	90 Hz	90 Hz
Amplitude Limit	-32 .. 0 dBFS	0 dBFS (=no limit)	0 dBFS (=no limit)
Subwoofer Settings	two sets for MDB off/on available, for parameters see Table 2–5		

2.4.3.1. Dynamic Amplification

Since the human impression of loudness depends on the frequency, a dynamic compression of the low frequencies adapts the sound to the human perception.

In order to prevent clipping and to adapt the system to the signal amplitude which is really present at the output of the device, the MDB contains a definable limit. The output signal amplitude is monitored and if it comes close to the limit, the gain is reduced automatically. Clipping effects are avoided.

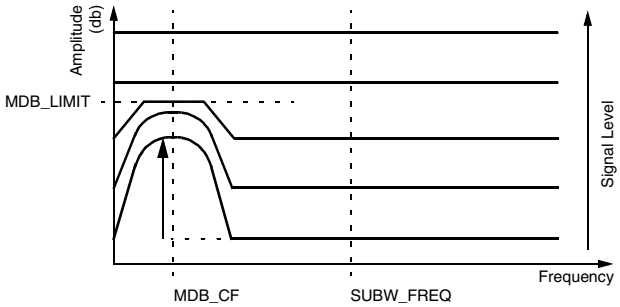

Fig. 2–5: Dynamic amplification

2.4.3.2. Adding Harmonics

MDB exploits the psychoacoustic phenomenon of the ‘missing fundamental’. Adding harmonics of the frequency components below the cutoff frequency gives the impression of actually hearing the low frequency fundamental. In other words: Although the loudspeaker system is not capable of generating such low frequencies, the listener has the impression that it reproduces them.

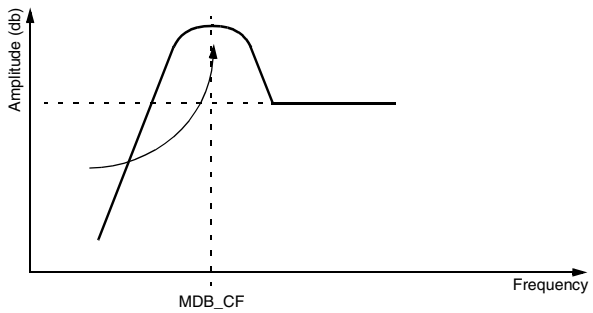

Fig. 2–6: Adding harmonics

3. Specifications

3.1. Outline Dimensions

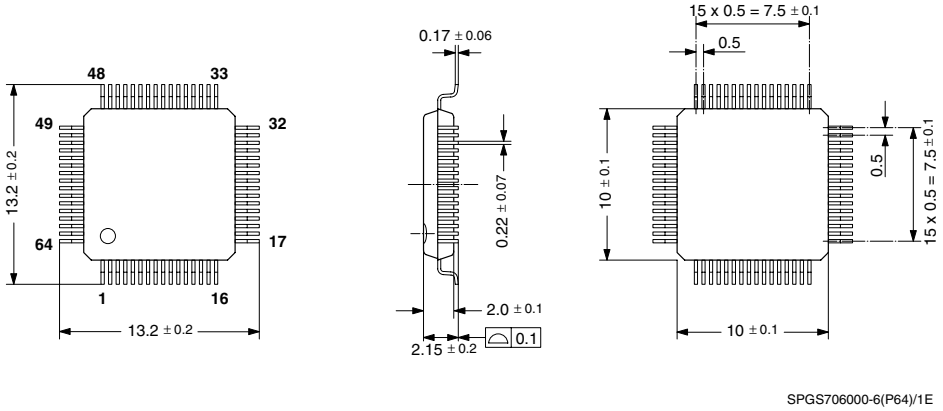

Fig. 3–1:
64-Pin Plastic Metric Quad Flat Pack
(PMQFP64)
Weight approximately 0.4 g
Dimensions in mm

3.2. Pin Connections and Short Descriptions

NC = not connected, leave vacant
LV = if not used, leave vacant
VSS = if not used, connect to VSS

X = obligatory; connect as described in circuit diagram
VDD = connect to VDD

Pin No.	Pin Name	Type	Connection (If not used)	Short Description
1	NC		LV	Not Connected
2	XTI	IN	X	Quartz Oscillator Pin 1
3	XTO	OUT	X	Quartz Oscillator Pin 2
4	AREG1	OUT	X	Regulator Output for analog parts except amplifiers
5	AVSS1	IN	X	VSS 1 for analog parts except amplifiers
6	AVSS0	IN	X	VSS 0 for audio output amplifiers
7	OUTL	OUT	LV	Audio Output: headphone left / speaker Left
8	OUTR	OUT	LV	Audio Output: headphone right /speaker Right
9	AREG0	OUT	X	Regulator Output for audio output amplifiers
10	AVDD	IN	X	analog VDD
11	RD	OUT	LV	GPIO Read
12	STRB	OUT	LV	GPIO Strobe
13	DAI	IN	VSS	I^2S Data Input
14	WSI	IN/OUT	VSS	I^2S Word Strobe

Pin No.	Pin Name	Type	Connection (If not used)	Short Description
15	CLI	IN/OUT	VSS	I^2S Bit Clock
16	DAO	OUT	LV	I^2S Data Output
17	ADR3/GPIO 11	IN	VSS	HID IO 11
18	ADR2/GPIO 10	IN	VSS	HID IO 10
19	ADR1/GPIO 9	IN	VSS	HID IO 9
20	ADR0/GPIO 8	IN	VSS	HID IO 8
21	GPIO 7	IN	VSS	HID IO 7
22	GPIO 6	IN	VSS	HID IO 6
23	GPIO 5	IN	VSS	HID IO 5
24	GPIO 4	IN	VSS	HID IO 4
25	GPIO 3	IN	VSS	HID IO 3
26	GPIO 2	IN	VSS	HID IO 2
27	GPIO 1	IN	VSS	HID IO 1
28	GPIO 0	IN	VSS	HID IO 0
29	SDA	IN/OUT	LV	I^2C Data
30	SCL	IN/OUT	LV	I^2C Clock
31	TRDY	OUT	LV	Test Output Pin
32	VBUS	IN	X	Sense USB Bus
33	NC		LV	Not Connected
34	NC		LV	Not Connected
35	VREG	OUT	X	Capacitor for internal supply
36	DMINUS	IN/OUT	X	USB DATA MINUS
37	DPLUS	IN/OUT	X	USB DATA PLUS
38	VSS	IN	X	Digital VSS
39	VDD	IN	X	Digital VDD
40	MCLK	OUT	LV	I^2S Master Clock (384 x 48 kHz)
41	USBCLK	OUT	LV	Direct ISO-Endpoint Output Clock
42	USBWSO	OUT	LV	Direct ISO-Endpoint Output Word Strobe
43	USBDAT	OUT	LV	Direct ISO-Endpoint Output Data
44	TEST	IN	VSS	Test Enable
45	$\overline{\text{RES}}$	IN	VDD	Power On Reset, active low
46	$\overline{\text{SUSPEND}}$	OUT	LV	Low-Power Mode Indicator

Pin No.	Pin Name	Type	Connection (If not used)	Short Description
47	SOF	OUT	LV	1-ms Start-Of-Frame Signal
48	SEN	IN	VSS	Suspend Enable
49	NC		LV	Not Connected
50	FOUTL	OUT	X	Output to left external filter
51	FOPL	IN/OUT	X	Filter Op Amp Inverting Input, left
52	FINL	IN/OUT	X	Input for FiltoutL
53	FOUTR	OUT	X	Output to right filter op amp
54	FOPR	IN/OUT	X	Right Filter op amp inverting input
55	FINR	IN/OUT	X	Input for FILTOUTR
56	OUTS	OUT	LV	Analog Output Subwoofer
57	FOPS	OUT	X	Output to Subwoofer external filter
58	NC		LV	Not Connected
59	ADCR	IN	VSS	Line Input Right
60	ADCL	IN	VSS	Line Input Left
61	MICBIAS	OUT	X	Supply Voltage for Microphone
62	MICIN	IN	VSS	Microphone Input
63	SGND	IN	X	Signal Reference Ground
64	SREF	IN/OUT	X	Signal Reference voltage

3.3. Pin Descriptions

3.3.1. Power Supply Pins

The UAC 3554B combines various analog and digital functions which may be used in different modes. For optimized performance, major parts have their own power supply pins. All VSS power supply pins must be connected.

VDD (39)
VSS (38)
The VDD and VSS power supply pair are connected internally with all digital parts of the UAC 3554B**.**

AVDD (10)
AVDD is the supply pin for the voltage regulators at AREG0(9) and AREG1(4).

AVSS0 (6)
AVSS0 is the ground connection for the headphone/ loudspeaker amplifier.

AVSS1 (5)
AVSS1 is the ground connection for the analog audio processing parts, except the headphone/loudspeaker amplifiers.

SREF (64)
Reference for analog audio signals. This pin is used as reference for the internal op amps. This pin must be blocked against SGND with a 3.3-µF capacitor.

Note: The pin has a typical DC level of 1.725 V. It can be used as reference input for external op amps when no current load is applied.

SGND (63)
Reference ground for the internal band-gap and biasing circuits. This pin should be connected to a clean ground potential. Any external distortions on this pin will affect the analog performance of the UAC 3554B.

AREG0 (9)
Voltage regulator output for headphone/loudspeaker amplifiers supply. Connect an external ceramic capacitor to stabilize the regulator output.

AREG1 (4)
Voltage regulator output for analog audio processing parts supply, except the headphone/loudspeaker amplifiers. Connect an external ceramic capacitor to stabilize the regulator output.

3.3.2. Analog Audio Pins

FOUTL (50)
FOPL (51)
FINL (52)
FOUTR (53)
FOPR (54)
FINR (55)
FOPS (57)
Filter op amps are provided in the analog baseband signal paths. These inverting op amps are freely accessible for external use by these pins.

The FOUTL/R pins are connected with the buffered output of the internal switch matrix. The FOPL/R pins are directly connected with the inputs of the inverting filter op amps. The FINL/R pins are connected to the outputs of the op amps.

ADCL (60)
ADCR (59)
Line Input pins

MICIN (62)
MICBIAS (61)
Microphone input pin and microphone power supply pin

OUTL (7)
OUTR (8)
OUTS (56)
These pins are connected to the internal output amplifiers. OUTL/R can be used for either line-out or stereo headphones. OUTS is the subwoofer output.

Caution: A short circuit at these pins for more than a momentary period may result in destruction of the internal circuits.

3.3.3. Interface Pins

DMINUS (36)
DPLUS (37)
Differential USB port pins. The DPLUS pin has an internal switchable pull-up resistor. Both pins must be connected to the USB bus via a series resistor.

VBUS (32)
Sense USB Bus

USBCLK (41)
Direct ISO Endpoint Output Clock

USBWSO (42)
Direct ISO Endpoint Word Strobe

USBDAT (43)
Direct ISO Endpoint Output Data

CLI (15)
Clock line for the I^2S bus. In master mode, this line is driven by the UAC 3554B; in slave mode, an external I^2S clock has to be supplied.

DAO (16)
Output of digital serial sound data of the UAC 3554B on the I^2S bus.

DAI (13)
Input of digital serial sound data to the UAC 355xB via I^2S bus.

WSI (14)
Word strobe line for the I^2S bus. In master mode, this line is driven by the UAC 355xB; in slave mode, an external I^2S word strobe has to be supplied.

MCLK (40)
I^2S master clock pin.

SCA (29)
Via this pin, the I^2C bus data is written to or read from the UAC 355xB.

SCL(30)
Via this pin, the I^2C bus clock signal has to be supplied.

3.3.4. Other Pins

XTI (2)
XTO (3)
The XTI pin is connected to the input of the internal crystal oscillator; the XTO pin to its output. Both pins should be directly connected to the crystal and two ground-connected capacitors (see application diagram).

SEN (48)
Digital input that prevents the device from entering the low-power mode. This pin is also used to signal remote wake-up

TEST (44)
Test enable. This pin is for test purposes only and must always be connected to VSS.

VREG (35)
Voltage regulator output for USB transceiver supply. Connect an external ceramic capacitor to stabilize the regulator output.

$\overline{\text{RES}}$ (45)
A Low signal at this pin resets the chip.

GPIO 0 ... ADR/GPIO 11
(28, 27, 26, 25, 24, 23, 22, 21, 20, 19, 18, 17)
These pins are configurable to be either input or output and can be used to connect audio function keys or signalling LEDs.

RD (11)
GPIO read pin

STRB (12)
GPIO strobe pin

$\overline{\text{SUSPEND}}$ (46)
This pin indicates that the host PC sets the USB bus to the suspend mode state.

SOF(47)
Start of Frame Signal. 1-ms signal that can be used for external application circuits.

TRDY (31)
Test Output Pin. This pin is intended for test purposes only and must not be connected.

3.4. Pin Configuration

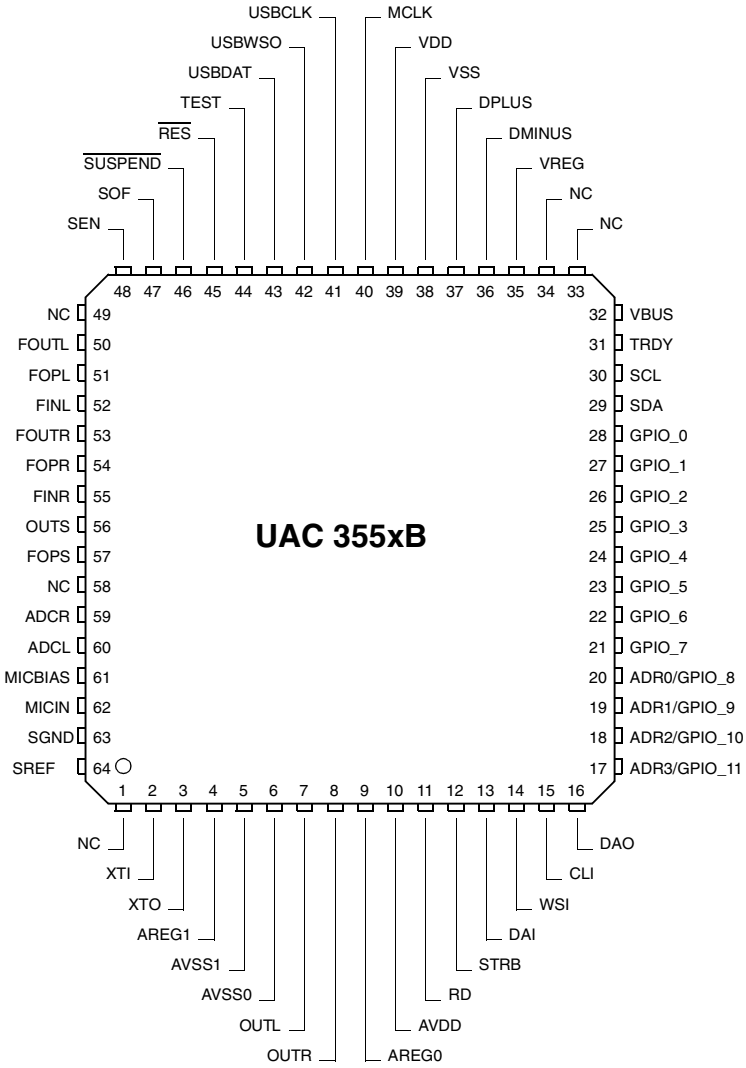

Fig. 3–2: PMQFP64 package

3.5. Pin Circuits

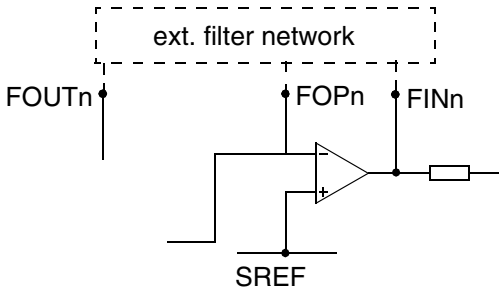

Fig. 3–3: Pins FINR, FOPR, FINL, FOPL

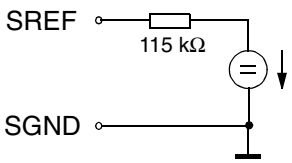

Fig. 3–4: Pins SREF, SGND

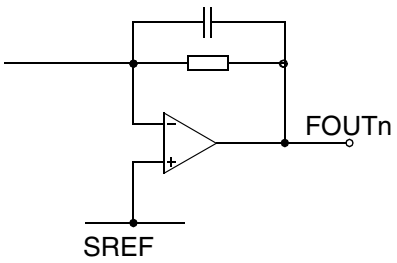

Fig. 3–5: Output Pins FOUTL, FOUTR

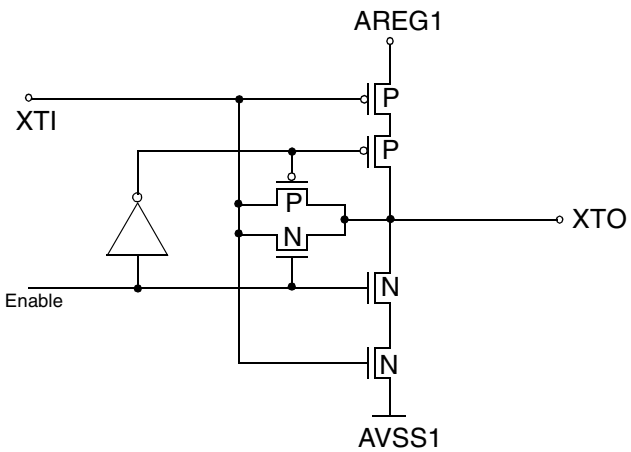

Fig. 3–6: Clock oscillator XTI, XTO

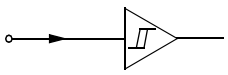

Fig. 3–7: Input Pins $\overline{\text{RES}}$, TEST, SEN, DAI

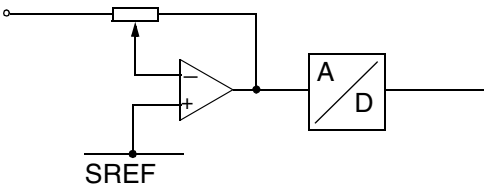

Fig. 3–8: Analog input pins MIC, MICBIAS, ADCL, ADCR

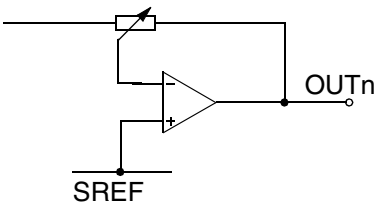

Fig. 3–9: Output Pins OUTL, OUTR

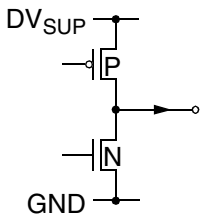

Fig. 3–10: Digital Output Pins SOF, $\overline{\text{SUSPEND}}$, TRDY

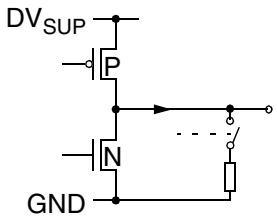

Fig. 3–11: Digital Output Pins MCLK, RD, STRB, DAO

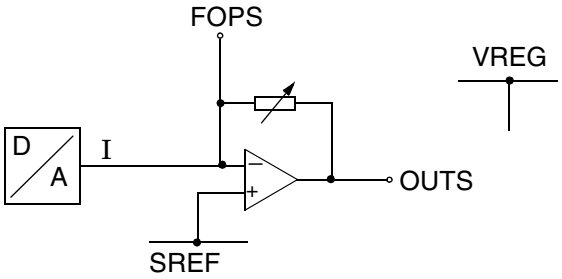

Fig. 3–12: Subwoofer Output Pin OUTS and Output to Subwoofer External Filter FOPS

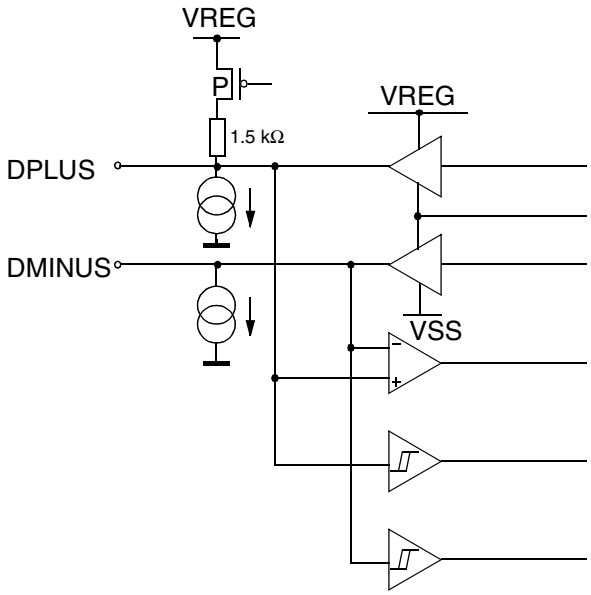

Fig. 3–13: Digital Input/Output Pins DMINUS, DPLUS

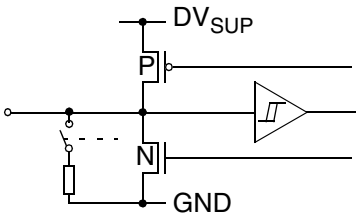

Fig. 3–14: Input/Output Pins GPIO0...GPIO11, WSI, CLI, USBCLK, USBWSO, USBDAT

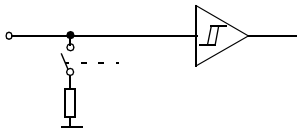

Fig. 3–15: Input Pin VBUS

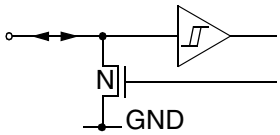

Fig. 3–16: Input/Output Pins SDA, SCL

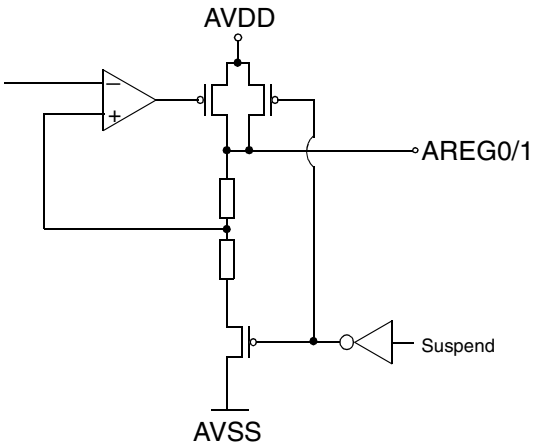

Fig. 3–17: Analog Voltage Supply Pins AVDD, AVSS, AREG0/1

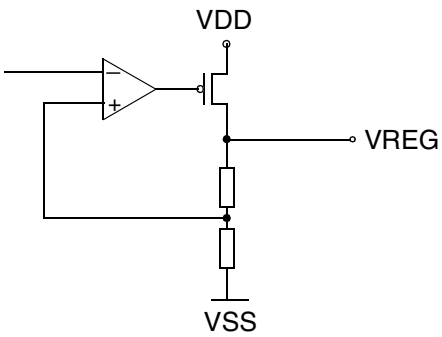

Fig. 3–18: Digital Voltage Supply Pins VDD, VSS, VREG

3.6. Electrical Characteristics

3.6.1. Absolute Maximum Ratings

Symbol	Parameter	Pin Name	Min.	Max.	Unit
T_A	Ambient Operating Temperature		0	70	°C
T_S	Storage Temperature		–40	125	°C
P_{Pmax}	Power Dissipation		–	650	mW
V_{SUPA}	Analog Supply Voltage[1)]	AVDD	–0.3	6	V
V_{SUPA}	Analog Supply Voltage[2)]	AVDD, AREG0/1	–0.3	6	V
V_{SUPD}	Digital Supply Voltage	VDD	–0.3	6	V
V_{Idig}	Input Voltage, all digital inputs		–0.3	V_{SUPD} + 0.3	V
I_{Idig}	Input Current, all digital inputs		–20	+20	mA
I_{Odig}	Output Current, all digital outputs		–50	+50	mA
V_{Iana}	Input Voltage, all analog inputs		–0.3	$V_{VAREG0/1}$+ 0.3	V
I_{Iana}	Input Current, all analog inputs		–5	+5	mA
I_{Oaudio}	Output Current, audio output[3)]	OUTL/R	–0.2	0.2	A
I_{AREG0}	Output Current, analog regulator	AREG0	–500	+20	mA[4)]
I_{AREG1}	Output Current, analog regulator	AREG1	–50	+20	mA[4)]

1) Internal regulators used
2) If internal regulators are not used, connect AVDD to AREG0/1.
3) These pins are **not** short-circuit proof!
4) Positive value means current flowing into the circuit

Stresses beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operating Conditions/Characteristics” of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

3.6.2. Recommended Operating Conditions

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
Temperature Ranges and Supply Voltages						
T_A	Ambient Temperature Range		0		70	°C
V_{SUPA}	Analog Audio Supply Voltage	AVDD	4.1	5.0	5.6	V
C_{SUPA}	Capacitor at analog supply pins to ground	AVDD		220		nF
V_{SUPD}	Digital Supply Voltage	VDD	4.1	5.0	5.6	V
C_{SUPD}	Capacitor at digital supply pin to ground	VDD		100		nF
C_{SUPUSB}	Capacitor at VBUS pin to ground	VBUS		22		pF
Analog Reference						
C_{SREF1}	Analog Reference Capacitor	SREF	1	3.3		µF
C_{SREF2}	Ceramic Capacitor in parallel	SREF		100		nF
Analog Audio Inputs						
C_{inAD}	DC-Decoupling Capacitor at A/D converter inputs	ADCL/R		390		nF
C_{inMI}	DC-Decoupling Capacitor at microphone input	MICIN		100		nF
Analog Audio Filter Inputs and Outputs						
Z_{AFLO}	Analog Filter Load Output[1)]	FOUTL/R	7.5		6	kΩ pF
Z_{AFLI}	Analog Filter Load Input[1)]	FINL/R	5.0		7.5	kΩ pF
$C_{FILTSUBW}$	Filter Capacitor for Subwoofer output	FOPS		2.2		nF
Analog Audio Outputs						
Z_{AOL_HP}	Output Load HP (22-Ω Series Resistor required)	OUTL/R	16	32 100		Ω pF
$Z_{AOLSUBW}$	Output load subwoofer DC-decoupling capacitor at sub-woofer output	OUTS	10	 470		kΩ nF
[1)] Please refer to Section 4.1. “Recommended Low-Pass Filters for Analog Outputs” on page 31						

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
Crystal Characteristics						
T_{AC}	Ambient Temperature Range		0		70	°C
F_P	Load Resonance Frequency at C_l = 20 pF	XTI		12		MHz
V_{ACLK}	Clock Amplitude	XTI, XTO	0.5		V_{REG1} –0.5	V_{PP}
$\Delta F/F_s$	Accuracy of Adjustment		–250		250	ppm
$\Delta F/F_s$	Frequency Variation versus Temperature		–250		250	ppm
R_{EQ}	Equivalent Series Resistance			12	30	Ω
C_0	Shunt (parallel) Capacitance			3	5	pF
Voltage Regulator						
C_{VREG}	Voltage Regulator Capacitor (ceramic, X7R)	VREG	330	1000		nF
C_{AREG0}	Voltage Regulator Capacitor (ceramic, X7R)	AREG0	330	470	600	nF
C_{AREG1}	Voltage Regulator Capacitor (ceramic, X7R)	AREG1	150	220	270	nF
Transceiver						
R_{USB}	Input Series Resistance	DPLUS/ DMINUS		24 (±5%)		Ω

3.6.3. Characteristics

At T_A = 0 to 70 °C, V_{SUPD} = 4.1 V to 5.6 V, V_{SUPA} = 4.1 V to 5.6 V. Typical values at T_A = 20 °C, V_{SUPD} = V_{SUPA} = 5.0 V, quartz frequency = 12 MHz, duty cycle = 50%, bass/treble: 0 dB, **M**icronas **D**ynamic **B**ass: off, AGC: off, equalizer: off (positive current flowing into the IC), 3-V Mode if not otherwise specified.

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Digital Supply							
I_{VDD}	Current Consumption[1)]	VDD		41 53		mA	reduced feature set full feature set
Digital Input Pin – Leakage							
I_I	Input Leakage Current	GPIO[11:0], AUXEN, RES			±1	µA	$V_{GND} \le V_I \le V_{SUP}$
Digital Output Pin							
V_{OH}	Output High Voltage	GPIO[11:0], SUSPEND, SOF, RD, STRB, DAI, WSI,CLI, DAO, SDA, SCL, MCLK	V_{SUPD} – 0.4			V	Pins set to output I_{out}=8 mA
V_{OL}	Output Low Voltage				0.4	V	
Analog Supply							
I_{AVDD}	Current Consumption Analog Audio	AVDD		11	15	mA	all analog blocks on, Mute
				120	170	µA	Suspend
				25		mA	$R_L \ge 32\ \Omega$ (external 22-Ω series resistor required) Volume = 0 dB, Input signal 1kHz at 0 dB_{FS}
$PSRR_{AA}$	Power Supply Rejection Ratio for Analog Audio Outputs (internal regulators active)	AVDD, OUTL/R/S		95		dB	1 kHz sine wave at 100 mV_{rms}
				55		dB	≤ 100 kHz sine wave at 100 mV_{rms}
[1)] no load attached to GPIOs							

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Microphone Bias							
$V_{MICBIAS}$	Open Circuit Voltage Microphone Bias	MICBIAS		3.1		V	3V-Mode
				4.1			5V-Mode
$I_{MICBIAS}$	Output Current Microphone Bias	MICBIAS			0.5	mA	
$R_{OUTMICB}$	Output Resistance Microphone Bias	MICBIAS		160		Ω	
$PSRR_{MICB}$	Power Supply Rejection Ratio for Microphone Bias	AVDD, MICBIAS		88		dB	internal regulators active, at maximum load current, 10 kHz sine wave at 100 mV_{rms}
Analog Supply Voltage Regulators							
V_{AREG}	Output Voltage	AREG0/1, AVSS0/1	3.33	3.5	3.67	V	
Reference Frequency Generation							
V_{DCXTI}	DC Voltage at Oscillator Pins	XTI/O		0.5* V_{Areg1}		V	
C_{LI}	Input Capacitance at Oscillator Pin	XTI		3		pF	
C_{LO}	Input Capacitance at Oscillator Pin	XTO		3		pF	
$V_{XTALOUT}$	Voltage Swing at Oscillator Pins (peak-peak)	XTI/O	0.6 * V_{Areg1}		1.0 * V_{Areg1}	V	
	Oscillator Start-Up Time				10	ms	
USB Transceiver							
V_{REG}	Regulator Voltage	VREG	3.25	3.4	3.55	V	C_L=1 µF
R_O	Driver Output Resistance including the 24-Ω external serial resistor	D+/D–	28		43	Ω	static, LOW or HIGH
t_r / t_f	Rise and Fall Times	D+/D–	4		20	ns	C_L=50 pF, driver mode
MA_TRTF	Rise/Fall Time Matching	D+/D–	90		111	%	C_L=50 pF, driver mode
V_{XOVER}	Crossover Voltage	D+/D–	1.3		2.0	V	C_L=50 pF, driver mode
V_{CM_DREC}	Differential Receiver Common-Mode Range	D+/D–	0.8		2.5	V	
V_{T_SREC}	Single-ended Receiver Threshold Voltage	D+/D–	0.8		2.0	V	
R_{pu}	Switchable Pull-up Resistor	VREG, D+		1.5		kΩ	USB connected

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Analog Audio							
V_{SREF}	Signal Reference Voltage	SREF					R_L >> 10 MΩ, referred to SGND
				1.725		V	3V-Mode
				2.3			5V-Mode
V_{AI}	Analog Line Input Clipping Level (at input volume 0 dB)	ADCL/R		848		mV_{rms}	3V-Mode
				1130			5V-Mode
V_{MI}	Microphone Input Clipping Level (at minimum input volume, i.e. 0 dB)	MICIN		100		mV_{rms}	3V-Mode
				133			5V-Mode
V_{AO1}	Analog Output Voltage AC[2)]	OUTL/R/S					BW = 20 Hz...20 kHz, $R_L \geq 10k\Omega$, volume = 0 dB, Input 1 kHz at −3 dB_{FS} digital (I^2S)
				848		mV_{rms}	3V-Mode
				1130			5V-Mode
V_{AO2}	Analog Output Voltage AC at maximum load	OUTL/R/S					BW = 20 Hz...20 kHz, $R_L \geq 32\ \Omega$, volume = 0 dB, Input 1 kHz at 0 dB_{FS} digital (I^2S), 22-Ω series resistor required
				530		mV_{rms}	3V-Mode
				700			5-V Mode
R_{inAI}	Analog Line Input Resistance	ADCL/R		85		kΩ	at minimum input volume, i.e. −3 dB
			10	14			at maximum input volume, i.e. +19.5 dB
R_{inMI}	Microphone input resistance	MICIN		137		kΩ	at minimum input volume, i.e. 0 dB
			8	11			at maximum input volume, i.e. +22.5 dB
R_{inAO}	Analog output resistance	OUTL/R		2	6	Ω	volume=0 dB
R_{inSO}	Analog output resistance subwoofer	OUTS		45		Ω	volume=0 dB
SNR_{AI}	Signal-to-noise ratio of line input[2)]	ADCL/R		90		dB	BW = 20 Hz...20 kHz, A-weighted, Input 1kHz at V_{AI}−20 dB, volume= 0 dB, digital output (I^2S)
SNR_{MI}	Signal-to-noise ratio of microphone input[2)]	MICIN		90		dB	BW = 20 Hz...20 kHz, A-weighted, Input 1kHz at V_{MI}−20 dB, volume= 0 dB, digital output (I^2S)

[2)] related to 0 dB_{FS} input level

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
THD_{AI}	Total harmonic distortion of analog inputs	ADCL/R MICIN		0.007	0.01	%	BW = 20 Hz...20 kHz, volume = 0 dB, Input 1 kHz at $-3\ dB_{FS} = V_{AI} - 3$ dB resp. V_{MI}-3 dB, digital output (I^2S)
$XTALK_{AI}$	Crosstalk attenuation left/right channel for analog inputs	ADCL/R MICIN	75	80		dB	BW = 20 Hz...20 kHz, volume = 0 dB, Input 1 kHz at $-3\ dB_{FS}$, digital output (I^2S)
PSRRA0	Power Supply Rejection Ratio	AREG0/1, OUTL/R		66		dB	1 kHz sine wave at 100 mV_{rms}
		AREG0/1, OUTL/R		20		dB	≤ 100 kHz sine wave at 100 mV_{rms}
$PSRR_{AI}$	Power supply rejection ratio for analog audio inputs	AVDD, ADCL/R MICIN		80		dB	1 kHz sine at 100 mV_{rms}, 3V-Mode, digital output (I^2S)
				65		dB	≤ 10 kHz sine at 100 mV_{rms}, 3V-Mode, digital output (I^2S)
$R_{D/A}$	D/A Pass Band Ripple	OUTL/R		0.1		dB	0...20 kHz (with 2nd order post filter)
$A_{D/A}$	D/A Stop Band Attenuation			40		dB	31 kHz...164 kHz (with 2nd order post filter)
THD_{HP}	Total Harmonic Distortion	OUTL/R		0.01		%	BW = 20 Hz...20 kHz, unweighted, $R_L \geq 10k\Omega$ 22-Ω series resistor required, volume = 0 dB, Input 1 kHz at $-3\ dB_{FS}$ digital (I^2S)
THD_{HP}	Total Harmonic Distortion	OUTL/R		0.02		%	BW = 20 Hz...20 kHz, unweighted, $R_L \geq 32\ \Omega$ 22-Ω series resistor required, volume = 0 dB, Input 1 kHz at $-3\ dB_{FS}$ digital (I^2S)
THD_{SUBW}	Total Harmonic Distortion	OUTS		0.02		%	BW = 20 Hz...20 kHz, $R_L \geq 10\ k\Omega$, volume = 0 dB, corner frequency set to 400Hz, Input 100Hz at $-3\ dB_{FS}$ digital (I^2S)
SNR_{AO1}	Signal-to-Noise Ratio[2)]	OUTL/R		90		dB	BW = 20 Hz...20 kHz, A-weighted, $R_L \geq 10k\Omega$, 22-Ω series resistor required, volume = 0 dB, Input 1 kHz at $-20\ dB_{FS}$ digital (I^2S)

[2)] related to 0 dB_{FS} input level

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
SNR_{AO2}	Signal-to-Noise Ratio[2)]	OUTL/R		90		dB	BW = 20 Hz...20 kHz, A-weighted, $R_L \geq 10k\Omega$, 22-Ω series resistor required, volume = –40 dB, Input 1 kHz at –3 dB_{FS} digital (I^2S)
SNR_{AS1}	Signal-to-Noise Ratio[2)] Subwoofer	OUTS		80		dB	BW = 20 Hz...20 kHz, A-weighted, $R_L \geq 10$ kΩ, volume = 0 dB, corner frequency set to 400 Hz, Input 100 Hz at –20 dB_{FS} digital (I^2S)
SNR_{AS2}	Signal-to-Noise Ratio[2)] Subwoofer	OUTS		80		dB	BW = 20 Hz...20 kHz, A-weighted, $R_L \geq 10$ kΩ, volume = –40 dB, corner frequency set to 400 Hz, Input 100 Hz at –3 dB_{FS} digital (I^2S)
Lev_{Mute}	Dynamic Range / Mute Level L/R	OUTL/R		–100		dB	BW = 20 Hz...22 kHz unweighted, no digital input signal, volume = Mute
Lev_{Mute}	Dynamic Range / Mute Level Subwoofer	OUTS		–100		dB	BW = 20 Hz...400 Hz unweighted, no digital input signal, corner frequency set to 400 Hz, volume = Mute
$G_{INL/R}$	Gain from ADC Inputs to Outputs	ADCL/R, OUTL/R	–0.5	0	0.5	dB	$R_L \geq 10$ kΩ, volume = 0 dB Input = –3 dB_{FS} $=V_{AI}$–3 dB
P_{HP}	Output Power (Speaker/Headphone)	OUTL/R		8		mW	R_L = 32 Ω, 3V-Mode, Volume = 0 dB, 22-Ω series resistor required, Input = 0 dB_{FS} digital (I^2S)
P_{HP}	Output Power in Bridge Mode (Speaker/Headphone)	OUTL/R		16		mW	R_L = 32 Ω, 22-Ω series resistor required, 3V-Mode, right channel inverted and output set to mono (bridge mode) Volume = 0 dB, Input = 0 dB_{FS} digital (I^2S)
VOL_{AO}	Output Volume Setting Range	OUTL/R	–114		0	dB	
$dVOL_{AO}$	Output Volume Step Size	OUTL/R		1		dB	
VOL_{GA}	Output Volume Error	OUTL/R	–0.5		0.5	dB	
VOL_{dGA}	Analog Output Volume Step Size Error	OUTL/R	–0.5		0.5	dB	

[2)] related to 0 dB_{FS} input level

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
$XTALK_{HP}$	Crosstalk[2)] Left/Right Channel (Headphone)	OUTL/R		–80		dB	R_L = 32 Ω, 22-Ω series resistor required, 3V-Mode, Volume = 0 dB, Input = –3 dB_{FS} digital (I^2S)
[2)] related to 0 dB_{FS} input level							

4. UAC 3554B Applications

4.1. Recommended Low-Pass Filters for Analog Outputs

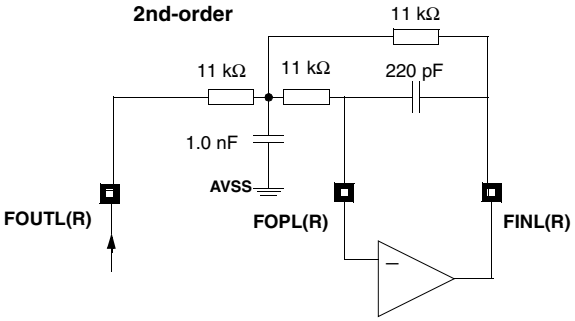

Fig. 4–1: 2nd-order low-pass filter

Table 4–1: Attenuation of 2nd-order low-pass filter

Frequency	Gain
24 kHz	–1.5 dB
30 kHz	–3.0 dB

4.2. Typical Application

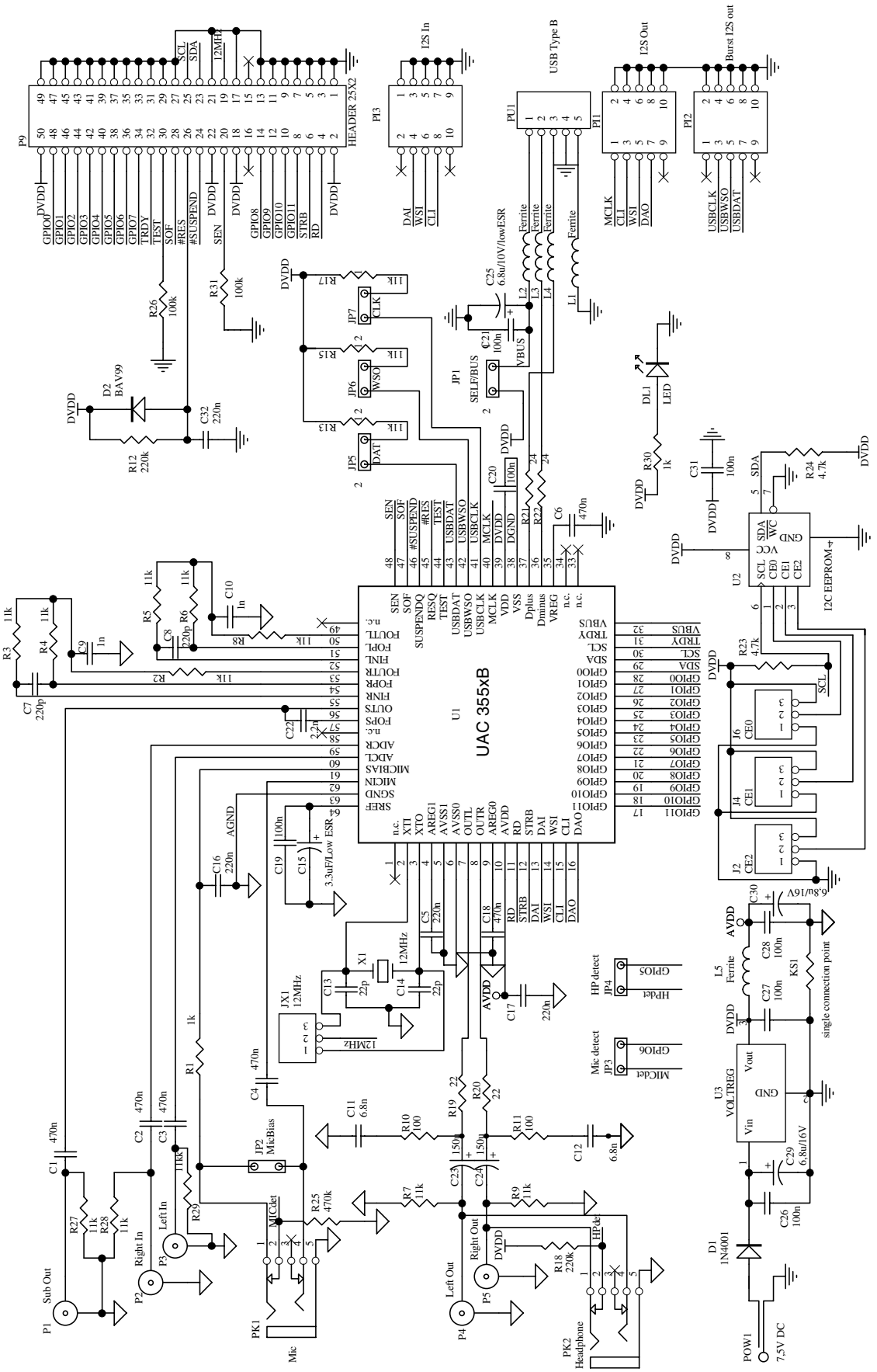

Fig. 4–2: Application circuit

5. Data Sheet History

1. Advance Information: “UAC 3554B, UAC 3556B Universal Serial Bus (USB) Codecs”, Aug. 2, 2001, 6251-544-1AI. First release of the advance information.

Micronas GmbH
Hans-Bunte-Strasse 19
D-79108 Freiburg (Germany)
P.O. Box 840
D-79008 Freiburg (Germany)
Tel. +49-761-517-0
Fax +49-761-517-2174
E-mail: docservice@micronas.com
Internet: www.micronas.com

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