DATA SHEET

TZA3010B
30 Mbits/s up to 3.2 Gbits/s
laser driver

Preliminary specification
File under Integrated Circuits, IC19

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Philips
Semiconductors

PHILIPS

FEATURES

General

- Multi-rate laser driver from 30 Mbits/s to 3.2 Gbits/s
- Bias current up to 100 mA
- Modulation current up to 60 mA
- Rise and fall times typical 100 ps
- Jitter below 20 ps (p-p)
- Retiming function with disable option
- Pulse width adjustment function
- Positive Emitter Coupled Logic (PECL) and Current Mode Logic (CML) compatible data and clock inputs
- 3.3 V supply voltage
- Optimized for use with a DC-coupled laser diode for both 3.3 and 5 V supply voltages.

Control

- Average power loop control
- Optional direct setting of modulation and bias currents.

Protection

- Enable function on bias and modulation currents
- Soft start on bias and modulation currents.

APPLICATIONS

- SDH/SONET optical transmission systems
- High current drivers for convertors
- High current drivers for high frequencies.

GENERAL DESCRIPTION

The TZA3010B is a fully integrated laser driver for optical transmission systems with data rates up to 3.2 Gbits/s. The TZA3010B laser driver incorporates the control and protection functions for a laser driver application with very few external components required and low power dissipation. The average loop controls the average monitor current in a programmable range from 300 to 1100 μA.

The design is made in the Philips BiCMOS RF process and is available in a HBCC32 package. The TZA3010B is intended for use in an application with a DC-coupled laser diode for both 3.3 and 5 V laser supply voltages.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TZA3010BVH	HBCC32	plastic, heatsink bottom chip carrier; 32 terminals; body 5 × 5 × 0.65 mm	SOT560-1

BLOCK DIAGRAM

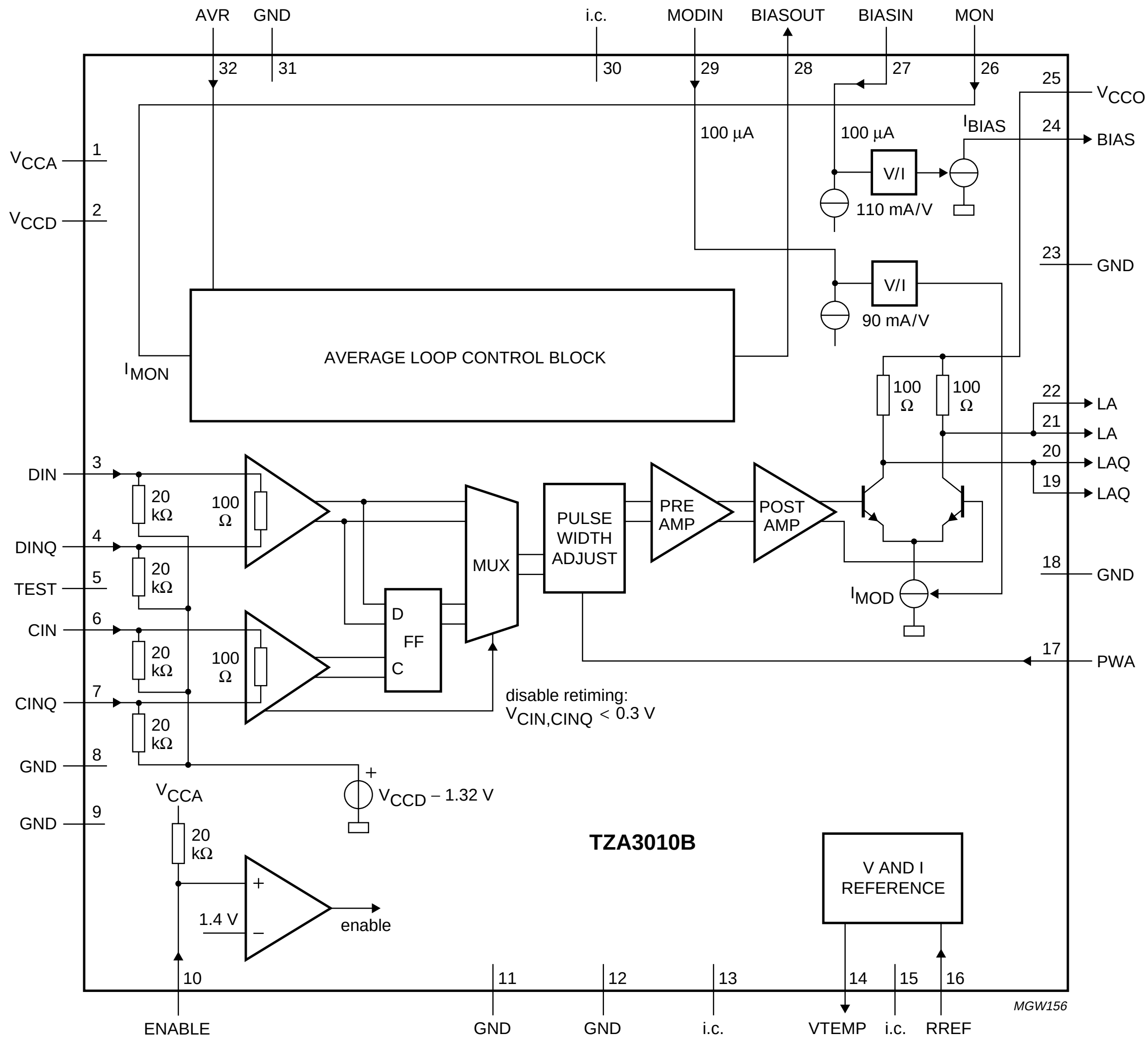


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
GND	die pad	common ground plane for V_{CCA}, V_{CCD}, V_{CCO}, RF and I/O
V_{CCA}	1	analog supply voltage
V_{CCD}	2	digital supply voltage
DIN	3	non-inverted data input (RF input)
DINQ	4	inverted data input (RF input)
TEST	5	test pin; must be connected to ground
CIN	6	non-inverted clock input (RF input)
CINQ	7	inverted clock input (RF input)
GND	8	ground supply
GND	9	ground supply
ENABLE	10	enable voltage input for modulation and bias current
GND	11	ground supply
GND	12	ground supply
i.c.	13	internally connected (leave open)
VTEMP	14	temperature dependent voltage output source
i.c.	15	internally connected (leave open)
RREF	16	reference current input; must be connected to ground with an accurate (1%) 10 kΩ resistor
PWA	17	pulse width adjustment input
GND	18	ground supply
LAQ	19	inverted laser modulation output (RF output); output for dummy load
LAQ	20	inverted laser modulation output (RF output); output for dummy load
LA	21	non-inverted laser modulation output (RF output); output for laser
LA	22	non-inverted laser modulation output (RF output); output for laser
GND	23	ground supply
BIAS	24	current source output for the laser bias current
V_{CCO}	25	supply voltage for the output stage and the laser diode
MON	26	current input for the monitor photo diode (RF input)
BIASIN	27	input voltage for the bias current setting
BIASOUT	28	output voltage of the control block for the bias current
MODIN	29	input voltage for the modulation current setting
i.c.	30	internally connected (leave open)
GND	31	ground supply
AVR	32	input current for the optical average power level setting

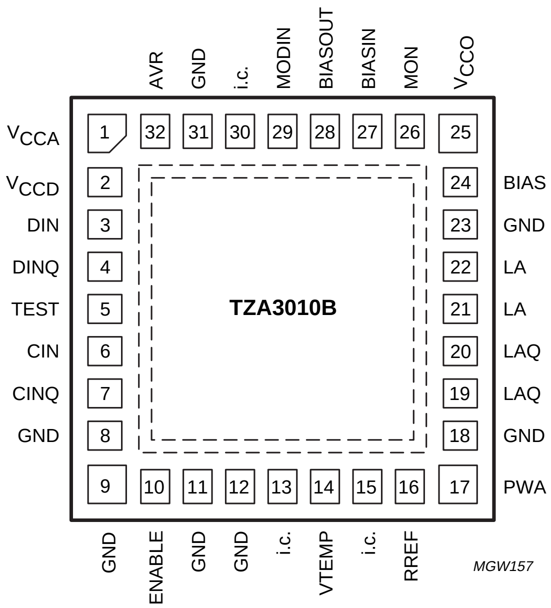


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Data and clock input

The TZA3010B operates with differential Positive Emitter Coupled Logic (PECL) and Current Mode Logic (CML) data and clock inputs with a voltage swing from 100 mV to 1 V (p-p). It is assumed that both the data and clock inputs carry a complementary signal with the specified peak-to-peak value (true differential excitation).

The circuit generates an internal common mode voltage for AC-coupled data and clock inputs, and for Single-Ended (SE) applications.

A DIN voltage above the DINQ voltage corresponds with the modulation current sinked by pin LA and with an optical ‘one’ level of the laser.

Retiming

The retiming function synchronizes the data with the clock to improve the jitter performance. The data latch switches on the rising edge of the clock input. The retiming function is disabled when both clock inputs are below 0.3 V.

Pulse width adjustment

The on-duration of the laser current can be adjusted from –100 to +100 ps. The adjustment time is set by resistor R_{PWA}. The maximum allowable capacitive load on pin PWA is 100 pF. Pulse width adjustment is disabled when pin PWA is short-circuited to ground.

Modulator output stage

The output stage is a high-speed bipolar differential pair with typical rise and fall times of 100 ps and with a modulation current source of up to 60 mA.

The modulation current switches between the LA and the LAQ outputs. For a good RF performance the inactive branch carries a small amount of the modulation current.

The LA output is optimized for the laser and the LAQ output is optimized for the dummy load.

The output stage of the TZA3010B is optimized for DC-coupled lasers.

Average loop control

The average power control loop maintains a constant average power level of the monitor current over temperature and lifetime of the laser. The average monitor current is programmable over a current range from 300 to 1100 μA by tuning the R_{AVR} setting resistor. The maximum allowable capacitive load on pins AVR and BIASOUT is 100 pF. The minimum capacitance on pin MON is 10 pF.

Direct current setting

The TZA3010B can also operate in open-loop mode with direct setting of the bias and modulation currents. The bias and modulation current sources are transconductance amplifiers and the output currents are determined by the BIASIN and MODIN voltages respectively. The bias current source has a bipolar output stage with minimum output capacitance for optimum RF performance.

Soft start

At power-up the bias and modulation current sources are released once the V_{CCA} voltage exceeds the 2.7 V level and the reference voltage has reached the correct value of 1.2 V.

The control loop starts with minimum bias and modulation currents at power-up and when the device is enabled. The current levels increase until the input current at pin MON matches the programmed average level.

Enable

A low enable input disables the bias and modulation current sources and the laser is off. A high enable input, or an open enable input, switches both current sources on and the laser is operational.

Reference block

The reference voltage is derived from a band gap circuit and is available at pin RREF. An accurate (1%) 10 kΩ resistor has to be connected to pin RREF to provide the internal reference current. The maximum allowable capacitive load on pin RREF is 100 pF.

The reference voltage on the setting pins PWA and AVR is buffered and derived from the band gap voltage.

The output voltage on pin VTEMP reflects the junction temperature of the TZA3010B, the temperature coefficient of VTEMP equals –2.1 mV/°C.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); all voltages are referenced to ground; positive currents flow into the device.

SYMBOL	PARAMETER	CONDITION	MIN.	MAX.	UNIT
V_{CCD}	digital supply voltage		–0.5	+3.5	V
V_{CCA}	analog supply voltage		–0.5	+3.5	V
V_{CCO}	output stage supply voltage		–0.5	+5.5	V
V_n	voltage on all input and output pins		–0.5	$V_{CCA,CCD}$ + 0.5	V
I_n	input current on pins				
	RREF, PWA and AVR		–1.0	0	mA
	VTEMP and BIASOUT		–1.0	+1.0	mA
	MON		0	5.0	mA
$V_{o(LA)}$	output voltage on pin LA	normal operation			
		V_{CCO} = 3.3 V	0.8	4.1	V
		V_{CCO} = 5 V	1.2	4.5	V
$V_{o(LAQ)}$	output voltage on pin LAQ	normal operation			
		V_{CCO} = 3.3 V	1.6	4.5	V
		V_{CCO} = 5 V	2.0	5.2	V
V_{BIAS}	voltage on pin BIAS	normal operation			
		V_{CCO} = 3.3 V	0.6	3.6	V
		V_{CCO} = 5 V	0.8	4.1	V
T_{amb}	ambient temperature		–40	+85	°C
T_j	junction temperature		–40	+125	°C
T_{stg}	storage temperature		–65	+150	°C

THERMAL CHARACTERISTICS

In compliance with JEDEC standards JESD51-5 and JESD51-7.

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient; 4 layer Printed Circuit Board in still air with 9 plated vias connected with the heatsink and the first ground plane in the PCB.	35	K/W

DC CHARACTERISTICS

T_{amb} = –40 to +85 °C; $R_{th(j-a)}$ = 58 K/W; P_{tot} = 420 mW; V_{CCA} = 3.14 to 3.47 V; V_{CCD} = 3.14 to 3.47 V; V_{CCO} = 3.14 to 3.47 V; R_{AVR} = 7.5 kΩ; R_{MODIN} = 6.2 kΩ; R_{BIASIN} = 6.8 kΩ; R_{PWA} = 10 kΩ; R_{RREF} = 10 kΩ (1%); positive currents flow into the device; all voltages are referenced to ground; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies: pins V_{CCA}, V_{CCD} and V_{CCO}						
I_{CCA}	analog supply current		30	40	50	mA
I_{CCD}	digital supply current		39	50	60	mA
I_{CCO}	output stage supply current	pins LA and LAQ open-circuit	13	17	22	mA
P_{tot}	total power dissipation	V_{BIAS} = V_{CCO} = 3.3 V; note 1	340	420	500	mW
Data and clock inputs: pins DIN and CIN						
$V_{i(p-p)}$	input voltage swing (peak-to-peak value)	$V_{i(DIN)}$ = V_{CCD} – 2 V to V_{CCD}; $V_{i(CIN)}$ = V_{CCD} – 2 V to V_{CCD}	100	–	1000	mV
$V_{int(cm)}$	internal common mode voltage	AC-coupled inputs	V_{CCD} – 1.45	V_{CCD} – 1.32	V_{CCD} – 1.20	V
V_{IO}	input offset voltage	note 2	–10	0	+10	mV
$Z_{i(dif)}$	differential input impedance		90	100	110	Ω
$Z_{i(cm)}$	common mode input impedance		7	10	12.5	kΩ
$V_{i(CIN)(dis)}$	input voltage on pin CIN for disabled retiming	V_{CIN} = V_{CINQ}	–	–	0.3	V
Monitor photodiode input: pin MON						
$V_{i(MON)}$	input voltage	$I_{av(MON)}$ = 300 to 1200 μA	1.13	1.25	1.33	V
$Z_{i(MON)}$	input impedance	$I_{av(MON)}$ = 300 to 1200 μA	–	40	–	Ω
Setting for average loop control: pins MON and AVR						
$I_{av(MON)(min)}$	minimum average monitor current setting	I_{AVR} = –240 μA	–	300	410	μA
$I_{av(MON)(max)}$	maximum average monitor current setting	I_{AVR} = –15 μA	1050	1200	–	μA
$V_{ref(AVR)}$	reference voltage on pin AVR	I_{AVR} = –290 to 0 μA; C_{AVR} < 100 pF	1.15	1.20	1.25	V
Control loop bias output: pin BIASOUT						
$I_{source(BIASOUT)}$	source current	$V_{BIASOUT}$ = 0.5 to 1.5 V; $C_{BIASOUT}$ < 100 pF	–	–	–200	μA
$I_{sink(BIASOUT)}$	sink current	$V_{BIASOUT}$ = 0.5 to 1.5 V; $C_{BIASOUT}$ < 100 pF	200	–	–	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Bias current source: pins BIASIN and BIAS						
$g_{m(BIAS)}$	transconductance	V_{BIASIN} = 0.5 to 1.5 V; V_{BIAS} = V_{CCO} = 3.3 V	92	110	128	mA/V
$I_{source(BIASIN)}$	source current on pin BIASIN	V_{BIASIN} = 0.5 to 1.5 V	–108	–100	–97	μA
$I_{BIAS(min)}$	minimum bias current	V_{BIASIN} = 0 to 0.5 V	0.1	0.2	0.3	mA
$I_{BIAS(dis)}$	bias current at disable	V_{ENABLE} < 0.8 V	–	–	10	μA
V_{BIAS}	output voltage on pin BIAS	normal operation				
		V_{CCO} = 3.3 V	0.6	–	3.6	V
		V_{CCO} = 5 V	0.8	–	4.1	V
Modulation current source: pin MODIN						
$g_{m(MOD)}$	transconductance	V_{MODIN} = 0.5 to 1.2 V; V_{LA} = V_{LAQ} = V_{CCO} = 3.3 V; see Fig.4; note 3	75	90	105	mA/V
$I_{source(MODIN)}$	source current on pin MODIN	V_{MODIN} = 0.5 to 1.2 V; note 3	–108	–100	–97	μA
Modulation current outputs: pins LA and LAQ						
$I_{o(LA)(min)(on)}$	minimum laser modulation output current at LA on	V_{MODIN} = 0 to 0.5 V; V_{LA} = V_{CCO} = 3.3 V; see Fig.4	3.0	3.8	4.7	mA
$I_{o(LAQ)(min)(on)}$	minimum inverted laser modulation output current at LA on	V_{MODIN} = 0 to 0.5 V; V_{LAQ} = V_{CCO} = 3.3 V	0.60	1.10	1.35	mA
$I_{o(LA)(min)(off)}$	minimum laser modulation output current at LA off	V_{MODIN} = 0 to 0.5 V; V_{LA} = V_{CCO} = 3.3 V; see Fig.4	–	0.2	0.40	mA
$Z_{o(LA,LAQ)}$	output impedance		88	100	120	Ω
$I_{o(dis)}$	inverted and non-inverted laser modulation output current at disable	V_{ENABLE} < 0.8 V; V_{LA} = V_{CCO} = 3.3 V	–	–	200	μA
$V_{o(LA)}$	output voltage on pin LA	normal operation				
		V_{CCO} = 3.3 V	0.8	–	4.1	V
		V_{CCO} = 5 V	1.2	–	4.5	V
$V_{o(LAQ)}$	output voltage on pin LAQ	normal operation				
		V_{CCO} = 3.3 V	1.6	–	4.5	V
		V_{CCO} = 5 V	2.0	–	5.2	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Enable function: pin ENABLE						
V_{IL}	LOW-level input voltage	bias and modulation current sources disabled	–	–	0.8	V
V_{IH}	HIGH-level input voltage	bias and modulation current sources enabled	2.0	–	–	V
$R_{pu(int)}$	internal pull-up resistance		13	20	25	kΩ
Reference block: pins RREF and VTEMP						
V_{RREF}	reference voltage	R_{RREF} = 10 kΩ (1%); C_{RREF} < 100 pF	1.15	1.20	1.25	V
V_{VTEMP}	temperature dependent voltage	T_j = 50 °C; C_{VTEMP} < 2 nF; note 4	1.15	1.20	1.25	V
TC_{VTEMP}	temperature coefficient of V_{VTEMP}	T_j = 0 to +125 °C	–	–2.1	–	mV/K
$I_{source(VTEMP)}$	source current on pin VTEMP		–	–	–1	mA
$I_{sink(VTEMP)}$	sink current on pin VTEMP		1	–	–	mA

Notes

1. The total power dissipation P_{tot} is calculated with $V_{BIAS} = V_{CCO}$ = 3.3 V, in the application V_{BIAS} will be V_{CCO} minus the laser diode voltage which results in a lower total power dissipation.
2. The specification of the offset voltage is guaranteed by design.
3. Pin MODIN has a maximum operation voltage of 1.2 V.
4. V_{VTEMP} equals: $V_{VTEMP} = 1.31\ V + TC_{VTEMP} \times T_j$, where the junction temperature equals: $T_j = T_{amb} + P_{tot} \times R_{th(ja)}$.

AC CHARACTERISTICS

T_{amb} = –40 to +85 °C; $R_{th(j-a)}$ = 58 K/W; P_{tot} = 420 mW; V_{CCA} = 3.14 to 3.47 V; V_{CCD} = 3.14 to 3.47 V; V_{CCO} = 3.14 to 3.47 V; R_{AVR} = 7.5 kΩ; R_{MODIN} = 6.2 kΩ; R_{BIASIN} = 6.8 kΩ; R_{PWA} = 10 kΩ; R_{RREF} = 10 kΩ (1%); positive currents flow into the device; all voltages are referenced to ground; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RF path						
BR	bit rate		0.03	–	3.2	Gb/s
$J_{o(p-p)}$	output jitter of pin LA (peak-to-peak value)	R_L = 25 Ω; note 1	–	–	20	ps
t_r,t_f	rise and fall time of pin LA	20% to 80%; R_L = 25 Ω	–	100	120	ps
$t_{su(i)(D)}$	data input set-up time		60	–	–	ps
$t_{h(i)(D)}$	data input hold time		60	–	–	ps
$t_{START(EN)}$	start-up time at enable	direct current setting; note 1	–	–	1	µs
Current control						
tc_{int}	internal time constant	average loop control; C_{MON} > 10 pF	30	–	–	ms
Pulse width adjustment						
$t_{PWA(min)}$	minimum pulse width adjustment on pin LA	R_{PWA} = 6.7 kΩ; C_{PWA} < 100 pF	–	–100	–90	ps
t_{PWA}	pulse width adjustment on pin LA	R_{PWA} = 10 kΩ; C_{PWA} < 100 pF	–20	0	+20	ps
$t_{PWA(max)}$	maximum pulse width adjustment on pin LA	R_{PWA} = 20 kΩ; C_{PWA} < 100 pF	100	–	–	ps

Note

1. The specification is guaranteed by design.

DESIGN EQUATIONS

Bias and modulation currents

The bias and modulation currents are determined by the voltages on pins BIASIN and MODIN. For average loop control the BIASIN voltage is applied by pin BIASOUT and the MODIN voltage is applied by an external voltage source or by external resistor R_{MODIN}. For direct setting of bias and the modulation current, the BIASIN and MODIN voltages have to be applied by external voltage sources or by R_{BIASIN} and R_{MODIN}:

$$I_{BIAS} = (R_{BIASIN} \times I_{BIASIN} - 0.5\ V) \times g_{m(BIAS)}$$

$$I_{MOD} = I_{LA(on)}(V_{LA} = V_{CCO}) = (R_{MODIN} \times I_{MODIN} - 0.5\ V) \times g_{m(MOD)} + 5\ mA$$

The bias current source operates with an input voltage range from 0.5 to 1.5 V. The modulation current source operates with an input voltage range from 0.5 to 1.2 V. The output currents are at their minimum level for an input voltage below 0.5 V; see Figs 3 and 4.

The bias and modulation current sources are temperature compensated and the adjusted current level remains stable over temperature. The bias and modulation currents increase with increasing values for resistors R_{BIASIN} and R_{MODIN} respectively, this allows resistor tuning to start at a minimum current level.

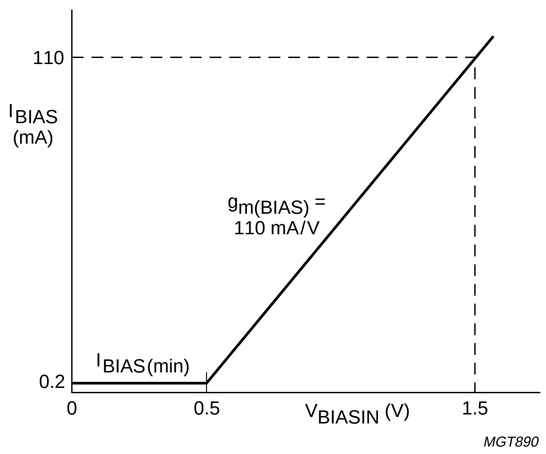


Fig.3 Bias current as a function of BIASIN voltage.

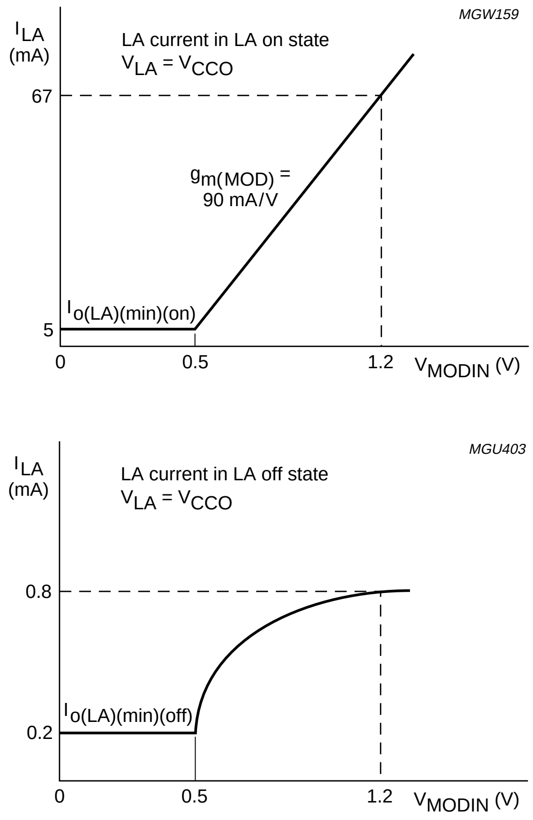


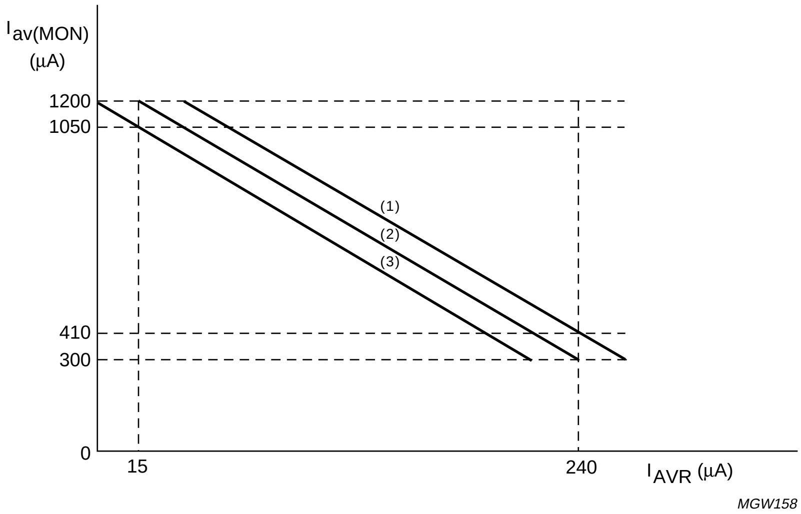
Fig.4 Modulation current as a function of MODIN voltage.

Average monitor current

The average monitor current $I_{av(MON)}$ in average loop operation is determined by the source current (I_{AVR}) on pin AVR. The current can be sunk by an external current source or by an external resistor (R_{AVR}) connected to ground, the equation for the typical values is:

$$I_{av(MON)} = 1260\ \mu A - 4.0 \times I_{AVR} = 1260\ \mu A - 4.0 \times \frac{V_{AVR}}{R_{AVR}}$$

The average monitor current increases with a decreasing I_{AVR} or increasing R_{AVR}, this allows resistor tuning of R_{AVR} to start at minimum I_{AVR} current level (see Fig.5).



(1) Maximum values.

(2) Typical values; $I_{av(MON)}$ = 1260 μA – 4.0 × I_{AVR} (μA).

(3) Minimum values.

Fig.5 Average monitor current as a function of I_{AVR}.

Pulse width adjustment

The pulse width adjustment time is determined by resistor R_{PWA}: $t_{PWA} = 200\ \text{ps} \times \frac{R_{PWA} - 10\ k\Omega}{R_{PWA}}$

The t_{PWA} range is from –100 to +100 ps which corresponds with a R_{PWA} range which is between a minimum resistance of 6.7 kΩ and a maximum resistance of 20 kΩ. The PWA function is disabled when the PWA input is short-circuited to ground, the t_{PWA} equals 0 ps for a disabled PWA function (see Fig.6).

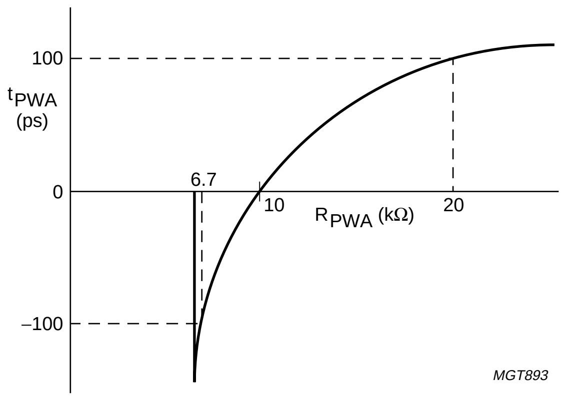
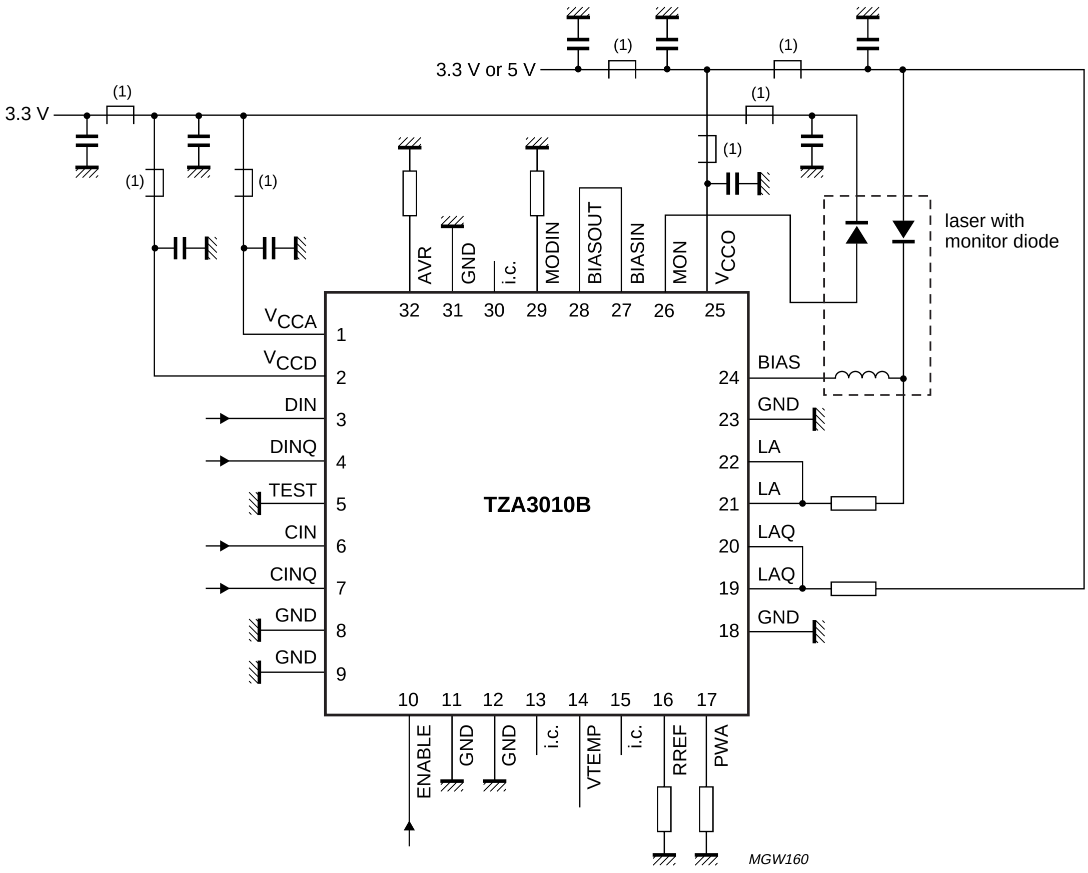


Fig.6 Pulse width adjustment.

APPLICATION INFORMATION

TZA3010B with average loop control

The application with the TZA3010B with average loop control and a DC-coupled laser at 3.3 or 5 V laser voltage is illustrated in Fig.7. The average power level is determined by resistor R_{AVR}. The average loop controls the bias current when the BIASOUT output is connected to the BIASIN input. The modulation current is determined by the MODIN input voltage which is generated by resistor R_{MODIN} and the 100 μA source current of pin MODIN.

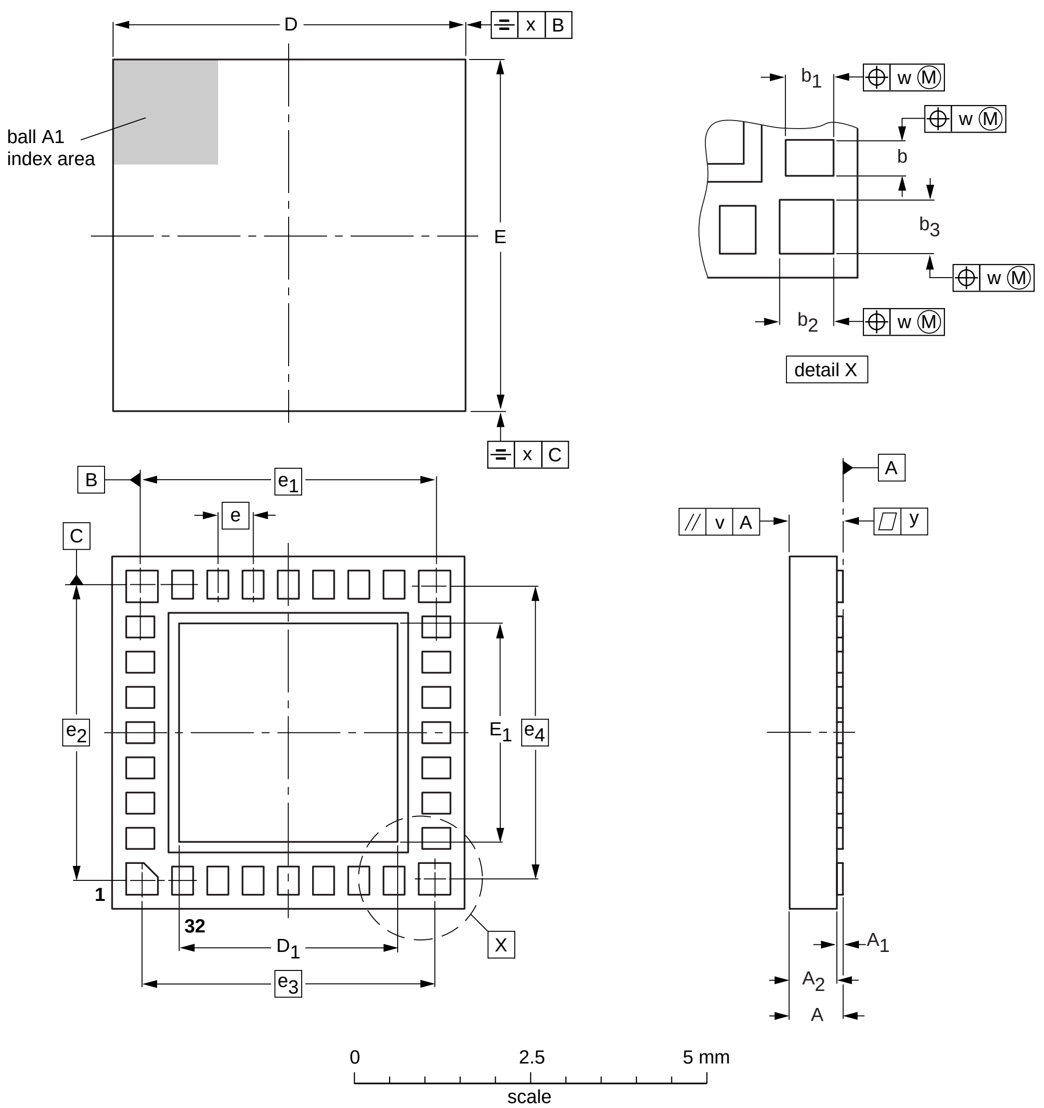


(1) Ferrite bead.

Fig.7 TZA3010B with DC-coupled laser and average loop control.

PACKAGE OUTLINE

HBCC32: plastic, heatsink bottom chip carrier; 32 terminals; body 5 x 5 x 0.65 mm **SOT560-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	b	b_1	b_2	b_3	D	D_1	E	E_1	e	e_1	e_2	e_3	e_4	v	w	x	y
mm	0.80	0.10 0.05	0.70 0.60	0.35 0.20	0.50 0.30	0.50 0.35	0.50 0.35	5.1 4.9	3.2 3.0	5.1 4.9	3.2 3.0	0.5	4.2	4.2	4.15	4.15	0.2	0.15	0.15	0.05

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT560-1		MO-217				~~99-09-10~~ 00-02-01

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, HBGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *“Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

DATA SHEET STATUS(1)	PRODUCT STATUS(2)	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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NOTES

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