TSC8051C3

8–Bit Microcontroller for Multi–Sync Digital Monitors

1. Introduction

The TSC8051C3 is a stand–alone high performance CMOS 8–bit embedded microcontroller and is designed for use in low–end to mid–end CRT monitors starting from 14” and up.

The TSC8051C3 includes the fully static 8–bit “80C51” CPU core with 256 bytes of RAM; 8 Kbytes of ROM or OTProm; two 16–bit timers; up to 12 PWM Channels; a 6 sources and 2–level interrupt controller; a Sync processor; a DDC controller; a full hardware multimaster I^2C controller; a watchdog timer; a power voltage monitor and on–chip oscillator.

This product is available in Mask ROM version for volume production as well as in OTP (One–Time–Programmable) or UV–Erasable window EPROM version for development purpose and pre–serial production.

The TSC8051C3 enables the users reducing a lot of external discrete components with it’s on–chip Sync Processor, DCC and I^2C controllers and 12 PWM Channels while bringing the maximum of flexibility.

2. Features

- Boolean processor
- Fully static design
- 8Kbytes of ROM or OTProm
- 256 bytes of RAM
- 2 x 16–bit timer/counter [T0 – T1]
- Programmable serial port
- 6 interrupt sources:
  - External inputs interrupt (2)
  - Timers interrupt (2)
  - UART/DDC interrupt
  - I^2C interrupt
- 2 power saving control modes:
  - Idle mode
  - Power–down mode
- Safety Features
  - Watchdog reset
  - Power fail reset
- SYNC processor:
  - Controlled Hsync and Vsync inputs
  - Controlled Hsync and Vsync outputs
  - Programmable clamp pulse output
- Up to 12 programmable 8–bit PWM channels:
  - 8 dedicated channels with 12V open–drain outputs
  - 4 shared channels with 5V open–drain outputs
- DDC controller:
  - DDC1 hardware
  - DDC2 hardware for DDC2B
- Multimaster master/slave I^2C controller for E^2PROM, OSD IC, deflection ICs, USB controller...
- On chip oscillator for crystal or ceramic resonator
- Up to 32 programmable I/O lines depending on the package
- 40 pins DIP, 44 pins PQFP, 44 and 52 pins PLCC packages
- Operating frequency: 0 to 12 MHz or 0 to 16 MHz
- Commercial and Industrial temperature ranges

3. Block Diagram

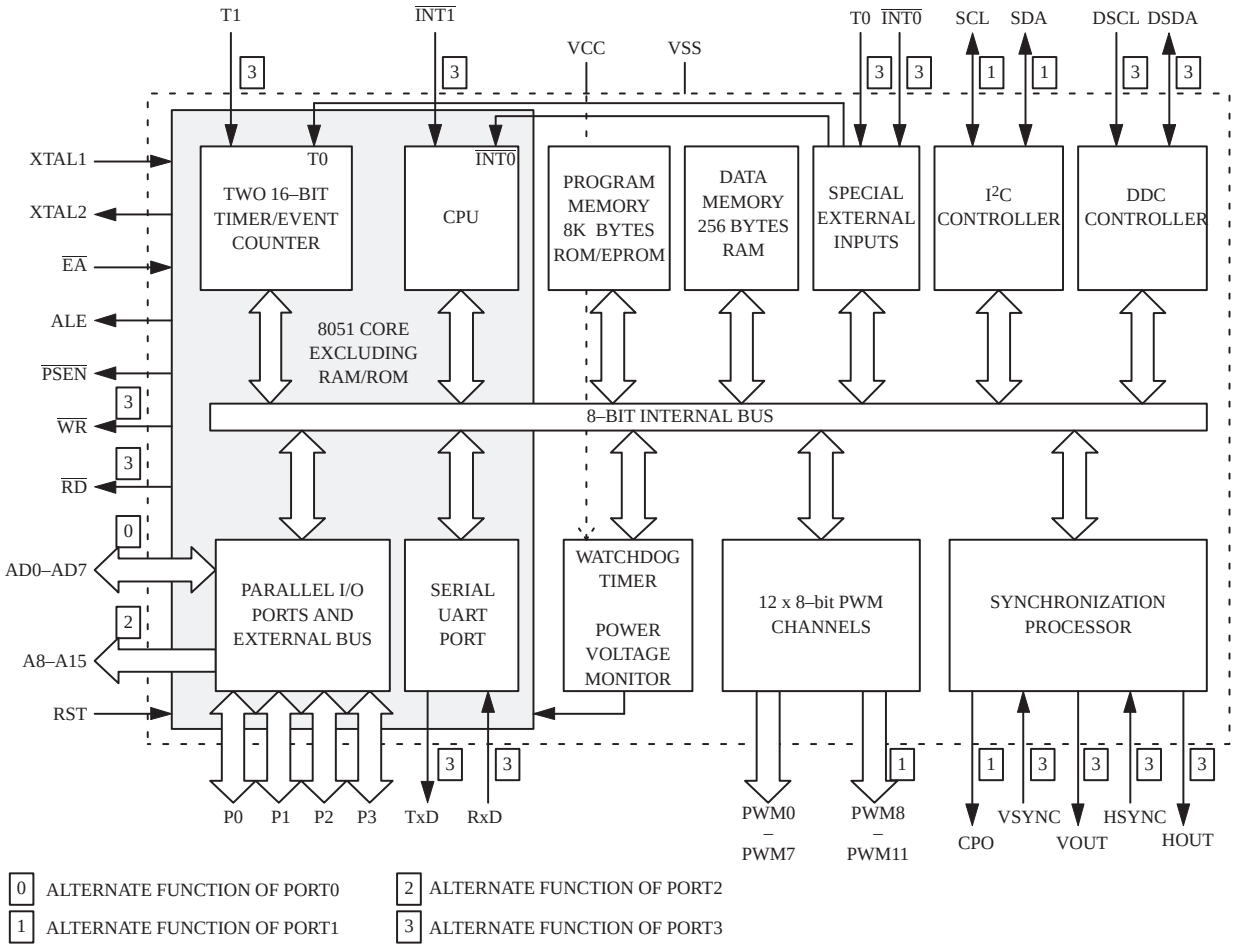


Figure 1 TSC8051C3 block diagram

4. Pin Configurations

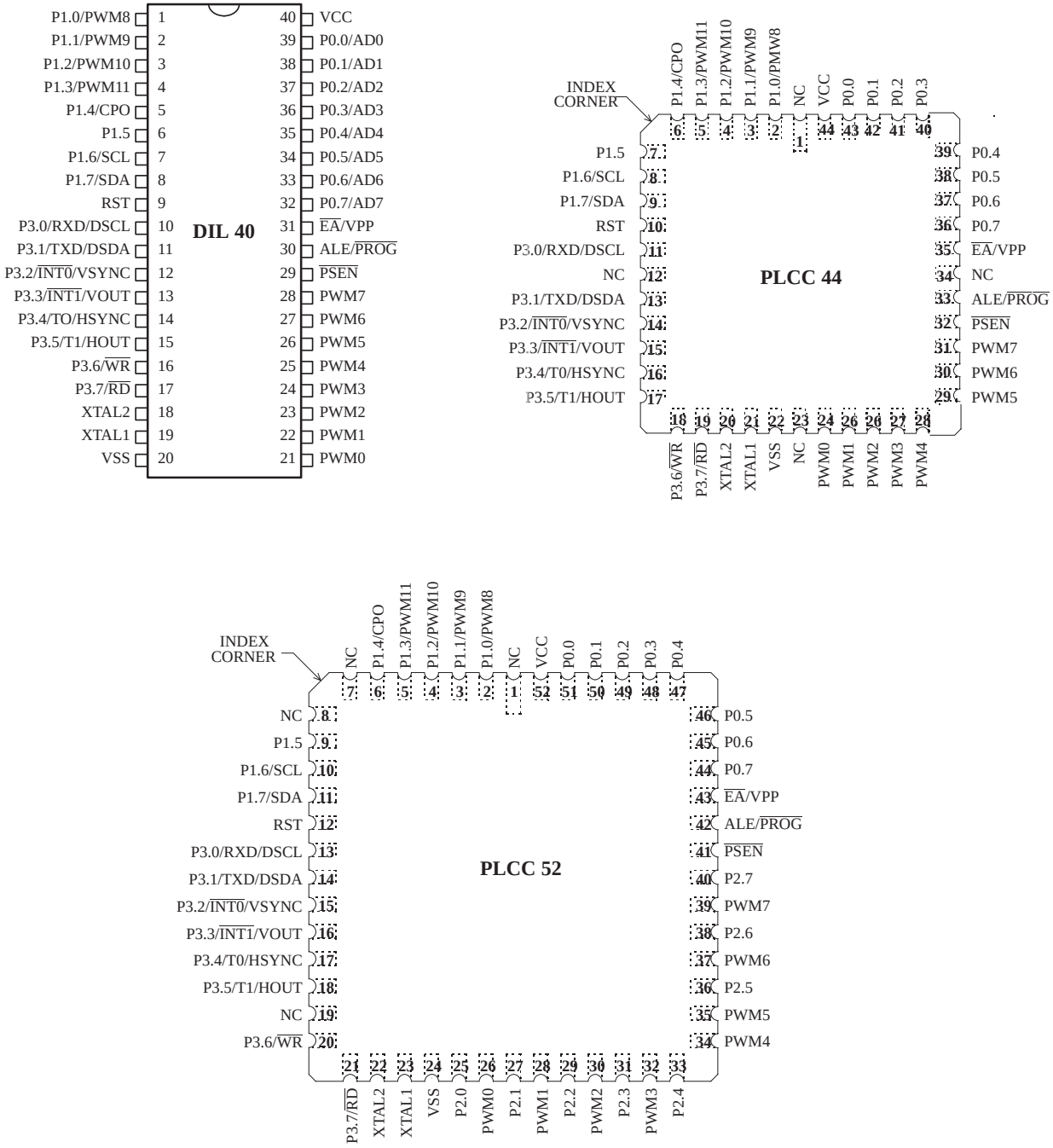


Figure 2 TSC8051C3 pin configurations

5. Pin Description

VSS

Circuit ground.

VCC

Power supply voltage.

RST

A high level on this pin for two machine cycles while the oscillator is running resets the device. An internal pulldown resistor permits power–on reset using only a capacitor connected to VCC.

PORT 0 (P0.0–P0.7)

Port 0 is an 8–bit open–drain bidirectional I/O port. Port 0 pins that have 1's written to them float, and in that state can be used as high–impedance inputs.

Port 0 is also the multiplexed low–order address and data bus during access to external Program and Data memory. In this application it uses strong internal pull–up when emitting 1's.

Port 0 can sink and source 8 LS TTL loads.

PORT 1 (P1.0–P1.7)

Port 1 is an 8–bit bidirectional I/O port. P1.0 to P1.5 are standard ports with internal pullups, P1.6 and P1.7 are open-drain ports. Port 1 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (IIL on the data–sheet) because of the internal pullups.

Port 1 also serves 4 programmable PWM open drain outputs, programmable CPO and SCL/SDA line for I^2C controller as listed below:

Port Pin	Alternate Function
P1.0	PWM8: Pulse Width Modulation output 8.
P1.1	PWM9: Pulse Width Modulation output 9.
P1.2	PWM10: Pulse Width Modulation output 10.
P1.3	PWM11: Pulse Width Modulation output 11.
P1.4	CPO: Horizontal Clamp Pulse Output.
P1.6	SCL: I^2C open–drain Serial Clock Line.
P1.7	SDA: I^2C open–drain Serial Data Line.

Port 1 can sink and source 3 LS TTL loads.
Port 1 receives the low–order address byte during EPROM programming and program verification.

PORT 2 (P2.0–P2.7)

Port 2 is an 8–bit bidirectional I/O port with internal pullups. Port 2 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (IIL on the data–sheet) because of the internal pullups.

Port 2 emits the high–order 8–bit address during fetches from external Program Memory and during accesses to external Data Memory that use 16–bit addresses. In this application it uses strong internal pull–up when emitting 1's.

Port 2 can sink and source 3 LS TTL loads.

PORT 3 (P3.0–P3.7)

Port 3 is an 8–bit bidirectional I/O port with internal pullups. Port 3 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (IIL on the data–sheet) because of the internal pullups.

Each line on this port has 2 or 3 functions either a general I/O or special control signal, as listed below:

Port Pin	Alternate Function
P3.0	RXD: serial input port. DSCL: DDC2 serial clock line.
P3.1	TXD: serial output port. DSDA: DDC1/2 serial data line.
P3.2	$\overline{INT0}$: external interrupt 0. VSYNC: vertical synchronization input.
P3.3	$\overline{INT1}$: external interrupt 1. VOUT: buffered Vsync output.
P3.4	T0: Timer 0 external input. HSYNC: horizontal synchronization input.
P3.5	T1: Timer 1 external input. HOUT: buffered Hsync output.
P3.6	$\overline{WR}$: external data memory write strobe.
P3.7	$\overline{RD}$: external data memory read strobe.

Port 3 can sink and source 3 LS TTL loads.

PWM0–7

These eight Pulse Width Modulation outputs are true 12V open–drain outputs and are floating after reset.

Some of these PWM pins receive the high order address bits and control signals during EPROM programming and program verification.

ALE/$\overline{PROG}$

The Address Latch Enable output signal occurs twice each machine cycle except during external data memory access. The negative edge of ALE strobes the address into external data memory or program memory. ALE can sink and source 8 LS TTL loads.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8Eh (MSCON). With the bit set, ALE is active only during MOVX, MOVC instructions and external fetches. Otherwise the pin is weakly pulled high.

ALE can sink/source 8 LS TTL inputs. It can drive CMOS inputs without external pullup.

Throughout the remainder of this datasheet, ALE will refer to the signal coming out of the ALE/$\overline{PROG}$ pin, and the pin will be referred to as the ALE/$\overline{PROG}$ pin.

$\overline{EA}$/VPP

When the External Access input is held high, the CPU executes out of internal program memory (unless the Program Counter exceeds 1FFFh). When $\overline{EA}$ is held low the CPU executes only out of external program memory. must not be left floating.

This pin also receives the programming supply voltage (VPP) during EPROM programming.

$\overline{PSEN}$

The Program Store Enable output signal remains high during internal program memory. An active low output occurs during an external program memory fetch. $\overline{PSEN}$ can sink and source 8 LS TTL loads.

XTAL1

Input to the inverting oscillator amplifier and input to the external clock generator circuits.

XTAL2

Output from the inverting oscillator amplifier. This pin should be non–connected when external clock is used.

6. Basic Functional Description

6.1. Idle And Power Down Operation

Figure 3 shows the internal Idle and Power Down clock configuration. As illustrated, Power Down operation stops the oscillator. Idle mode operation allows the interrupt, serial port, and timer blocks to continue to operate while the clock to the CPU is gated off.

These special modes are activated by software via the PCON register (see Table 6), its hardware address is 87h and is not bit addressable. If 1's are written to PD and IDL at the same time, PD takes precedence.

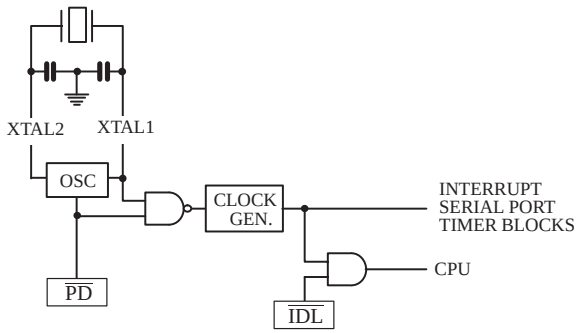


Figure 3 Idle and Power Down Block diagram

6.1.1. Idle Mode

The instruction that sets PCON.0 is the last instruction executed before the Idle mode is activated. Once in the Idle mode the CPU status is preserved in its entirety: the Stack Pointer, Program Counter, Program Status Word, Accumulator, RAM, and all other register maintain their data during Idle Table 1 describes the status of the external pins during Idle mode.

There are two ways to terminate the Idle mode. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware terminating Idle mode. The interrupt is serviced, and following RETI, the next instruction to be executed will be the one following the instruction that wrote 1 to PCON.0.

The flag bits GF0 and GF1 may be used to determine whether the interrupt was received during normal execution or during the Idle mode. For example, the instruction that writes to PCON.0 can also set or clear one or both flag bits. When Idle mode is terminated by an enabled interrupt, the service routine can examine the status of the flag bits.

The second way of terminating the Idle is with a hardware reset. Since the oscillator is still running, the hardware reset needs to be active for only 2 machine cycles (24 oscillator periods) to complete the reset operation.

6.1.2. Power Down Mode

The instruction that sets PCON.1 is the last executed prior to entering power down. Once in power down, the oscillator is stopped. The contents of the onchip RAM and the Special Function Register are saved during power down mode. A hardware reset is the only way of exiting the power down mode. The hardware reset initiates the Special Function Register. In the Power Down mode, VCC may be lowered to minimize circuit power consumption. Care must be taken to ensure the voltage is not reduced until the power down mode is entered, and that the voltage is restored before the hardware reset is applied which frees the oscillator. Reset should not be released until the oscillator has restarted and stabilized. Table 1 describes the status of the external pins while in the power down mode. It should be noted that if the power down mode is activated while in external program memory, the port data that is held in the Special Function Register P2 is restored to Port 2. If the data is a 1, the port pin is held high during the power down mode by the strong pullup transistor.

Table 1 Status of the external pins during Idle and Power Down modes

Mode	Program Memory	ALE	PSEN	Port 0	Port 1	Port 2	Port 3	PWMx
Idle	Internal	1	1	Port Data	Port Data	Port Data	Port Data	Floating
Idle	External	1	1	Floating	Port Data	Address	Port Data	Floating
Power Down	Internal	0	0	Port Data	Port Data	Port Data	Port Data	Floating
Power Down	External	0	0	Floating	Port Data	Port Data	Port Data	Floating

6.2. Stop Clock Mode

Due to static design, the TSC8051C3 clock speed can be reduced down to 0 MHz without any data loss in memory or register. This mode allows step by step code execution, and permits to reduce system power consumption by bringing the clock frequency down to any value. When the clock is stopped, the power consumption is the same as in the Power Down Mode.

6.3. I/O Ports Structure

The TSC8051C3 has four 8–bit ports. Each port consist of a latch (special function register P0 to P3), an input buffer and an output driver. These ports are the same as in 80C51, with the exception of the additional functions of port 1 and port 3 (see Pin Description section).

6.4. I/O Configurations

Figure 4 shows a functional diagram of the generic bit latch and I/O buffer in each of the four ports. The bit latch, (one bit in the port SFR) is represented as a D type flip–flop. A ‘write to latch’ signal from the CPU latches a bit from the internal bus and a ‘read latch’ signal from the CPU places the Q output of the flip–flop on the internal bus. A ‘read pin’ signal from the CPU places the actual pin logical level on the internal bus.
Some instructions that read a port read the actual pin, and other instructions read the latch (SFR).

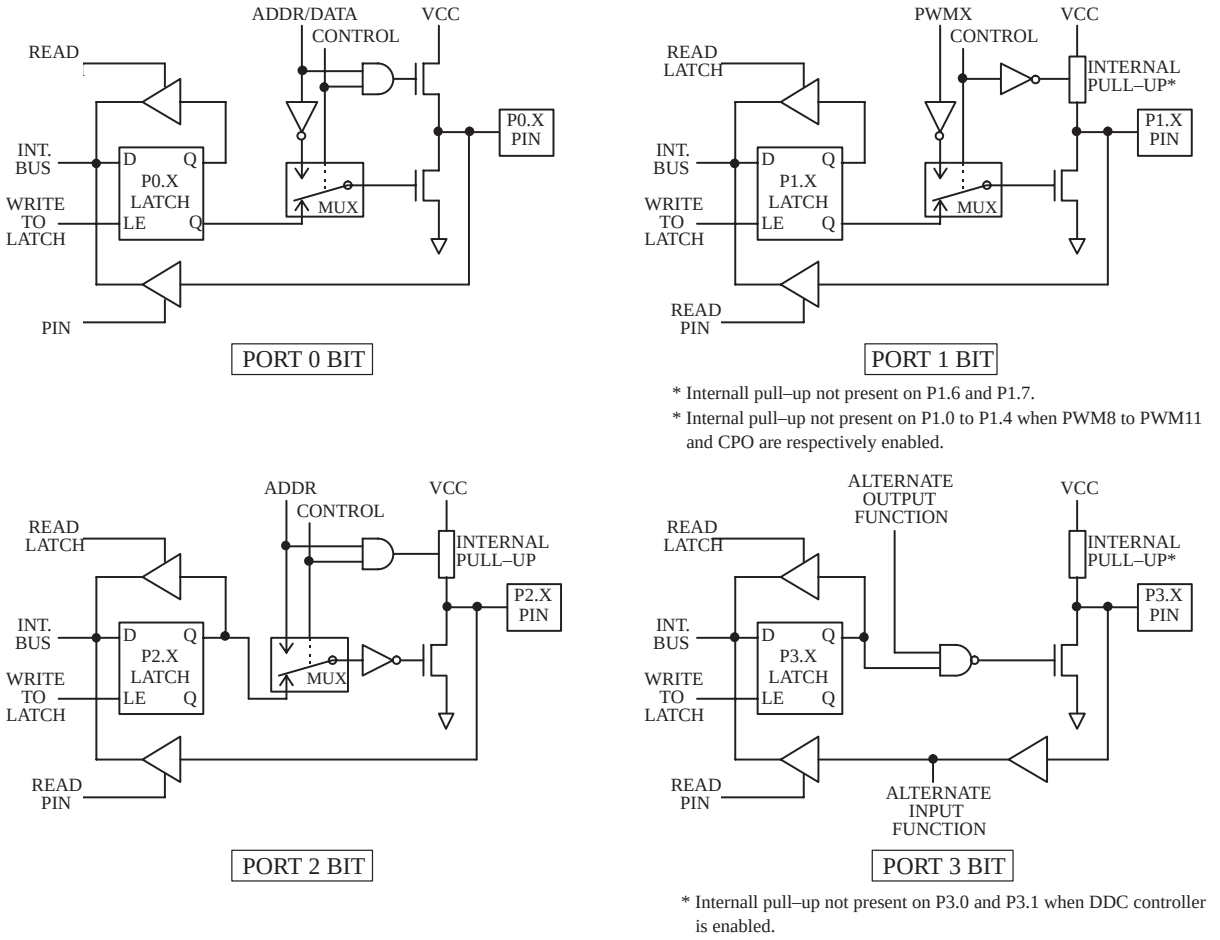


Figure 4 Port Bit Latches and I/O buffers

6.5. Reset Circuitry

The reset circuitry for the TSC8051C3 is connected to the reset pin RST. A Schmitt trigger is used at the input for noise rejection (see Figure 5).

A reset is accomplished by holding the RST pin high for at least two machine cycles (24 oscillator periods) while the oscillator is running. The CPU responds by executing an internal reset. It also configures the ALE and PSEN pins as inputs (they are quasi–bidirectional). A Watchdog timer underflow if enabled and a power failure if power fail reset is enabled will force a reset condition to the TSC8051C3 by an internal connection (see security features section).
The internal reset is executed during the second cycle in which reset is high and is repeated every cycle until RST goes low. It leaves the internal registers as follows:

Table 2 Special Function Registers reset value

Register	Content
ACC	00h
B	00h
DPTR	0000h
DCON	XXXX 0000b
DDAT	XXh
EICON	XXXX X000b
HWDR	0XXX 0000b
IE	0X00 0000b
IP	XX00 0000b
MSCON	XXXX XXX0b
P0–P3	FFh
PC	0000h
PCON	0XX0 0000b
PSW	00h
PWM0–11	00h
PWMCON	XXXX XXX0b
MXCR0	00h
MXCR1	X0h
S1ADR	00h
S1CON	0000 0000b
S1DAT	00h
S1STA	F8h
SBUF	00h
SCON	0000 0000b
SOCR	0000 0000b
SP	07h
TCON	0000 0000b
TH0, TH1	00h
TL0, TL1	00h
TMOD	0000 0000b

The internal RAM is not affected by reset. At power–on reset, the RAM content is indeterminate.

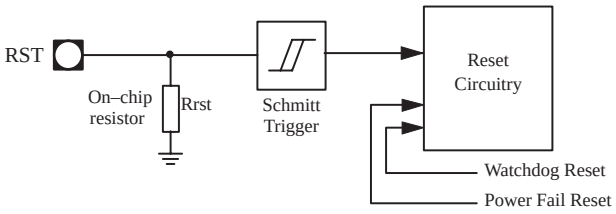


Figure 5 On–Chip Reset Configuration

An automatic reset can be obtained when VCC is turned on by connecting the RST pin to VCC through a 1µF capacitor providing the VCC setting time does not exceed 1ms and the oscillator start–up time does not exceed 10ms. This power–on reset circuit is shown in Figure 6. When power comes on, the current drawn by RST starts to charge the capacitor. The voltage at RST is the difference between VCC and the capacitor voltage, and decreases from VCC as the capacitor charges. V_{RST} must remain above the lower threshold of the Schmitt trigger long enough to effect a complete reset. The time required is the oscillator start–up time, plus 2 machine cycles.

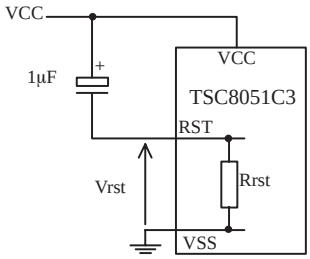


Figure 6 Power–on Reset Circuit

6.6. Oscillator Characteristics

XTAL1 and XTAL2 are respectively the input and output of an inverting amplifier which is configured for use as an on–chip oscillator. As shown in Figure 7, either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected as shown in Figure 8.

There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide–by–two flip–flop. The minimum high and low times specified on the data sheet must be observed however.

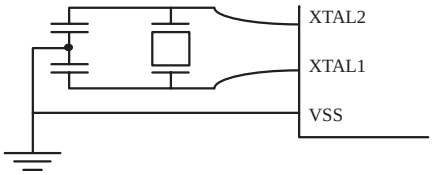


Figure 7 Crystal Oscillator

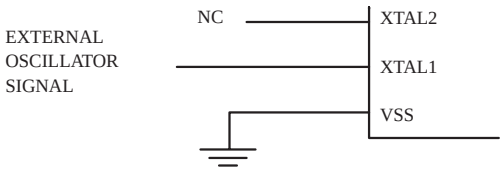


Figure 8 External Drive Configuration

6.7. Memory organization

The memory organisation of the TSC8051C3 is the same as in the 80C51, with the exception that the TSC8051C3 has 8Kbytes ROM, 256 bytes RAM, and additional SFRs. Details of the differences are given in the following paragraphs.

In the TSC8051C3, the lowest 8K of the 64K program memory address space is filled by internal ROM. Depending on the package used, external access is available or not. By tying the $\overline{EA}$ pin high, the processor fetches instructions from internal program ROM. Bus expansion for accessing program memory from 8K upward is automatic since external instruction fetches occur automatically when the program counter exceeds 1FFFh. If the $\overline{EA}$ pin is tied low, all program memory fetches are from external memory. The execution speed is the same regardless of whether fetches are from external or internal program memory. If all storage is on–chip, then byte location 1FFFh should be left vacant to prevent an undesired pre–fetch from external program memory address 2000h.

Certain locations in program memory are reserved for specific purposes. Locations 0000h to 0002h are reserved for the initialisation program. Following reset, the CPU always begins execution at location 0000h. Locations 0003h to 0033h are reserved for the six interrupt request service routines.

The internal data memory space is divided into a 256–bytes internal RAM address space and a 128 bytes special function register address space.The internal data RAM address space is from 0 to FFh. Four 8–bit register banks occupy locations 0 to 1Fh. 128 bit locations of the internal data RAM are accessible through direct addressing. These bits reside in 16 bytes of internal RAM at location 20h to 2Fh. The stack can be located anywhere in the internal data RAM address space by loading the 8–bit stack pointer (SP).

The SFR address space is from 80h to FFh. All registers except the program counter and the four 8–bit register banks reside in this address space. Memory mapping of the SFRs allows them to be accessed as easily as internal RAM, and as such, they can be operated on by most instructions. The mapping in the SFR address space of the 46 SFRs is shown in Table 3. The SFR names in italic are TSC8051C3 new SFRs and are described in Peripherals Functional Description section. The SFR names in bold are bit addressable.

Table 3 Special Function Register mapping

	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F
F8					*PWM8*	*PWM9*	*PWM10*	*PWM11*
F0	**B**				*PWM4*	*PWM5*	*PWM6*	*PWM7*
E8					*PWM0*	*PWM1*	*PWM2*	*PWM3*
E0	**ACC**				*EICON*	*SOCR*	*HWDR*	*MXCR0*
D8	***S1CON***	*S1STA*	*S1DAT*	*S1ADR*				*PWMCON*
D0	**PSW**							*MXCR1*
C8	***DCON***	*DDAT*						
C0								
B8	**IP**							
B0	**P3**							
A8	**IE**							
A0	**P2**							
98	**SCON**	SBUF						
90	**P1**							
88	**TCON**	TMOD	TL0	TL1	TH0	TH1	MSCON	
80	**P0**	SP	DPL	DPH				PCON

6.8. Interrupts

The TSC8051C3 has six interrupt sources, each of which can be assigned one of two priority levels. The five interrupt sources common to the 80C51 are the external interrupts (INT0 and INT1), the timer 0 and timer 1 interrupts (IT0 and IT1), and the SIO1 interrupt (SI). In the TSC8051C3, the standard serial I/O is called SIO0.

The fifth interrupt (the SIO0 interrupt) is generated by three different sources (see Figure 9): the DDC1 controller interrupt (DDI flag), the SIO0 interrupts (RI and TI flags).

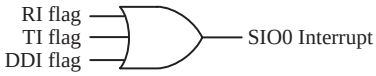


Figure 9 SIO0 Interrupt Sources

6.8.1. Interrupt Enable Register

Each interrupt source can be individually enabled or disabled by setting or clearing a bit in the IE: Interrupt Enable register (see Table 7). All interrupts sources can also be globally enabled or disabled by setting or clearing the EA bit in IE register.

6.8.2. Interrupt Priority Structure

Each interrupt source can be assigned one of two priority levels. Interrupt priority levels are defined by the IP: Interrupt Priority register (see Table 8). Setting a bit in the interrupt priority register selects a high priority interrupt, clearing it selects a low priority interrupt.

A low priority interrupt service routine may be interrupted by a high priority interrupt. A high priority interrupt service routine cannot be interrupted by any other interrupt source. If two requests of different priority levels occur simultaneously, the high priority level request is serviced. If requests of same priority are received simultaneously, an internal polling sequence determines which request is serviced. Thus, within each priority level, there is a second priority structure determined by the polling sequence according to Table 4.

Table 4 Interrupt priority source level

Order	Source	Priority Within Level
1	INT0	(highest)
2	Timer 0	↑
3	INT1	
4	Timer 1	
5	SIO0	↓
6	SIO1	(lowest)

6.8.3. Interrupt Handling

The interrupt flags are sampled at S5P2 of every machine cycle. The samples are polled during the following machine cycle. If one of the flags was in a set condition at S5P2 of the previous machine cycle, the polling cycle will find it and the interrupt system will generate a LCALL to the appropriate service routine, provided this hardware–generated LCALL is not blocked by any of the following conditions:

1. An interrupt of higher or equal priority is already in progress.
2. The current (polling) cycle is not the final cycle in the execution of the instruction in progress.
3. The instruction in progress is RETI or any access to the IE or IP SFR.

Any of these three conditions will block the generation of the LCALL to the interrupt service routine. Note that if an interrupt is active but not being responded to for one of the above conditions, if the flag is not still active when the blocking condition is removed, the denied interrupt will not be serviced. In other words, the facts that the interrupt flag was once active but not serviced is not memorized. Every polling cycle is new.

The processor acknowledges an interrupt request by executing a hardware–generated LCALL to the appropriate service routine. In some cases it also clears the flag that generated the interrupt, and in other case it does not. It clears the timer 0, timer 1, and external interrupt flags. An external interrupt flag (IE0 or IE1) is cleared only if it was transition–activated. All other interrupt flags are not cleared by hardware and must be cleared by the software. The LCALL pushes the contents of the program counter onto the stack (but it does not save the PSW) and reloads the PC with an address that depends on the source of the interrupt being vectored to according to Table 5.

Table 5 Interrupt vector address

Source	Vector Address
IE0	0003h
TF0	000Bh
IE1	0013h
TF1	001Bh
RI + TI + DCI	0023h
SI	002Bh

Execution proceeds from the vector address until the RETI instruction is encountered. The RETI instruction clears the ‘priority level active’ flip–flop that was set when this interrupt was acknowledged. It then pops two bytes from the the top of the stack and reloads the program counter with them. Execution of the interrupted program continues from where it was interrupted.

6.9. Registers

Table 6 PCON: Power Control register (87h)

7	6	5	4	3	2	1	0
SMOD	**–**	**–**	**PFRE**	**GF1**	**GF0**	**PD**	**IDL**

Bit Number	Bit Mnemonic	Description
7	SMOD	**Serial Port Mode bit** Set to select double baud rate in mode 1, 2 or 3.
6–5	–	**Reserved** Do not write 1 in these bits.
4	PFRE	**Power Fail Reset Enable bit** Set to enable power fail reset.
3	GF1	**General purpose Flag** Set by software for general purpose usage. Clear by software for general purpose usage.
2	GF0	**General purpose Flag** Set by software for general purpose usage. Clear by software for general purpose usage.

Bit Number	Bit Mnemonic	Description
1	PD	**Power Down mode bit** Set to enter power down mode. Clear by hardware when reset occurs.
0	IDL	**Idle mode bit** Set to enter idle mode. Clear by hardware when interrupt or reset occur.

If 1's are written to PD and IDL at the same time, PD takes precedence. PCON is read/write, its reset value is 0XX0 0000b. PFRE bit is not affected by internal reset sources.

Table 7 IE: Interrupt Enable register (A8h)

7	6	5	4	3	2	1	0
EA	**–**	**ES1**	**ES0**	**ET1**	**EX1**	**ET0**	**EX0**

Bit Number	Bit Mnemonic	Description
7	EA	**Enable All Interrup bit** Set to enable interrupts.
6	–	**Reserved** Do not write 1 in these bits.
5	ES1	**Enable SIO1 (I^2C) Interrupt** Set to enable SIO1 interrupt.
4	ES0	**Enable SIO0 (UART) Interrupt** Set to enable SIO0 interrupt.
3	ET1	**Enable Timer 1 Interrupt** Set to enable timer 1 interrupt.
2	EX1	**Enable External Interrupt 1** Set to enable external interrupt 1.
1	ET0	**Enable Timer 0 Interrupt** Set to enable timer 0 interrupt.
0	EX0	**Enable External Interrupt 0** Set to enable external interrupt 0.

IE is read/write and bit–addressable, its reset value is 0X00 0000b.

Table 8 IP: Interrupt Priority register (B8h)

7	6	5	4	3	2	1	0
–	**–**	**PS1**	**PS0**	**PT1**	**PX1**	**PT0**	**PX0**

Bit Number	Bit Mnemonic	Description
7–6	–	**Reserved** Do not write 1 in these bits.
5	PS1	**SIO1 (I^2C) Interrupt Priority Level** Set to select high priority level.
4	PS0	**SIO0 (UART) Interrupt Priority Level** Set to select high priority level.
3	PT1	**Timer 1 Interrupt Priority Level** Set to select high priority level.

Bit Number	Bit Mnemonic	Description
2	PX1	**External Interrupt 1 Priority Level** Set to select high priority level.
1	PT0	**Timer 0 Interrupt Priority Level** Set to select high priority level.
0	PX0	**External Interrupt 0 Priority Level** Set to select high priority level.

IP is read/write and bit–addressable, its reset value is XX00 0000b.

Peripherals Functional Description

For detailed functional description of standard 80C51 peripherals, please refer to C51 Family, Hardware Description and Programmer's Guides.

7. Security features

7.1. Watchdog Timer

The watchdog timer consists of a 4–bit timer with a 17–bit prescaler as shown in Figure 10. The prescaler is fed with a signal whose frequency is 1/12 the oscillator frequency (1MHz with a 12MHz oscillator).

The 4–bit timer is decremented every 'T' seconds, where: T= 12 x 131072 x 1/Fosc. Thus, the interval may vary from Tmin to Tmax depending on the frequency (see Table 9) in 16 possible steps (see Table 10).

The watchdog timer has to be reloaded (write to HWDR) within periods that are shorter than the programmed watchdog interval, otherwise the watchdog timer will underflow and a system reset will be generated which will reset the TSC8051C3.

Table 9 Watchdog timer limit value

Fosc	12 MHz	16 MHz
T= Tmin	131.07 ms	98.30 ms
Tmax	2097.1ms	1572.9 ms

Table 10 Watchdog timer interval value

WT3	WT2	WT1	WT0	Interval
0	0	0	0	T x 16
0	0	0	1	T x 1
0	0	1	0	T x 2
:	:	:	:	:
:	:	:	:	:
1	1	1	1	T x 15

Once the watchdog timer is enabled by setting WTE bit, it cannot be disabled anymore, except by a system reset.

The watchdog timer is frozen during idle or power down mode.

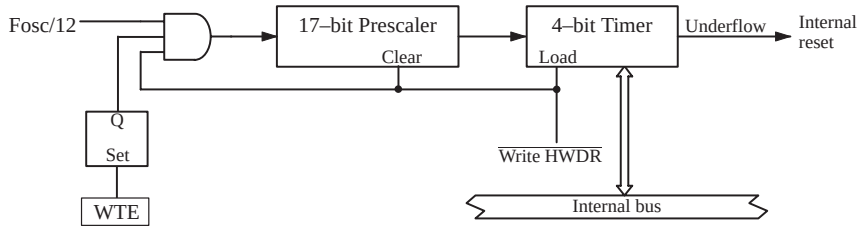


Figure 10 Watchdog timer block diagram

7.2. Power Fail Reset

The TSC8051C3 implements a programmable power fail reset mechanism that avoids the microcontroller running while VCC is under working voltage (see Figure 12). This system generates an internal reset when VCC falls: during VCC failure or power supply switch off.

When VCC falls below VLOW (see DC Electrical Characteristics), reset is asserted and maintained until power supply is completely off. If VCC rises above VLOW, reset is maintained during at least 2 machine cycles to be well detected by the CPU core. To avoid spurious reset, power glitches of pulses width less than 2 to 3 f_{OSC} periods are filtered out (see Figure 11).

The PFR must be enabled by setting PFRE bit in PCON register bit location 4 (see Idle and Power Down Operation section).

The PFR is disabled during Idle and power down modes. Since it is enabled, PFR can no longer be disabled by software. Writing 0 to PFRE bit has no effect, the only way to clear the PFRE bit is to apply an external reset. To avoid period during which PFR is disabled, internal reset sources do not disable PFR.

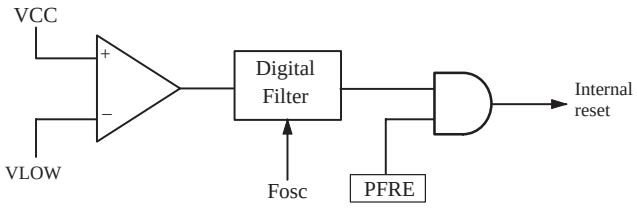


Figure 11 Power Fail Reset block diagram

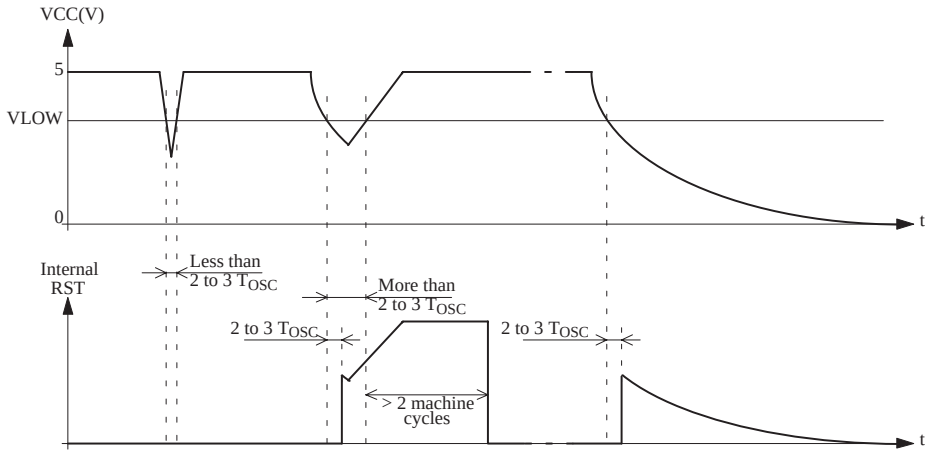


Figure 12 Power Fail Reset timing diagram

7.3. Registers

Table 11 HWDR: Watchdog Timer Control register (E6h)

7	6	5	4	3	2	1	0
WTE	**–**	**–**	**–**	**WT3**	**WT2**	**WT1**	**WT0**

Bit Number	Bit Mnemonic	Description
7	WTE	**Watchdog Timer Enable bit** Set to enable watchdog timer operation. Clearing this bit does not disable watchdog timer.
6–4	–	**Reserved** Do not write 1 in these bits.
3–0	WT3–WT0	**Watchdog Timer Interval** See Table 10.

HWDR is read/write, its reset value is 0XXX 0000b.

8. Pulse Width Modulated Outputs

The TSC8051C3 contains twelve pulse width modulated output channels. These channels generate pulses of programmable duty cycle with an 8–bit resolution.

Figure 13 shows the PMW block diagram. The 8–bit counter counts modulo 256 by default i.e., from 0 to 255 inclusive but can count modulo 254 i.e., from 0 to 253 inclusive by programming CMOD bit in PWMCON (see Table 18). The counter clock is supplied by the oscillator frequency. Thus, the repetition frequency Fpwm is constant and equals to the oscillator frequency divided by 256 or 254 (see Table 12). The 8–bit counter is common to all PWM channels, its value is compared to the contents of the twelve registers: PWM0 to PWM11. Provided the content of each of these registers is greater than the counter value, the corresponding output is set low. If the contents of these registers are equal to, or less than the counter value the output will be high.

The pulse–width ratio is therefore defined by the contents of these registers, and is in the range of 0 (all ‘0’ written to PWM register) to 255/256 or 1 (all ‘1’ written to PWM register) and may be programmed in increments of 1/256 or 1/254. When the 8–bit counter counts modulo 254, it can never reach the value of the PWM registers when they are loaded with FEh or FFh.

When a compare register PWM0 to PWM11 (see Table 15) is loaded with a new value, the associated output is updated immediately. It does not have to wait until the end of the current counter period. All the PWM outputs are open–drain outputs with standard current drive and standard maximum voltage capability. When they are disabled, eight of them (PWM0 to PWM7) are in high impedance while the other four (PWM8 to PWM11) are standard Port outputs with internal pull–ups.

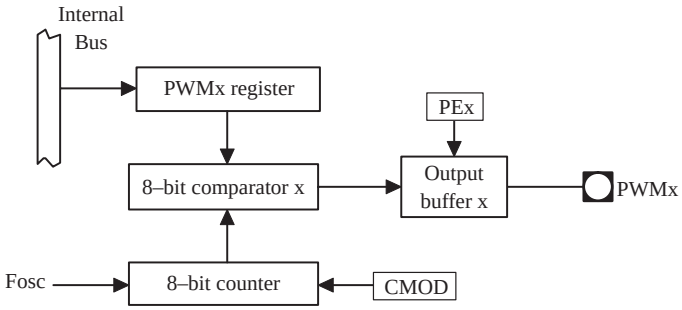


Figure 13 Pulse width modulated outputs block diagram

Table 12 PWM repetition frequency

Fosc		12 MHz	16 MHz
Fpwm	CMOD= 0	46.875 KHz	62.5 KHz
	CMOD= 1	47.244 KHz	63 KHz

Two 8–bit enable registers: MXCR0 and MXCR1 are used to enable or disable PWM outputs. MXCR0 is used to control PWM0 to PWM7 (see Table 16) and MXCR1 is used to control PWM8 to PWM11 (see Table 17), these PWMs are multiplexed with PORT 1 as described in Table 13.

PWM will not operate in idle and power down modes (frozen counter). When idle or power down mode is entered, the PWM0 to PWM7 output pins are floating and PWM8 to PWM11 pins are set to general purpose P1 port with the value of P1 SFR.

Table 13 PWM alternate pins

Channel	Pin assignment
PWM8	P1.0
PWM9	P1.1
PWM10	P1.2
PWM11	P1.3

Table 14 PWM SFR register addresses

Channel	SFR address
PWM0	ECh
PWM1	EDh
PWM2	EEh
PWM3	EFh
PWM4	F4h
PWM5	F5h
PWM6	F6h
PWM7	F7h
PWM8	FCh
PWM9	FDh
PWM10	FEh
PWM11	FFh

Figure 14 shows a PWM programming example with PWM register content 55h and counter modulo 256.

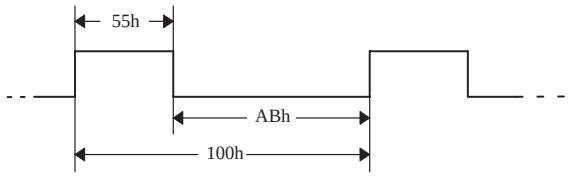


Figure 14 PWM programming example

8.1. Registers

Table 15 PWMx: Pulse Width Modulator register x (see Table 14 for address)

7	6	5	4	3	2	1	0
PW7	**PW6**	**PW5**	**PW4**	**PW3**	**PW2**	**PW1**	**PW0**

Bit Number	Bit Mnemonic	Description
7–0	PW7–PW0	**8–bit PWMx register value.**

PWMx are write only, their reset value is 00h.

Table 16 MXCR0: PWM Enable register 0 (E7h)

7	6	5	4	3	2	1	0
PE7	**PE6**	**PE5**	**PE4**	**PE3**	**PE2**	**PE1**	**PE0**

Bit Number	Bit Mnemonic	Description
7–0	PE7–PE0	**PWM7 to PWM0 Enable bit** Set to enable PWM7 to PWM0 output. Clear to disable PWM7 to PWM0 output.

MXCR0 is read/write, its reset value is 00h.

Table 17 MXCR1: PWM Enable register 1 (D7h)

7	6	5	4	3	2	1	0
–	–	–	–	**PE11**	**PE10**	**PE9**	**PE8**

Bit Number	Bit Mnemonic	Description
7–4	–	**Reserved** Do not write 1 in these bits.
3–0	PE11–PE8	**PWM11 to PWM8 Enable bit** Set to enable PWM11 to PWM8 output. Clear to disable PWM11 to PWM8 output.

MXCR1 is read/write, its reset value is X0h.

Table 18 PWMCON: PWM Control register (DFh)

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	**CMOD**

Bit Number	Bit Mnemonic	Description
7–1	–	**Reserved** Do not write 1 in these bits.
0	CMOD	**Counter Modulo bit** Set to select modulo 254. Clear to select modulo 256.

PWMCON is read/write, its reset value is XXXX XXX0b.

9. Synchronization Processor

9.1. Overview

The features of the sync processor include software polarity detection, Hsync and Vsync signals counting using Timer 0, programmable sync signals inputs and outputs, and horizontal clamp pulse generator.

The CPU interfaces to the sync processor logic via the following two 8–bit special function registers: SOCR, the Synchronization Output Control register (see Table 20) and EICON, the External Input Control register (see Table 21).

9.2. Hsync and Vsync Outputs

SOCR is used to configure P3.3 and P3.5 pins as buffered Vsync and Hsync outputs or as general purpose I/Os. When either Hsync or Vsync is selected, the output level can be respectively programmed as P3.4 or P3.2 input level (inverted or not), or as a low level if not enabled. Figure 15 shows the programmable Hsync and Vsync output block diagram.

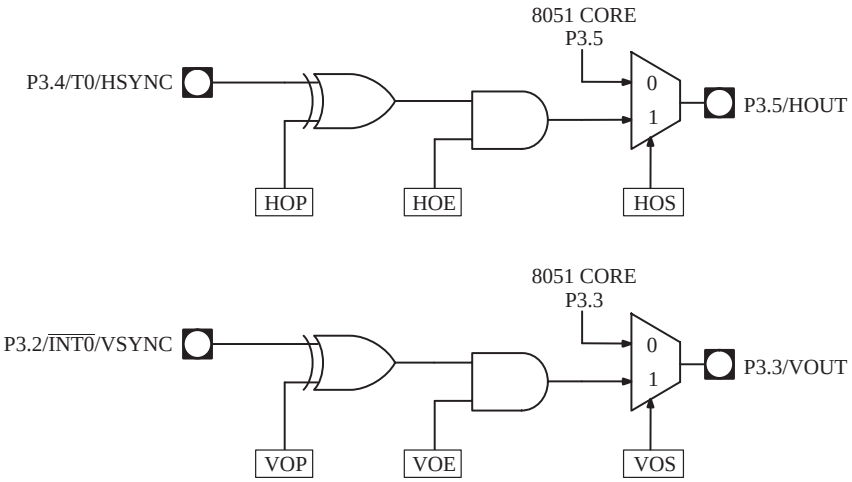


Figure 15 Hsync and Vsync Outputs Block Diagram

9.3. Hsync and Vsync Inputs

I0L bit in EICON is used to control $\overline{INT0}$/VSYNC input. Thus, an interrupt on either falling or rising edge and on either high or low level can be requested. Figure 16 shows the programmable $\overline{INT0}$/VSYNC input block diagram.

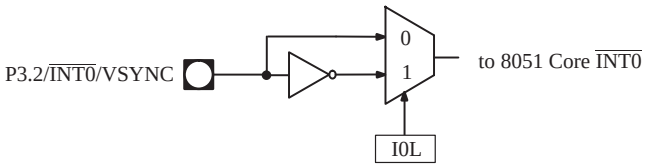


Figure 16 $\overline{INT0}$/VSYNC Input Block Diagram

T0L and T0S bits in EICON are used to control T0/HSYNC input as short pulses input capture to be able to count them with timer 0. Pulse duration shorter than 1 clock period is rejected; depending on the position of the sampling point in the pulse, pulse duration longer than 1 clock period and shorter than 2 clock period may be rejected or accepted; and pulse duration longer than 2 clock period is accepted. Moreover selection of negative or positive pulses can be programmed.

Accepted pulse is lengthened up to 1 cycle period to be sampled by the 8051 core (one time per machine cycle: 12 clock periods), this implies that the maximum pulse frequency is unchanged and equal to $f_{OSC}/24$. Figure 17 shows the programmable T0/HSYNC input block diagram. The Digital Timer Delay samples T0/HSYNC pulses and rejects or lengthens them.

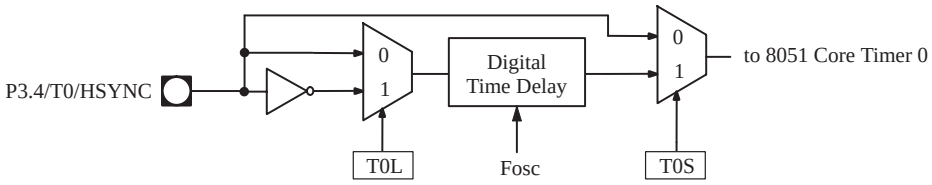


Figure 17 T0/HSYNC Input Block Diagram

9.4. Horizontal Clamp Pulse Output

The TSC8051C3 provides fully programmable clamp pulse output signal to pre–amplifier IC. User can program a pulse with positive or negative polarity at either the falling or rising edge of the HSYNC signal depending on its polarity.

Figure 18 shows the CPO block diagram. CPE bit in SOCR is used to configure P1.4 pin as general purpose I/O or as open drain clamp pulse output, so enables the CPO. CPP bit in SOCR is used to select the clamp pulse signal polarity. Depending on the HSYNC polarity selected by the T0L bit, Clamp pulse is generated on the falling edge (negative polarity) or on the rising edge (positive polarity) as shown in Figure 19.

The clamp pulse duration depends on the oscillator frequency by the following formula:

Tcpo= Tosc · (6.5 ± 0.5) (see Table 19).

Table 19 Clamp pulse width

Fosc	12 MHz	16 MHz
Tcpo	542 ± 42 ns	406 ± 31 ns

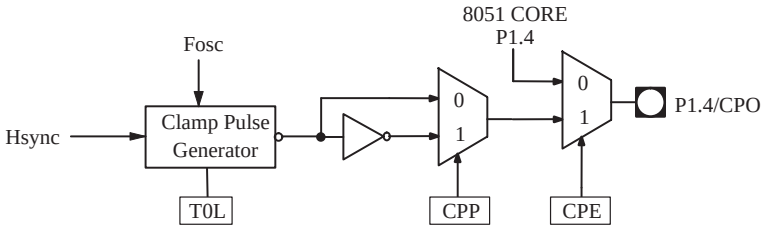


Figure 18 Clamp pulse output block diagram

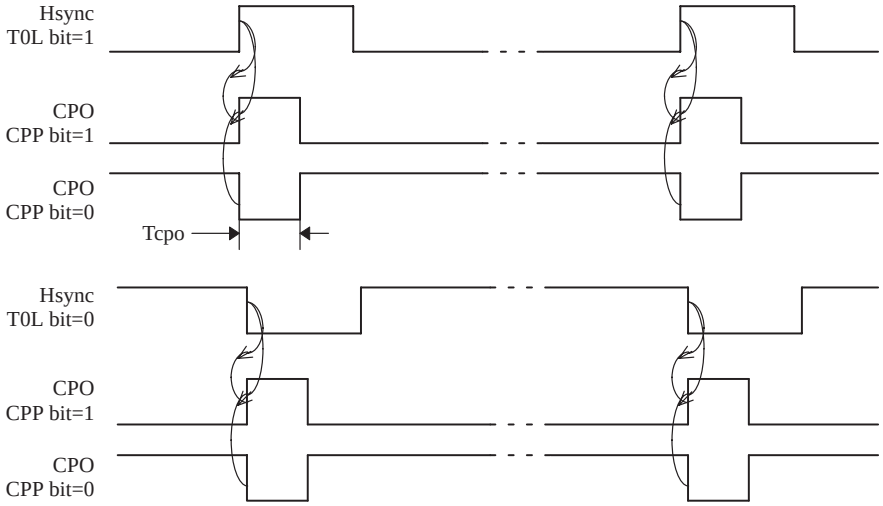


Figure 19 Clamp pulse output waveform

9.5. Registers

Table 20 SOCR: Synchronization Output Control register (E5h)

7	6	5	4	3	2	1	0
CPP	**CPE**	**VOS**	**HOS**	**VOP**	**VOE**	**HOP**	**HOE**

Bit Number	Bit Mnemonic	Description
7	CPP	**Clamp Pulse Polarity bit** Set to select positive polarity pulses. Clear to select negative polarity pulses.
6	CPE	**Clamp Pulse Enable bit** Set to enable CPO output. Clear to enable P1.4 I/O port.
5	VOS	**Vsync Output Selection bit** Set to enable Vsync output. Clear to enable P3.3 I/O port.
4	HOS	**Hsync Output Selection bit** Set to enable Hsync output. Clear to enable P3.5 I/O port.
3	VOP	**Vsync Output Polarity bit** Set to output inverted Vsync signal. Clear to output Vsync signal.
2	VOE	**Vsync Output Enable bit** Set to enable Vsync signal.
1	HOP	**Hsync Output Polarity bit** Set to output inverted Hsync signal. Clear to output Hsync signal.
0	HOE	**Hsync Output Enable bit** Set to enable Hsync signal output.

SOCR is read/write, its reset value is 0000 0000b.

Table 21 EICON: External Input Control register (E4h)

7	6	5	4	3	2	1	0
–	**–**	**–**	**–**	**–**	**T0L**	**T0S**	**I0L**

Bit Number	Bit Mnemonic	Description
7–3	–	**Reserved** Do not write 1 in these bits.
2	T0L	**T0/HSYNC Input Level bit** Set to capture positive Hsync pulse. Clear to capture negative Hsync pulse.
1	T0S	**T0/HSYNC Input Selection bit** Set to select short pulse capture on T0/HSYNC input. Clear to select standard T0/HSYNC input.
0	I0L	**$\overline{\text{INT0}}$/VSYNC Input Level bit** Set to input inverted Vsync signal. Clear to input Vsync signal.

EICON is read/write, its reset value is XXXX X000b.

10. DDC Controller

10.1. Overview

The VESA Data Display Channel (DDC) specification defines two classes of monitors: DDC1/2B and DDC1/2AB. DDC1/2B store monitor capability information in an I^2C device. This type of monitor does not support remote control. DDC1/2AB are ACCESS.bus devices. They can provide greater capability information and allow the host to control monitor features remotely. TSC8051C3 provides only DDC1 and DDC2B capability.

DDC1 is a uni–directional channel from display to host. The 128 bytes of the Extended Display Identification Data frame (EDID) are continuously transferred from the display to the host on the serial line (DSDA), clocked by Vsync signal.

DDC2 is a bi–directional data channel between display and host based on the I^2C bus. DDC2B is a simple protocol to read the EDID frame.

The DDC hardware is composed of the DDC1 hardware and the DDC2B hardware. Figure 20 shows the DDC implementation block diagram. DDC1 hardware is supported by a specific controller. The DDC2B hardware is a simple link from DDC pins to I^2C pins on which E^2PROM is connected.

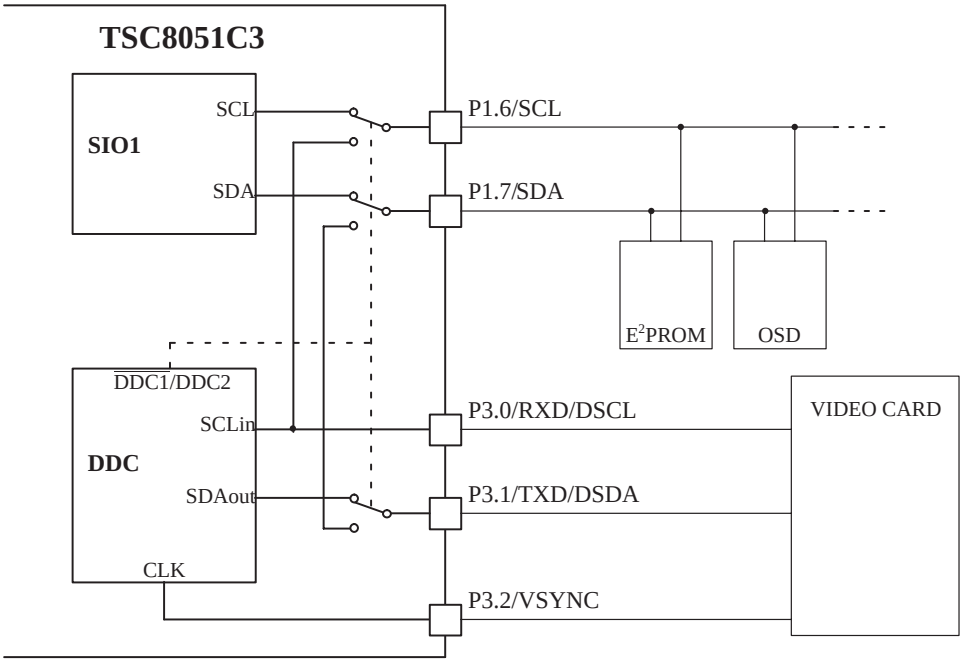
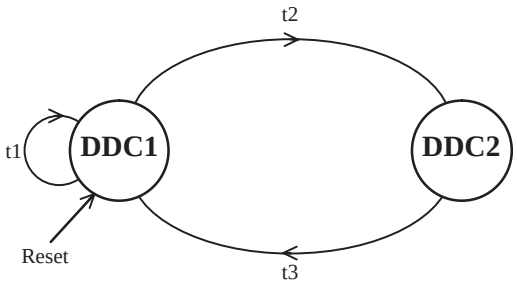


Figure 20 DDC implementation block diagram

When monitor is in DDC1 mode, data from the EDID frame are serially clocked out to DSDA line on the rising edge of the Vsync input signal. The data stream is sent in 9–bit packet which includes a null bit (9th bit) as packet separator. (see Figure 25).

When a falling edge is detected on DSCL line, the monitor switches from DDC1 to DDC2 mode (see Figure 26). In DDC2 mode, an hardware link is closed between DSCL to SCL line and DSDA to SDA line. Thus, video card has a direct access to E^2PROM and can get the EDID frame at the host bit–rate without any latency time. After 128 Vsync pulses while the DSCL line is idle (no more DDC2 transfer) monitor reverts to DDC1 mode and continues to send the EDID frame. Figure 21 shows the DDC1 to DDC2 and DDC2 to DDC1 transitions.



Transitions :

t1: Data interrupt request

t2: DSCL falling edge

t3: 128 Vsync pulses time–out

Figure 22 DDC1 / DDC2 transitions state machine

10.2. Operation

The CPU interfaces to the DDC hardware via the following two 8–bit special function registers: DCON the DDC Control register (see Table 22) and DDAT the DDC1 Data register (see Table 23). Figure 23 shows the DDC hardware block diagram.

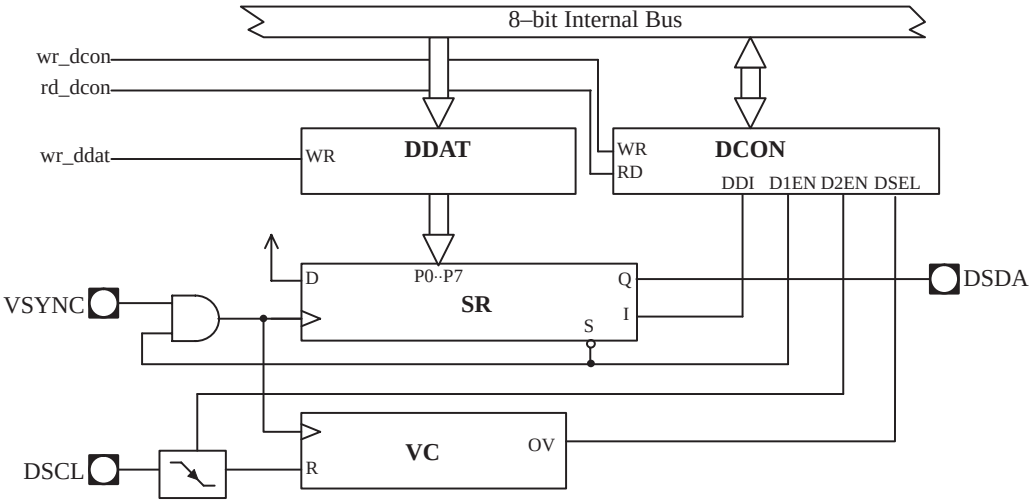


Figure 23 DDC hardware block diagram

10.2.1. Enabling DDC

The DDC is enabled by setting the D1EN and D2EN bits in DCON. After reset, DDC1 mode is enabled (DSEL= 0), DDAT is empty, its content is undefined. Prior to enable DDC, first data of the EDID frame must be loaded in DDAT. Thus, when D1EN is set this data is loaded in the shift register on the first Vsync rising edge and is shifted out on the next rising edges (see Figure 24). If no Vsync is present, the DSDA line is released, (high level).

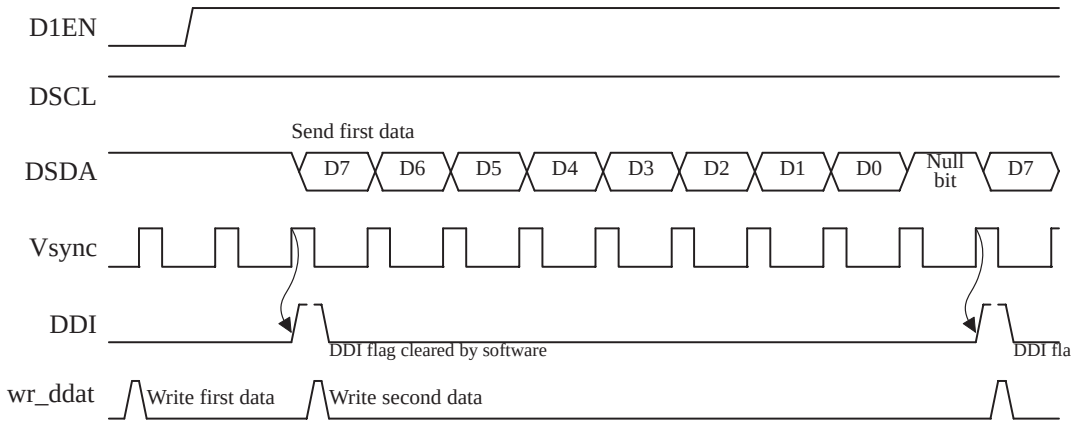


Figure 24 DDC1 start transfer timing diagram

10.2.2. Sending EDID data frame

As soon as DDAT becomes empty (after transfer to the Shift register), DDI flag is set and generates an interrupt (if ES1 and EA set in IE SFR), this informs user to load the next data of the EDID frame in DDAT and to clear the DDI flag to acknowledge interrupt (see Figure 25).

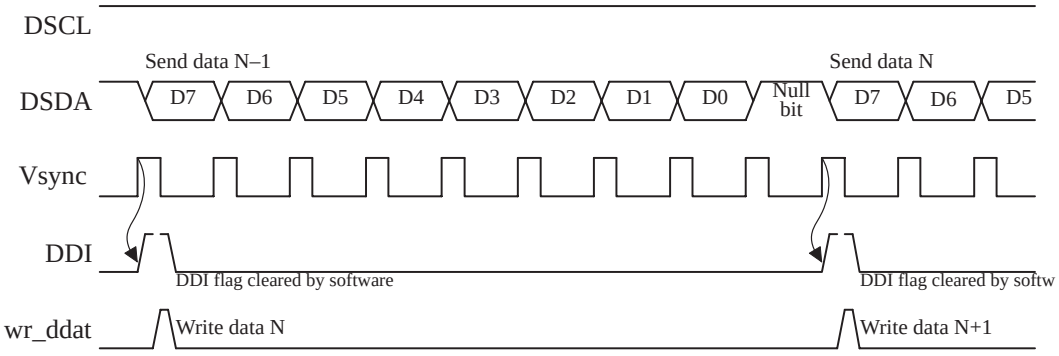


Figure 25 DDC1 byte transfer timing diagram

10.2.3. DDC1 to DDC2 Transition

Once DDC2 enabled, when a falling edge is detected on DSCL line, DDC2 mode is entered (DSEL is set), DDC2 link is established releasing DSDA line (see Figure 26).

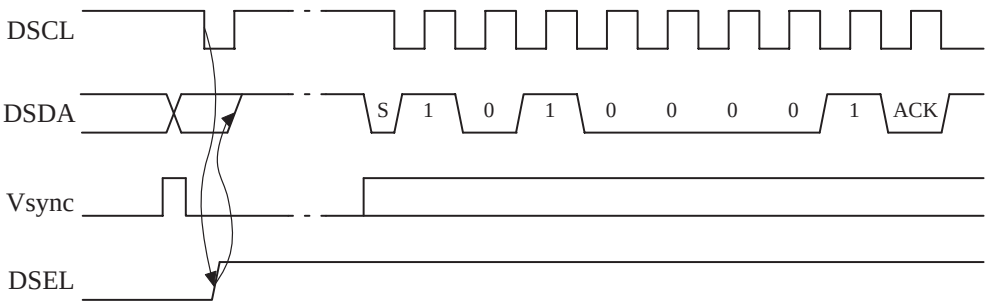


Figure 26 DDC1 to DDC2 mode transition timing diagram

10.2.4. DDC1 mode recovery

The DDC hardware reverts to DDC1 (DSEL= 0) after 128 Vsync pulses while the DSCL line is idle (see Figure 27).

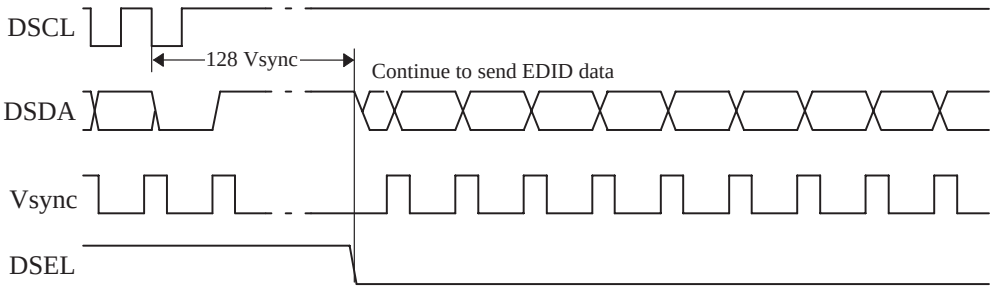


Figure 27 DDC1 mode recovery

10.2.5. DDC interrupts

The DDC hardware shares the same interrupt than UART: the SIO0 interrupt. This interrupt is generated by the RI or TI flags in SCON (UART interrupt) or by DDI flags in DCON (DDC1 interrupt). When DDI flag is set, user must load DDAT register with the next EDID data byte and then clear this flag.

10.2.6. DDC1 timing waveforms

Figure 28 shows the DDC1 timing waveform. Data is clocked on the rising edge of Vsync and shall be valid 30 µs after the rising edge, it shall remain valid until the next rising edge. The minimum time between the falling edge of the clock and the next rising edge shall be 20 µs. The minimum clock pulse high time shall be 20 µs. For DDC1 operation, Vsync shall start at the normal frame frequency. Once data is sensed on the data line, Vsync may be increased to a maximum of 25KHz.

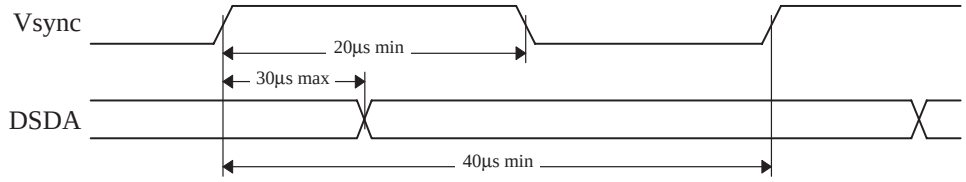


Figure 28 DDC1 timing waveform

10.3. Registers

Table 22 DCON: DDC Control register (C8h)

7	6	5	4	3	2	1	0
–	–	–	–	D2EN	DSEL	DDI	D1EN

Bit Number	Bit Mnemonic	Description
7–4	–	**Reserved** Do not write 1 in these bits.
3	D2EN	**DDC2 Enable bit** Set to enable DDC2 recognition (DSCL falling edge detection) and DDC2 activation. Clear to disable DDC2 controller.
2	DSEL	**DDC Selection bit** Set by hardware when DDC2 mode is activated (falling edge detected on DSCL line). Cleared by hardware when DDC1 mode is activated: after DDC2 time–out. Can be set or cleared by software to provide direct E^2PROM access during manufacturing set–up.
1	DDI	**DDC1 Data Interrupt Flag** Set by hardware after DDC1 data register is transferred to the shift register. Clear to acknowledge interrupt after DDC1 data register is loaded.
0	D1EN	**DDC1 Enable bit** Set to enable DDC controller. Clear to disable DDC controller.

DCON is read/write and bit addressable, its reset value is XXXX 0000b.

Table 23 DDAT: DDC1 data register (C9h)

7	6	5	4	3	2	1	0
DD7	DD6	DD5	DD4	DD3	DD2	DD1	DD0

Bit Number	Bit Mnemonic	Description
7–0	DD7–DD0	**DDC1 Data byte** Load with an EDID byte to send to host.

DDAT is read/write, its reset value is XXh.

11. SIO1 the I²C Controller

11.1. Overview

The I²C bus is a bi–directional two–wire serial communication standard. It is designed primarily for simple but efficient inter–integrated circuit (I²C) control. The bus is made of two lines: one Serial Clock (SCL) and one Serial Data (SDA) that carry information between the ICs connected to them. The serial data transfer is limited to 100kbit/s in basic mode. Various communication configuration can be designed using this bus; however, the TSC8051C3 implements the four standard master and slave transfer modes with multimaster capability. All the devices connected to the bus can be either master or slave. Figure 29 shows a typical I²C bus configuration using TSC8051C3 in monitor.

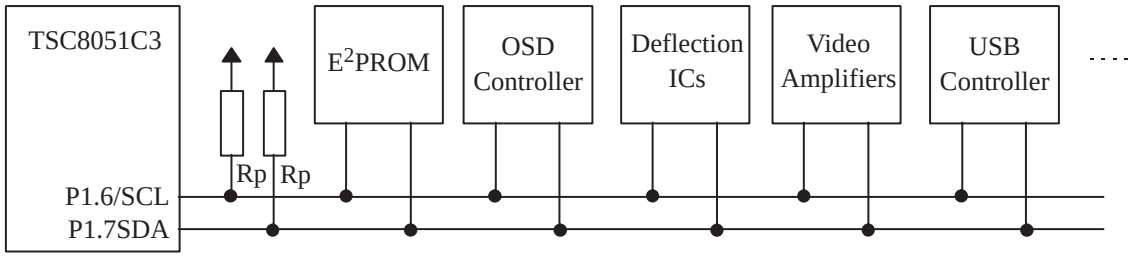


Figure 29 Typical I²C Bus Configuration

11.2. Operation

The CPU interfaces to the I²C logic via the following four 8–bit special function registers: S1CON the Synchronous Serial Control register (see Table 30); S1DAT the Synchronous Serial Data register (see Table 31); S1STA the Synchronous Serial Status register (see Table 32) and S1ADR, the Synchronous Serial Address register (see Table 33).

The SIO1 logic interfaces to the external I²C bus via two port 1 pins: P1.6/SCL and P1.7/SDA. The output latches of P1.6 and P1.7 must be set to logic 1 in order to enable SIO1 (alternate functions).

S1CON is used to enable the I²C interface, to program the bit rate (see Table 24), to enable slave modes, to acknowledge or not a received data, to send a START or a STOP condition on the I²C bus, and to acknowledge a serial interrupt. An hardware reset disables SIO1.

S1STA contains a status code which reflects the status of the I²C logic and the I²C bus. The three least significant bits are always zero. The five most significant bits contain the status code. There are 26 possible status code. When S1STA contains F8h, no relevant state information is available and no SIO1 interrupt is requested. A valid status code is available in S1STA one machine cycle after the Synchronous Serial Interrupt flag (SI) is set by hardware and is still present one machine cycle after SI has been reset by software. Table 25 to Table 29 give the status for the master modes, the slave modes and miscellaneous states.

S1DAT contains a serial data byte to be transmitted or a byte which has just been received. It is addressable while it is not in process of shifting a byte. This occurs when I²C logic is in a defined state and SI is set. Data in S1DAT remains stable as long as SI is set. While data is being shifted out, data on the bus is simultaneously shifted in; S1DAT always contains the last byte present on the bus.

S1ADR may be loaded with the 7–bit slave address (7 most significant bits) to which SIO1 will respond when programmed as a slave transmitter or receiver. The LSB is used to enable general call address (00h) recognition.

Figure 30 shows how a data transfer is accomplished on the I²C bus.

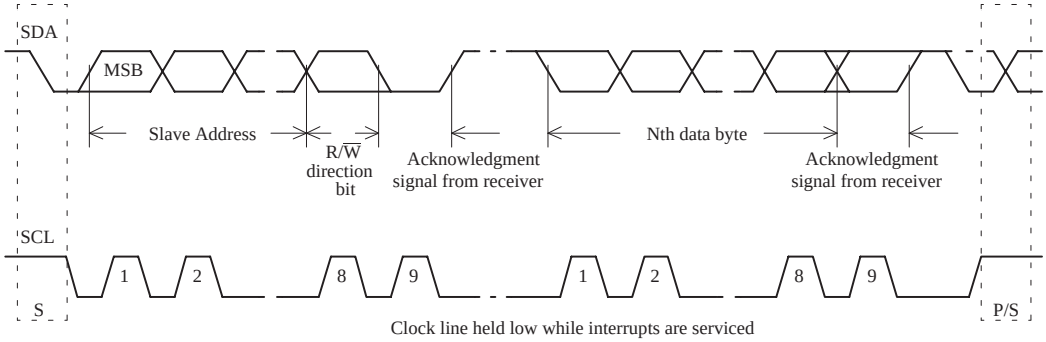


Figure 30 Complete data transfer on I^2C bus

The four operating modes are:

- Master Transmitter
- Master Receiver
- Slave Transmitter
- Slave Receiver

Data transfer in each mode of operation are shown in Figure 31 to Figure 34. These figures contain the following abbreviations:

A	Acknowledge bit (low level on SDA)
$\overline{A}$	Not acknowledge bit (high level on SDA)
Data	8–bit data byte
P	Stop condition
MR	Master Receive
MT	Master Transmit
S	Start condition
SLA	Slave Address
GCA	General Call Address (00h)
R	Read bit (high level on SDA)
W	Write bit (low level on SDA)

In these figures, circles are used to indicate when SI is set. The numbers in the circles show the status code held in S1STA. At each point, a proper service routine must be executed to continue or complete the serial transfer. These service routines are not critical since the serial transfer is suspended until SI is cleared by software.

When the serial interrupt routine is entered, the status code in S1STA is used to branch to the appropriate service routine. For each status code, the required software action and details of the following serial transfer are given in Table 25 to Table 28.

11.2.1. Master transmitter mode

In the master transmitter mode, a number of data bytes are transmitted to a slave receiver (see Figure 31). Before the master transmitter mode can be entered, S1CON must be initialized as follows:

CR2	S1E	STA	STO	SI	AA	CR1	CR0
bit rate	1	0	0	0	X	bit rate	bit rate

CR0, CR1 and CR2 select one predefined serial bit rate. S1E must be set to enable I^2C interface. STA, STO and SI must be cleared.

The master transmitter mode may now be entered by setting the STA bit. The I^2C logic will now test the I^2C bus and generate a START condition as soon as the bus becomes free. When a START condition is transmitted, SI is set, and the status code in S1STA will be 08h. This status must be used to vector to an interrupt routine that loads S1DAT with the slave address and the data direction bit (SLA+W). SI must then be cleared before the serial transfer can continue.

When the slave address and the direction bit have been transmitted and an acknowledgement bit has been received, SI is set again and a number of status code in S1STA are possible: 18h, 20h or 38h for the master mode and also 68h, 78h or B0h if the slave mode was enabled (AA bit set). The appropriate action to be taken for each of these status code is detailed in Table 25. This scheme is repeated until a STOP condition is transmitted.

S1E, CR2, CR1 and CR0 are not affected by the serial transfer and are not referred to in Table 25. After a repeated START condition (state 10h) I^2C logic may switch to the master receiver mode by loading S1DAT with SLA+R.

11.2.2. Master receiver mode

In the master receiver mode, a number of data bytes are received from a slave transmitter (See Figure 32). The transfer is initialized as in the master transmitter mode. When the START condition has been transmitted, the service routine must load S1DAT with the 7–bit slave address and the data direction bit (SLA+R). SI must then be cleared before the serial transfer can continue.

When the slave address and the direction bit have been transmitted and an acknowledgement bit has been received, SI is set again and a number of status code in S1STA are possible: 40h, 48h or 38h for the master mode and also 68h, 78h or B0h if the slave mode was enabled (AA bit set). The appropriate action to be taken for each of these status code is detailed in Table 26. This scheme is repeated until a STOP condition is transmitted.

S1E, CR2, CR1 and CR0 are not affected by the serial transfer and are not referred to in Table 26. After a repeated START condition (state 10h) I^2C logic may switch to the master transmitter mode by loading S1DAT with SLA+W.

11.2.3. Slave receiver mode

In the slave receiver mode, a number of data bytes are received from a master transmitter (see Figure 33). To initiate the slave receiver mode, S1ADR and S1CON must be loaded as follows:

A7	A6	A5	A4	A3	A2	A1	GC
◄			own slave address			►	

The upper 7 bits are the address to which SIO1 will respond when addressed by a master. If the LSB (GC) is set SIO1 will respond to the general call address (00h); otherwise it ignores the general call address.

CR2	S1E	STA	STO	SI	AA	CR1	CR0
bit rate	1	0	0	0	1	bit rate	bit rate

CR0, CR1 and CR2 have no effect in the slave mode. S1E must be set to enable SIO1. The AA bit must be set to enable the own slave address or the general call address recognition. STA, STO and SI must be cleared.

When S1ADR and S1CON have been initialized, SIO1 waits until it is addressed by its own slave address followed by the data direction bit which must be logic 0 (W) for SIO1 to operate in the slave receiver mode. After its own slave address and the W bit have been received, SI is set and a valid status code can be read from S1STA. This status code is used to vector to an interrupt service routine, and the appropriate action to be taken for each of these status code is detailed in Table 27. The slave receiver mode may also be entered if arbitration is lost while SIO1 is in the master mode (see states 68h and 78h).

If the AA bit is reset during a transfer, SIO1 will return a not acknowledge (logic 1) to SDA after the next received data byte. While AA is reset, SIO1 does not respond to its own slave address. However, the I^2C bus is still monitored and address recognition may be resume at any time by setting AA. This means that the AA bit may be used to temporarily isolate SIO1 from the I^2C bus.

11.2.4. Slave transmitter mode

In the slave transmitter mode, a number of data bytes are transmitted to a master receiver (see Figure 34). Data transfer is initialized as in the slave receiver mode. When S1ADR and S1CON have been initialized, SIO1 waits until it is ad-

dressed by its own slave address followed by the data direction bit which must be logic 1 (R) for SIO1 to operate in the slave transmitter mode. After its own slave address and the R bit have been received, the serial interrupt flag is set and a valid status code can be read from S1STA. This status code is used to vector to an interrupt service routine, and the appropriate action to be taken for each of these status code is detailed in Table 28. The slave transmitter mode may also be entered if arbitration is lost while SIO1 is in the master mode (see state B0h).

If the AA bit is reset during a transfer, SIO1 will transmit the last byte of the transfer and enter state C0h or C8h. SIO1 is switched to the not addressed slave mode and will ignore the master receiver if it continues the transfer. Thus the master receiver receives all 1's as serial data. While AA is reset, SIO1 does not respond to its own slave address. However, the I^2C bus is still monitored and address recognition may be resume at any time by setting AA. This means that the AA bit may be used to temporarily isolate SIO1 from the I^2C bus.

Table 24 Serial clock rates

CR2	CR1	CR0	Bit frequency (kHz)		F_{OSC} divided by
			F_{OSC}= 12MHz	F_{OSC}= 16MHz	
0	0	0	47	62.5	256
0	0	1	53.5	71.5	224
0	1	0	62.5	83	192
0	1	1	75	100	160
1	0	0	12.5	16.5	960
1	0	1	100	–	120
1	1	0	–	–	60
1	1	1	0.5 < . < 62.5	0.67 < . < 83	96 · (256 – reload value Timer 1) (reload value range: 0–254 in mode 2)

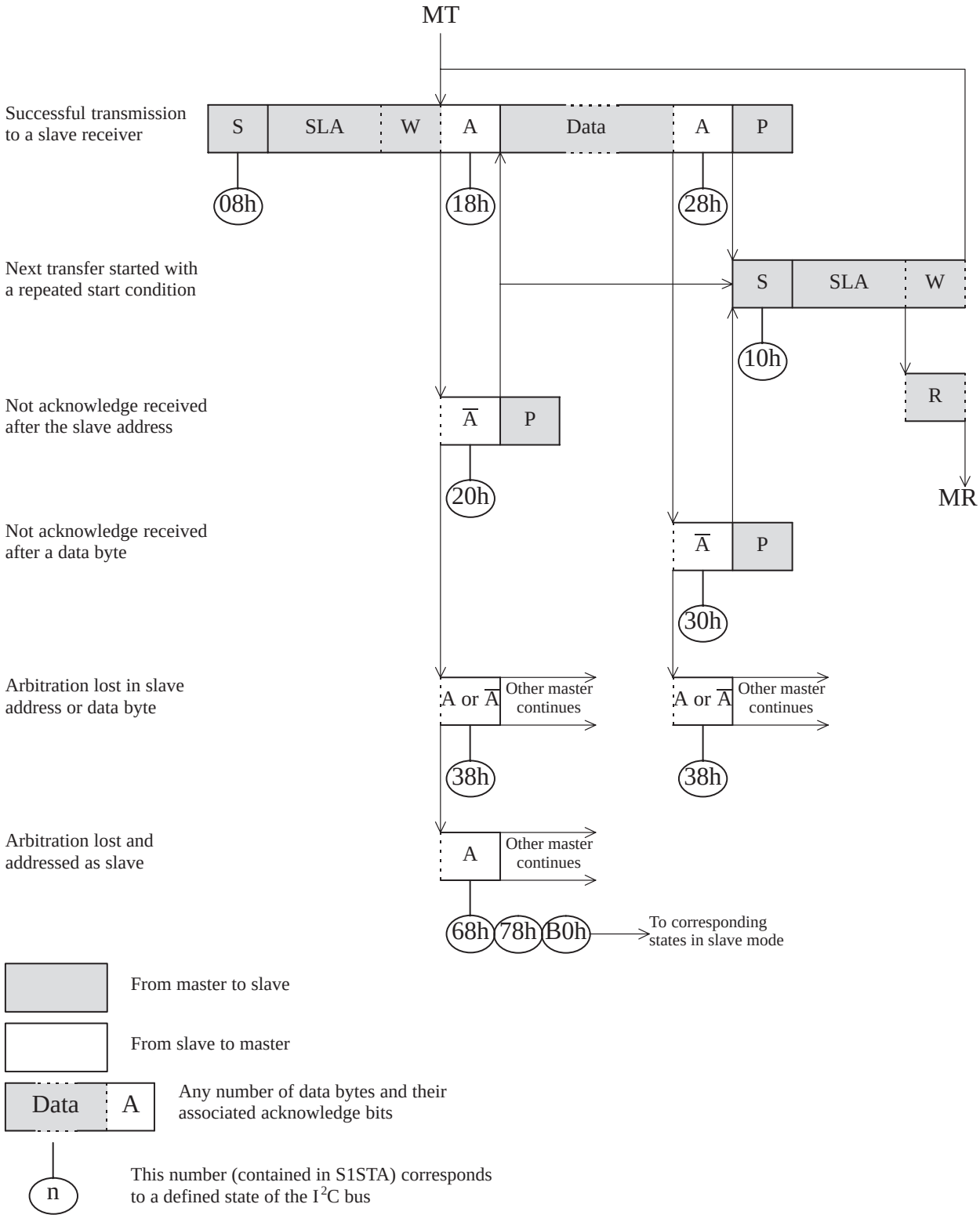


Figure 31 Format and States in the master transmitter mode

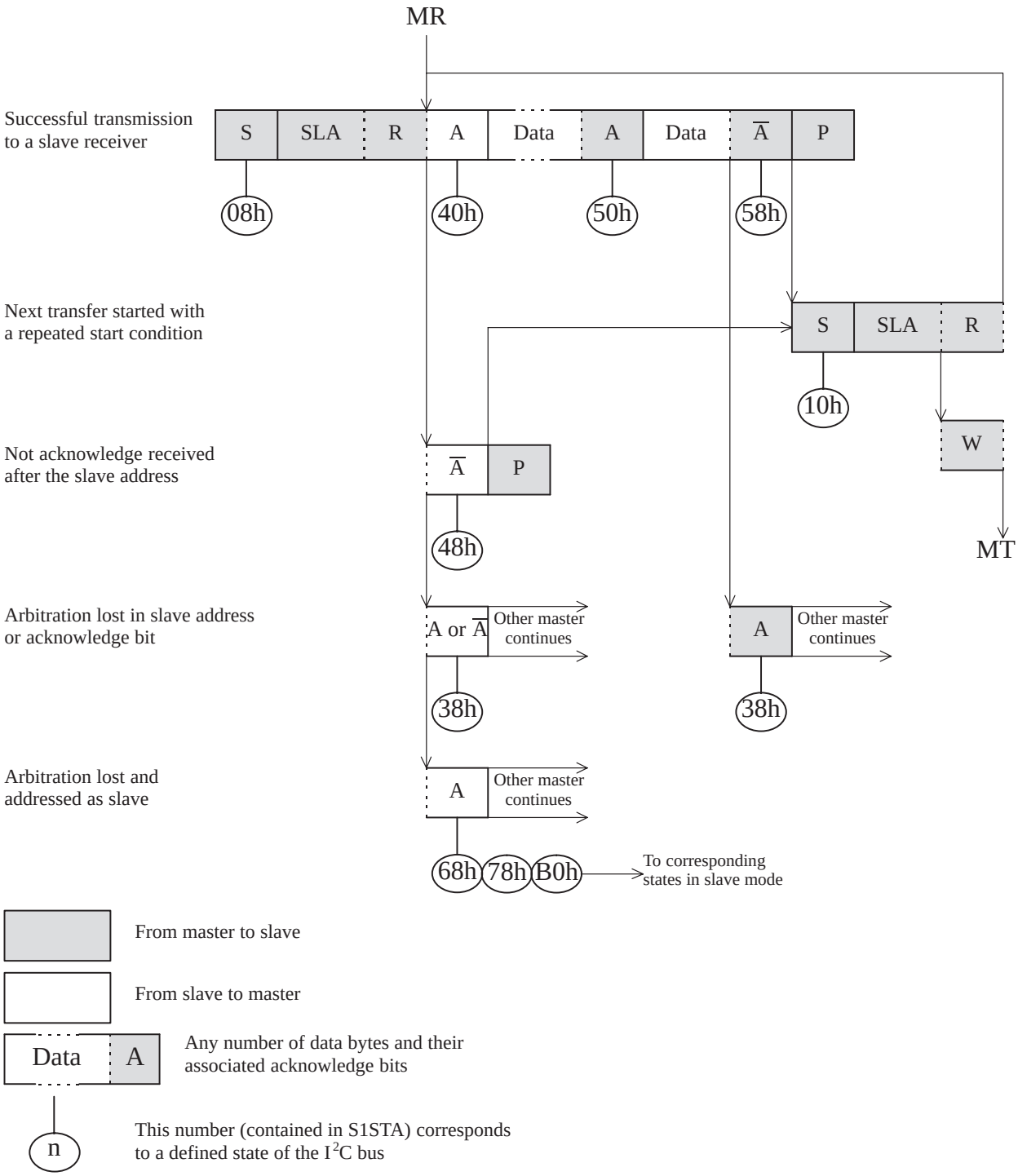


Figure 32 Format and states in the master receiver mode

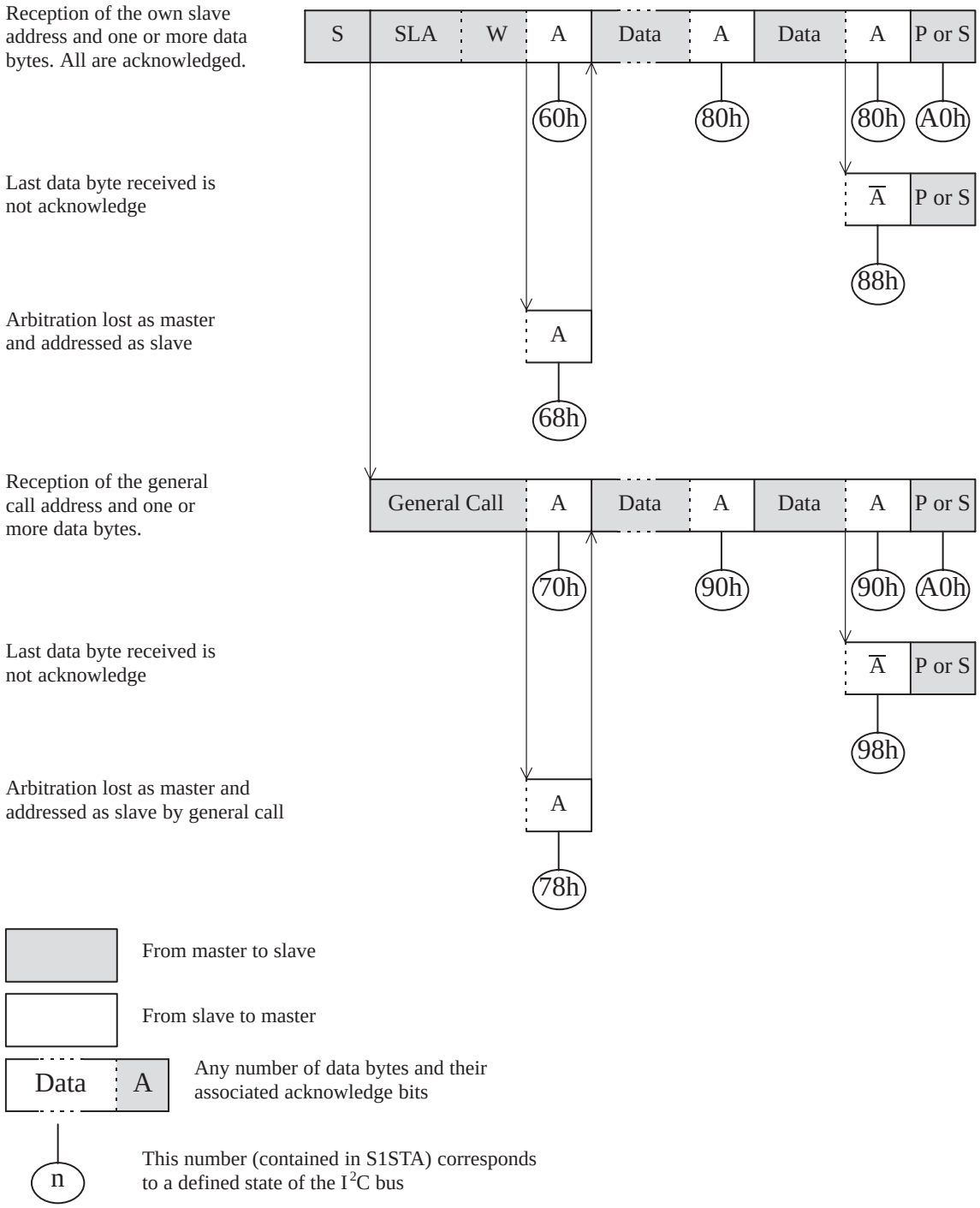


Figure 33 Format and states in the slave receiver mode

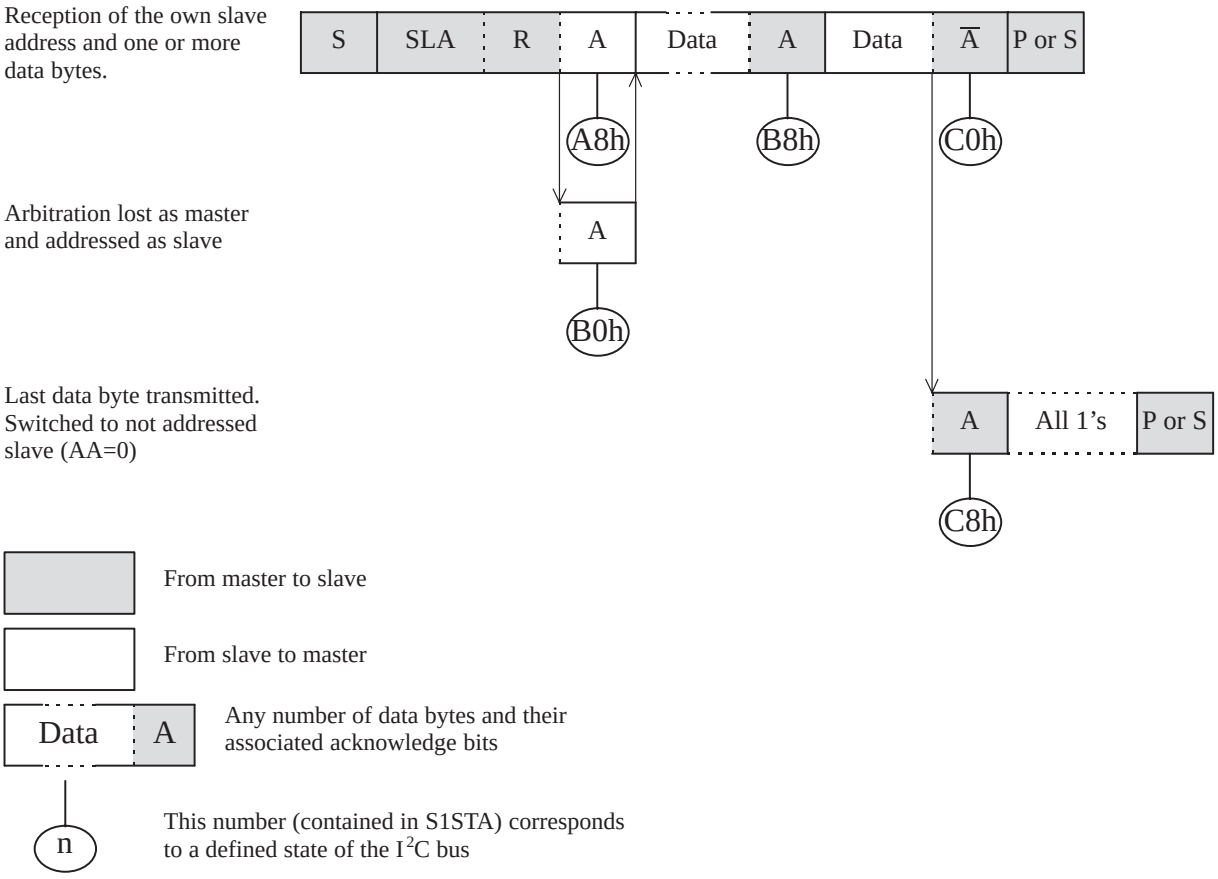


Figure 34 Format and states in the slave transmitter mode

Table 25 Status for master transmitter mode

Status Code	Status of the I^2C bus and I^2C hardware	Application software response					Next action taken by I^2C hardware
		To/From S1DAT	To S1CON				
S1STA			STA	STO	SI	AA	
08h	A START condition has been transmitted	Write SLA+W	X	0	0	X	SLA+W will be transmitted
10h	A repeated START condition has been transmitted	Write SLA+W	X	0	0	X	SLA+W will be transmitted
		Write SLA+R	X	0	0	X	SLA+R will be transmitted and SIO1 will switched to master receiver mode
18h	SLA+W has been transmitted; ACK has been received	Write data byte	0	0	0	X	Data byte will be transmitted
		No S1DAT action	1	0	0	X	Repeated START will be transmitted
		No S1DAT action	0	1	0	X	STOP condition will be transmitted and STO flag will be reset
		No S1DAT action	1	1	0	X	STOP condition followed by a START condition will be transmitted and STO flag will be reset
20h	SLA+W has been transmitted; NOT ACK has been received	Write data byte	0	0	0	X	Data byte will be transmitted
		No S1DAT action	1	0	0	X	Repeated START will be transmitted
		No S1DAT action	0	1	0	X	STOP condition will be transmitted and STO flag will be reset
		No S1DAT action	1	1	0	X	STOP condition followed by a START condition will be transmitted and STO flag will be reset
28h	Data byte has been transmitted; ACK has been received	Write data byte	0	0	0	X	Data byte will be transmitted
		No S1DAT action	1	0	0	X	Repeated START will be transmitted
		No S1DAT action	0	1	0	X	STOP condition will be transmitted and STO flag will be reset
		No S1DAT action	1	1	0	X	STOP condition followed by a START condition will be transmitted and STO flag will be reset
30h	Data byte has been transmitted; NOT ACK has been received	Write data byte	0	0	0	X	Data byte will be transmitted
		No S1DAT action	1	0	0	X	Repeated START will be transmitted.
		No S1DAT action	0	1	0	X	STOP condition will be transmitted and STO flag will be reset
		No S1DAT action	1	1	0	X	STOP condition followed by a START condition will be transmitted and STO flag will be reset
38h	Arbitration lost in SLA+W or data bytes	No S1DAT action	0	0	0	X	I^2C bus will be released and not addressed slave mode will be entered
		No S1DAT action	1	0	0	X	A START condition will be transmitted when the bus becomes free

Table 26 Status for master receiver mode

Status Code	Status of the I^2C bus and I^2C hardware	Application software response					Next action taken by I^2C hardware
		To/From S1DAT	To S1CON				
S1STA			STA	STO	SI	AA	
08h	A START condition has been transmitted	Write SLA+R	X	0	0	X	SLA+R will be transmitted
10h	A repeated START condition has been transmitted	Write SLA+R	X	0	0	X	SLA+R will be transmitted
		Write SLA+W	X	0	0	X	SLA+W will be transmitted then logic will switched to master transmitter mode
38h	Arbitration lost in SLA+R or data bytes	No S1DAT action	0	0	0	X	I^2C bus will be released and not addressed slave mode will be entered
		No S1DAT action	1	0	0	X	A START condition will be transmitted when the bus becomes free
40h	SLA+R has been transmitted; ACK has been received	No S1DAT action	0	0	0	0	Data byte will be received and NOT ACK will be returned
		No S1DAT action	0	0	0	1	Data byte will be received and ACK will be returned

Status Code	Status of the I²C bus and I²C hardware	Application software response					Next action taken by I²C hardware
		To/From S1DAT	To S1CON				
S1STA			STA	STO	SI	AA	
48h	SLA+R has been transmitted; NOT ACK has been received	No S1DAT action	1	0	0	X	Repeated START condition will be transmitted
		No S1DAT action	0	1	0	X	STOP condition will be transmitted and STO flag will be reset
		No S1DAT action	1	1	0	X	STOP condition followed by a START condition will be transmitted and STO flag will be reset
50h	Data byte has been received; ACK has been returned	Read data byte	0	0	0	0	Data byte will be received and NOT ACK will be returned
		Read data byte	0	0	0	1	Data byte will be received and ACK will be returned
58h	Data byte has been received; NOT ACK has been returned	Read data byte	1	0	0	X	Repeated START condition will be transmitted
		Read data byte	0	1	0	X	STOP condition will be transmitted and STO flag will be reset
		Read data byte	1	1	0	X	STOP condition followed by a START condition will be transmitted and STO flag will be reset

Table 27 Status for slave receiver mode

Status Code	Status of the I²C bus and I²C hardware	Application software response					Next action taken by I²C hardware
		To/From S1DAT	To S1CON				
S1STA			STA	STO	SI	AA	
60h	Own SLA+W has been received; ACK has been returned	No S1DAT action	X	0	0	0	Data byte will be received and NOT ACK will be returned
		No S1DAT action	X	0	0	1	Data byte will be received and ACK will be returned
68h	A repeated START condition has been transmitted	No S1DAT action	X	0	0	0	Data byte will be received and NOT ACK will be returned
		No S1DAT action	X	0	0	1	Data byte will be received and ACK will be returned
70h	General call address has been received; ACK has been returned	No S1DAT action	X	0	0	0	Data byte will be received and NOT ACK will be returned
		No S1DAT action	X	0	0	1	Data byte will be received and ACK will be returned
78h	SLA+R has been transmitted; NOT ACK has been received	No S1DAT action	X	0	0	0	Data byte will be received and NOT ACK will be returned
		No S1DAT action	X	0	0	1	Data byte will be received and ACK will be returned
80h	Previously addressed with own SLA+W; data has been received; ACK has been returned	No S1DAT action	X	0	0	0	Data byte will be received and NOT ACK will be returned
		No S1DAT action	X	0	0	1	Data byte will be received and ACK will be returned
88h	Previously addressed with own SLA+W; data has been received; NOT ACK has been returned	Read data byte	0	0	0	0	Switched to the not addressed slave mode; no recognition of own SLA or GCA
		Read data byte	0	0	0	1	Switched to the not addressed slave mode; own SLA will be recognized; GCA will be recognized if GC=logic 1
		Read data byte	1	0	0	0	Switched to the not addressed slave mode; no recognition of own SLA or GCA. A START condition will be transmitted when the bus becomes free
		Read data byte	1	0	0	1	Switched to the not addressed slave mode; own SLA will be recognized; GCA will be recognized if GC=logic 1. A START condition will be transmitted when the bus becomes free
90h	Previously addressed with general call; data has been received; ACK has been returned	Read data byte	X	0	0	X	Data byte will be received and NOT ACK will be returned
		Read data byte	X	0	0	X	Data byte will be received and ACK will be returned

Status Code	Status of the I²C bus and I²C hardware	Application software response					Next action taken by I²C hardware
		To/From S1DAT	To S1CON				
S1STA			STA	STO	SI	AA	
98h	Previously addressed with general call; data has been received; NOT ACK has been returned	Read data byte	0	0	0	0	Switched to the not addressed slave mode; no recognition of own SLA or GCA
		Read data byte	0	0	0	1	Switched to the not addressed slave mode; own SLA will be recognized; GCA will be recognized if GC=logic 1
		Read data byte	1	0	0	0	Switched to the not addressed slave mode; no recognition of own SLA or GCA. A START condition will be transmitted when the bus becomes free
		Read data byte	1	0	0	1	Switched to the not addressed slave mode; own SLA will be recognized; GCA will be recognized if GC=1. A START condition will be transmitted when the bus becomes free
A0h	A STOP condition or repeated START condition has been received while still addressed as slave	No S1DAT action	0	0	0	0	Switched to the not addressed slave mode; no recognition of own SLA or GCA
		No S1DAT action	0	0	0	1	Switched to the not addressed slave mode; own SLA will be recognized; GCA will be recognized if GC=logic 1
		No S1DAT action	1	0	0	0	Switched to the not addressed slave mode; no recognition of own SLA or GCA. A START condition will be transmitted when the bus becomes free
		No S1DAT action	1	0	0	1	Switched to the not addressed slave mode; own SLA will be recognized; GCA will be recognized if GC=logic 1. A START condition will be transmitted when the bus becomes free

Table 28 Status for slave transmitter mode

Status Code	Status of the I²C bus and I²C hardware	Application software response					Next action taken by I²C hardware
		To/From S1DAT	To S1CON				
S1STA			STA	STO	SI	AA	
A8h	Own SLA+R has been received; ACK has been returned	Write data byte	X	0	0	0	Data byte will be transmitted
		Write data byte	X	0	0	1	Data byte will be transmitted
B0h	Arbitration lost in SLA+R/W as master; own SLA+R has been received; ACK has been returned	Write data byte	X	0	0	0	Data byte will be transmitted
		Write data byte	X	0	0	1	Data byte will be transmitted
B8h	Data has been transmitted; NOT ACK has been received	Write data byte	X	0	0	0	Data byte will be transmitted
		Write data byte	X	0	0	1	Data byte will be transmitted

Status Code	Status of the I^2C bus and I^2C hardware	Application software response					Next action taken by I^2C hardware
		To/From S1DAT	To S1CON				
S1STA			STA	STO	SI	AA	
C0h	Data has been transmitted; NOT ACK has been received	No S1DAT action	0	0	0	0	Switched to the not addressed slave mode; no recognition of own SLA or GCA
		No S1DAT action	0	0	0	1	Switched to the not addressed slave mode; own SLA will be recognized; GCA will be recognized if GC=logic 1
		No S1DAT action	1	0	0	0	Switched to the not addressed slave mode; no recognition of own SLA or GCA. A START condition will be transmitted when the bus becomes free
		No S1DAT action	1	0	0	1	Switched to the not addressed slave mode; own SLA will be recognized; GCA will be recognized if GC=logic 1. A START condition will be transmitted when the bus becomes free
C8h	Last data has been transmitted (AA=0); ACK has been received	No S1DAT action	0	0	0	0	Switched to the not addressed slave mode; no recognition of own SLA or GCA
		No S1DAT action	0	0	0	1	Switched to the not addressed slave mode; own SLA will be recognized; GCA will be recognized if GC=logic 1
		No S1DAT action	1	0	0	0	Switched to the not addressed slave mode; no recognition of own SLA or GCA. A START condition will be transmitted when the bus becomes free
		No S1DAT action	1	0	0	1	Switched to the not addressed slave mode; own SLA will be recognized; GCA will be recognized if GC=logic 1. A START condition will be transmitted when the bus becomes free

Table 29 Status for miscellaneous states

Status Code	Status of the I^2C bus and I^2C hardware	Application software response					Next action taken by I^2C hardware
		To/From S1DAT	To S1CON				
S1STA			STA	STO	SI	AA	
F8h	No relevant state information available; SI= 0	No S1DAT action	No S1CON action				Wait or proceed current transfer
00h	Bus error due to an illegal START or STOP condition. State 00h can also occur when interference causes I^2C logic to enter an undefined state	No S1DAT action	0	1	0	X	Only the internal hardware is affected, no STOP condition is sent on the bus. In all cases, the bus is released and STO is reset

11.3. Registers

Table 30 S1CON: Synchronous Serial Control register (D8h)

7	6	5	4	3	2	1	0
CR2	**S1E**	**STA**	**STO**	**SI**	**AA**	**CR1**	**CR0**

Bit Number	Bit Mnemonic	Description
7	CR2	**Control bit rate 2** See Table 24.
6	S1E	**SIO1 Enable bit** Set to enable I^2C controller.

Bit Number	Bit Mnemonic	Description
5	STA	**Start flag** Set to send a start condition on the bus. Clear not to send a start condition on the bus.
4	STO	**Stop flag** Set to send a stop condition on the bus. Clear not to send a stop condition on the bus.
3	SI	**Serial Interrupt flag** Set by hardware when a serial interrupt is requested. Clear by software to acknowledge interrupt.
2	AA	**Assert Acknowledge flag** Set in receiver mode, to force a not acknowledge. Clear in receiver mode to force an acknowledge. This bit has no effect when in transmitter mode.
1	CR1	**Control bit rate 1** See Table 24.
0	CR0	**Control bit rate 0** See Table 24.

S1CON is read/write and bit addressable, its reset value is 0000 0000b.

Table 31 S1STA: Synchronous Serial Status register (D9h)

7	6	5	4	3	2	1	0
SC4	**SC3**	**SC2**	**SC1**	**SC0**	**0**	**0**	**0**

Bit Number	Bit Mnemonic	Description
7–3	SC4–SC0	**Status code bits 0 to 4** See Table 25 to Table 29.
2–0	0	**Always 0**

S1STA is read/write, its reset value is F8h.

Table 32 S1DAT: Synchronous Serial Data register (DAh)

7	6	5	4	3	2	1	0
SD7	**SD6**	**SD5**	**SD4**	**SD3**	**SD2**	**SD1**	**SD0**

Bit Number	Bit Mnemonic	Description
7–1	SD7–SD1	**Address bits 7 to 1 or Data bits 7 to 1**
0	SD0	**Address bit 0 (R/$\overline{W}$) or Data bit 0**

S1DAT is read/write, its reset value is 00h.

Table 33 S1ADR: Synchronous Serial Slave Address register (DBh)

7	6	5	4	3	2	1	0
A7	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**GC**

Bit Number	Bit Mnemonic	Description
7–1	A7–A1	**Slave Address bits 7 to 1**
0	GC	**General Call bit** Set to enable the general call address recognition.

S1ADR is read/write, its reset value is 00h.

12. EPROM

12.1. EPROM Structure

The TSC8051C3 EPROM is divided in two different arrays:

- the code array: 8 Kbytes.
- the encryption array: 64 bytes.

In addition a third non programmable array is implemented:

- the signature array: 4 bytes.

12.2. EPROM Lock System

The program Lock system, when programmed, protects the on–chip program against software piracy.

12.2.1. Encryption Array

Within the EPROM array are 64 bytes of encryption array that are initially unprogrammed (all 1's). Every time a byte is addressed during program verify, 6 address lines are used to select a byte of the encryption array. This byte is then exclusive–NOR'ed (XNOR) with the code byte, creating an encryption verify byte. The algorithm, with the encryption array in the unprogrammed state, will return the code in its original, unmodified form.

When using the encryption array, one important factor needs to be considered. If a byte has the value FFh, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the content of the encryption array. For this reason all the unused code bytes should be programmed with random values. This will ensure program protection.

12.3. EPROM Programming

12.3.1. Set–up modes

In order to program and verify the EPROM or to read the signature bytes, the TSC8051C3 is placed in specific set–up modes (see Figure 35).

Control and program signals must be held at the levels indicated in Table 34.

12.3.2. Definition of terms

Address Lines: P1.0–P1.7, PWM0–PWM4 respectively for A0–A12

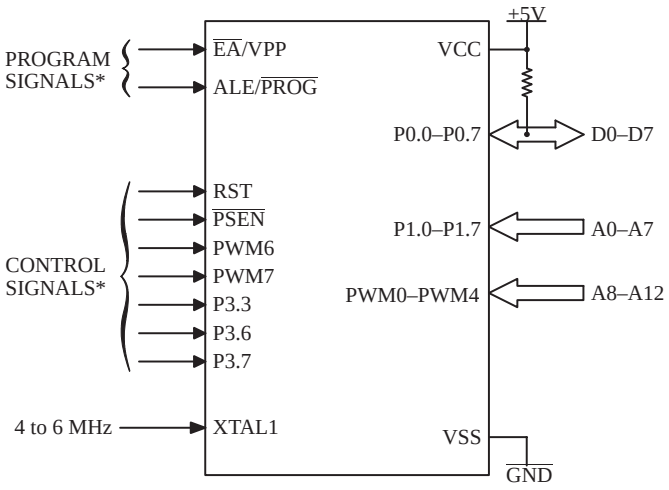
Data Lines: P0.0–P0.7 for D0–D7

Control Signals: RST, $\overline{PSEN}$, PWM6, PWM7, P3.3, P3.6, P3.7.

Program Signals: ALE/$\overline{PROG}$, $\overline{EA}$/VPP.

Table 34 EPROM Set–up Modes

Mode	RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}$/VPP	PWM6	PWM7	P3.3	P3.6	P3.7
Program Code data	1	0	⎍⎍	12.75V	0	1	1	1	1
Verify Code data	1	0	1	1	0	⎍	0	1	1
Program Encryption Array Address 0–3Fh	1	0	⎍⎍	12.75V	0	1	1	0	1
Read Signature Bytes	1	0	1	1	0	⎍	0	0	0



* See Table 34 for proper value on these inputs

Figure 35 Set–up modes configuration

12.3.3. Programming algorithm

The Improved Quick Pulse algorithm is based on the Quick Pulse algorithm and decreases the number of pulses applied during byte programming from 25 to 5.

To program the TSC8051C3 the following sequence must be exercised:

- Step 1: Input the valid address on the address lines.
- Step 2: Input the appropriate data on the data lines.
- Step 3: Activate the combination of control signals.
- Step 4: Raise $\overline{EA}$/VPP from VCC to VPP (typical 12.75V).
- Step 5: Pulse ALE/$\overline{PROG}$ 5 times.

Repeat step 1 through 5 changing the address and data for the entire array or until the end of the object file is reached (see Figure 36).

12.3.4. Verify algorithm

Code array verify must be done after each byte or block of bytes is programmed. In either case, a complete verify of the programmed array will ensure reliable programming of the TSC8051C3.

To verify the TSC8051C3 code the following sequence must be exercised :

- Step 1: Activate the combination of program signals.
- Step 2: Input the valid address on the address lines.
- Step 3: Input the appropriate data on the data lines.
- Step 4: Activate the combination of control signals.

Repeat step 2 through 4 changing the address and data for the entire array (see Figure 36).

The encryption array cannot be directly verified. Verification of the encryption array is done by observing that the code array is well encrypted.

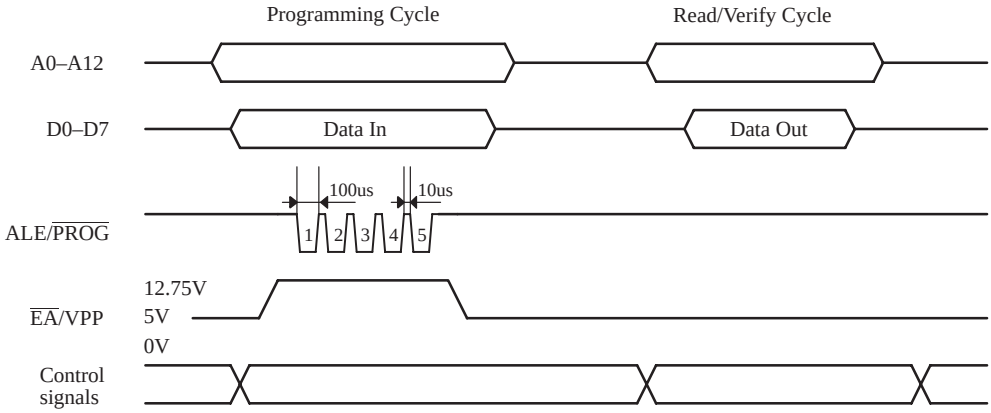


Figure 36 Programming and verification signal's waveform

12.4. Signature bytes

The TSC8051C3 has four signature bytes in location 30h, 31h, 60h and 61h. To read these bytes follow the procedure for EPROM verify but activate the control lines provided in Table 34 for Read Signature Bytes. Table 35 shows the content of the signature byte for the TSC8051C3.

Table 35 Signature bytes content

Location	Contents	Comment
30h	58h	Customer selection byte: TEMIC
31h	58h	Family selection byte: C51
60h	ADh	TSC8051C3
61h	XXh	Product revision number

12.5. EPROM Erasure (Windowed Packages Only)

Erasing the EPROM erases the code array and also the encryption array, returning the parts to full functionality.

Erasure leaves all the EPROM cells in a 1's state.

12.5.1. Erasure Characteristics

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Å) to an integrated dose at least 15 W–sec/cm^2. Exposing the EPROM to an ultraviolet lamp of 12,000 µW/cm^2 rating for 30 minutes, at a distance of about 25 mm, should be sufficient.

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelength shorter than approximately 4,000 Å. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room–level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

13. Electrical Characteristics

13.1. Absolute Maximum Ratings(1)

Ambiant Temperature Under Bias:
C = commercial . . . . . 0°C to 70°C
I = industrial . . . . . –40°C to 85°C
Storage Temperature . . . . . –65°C to + 150°C
Voltage on VCC to VSS . . . . . –0.5 V to + 7 V
Voltage on VPP to VSS . . . . . –0.5 V to + 13 V
Voltage on PWM0–7 to VSS . . . . . –0.5 V to + 13 V
Voltage on Any Pin to VSS . . . –0.5 V to VCC + 0.5 V
Power Dissipation . . . . . 1 W(2)

Notice:

1. *Stresses at or above those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.*
2. *This value is based on the maximum allowable die temperature and the thermal resistance of the package.*

13.2. DC Parameters

T_A = 0°C to +70°C; VSS = 0V; VCC = 5V ± 10%; F = 0 to 16 MHz.
T_A = –40°C to +85°C; VSS = 0V; VCC = 5V ± 10%; F = 0 to 16 MHz.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VIL	Input Low Voltage	–0.5		0.2 VCC – 0.1	V	
VIH	Input High Voltage except XTAL1, RST	0.2 VCC + 0.9		VCC + 0.5	V	
VIH1	Input High Voltage, XTAL1, RST	0.7 VCC		VCC + 0.5	V	
VOL	Output Low Voltage, ports 1, 2, 3 (6)			0.3 0.45 1.0	V V V	IOL = 100µA(4) IOL = 1.6mA(4) IOL = 3.5mA(4)
VOL1	Output Low Voltage, port 0, ALE, $\overline{PSEN}$, PWM0–7 (6)			0.3 0.45 1.0	V V V	IOL = 200µA(4) IOL = 3.2mA(4) IOL = 7.0mA(4)
VOH	Output High Voltage, ports 1, 2, 3	VCC – 0.3 VCC – 0.7 VCC – 1.5			V V V	IOH = –10µA IOH = –30µA IOH = –60µA VCC = 5V ± 10%
VOH1	Output High Voltage, port 0, ALE, $\overline{PSEN}$	VCC – 0.3 VCC – 0.7 VCC – 1.5			V V V	IOH = –200µA IOH = –3.2mA IOH = –7.0mA VCC = 5V ± 10%
VLOW	Power Fail Reset Low Voltage	3	3.5 (5)	4	V	
RRST	RST Pulldown Resistor	50	90 (5)	200	kΩ	
IIL	Logical 0 Input Current ports 1, 2 and 3			–50	µA	Vin = 0.45V
ILI	Input Leakage Current			±10	µA	0.45 < Vin < VCC
ITL	Logical 1 to 0 Transition Current, ports 1, 2, 3			–650	µA	Vin = 2.0V
CIO	Capacitance of I/O Buffer			10	pF	fc = 1MHz, T_A = 25°C

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
IPD	Power Down Current		TBD (5)	TBD	µA	VCC = 2.0V to 5.5V(3)
ICC	Power Supply Current (7)					
	Active Mode 12MHz		TBD (5)	TBD	mA	VCC = 5.5V(1)
	Idle Mode 12MHz		TBD (5)	TBD	mA	VCC = 5.5V(2)
	Active Mode 16MHz		TBD (5)	TBD	mA	VCC = 5.5V(1)
	Idle Mode 16MHz		TBD (5)	TBD	mA	VCC = 5.5V(2)

Notes for DC Electrical Characteristics

1. Operating ICC is measured with all output pins disconnected; XTAL1 driven with TCLCH, TCHCL = 5 ns (see Figure 40), VIL = VSS + 0.5V, VIH = VCC – 0.5V; XTAL2 N.C.; $\overline{EA}$ = RST = Port 0 = VCC. ICC would be slightly higher if a crystal oscillator used (see Figure 37).
2. Idle ICC is measured with all output pins disconnected; XTAL1 driven with TCLCH, TCHCL = 5ns, VIL = VSS + 0.5V, VIH = VCC–0.5V; XTAL2 N.C; Port 0 = VCC; $\overline{EA}$ = RST = VSS (see Figure 38).
3. Power Down ICC is measured with all output pins disconnected; $\overline{EA}$ = VSS, PORT 0 = VCC; XTAL2 NC.; RST = VSS (see Figure 39).
4. Capacitance loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the VOLs of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1 to 0 transitions during bus operation. In the worst cases (capacitive loading 100pF), the noise pulse on the ALE line may exceed 0.45V with maxi VOL peak 0.6V. A Schmitt Trigger use is not necessary.
5. Typicals are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and 5V.
6. Under steady state (non–transient) conditions, IOL must be externally limited as follows:
   Maximum IOL per port pin: 10 mA
   Maximum IOL per 8–bit port:
   Port 0: 26 mA
   Ports 1, 2 and 3: 15 mA
   Maximum total IOL for all output pins: 71 mA
   If IOL exceeds the test condition, VOL may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
7. For other values, please contact your sales office.

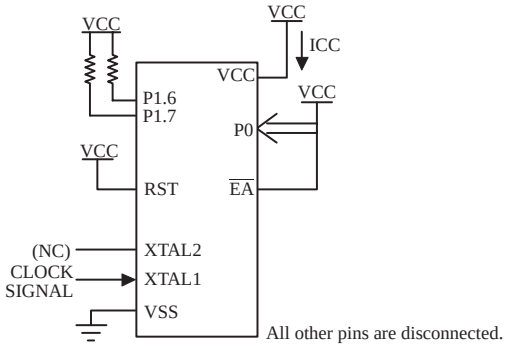


Figure 37 ICC Test Condition, Active Mode

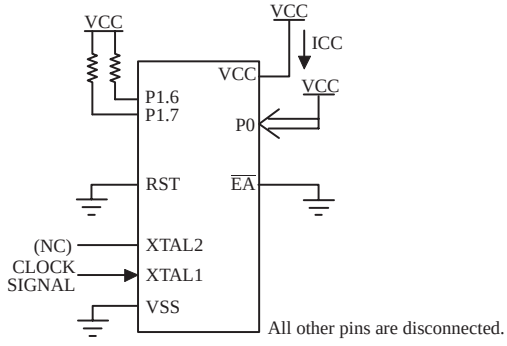


Figure 38 ICC Test Condition, Idle Mode

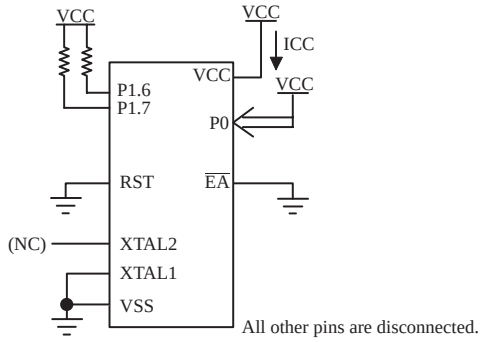


Figure 39 ICC Test Condition, Power Down Mode

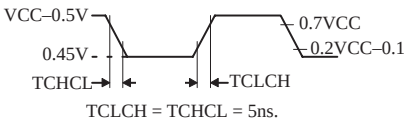


Figure 40 Clock Signal Waveform for ICC Tests in Active and Idle Modes

13.3. AC Parameters

13.3.1. Explanation of the AC Symbols

Each timing symbol has 5 characters. The first character is always a “T” (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

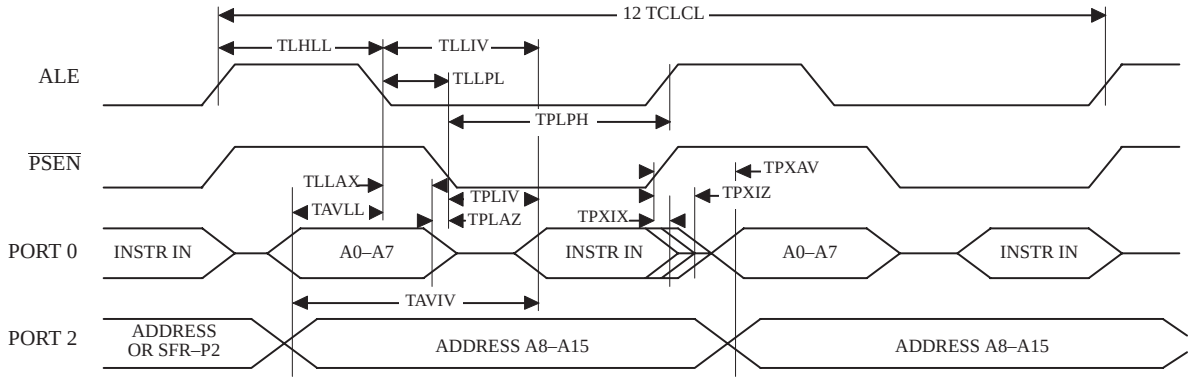
Example: TAVLL = Time for Address Valid to ALE Low.
TLLPL = Time for ALE Low to $\overline{\text{PSEN}}$ Low.

T_A = 0 to +70°C; VSS = 0V VCC = 5V±10%; 0 to 12MHz
T_A = –40°C to +85°C; VSS = 0V; VCC = 5V ± 10%; F = 0 to 12MHz.
(Load Capacitance for PORT 0, ALE and PSEN = 100pf; Load Capacitance for all other outputs = 80 pF.)

13.3.2. External Program Memory Characteristics

Symbol	Parameter	0 to 12MHz		Units
		Min	Max	
TLHLL	ALE pulse width	2TCLCL – 40		ns
TAVLL	Address Valid to ALE	TCLCL – 40		ns
TLLAX	Address Hold After ALE	TCLCL – 30		ns
TLLIV	ALE to Valid Instruction In		4TCLCL – 100	ns
TLLPL	ALE to $\overline{\text{PSEN}}$	TCLCL – 30		ns
TPLPH	$\overline{\text{PSEN}}$ Pulse Width	3TCLCL – 45		ns
TPLIV	$\overline{\text{PSEN}}$ to Valid Instruction In		3TCLCL – 105	ns
TPXIX	Input Instruction Hold After $\overline{\text{PSEN}}$	0		ns
TPXIZ	Input Instruction FloatAfter $\overline{\text{PSEN}}$		TCLCL – 25	ns
TPXAV	$\overline{\text{PSEN}}$ to Address Valid	TCLCL – 8		ns
TAVIV	Address to Valid Instruction In		5TCLCL – 105	ns
TPXAV	$\overline{\text{PSEN}}$ Low to Address Float		10	ns

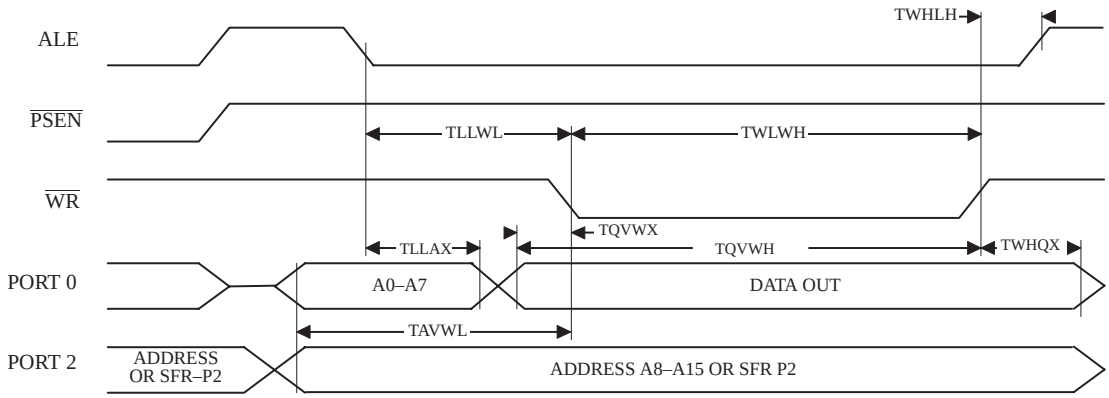
13.3.3. External Program Memory Read Cycle



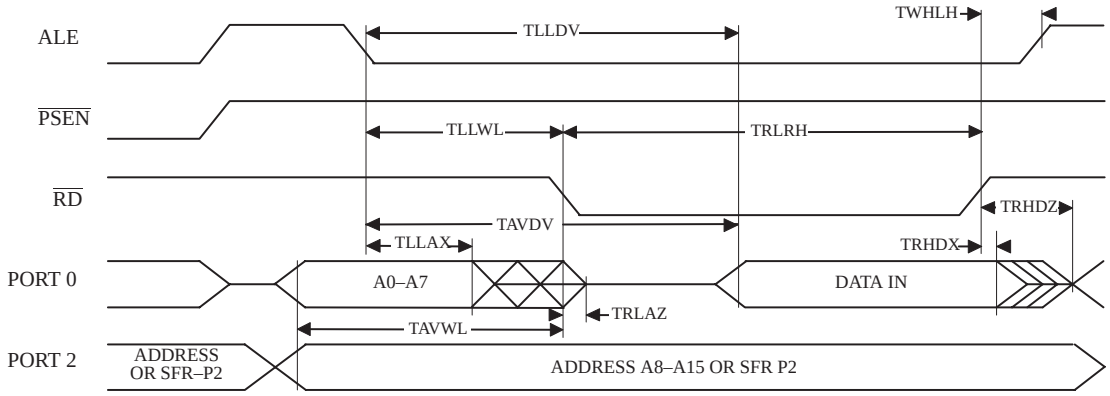
13.3.4. External Data Memory Characteristics

Symbol	Parameter	0 to 12MHz		Units
		Min	Max	
TRLRH	$\overline{RD}$ Pulse Width	6TCLCL–100		ns
TWLWH	$\overline{WR}$ Pulse Width	6TCLCL–100		ns
TRLDV	$\overline{RD}$ to Valid Data In		5TCLCL–165	ns
TRHDX	Data Hold After $\overline{RD}$	0		ns
TRHDZ	Data Float After $\overline{RD}$		2TCLCL–60	ns
TLLDV	ALE to Valid Data In		8TCLCL–150	ns
TAVDV	Address to Valid Data In		9TCLCL–165	ns
TLLWL	ALE to $\overline{WR}$ or $\overline{RD}$	3TCLCL–50	3TCLCL+50	ns
TAVWL	Address to $\overline{WR}$ or $\overline{RD}$	4TCLCL–130		ns
TQVWX	Data Valid to $\overline{WR}$ Transition	TCLCL–50		ns
TQVWH	Data set–up to $\overline{WR}$ High	7TCLCL–150		ns
TWHQX	Data Hold After $\overline{WR}$	TCLCL–50		ns
TRLAZ	$\overline{RD}$ Low to Address Float		0	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE high	TCLCL–40	TCLCL+40	ns

13.3.5. External Data Memory Write Cycle



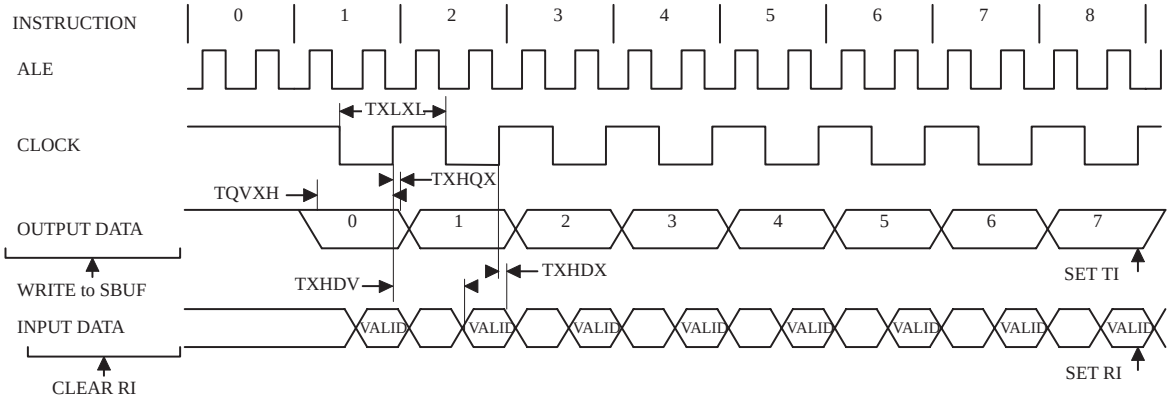
13.3.6. External Data Memory Read Cycle



13.3.7. Serial Port Timing – Shift Register Mode

Symbol	Parameter	0 to 12MHz		Units
		Min	Max	
TXLXL	Serial port clock cycle time	12TCLCL		ns
TQVHX	Output data set–up to clock rising edge	10TCLCL–133		ns
TXHQX	Output data hold after clock rising edge	2TCLCL–117		ns
TXHDX	Input data hold after clock rising edge	0		ns
TXHDV	Clock rising edge to input data valid		10TCLCL–133	ns

13.3.8. Shift Register Timing Waveforms



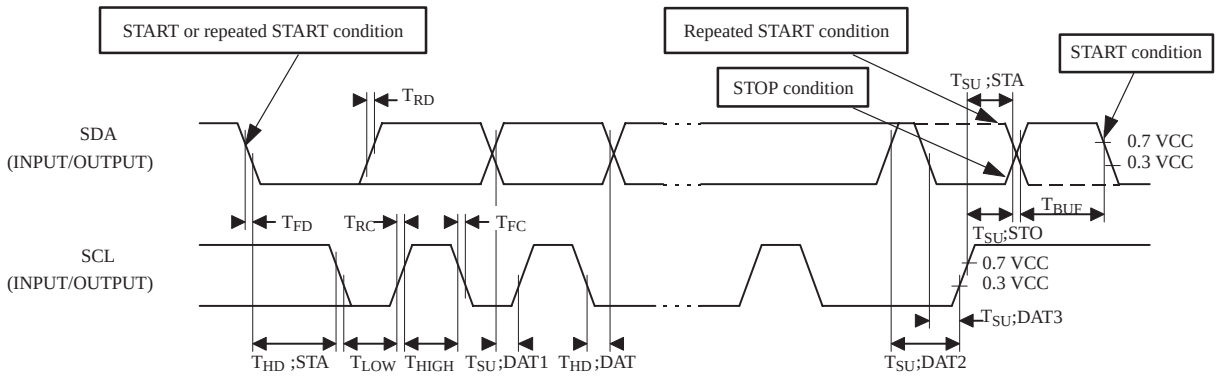
13.3.9. SIO1 (I^2C) Interface Timing

Symbol	Parameter	Input	Output
$T_{HD;STA}$	Start condition hold time	≥ 14 T_{CLCL}	> 4.0µs (1)
T_{LOW}	SCL low time	≥ 16 T_{CLCL}	> 4.7µs (1)
T_{HIGH}	SCL high time	≥ 14 T_{CLCL}	> 4.0µs (1)
T_{RC}	SCL rise time	≤ 1µs	– (2)
T_{FC}	SCL fall time	≤ 0.3µs	< 0.3µs (3)
$T_{SU;DAT1}$	Data set–up time	≥ 250ns	> 20 T_{CLCL} – T_{RD}
$T_{SU;DAT2}$	SDA set–up time (before repeated START condition)	≥ 250ns	> 1µs (1)
$T_{SU;DAT3}$	SDA set–up time (before STOP condition)	≥ 250ns	> 8 T_{CLCL}
$T_{HD;DAT}$	Data hold time	≥ 0ns	> 8 T_{CLCL} – T_{FC}
$T_{SU;STA}$	Repeated START set–up time	≥ 14 T_{CLCL}	> 4.7µs (1)
$T_{SU;STO}$	STOP condition set–up time	≥ 14 T_{CLCL}	> 4.0µs (1)
T_{BUF}	Bus free time	≥ 14 T_{CLCL}	> 4.7µs (1)
T_{RD}	SDA rise time	≤ 1µs	– (2)
T_{FD}	SDA fall time	≤ 0.3µs	< 0.3µs (3)

Notes

1. At 100 kbit/s. At other bit–rates this value is inversely proportional to the bit–rate of 100 kbit/s.
2. Determined by the external bus–line capacitance and the external bus–line pull–up resistor, this must be < 1µs.
3. Spikes on the SDA and SCL lines with a duration of less than 3 T_{CLCL} will be filtered out. Maximum capacitance on bus–lines SDA and SCL = 400pF

13.3.10. SIO1 (I^2C) Timing Waveforms

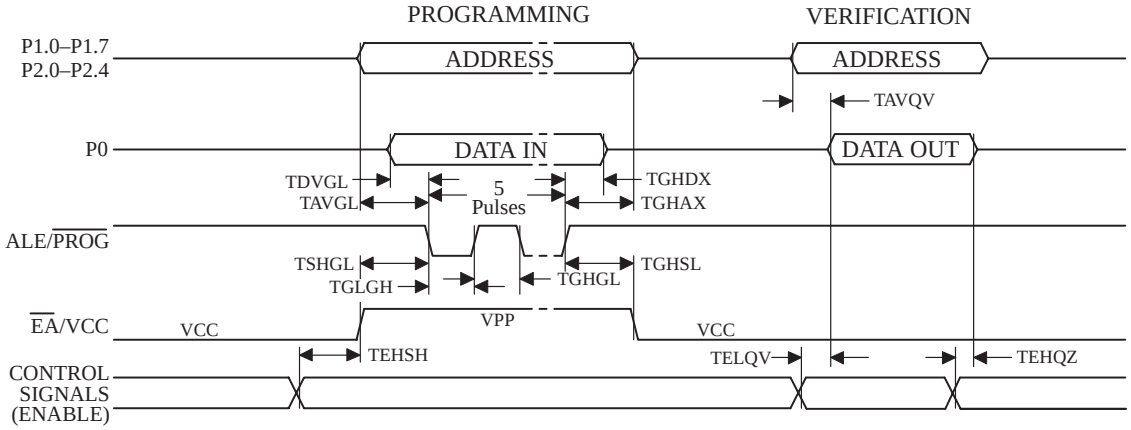


13.3.11. EPROM Programming and Verification Characteristics

T_A = 21°C to 27°C; VSS = 0V; VCC = 5V ± 10%.

Symbol	Parameter	Min	Max	Units
VPP	Programming Supply Voltage	12.5	13	V
IPP	Programming Supply Current		75	mA
1/TCLCL	Oscillator Frquency	4	6	MHz
TAVGL	Address Setup to $\overline{PROG}$ Low	48 TCLCL		
TGHAX	Adress Hold after $\overline{PROG}$	48 TCLCL		
TDVGL	Data Setup to $\overline{PROG}$ Low	48 TCLCL		
TGHDX	Data Hold after $\overline{PROG}$	48 TCLCL		
TEHSH	(Enable) High to VPP	48 TCLCL		
TSHGL	VPP Setup to $\overline{PROG}$ Low	10		µs
TGHSL	VPP Hold after $\overline{PROG}$	10		µs
TGLGH	$\overline{PROG}$ Width	90	110	µs
TAVQV	Address to Valid Data		48 TCLCL	
TELQV	ENABLE Low to Data Valid		48 TCLCL	
TEHQV	Data Float after ENABLE	0	48 TCLCL	
TGHGL	$\overline{PROG}$ High to $\overline{PROG}$ Low	10		µs

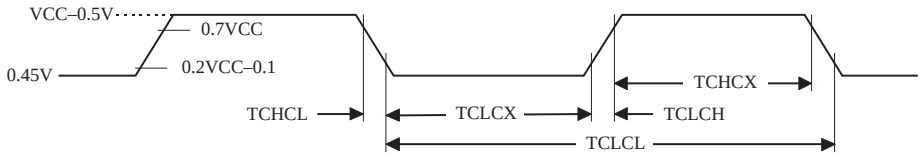
13.3.12. EPROM Programming and Verification Waveforms



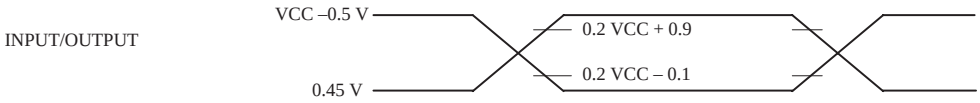
13.3.13. External Clock Drive Characteristics (XTAL1)

Symbol	Parameter	Min	Max	Units
TCLCL	Oscillator Period	62.5		ns
TCHCX	High Time	5		ns
TCLCX	Low Time	5		ns
TCLCH	Rise Time		5	ns
TCHCL	Fall Time		5	ns

13.3.14. External Clock Drive Waveforms

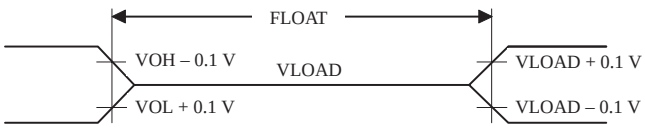


13.3.15. AC Testing Input/Output Waveforms



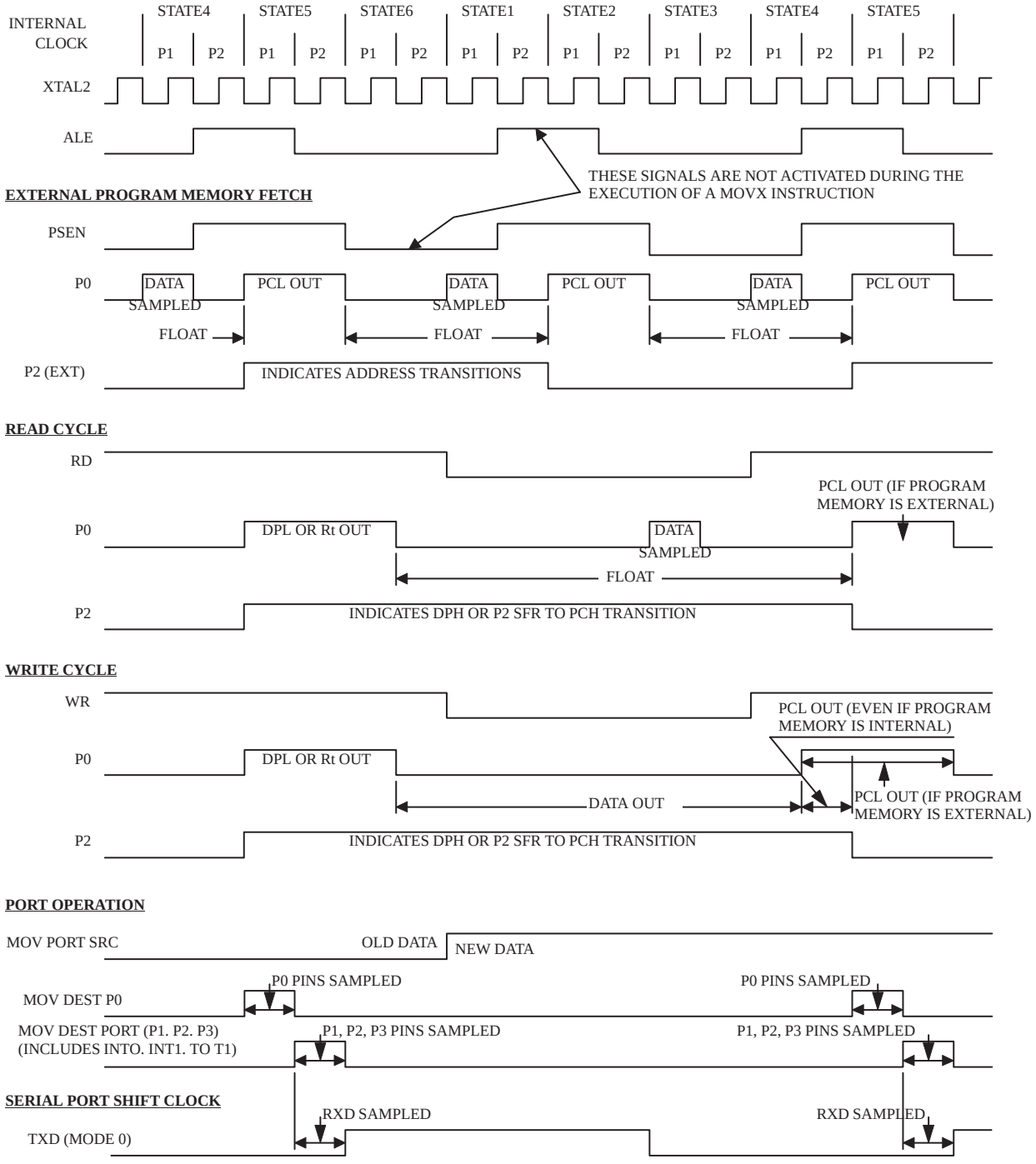
AC inputs during testing are driven at VCC – 0.5 for a logic “1” and 0.45V for a logic “0”. Timing measurement are made at VIH min for a logic “1” and VIL max for a logic “0”.

13.3.16. Float Waveforms



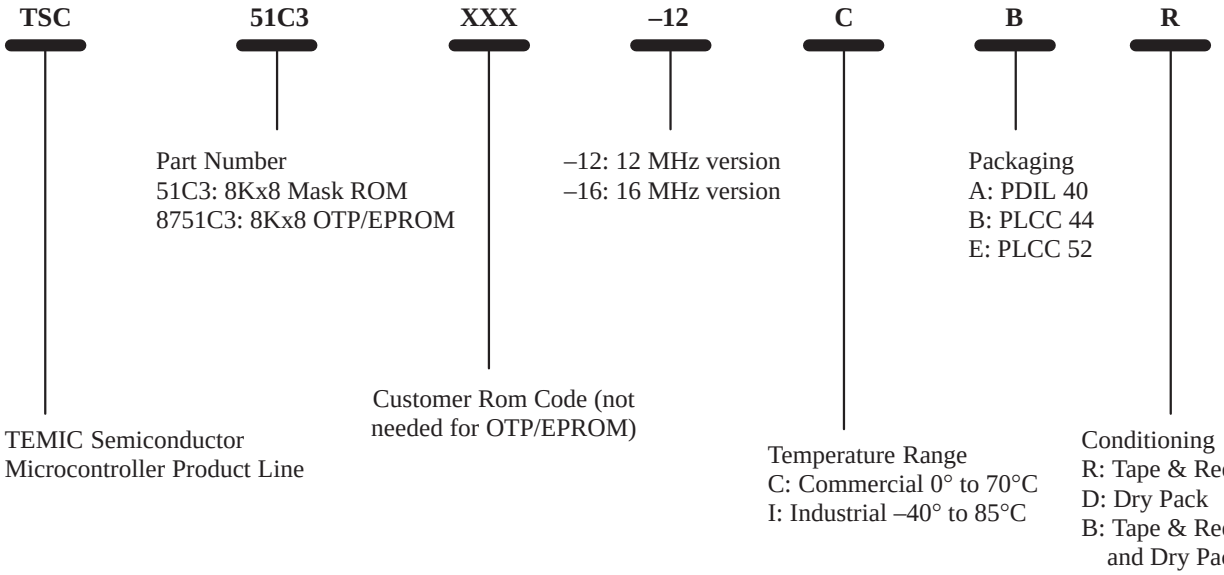
For timing purposes as port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded VOH/VOL level occurs. IOL/IOH ≥ ± 20mA.

13.3.17. Clock Waveforms



This diagram indicates when signals are clocked internally. The time it takes the signals to propagate to the pins, however, ranges from 25 to 125ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component. Typically though (T_A=25°C fully loaded) $\overline{RD}$ and $\overline{WR}$ propagation delays are approximately 50ns. The other signals are typically 85ns. Propagation delays are incorporated in the AC specifications.

14. Ordering Information



Examples

Part Number	Description
TSC51C3XXX–12CA	Mask ROM XXX, 12 MHz, 0 to 70°C, PDIL 40
TSC8751C3–16CER	OTP, 16 MHz, 0 to 70°C, PLCC 52, Tape and Reel

Development Tools

Reference	Description
ANM059	Application Note: “How to recognize video mode and generate free running synchronization signals using TSC8051C1/C2/C3 Microcontroller”

Product Marking

TEMIC
Customer P/N
Temic P/N
© Intel 80, 82
YYWW Lot Number