



TS4972

1.2W AUDIO POWER AMPLIFIER WITH STANDBY MODE ACTIVE HIGH

- OPERATING FROM $V_{CC} = 2.5V$ to $5.5V$
- RAIL TO RAIL **OUTPUT**
- 1.2W OUTPUT POWER @ $V_{CC}=5V$, THD=1%,
F=1kHz, with 8Ω Load
- ULTRA LOW CONSUMPTION IN STANDBY
MODE (**10nA**)
- **75dB** PSRR @ 217Hz from 2.5 to 5V
- LOW POP & CLICK
- ULTRA LOW DISTORTION (**0.05%**)
- UNITY GAIN STABLE
- **FLIP CHIP PACKAGE** $8 \times 300\mu m$ bumps

DESCRIPTION

The TS4972 is an Audio Power Amplifier capable of delivering 1.6W of continuous RMS output power into a 4Ω load @ 5V.

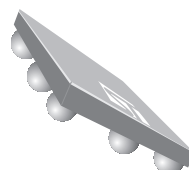
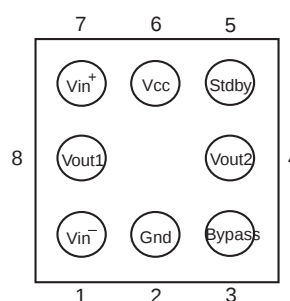
This Audio Amplifier is exhibiting 0.1% distortion level (THD) from a 5V supply for a $P_{out} = 250mW$ RMS. An external standby mode control reduces the supply current to less than 10nA. An internal shutdown protection is provided.

The TS4972 has been designed for high quality audio applications such as mobile phones and to minimize the number of external components.

The unity-gain stable amplifier can be configured by external gain setting resistors.

PIN CONNECTIONS (Top View)

TS4972JT - FLIP CHIP



APPLICATIONS

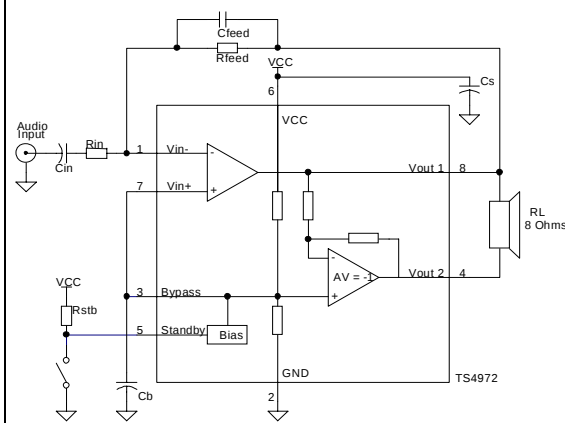
- Mobile Phones (Cellular / Cordless)
- PDAs
- Laptop/Notebook computers
- Portable Audio Devices

ORDER CODE

Part Number	Temperature Range	Package	Marking
		J	
TS4972IJT	-40, +85°C	•	4972

J = Flip Chip Package - only available in Tape & Reel (JT)

TYPICAL APPLICATION SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage ¹⁾	6	V
V_i	Input Voltage ²⁾	G_{ND} to V_{CC}	V
T_{oper}	Operating Free Air Temperature Range	-40 to + 85	°C
T_{stg}	Storage Temperature	-65 to +150	°C
T_j	Maximum Junction Temperature	150	°C
R_{thja}	Thermal Resistance Junction to Ambient ³⁾	200	°C/W
P_d	Power Dissipation	Internally Limited ⁴⁾	
ESD	Human Body Model	2	kV
ESD	Machine Model	200	V
Latch-up	Latch-up Immunity	Class A	
	Lead Temperature (soldering, 10sec)	250	°C

1. All voltages values are measured with respect to the ground pin.

2. The magnitude of input signal must never exceed $V_{CC} + 0.3V$ / $G_{ND} - 0.3V$

3. Device is protected in case of over temperature by a thermal shutdown active @ 150°C.

4. Exceeding the power derating curves during a long period, involves abnormal operating condition.

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2.5 to 5.5	V
V_{ICM}	Common Mode Input Voltage Range	G_{ND} to $V_{CC} - 1.2V$	V
V_{STB}	Standby Voltage Input : Device ON Device OFF	$G_{ND} \leq V_{STB} \leq 0.5V$ $V_{CC} - 0.5V \leq V_{STB} \leq V_{CC}$	V
R_L	Load Resistor	4 - 32	Ω
R_{thja}	Thermal Resistance Junction to Ambient ¹⁾	90	°C/W

1. With Heat Sink Surface = 125mm²

ELECTRICAL CHARACTERISTICS $V_{CC} = +5V$, GND = 0V, $T_{amb} = 25^{\circ}C$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		6	8	mA
$I_{STANDBY}$	Standby Current ¹⁾ No input signal, $V_{stdby} = V_{CC}$, $R_L = 8\Omega$		10	1000	nA
V_{OO}	Output Offset Voltage No input signal, $R_L = 8\Omega$		5	20	mV
P_O	Output Power THD = 1% Max, $f = 1kHz$, $R_L = 8\Omega$		1.2		W
THD + N	Total Harmonic Distortion + Noise $P_O = 250mW$ rms, $G_v = 2$, $20Hz < f < 20kHz$, $R_L = 8\Omega$		0.1		%
PSRR	Power Supply Rejection Ratio ²⁾ $f = 217Hz$, $R_L = 8\Omega$, $R_{Feed} = 22K\Omega$, Vripple = 200mV rms		75		dB
Φ_M	Phase Margin at Unity Gain $R_L = 8\Omega$, $C_L = 500pF$		70		Degrees
GM	Gain Margin $R_L = 8\Omega$, $C_L = 500pF$		20		dB
GBP	Gain Bandwidth Product $R_L = 8\Omega$		2		MHz

1. Standby mode is activated when V_{stdby} is tied to V_{CC} 2. Dynamic measurements - $20 \cdot \log(rms(V_{out})/rms(V_{ripple}))$. Vripple is an added sinus signal to V_{CC} @ $f = 217Hz$ $V_{CC} = +3.3V$, GND = 0V, $T_{amb} = 25^{\circ}C$ (unless otherwise specified)³⁾

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		5.5	8	mA
$I_{STANDBY}$	Standby Current ¹⁾ No input signal, $V_{stdby} = V_{CC}$, $R_L = 8\Omega$		10	1000	nA
V_{OO}	Output Offset Voltage No input signal, $R_L = 8\Omega$		5	20	mV
P_O	Output Power THD = 1% Max, $f = 1kHz$, $R_L = 8\Omega$		500		mW
THD + N	Total Harmonic Distortion + Noise $P_O = 250mW$ rms, $G_v = 2$, $20Hz < f < 20kHz$, $R_L = 8\Omega$		0.1		%
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GBP	Gain Bandwidth Product $R_L = 8\Omega$		2		MHz

1. Standby mode is activated when V_{stdby} is tied to V_{CC} 2. Dynamic measurements - $20 \cdot \log(rms(V_{out})/rms(V_{ripple}))$. Vripple is an added sinus signal to V_{CC} @ $f = 217Hz$

3. All electrical values are made by correlation between 2.6V and 5V measurements

ELECTRICAL CHARACTERISTICS

$V_{CC} = 2.6V$, $GND = 0V$, $T_{amb} = 25^{\circ}C$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		5.5	8	mA
$I_{STANDBY}$	Standby Current ¹⁾ No input signal, $V_{stdby} = V_{CC}$, $R_L = 8\Omega$		10	1000	nA
V_{OO}	Output Offset Voltage No input signal, $R_L = 8\Omega$		5	20	mV
P_o	Output Power THD = 1% Max, $f = 1kHz$, $R_L = 8\Omega$		300		mW
THD + N	Total Harmonic Distortion + Noise $P_o = 200mW$ rms, $G_v = 2$, $20Hz < f < 20kHz$, $R_L = 8\Omega$		0.1		%
PSRR	Power Supply Rejection Ratio ²⁾ $f = 217Hz$, $R_L = 8\Omega$, $R_{Feed} = 22K\Omega$, $V_{ripple} = 200mV$ rms		75		dB
Φ_M	Phase Margin at Unity Gain $R_L = 8\Omega$, $C_L = 500pF$		70		Degrees
GM	Gain Margin $R_L = 8\Omega$, $C_L = 500pF$		20		dB
GBP	Gain Bandwidth Product $R_L = 8\Omega$		2		MHz

1. Standby mode is activated when V_{stdby} is tied to V_{CC}

2. Dynamic measurements - $20 \cdot \log(rms(V_{out})/rms(V_{ripple}))$. Ripple is an added sinus signal to V_{CC} @ $f = 217Hz$

Components	Functional Description
R_{in}	Inverting input resistor which sets the closed loop gain in conjunction with R_{feed} . This resistor also forms a high pass filter with C_{in} ($f_c = 1 / (2 \times \pi \times R_{in} \times C_{in})$)
C_{in}	Input coupling capacitor which blocks the DC voltage at the amplifier input terminal
R_{feed}	Feed back resistor which sets the closed loop gain in conjunction with R_{in}
C_s	Supply Bypass capacitor which provides power supply filtering
C_b	Bypass pin capacitor which provides half supply filtering
C_{feed}	Low pass filter capacitor allowing to cut the high frequency (low pass filter cut-off frequency $1 / (2 \times \pi \times R_{feed} \times C_{feed})$)
R_{stb}	Pull-up resistor which fixes the right supply level on the standby pin
G_v	Closed loop gain in BTL configuration = $2 \times (R_{feed} / R_{in})$

REMARKS

1. All measurements, except PSRR measurements, are made with a supply bypass capacitor $C_s = 100\mu F$.
2. External resistors are not needed for having better stability when supply @ V_{CC} down to 3V. By the way, the quiescent current remains the same.
3. The standby response time is about 1 μs .

Fig. 1 : Open Loop Frequency Response

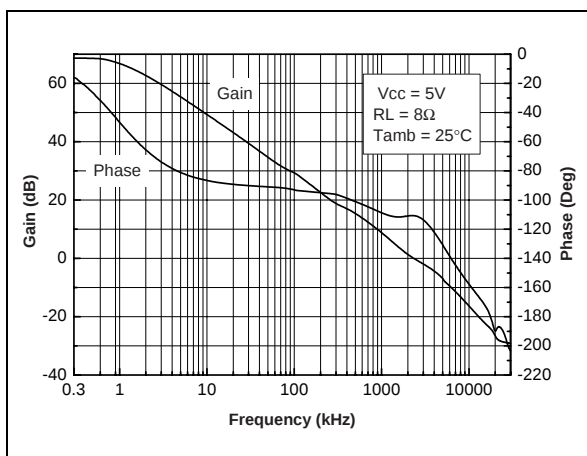


Fig. 2 : Open Loop Frequency Response

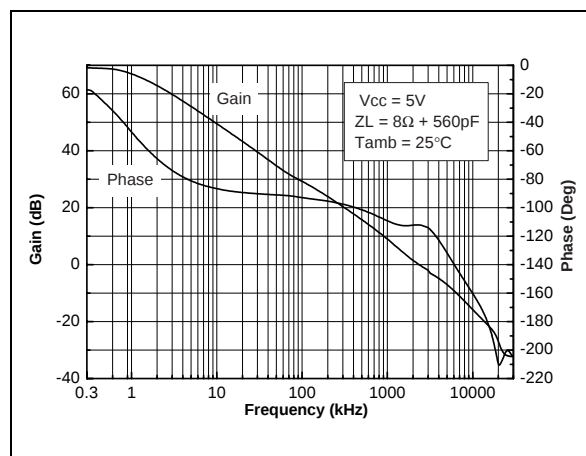


Fig. 3 : Open Loop Frequency Response

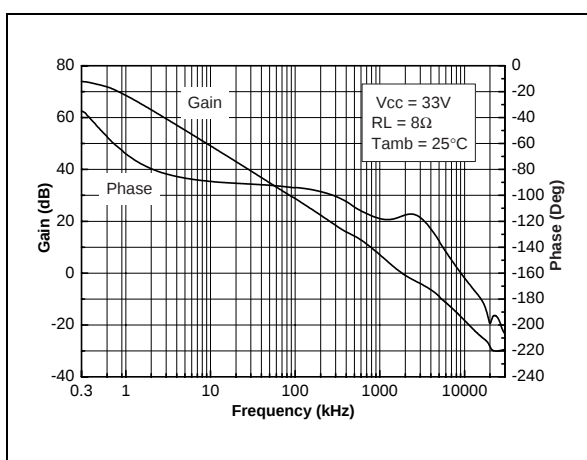


Fig. 4 : Open Loop Frequency Response

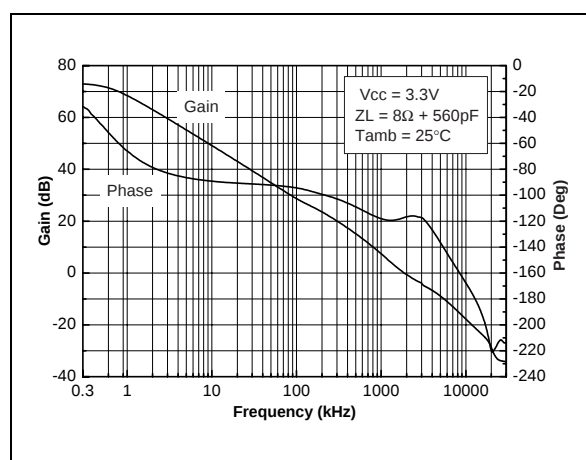


Fig. 5 : Open Loop Frequency Response

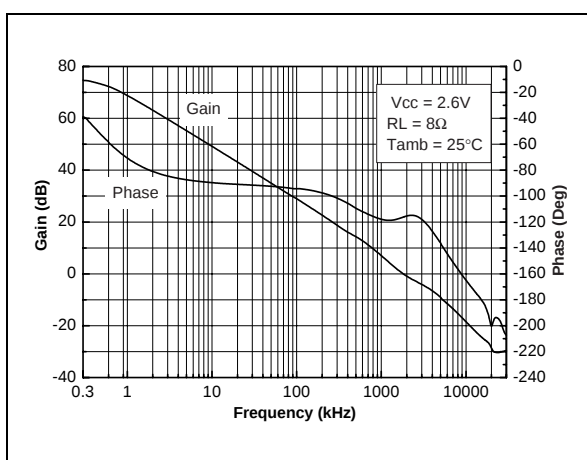


Fig. 6 : Open Loop Frequency Response

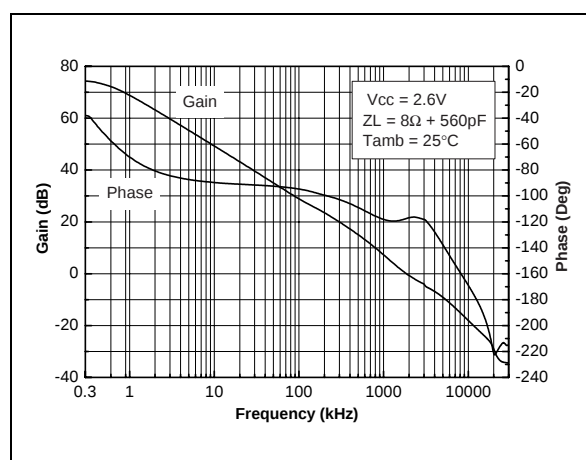


Fig. 7 : Open Loop Frequency Response

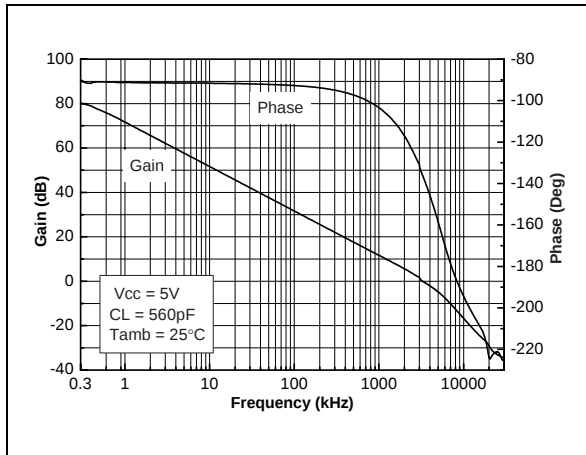


Fig. 8 : Open Loop Frequency Response

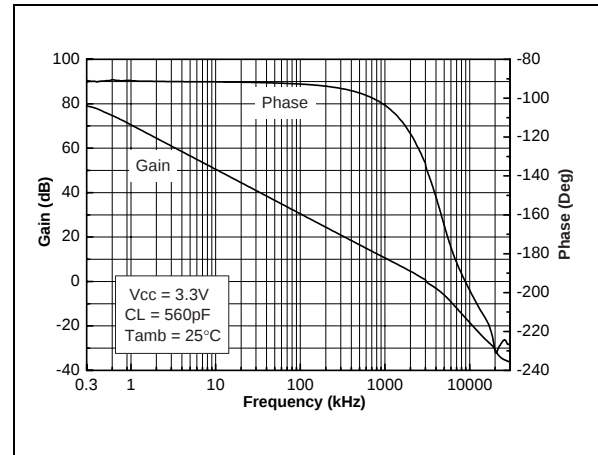


Fig. 9 : Open Loop Frequency Response

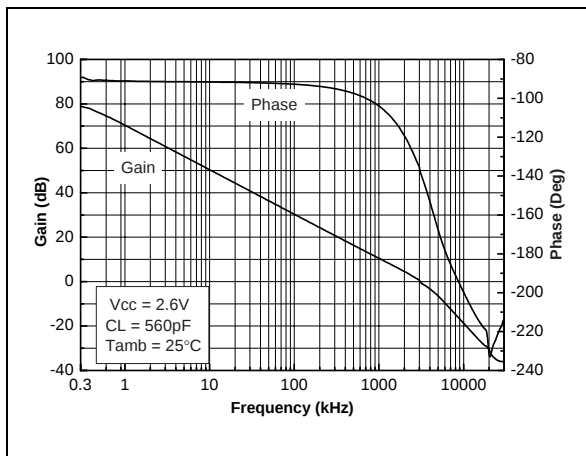


Fig. 10 : Power Supply Rejection Ratio (PSRR) vs Power supply

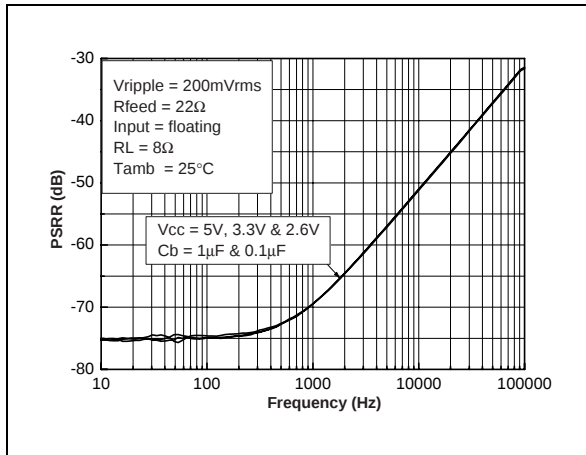


Fig. 11 : Power Supply Rejection Ratio (PSRR) vs Feedback Capacitor

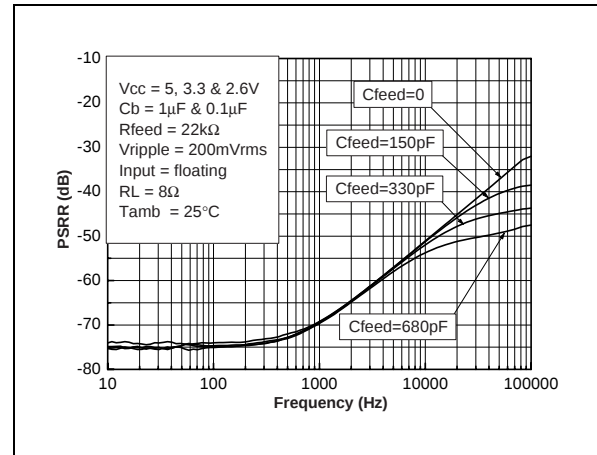


Fig. 12 : Power Supply Rejection Ratio (PSRR) vs Bypass Capacitor

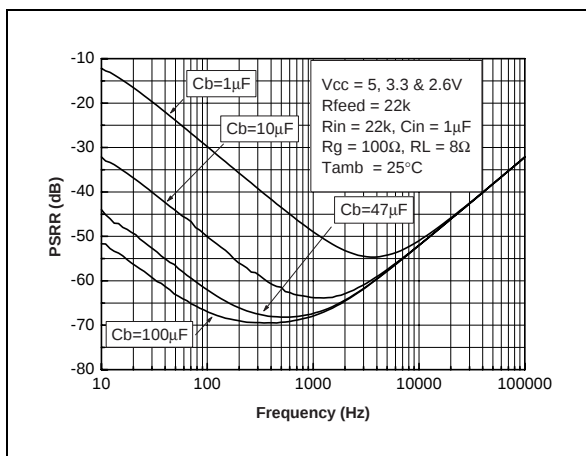


Fig. 13 : Power Supply Rejection Ratio (PSRR) vs Input Capacitor

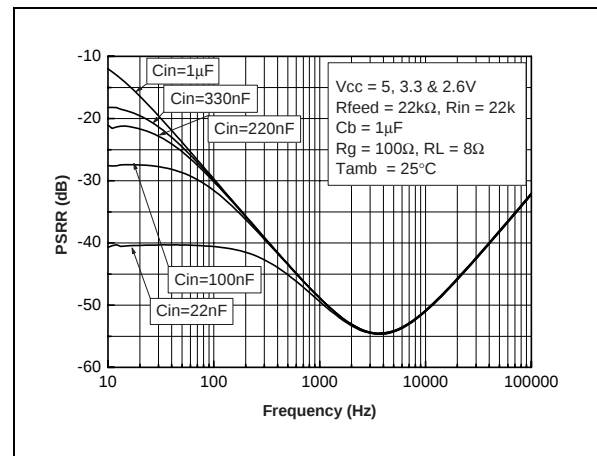


Fig. 14 : Power Supply Rejection Ratio (PSRR) vs Feedback Resistor

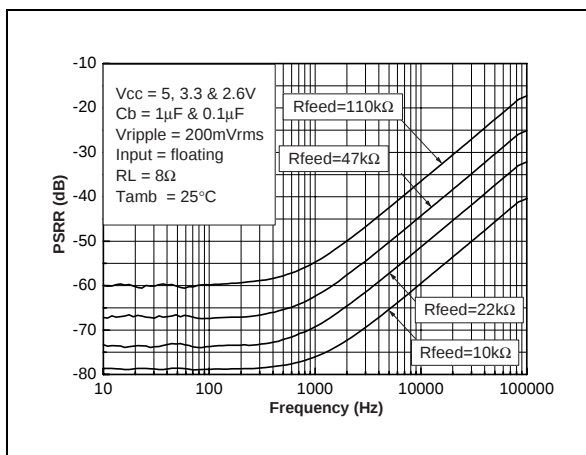


Fig. 15 : Pout @ THD + N = 1% vs Supply Voltage vs RL

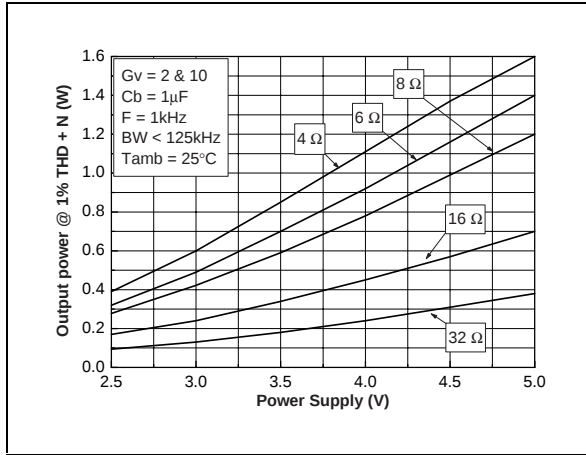


Fig. 16 : Pout @ THD + N = 10% vs Supply Voltage vs RL

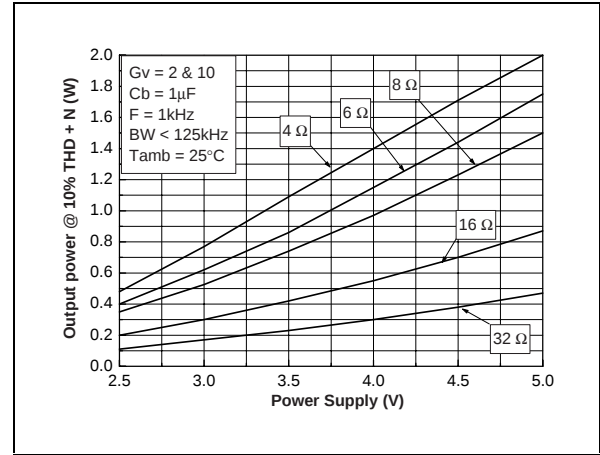


Fig. 17 : Power Dissipation vs Pout

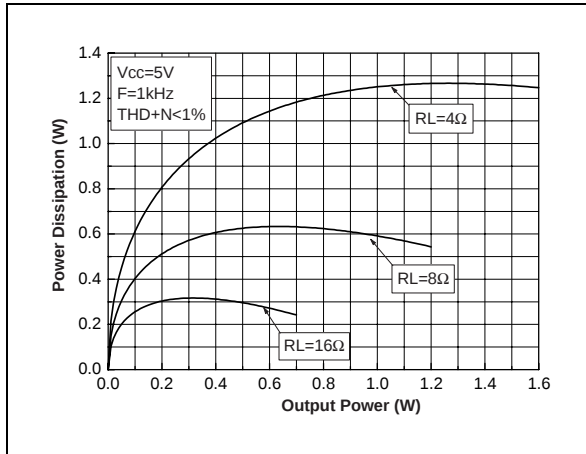


Fig. 18 : Power Dissipation vs Pout

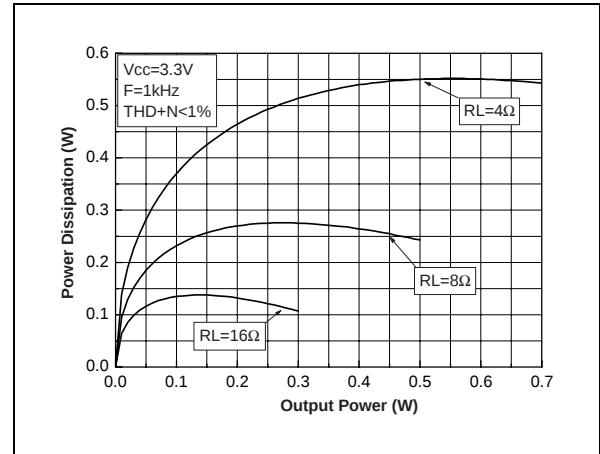


Fig. 19 : Power Dissipation vs Pout

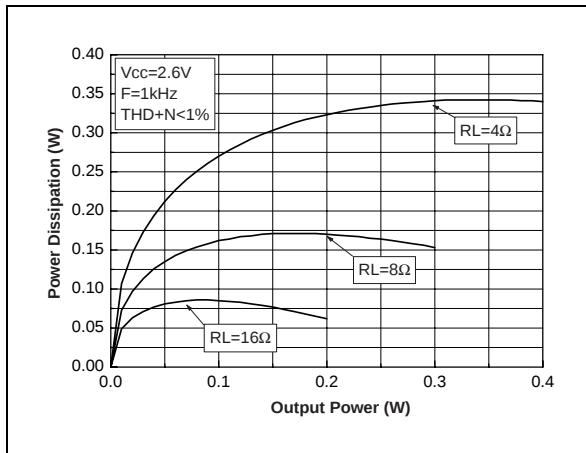


Fig. 20 : Power Derating Curves

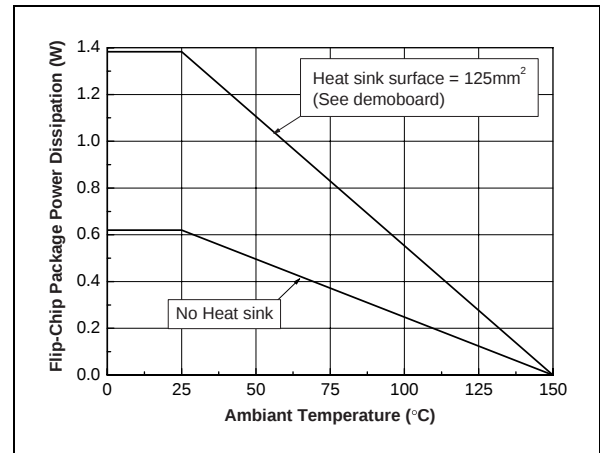


Fig. 21 : THD + N vs Output Power

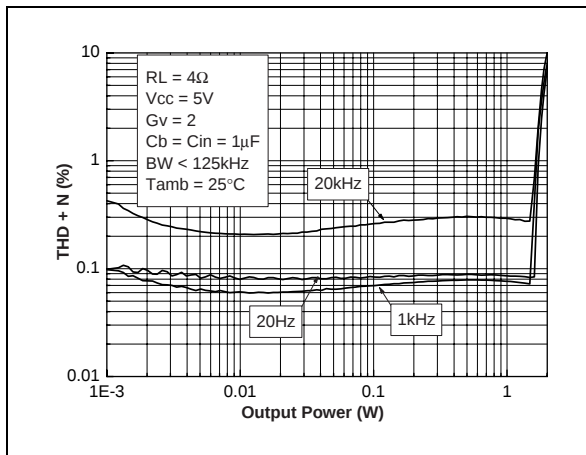


Fig. 22 : THD + N vs Output Power

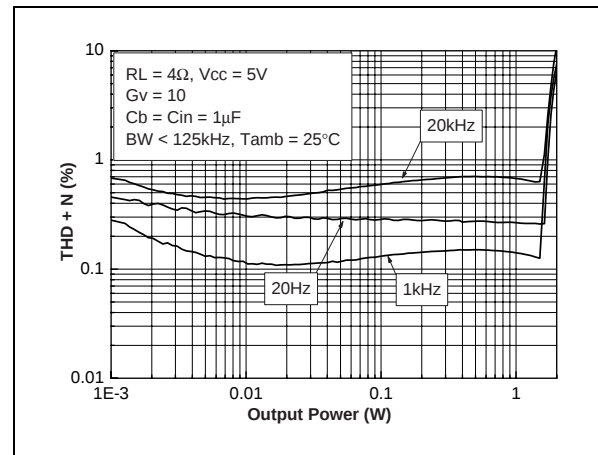


Fig. 23 : THD + N vs Output Power

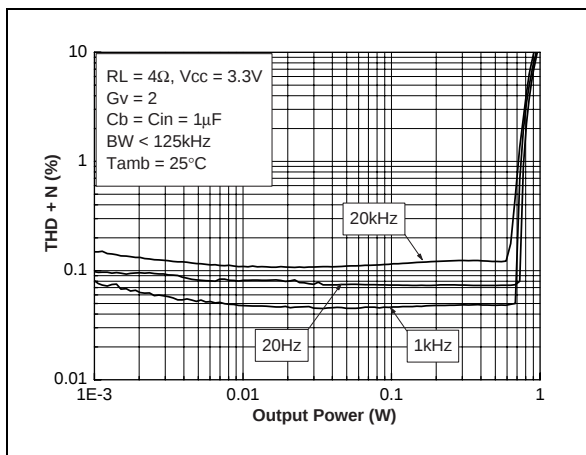


Fig. 24 : THD + N vs Output Power

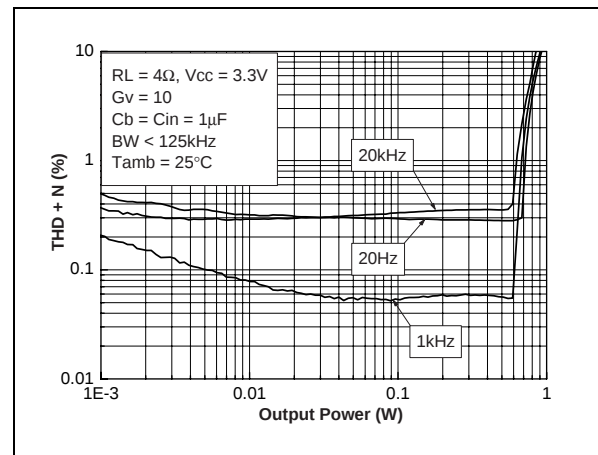


Fig. 25 : THD + N vs Output Power

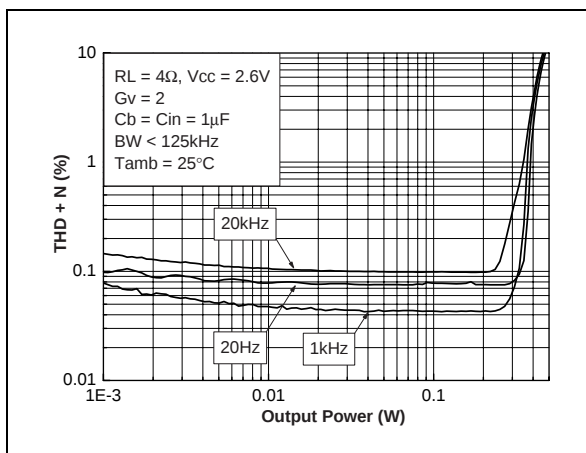


Fig. 26 : THD + N vs Output Power

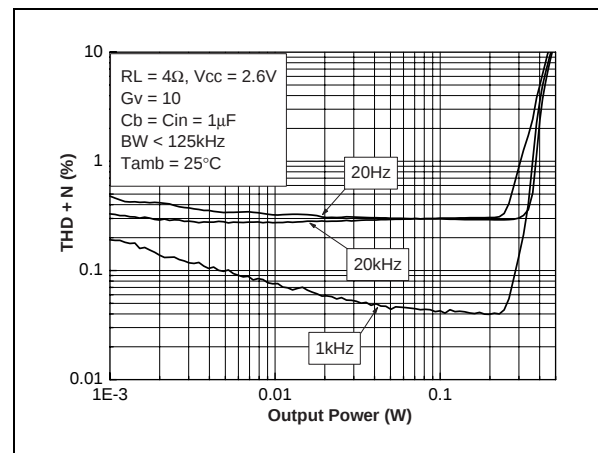


Fig. 27 : THD + N vs Output Power

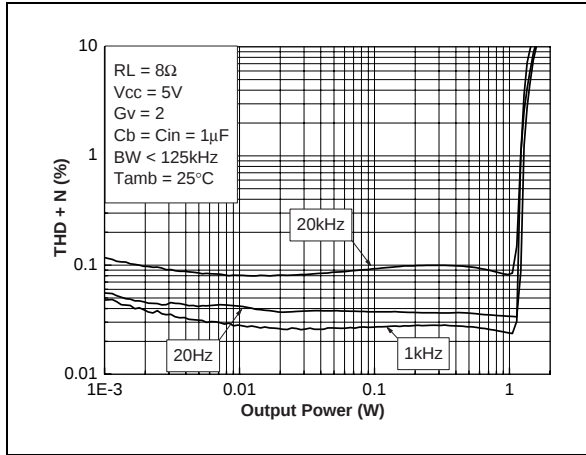


Fig. 28 : THD + N vs Output Power

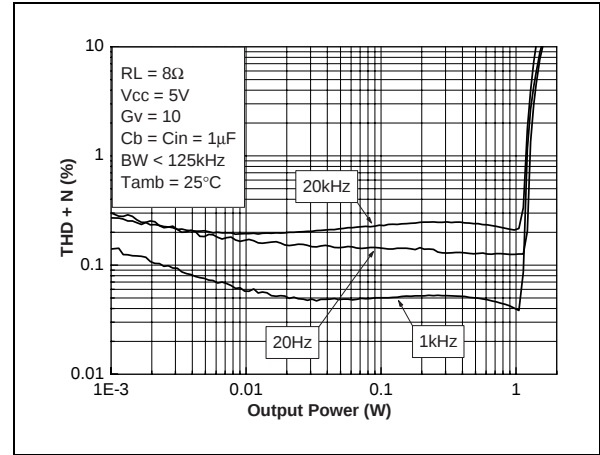


Fig. 29 : THD + N vs Output Power

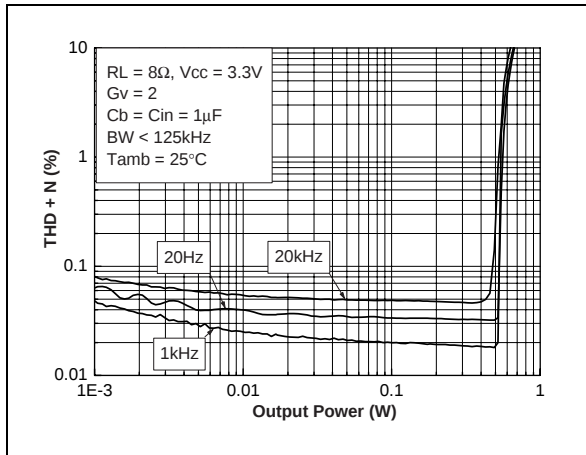


Fig. 30 : THD + N vs Output Power

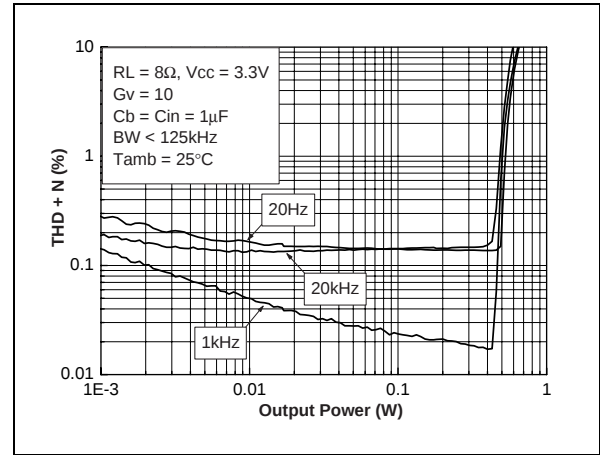


Fig. 31 : THD + N vs Output Power

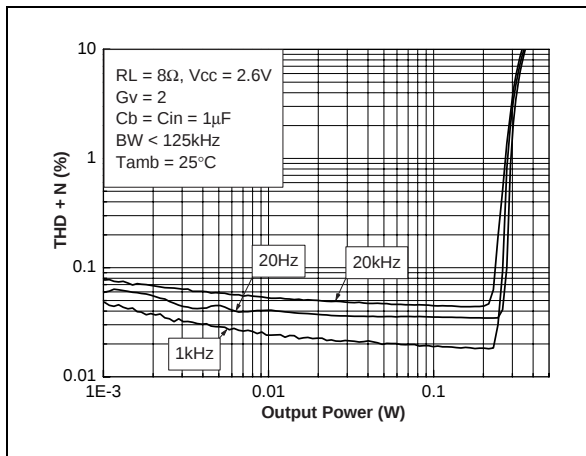


Fig. 32 : THD + N vs Output Power

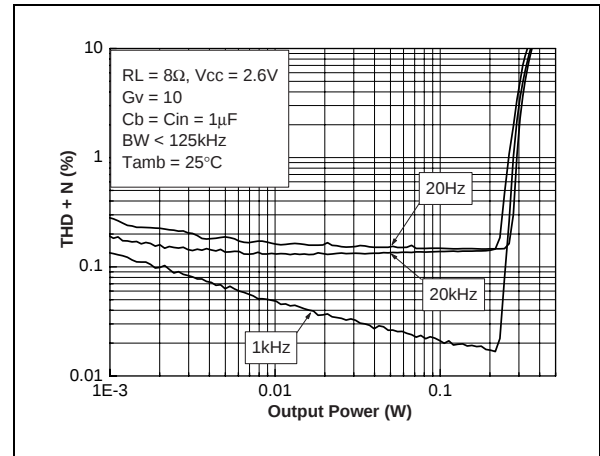


Fig. 33 : THD + N vs Output Power

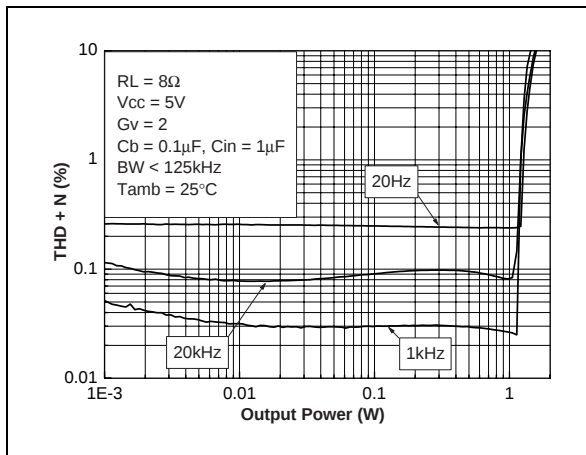


Fig. 34 : THD + N vs Output Power

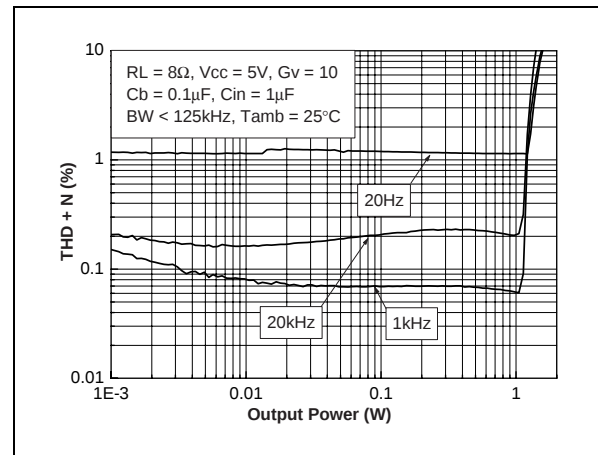


Fig. 35 : THD + N vs Output Power

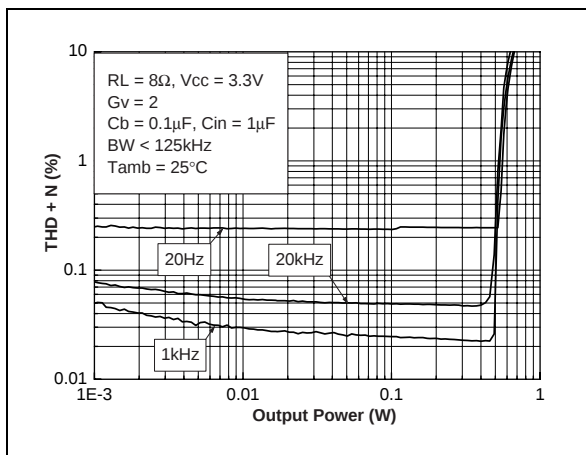


Fig. 36 : THD + N vs Output Power

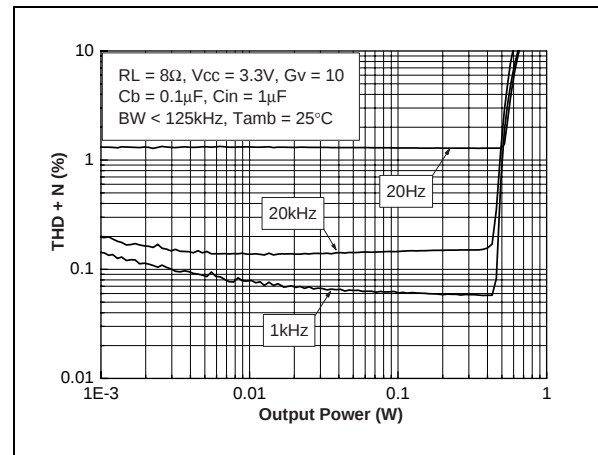


Fig. 37 : THD + N vs Output Power

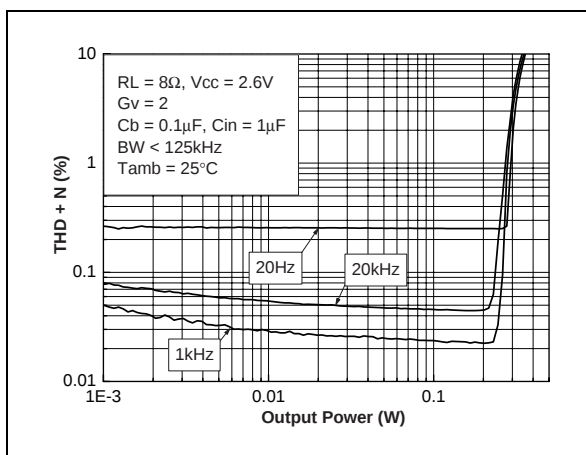


Fig. 38 : THD + N vs Output Power

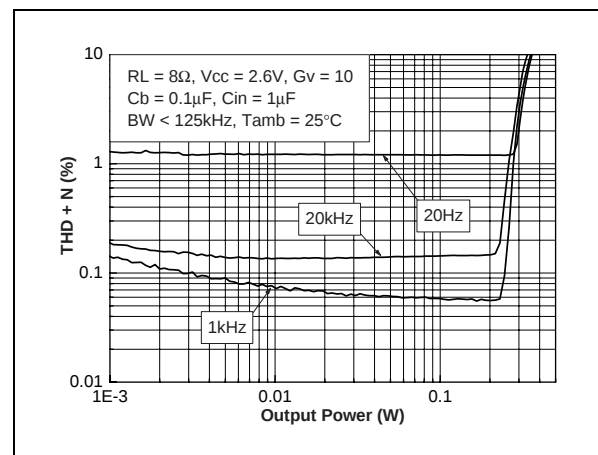


Fig. 39 : THD + N vs Output Power

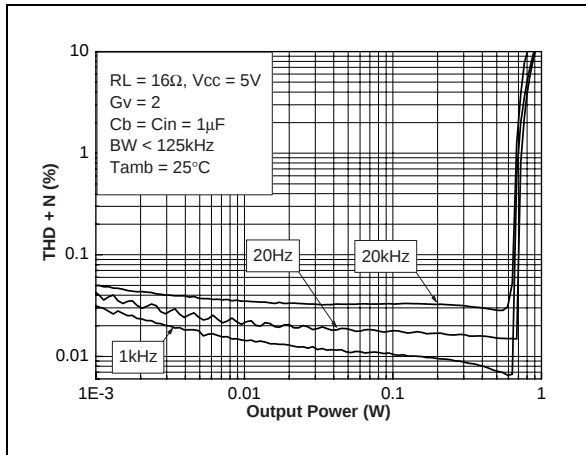


Fig. 40 : THD + N vs Output Power

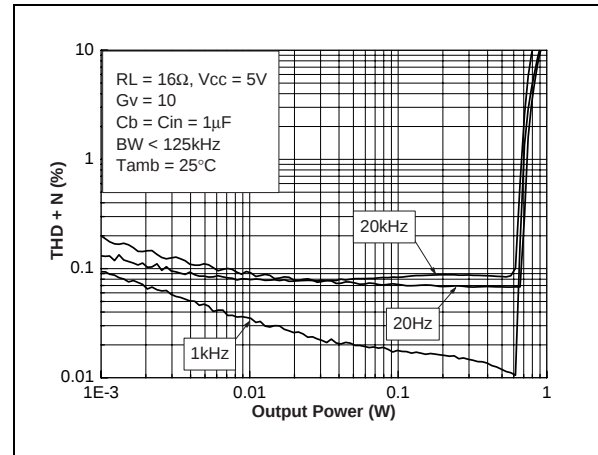


Fig. 41 : THD + N vs Output Power

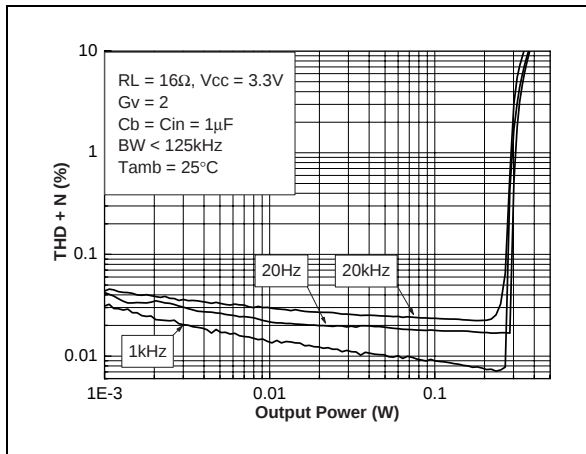


Fig. 42 : THD + N vs Output Power

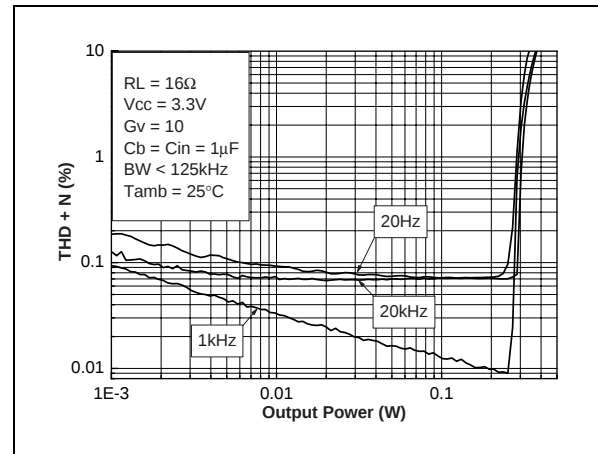


Fig. 43 : THD + N vs Output Power

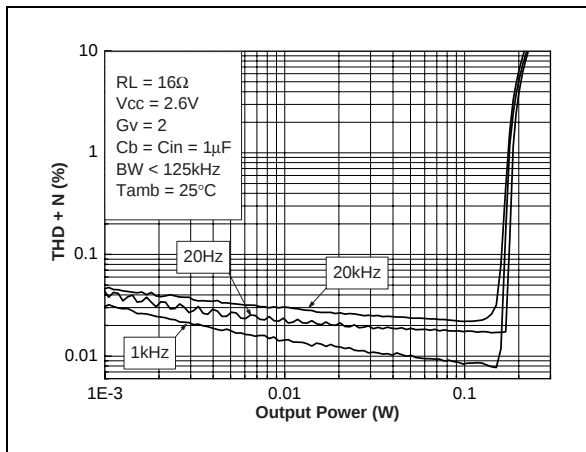


Fig. 44 : THD + N vs Output Power

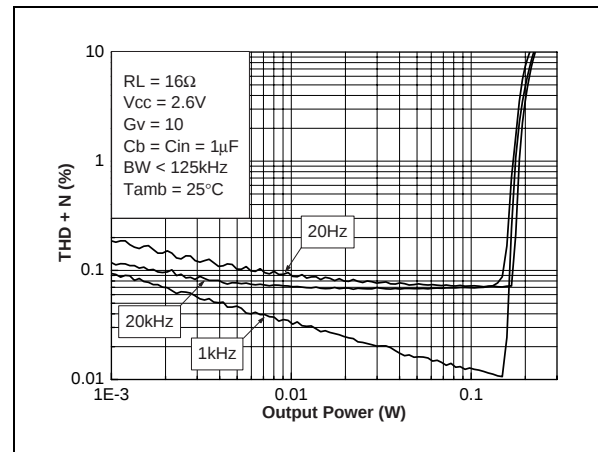


Fig. 45 : THD + N vs Frequency

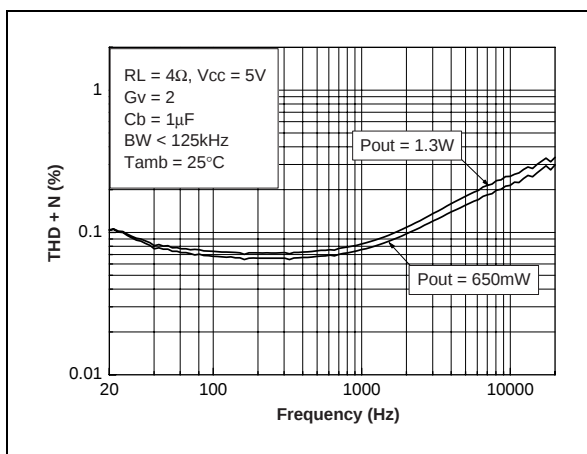


Fig. 46 : THD + N vs Frequency

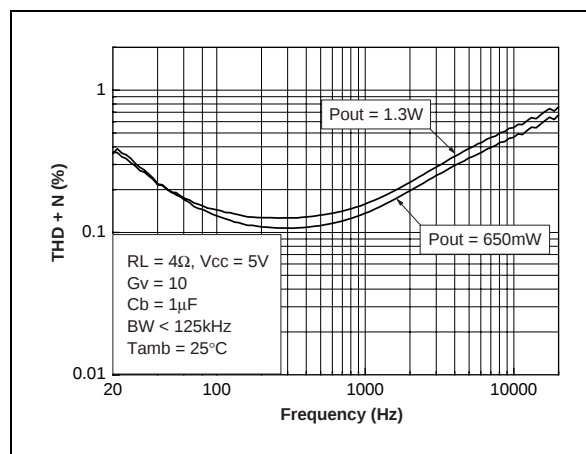


Fig. 47 : THD + N vs Frequency

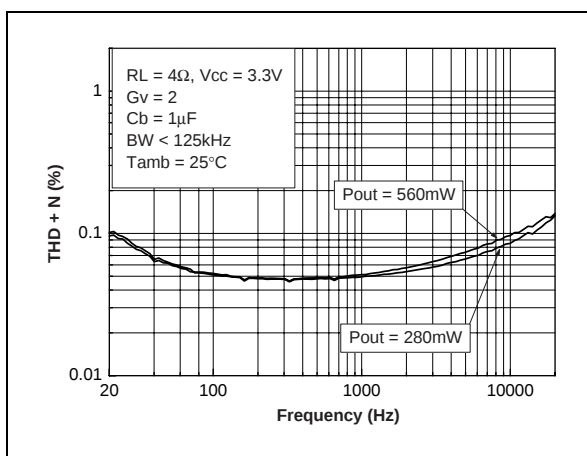


Fig. 48 : THD + N vs Frequency

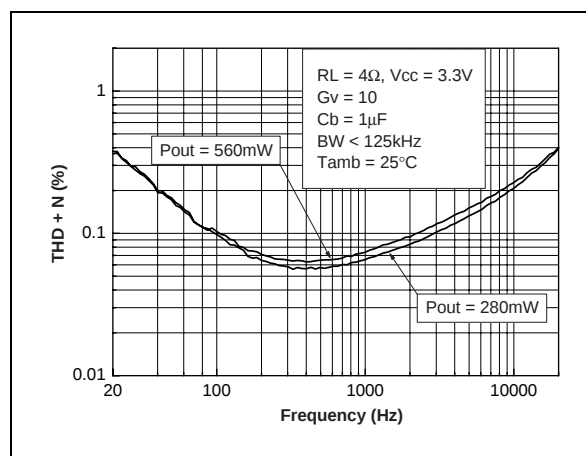


Fig. 49 : THD + N vs Frequency

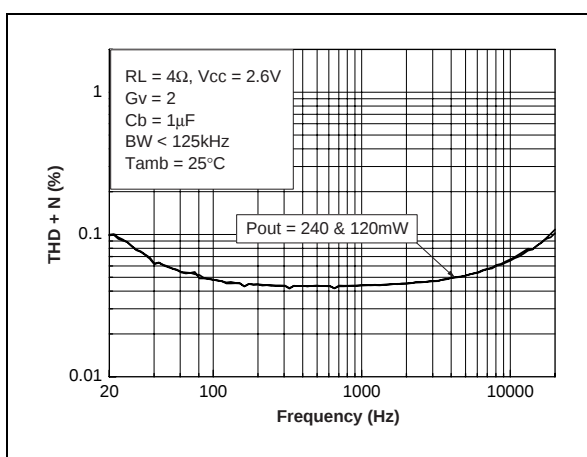


Fig. 50 : THD + N vs Frequency

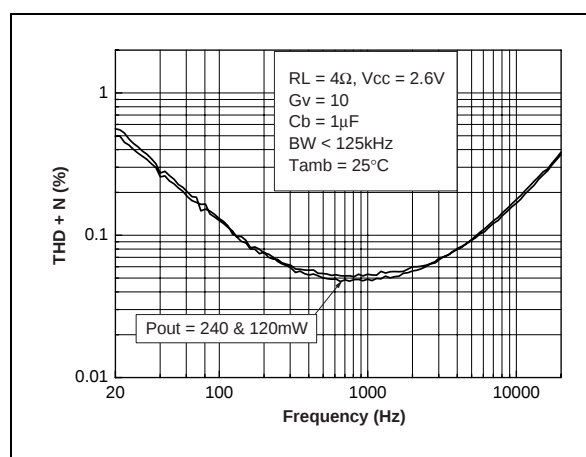


Fig. 51 : THD + N vs Frequency

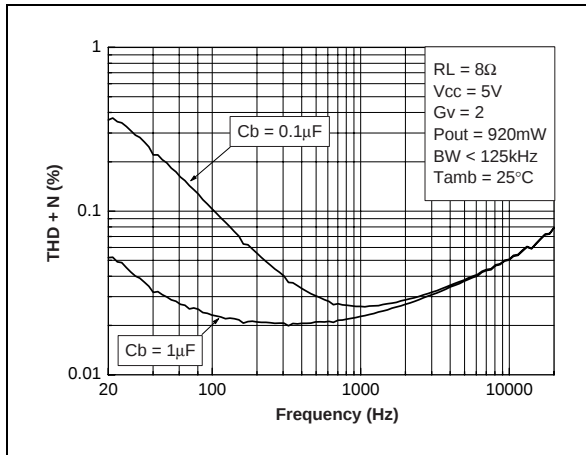


Fig. 52 : THD + N vs Frequency

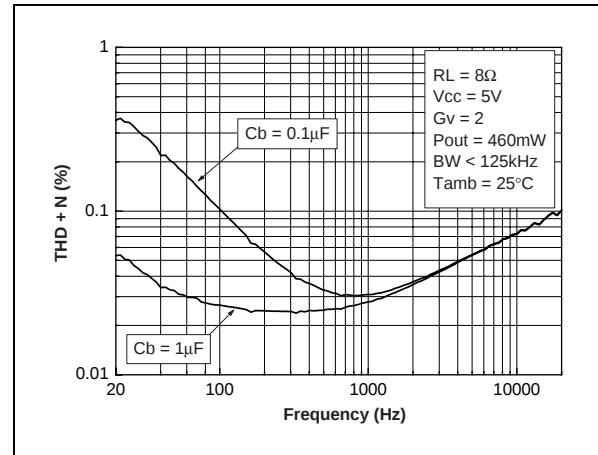


Fig. 53 : THD + N vs Frequency

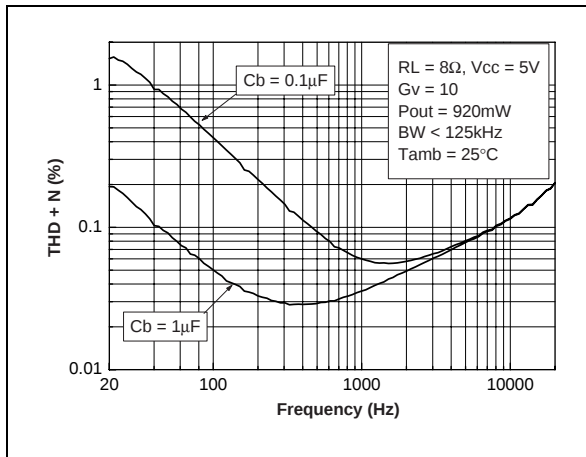


Fig. 54 : THD + N vs Frequency

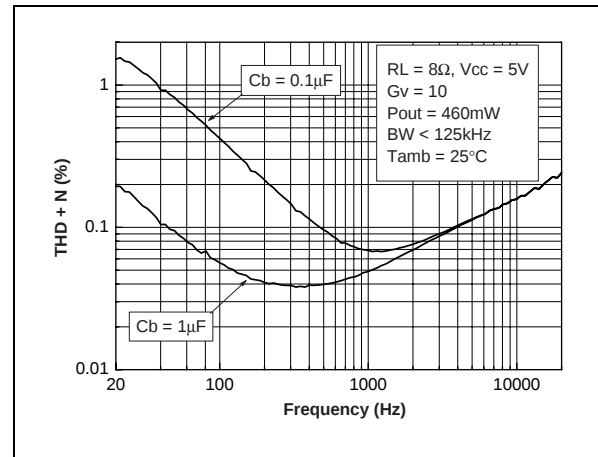


Fig. 55 : THD + N vs Frequency

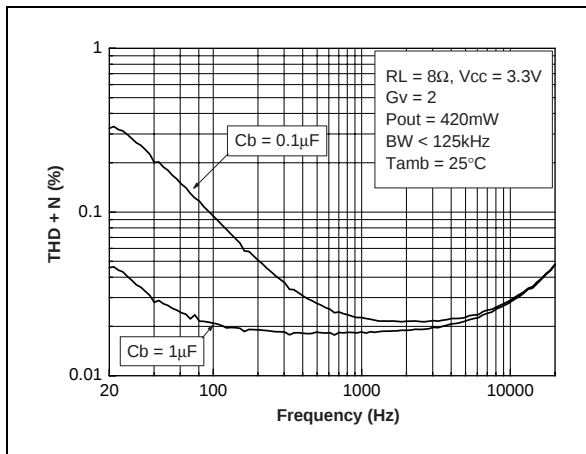


Fig. 56 : THD + N vs Frequency

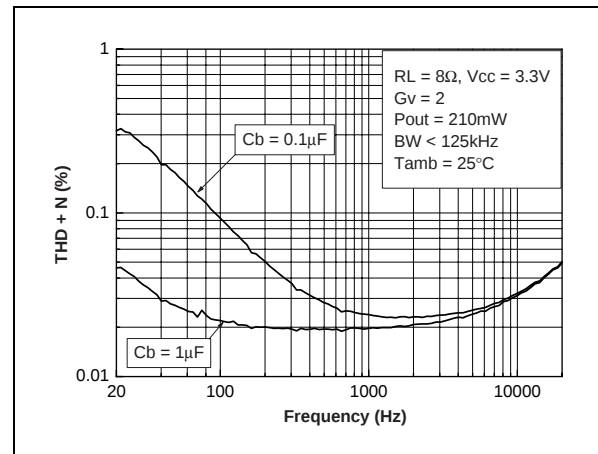


Fig. 57 : THD + N vs Frequency

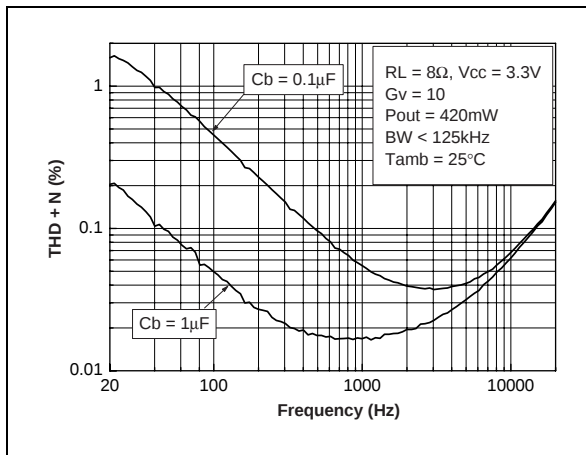


Fig. 58 : THD + N vs Frequency

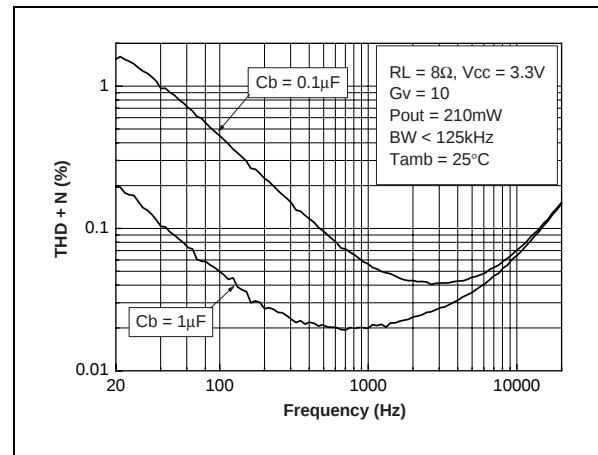


Fig. 59 : THD + N vs Frequency

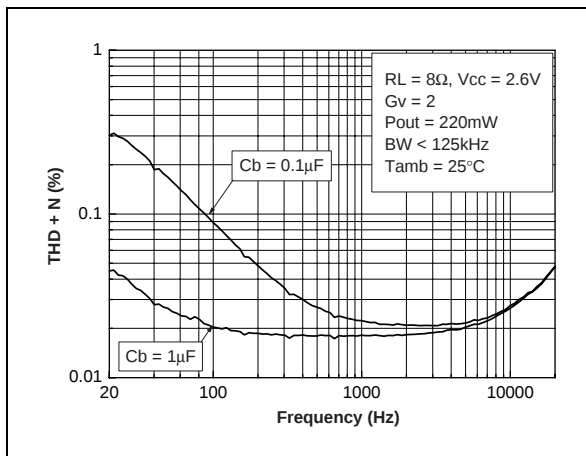


Fig. 60 : THD + N vs Frequency

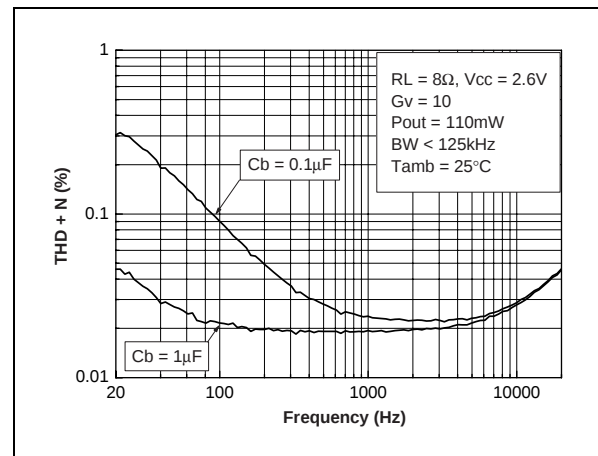


Fig. 61 : THD + N vs Frequency

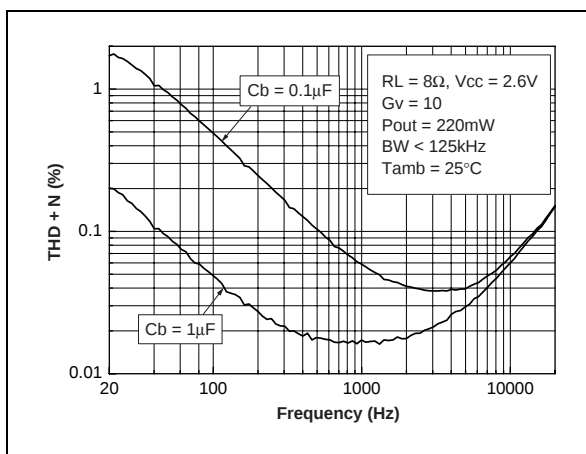


Fig. 62 : THD + N vs Frequency

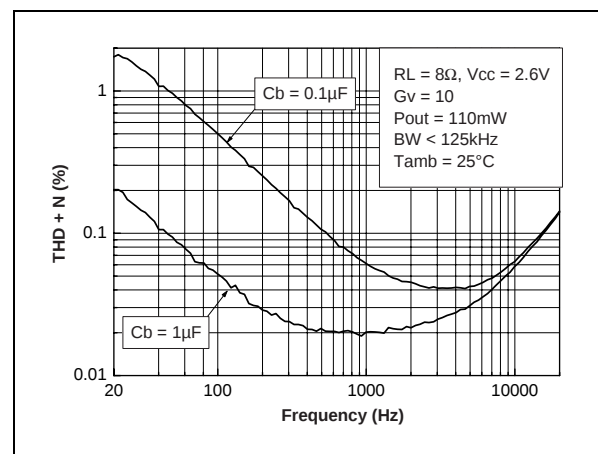


Fig. 63 : THD + N vs Frequency

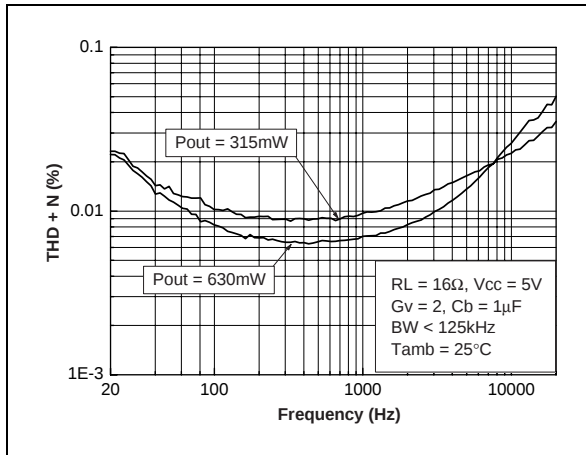


Fig. 64 : THD + N vs Frequency

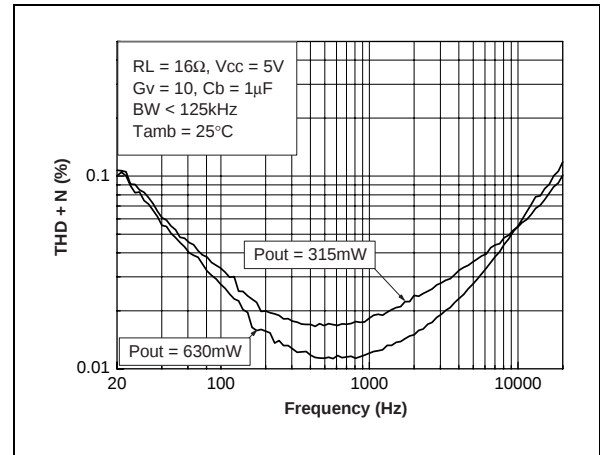


Fig. 65 : THD + N vs Frequency

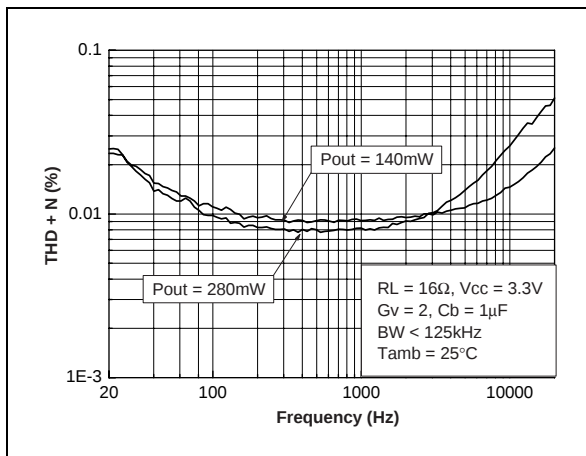


Fig. 66 : THD + N vs Frequency

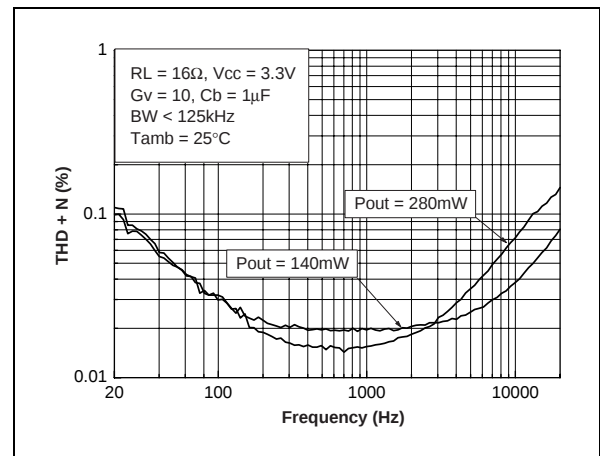


Fig. 67 : THD + N vs Frequency

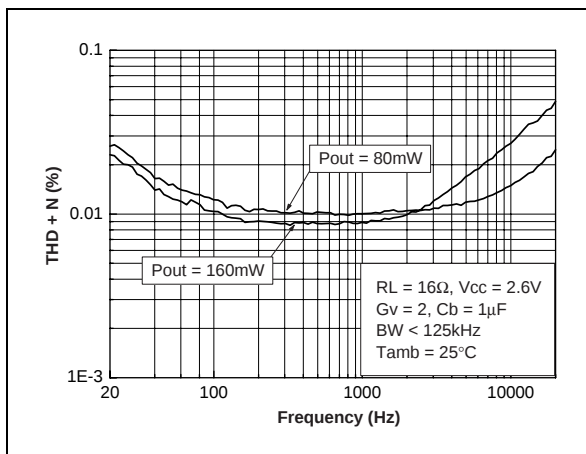


Fig. 68 : THD + N vs Frequency

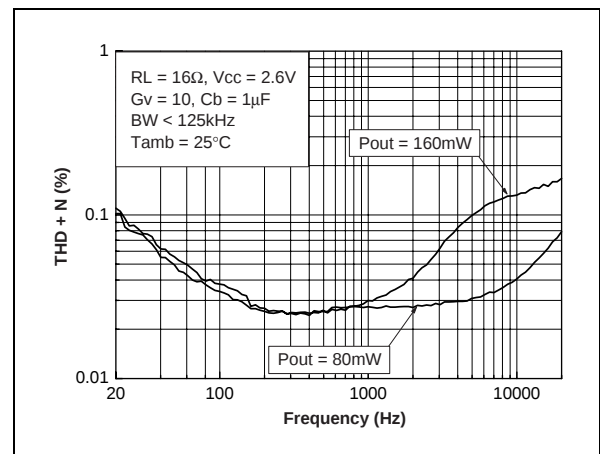


Fig. 69 : Signal to Noise Ratio vs Power Supply with Unweighted Filter (20Hz to 20kHz)

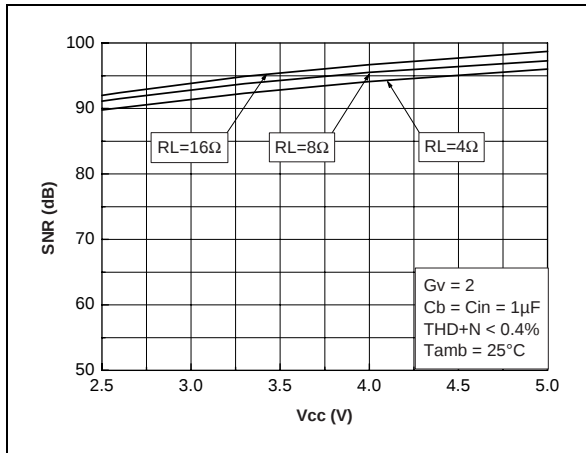


Fig. 70 : Signal to Noise Ratio vs Power Supply with Unweighted Filter (20Hz to 20kHz)

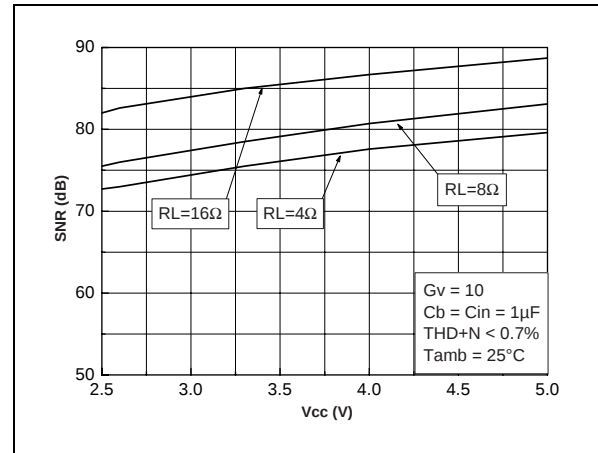


Fig. 71 : Signal to Noise Ratio vs Power Supply with Weighted Filter Type A

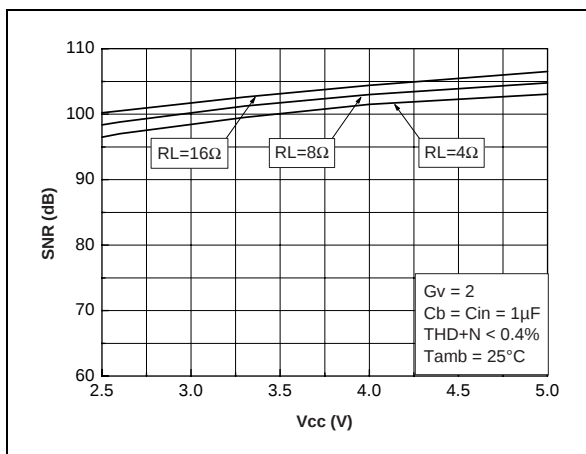


Fig. 72 : Signal to Noise Ratio vs Power Supply with Weighted Filter Type A

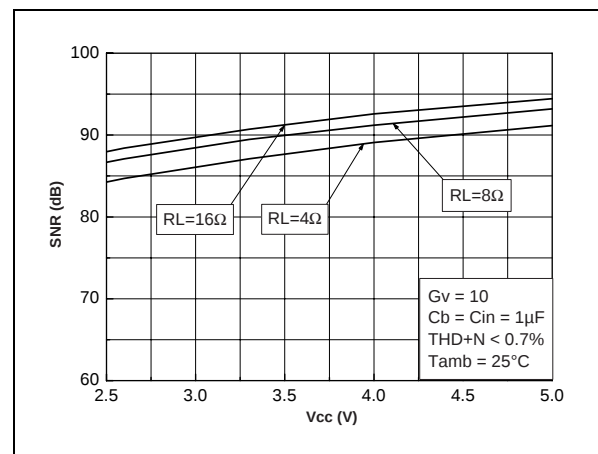


Fig. 73 : Frequency Response Gain vs C_{in} , & C_{feed}

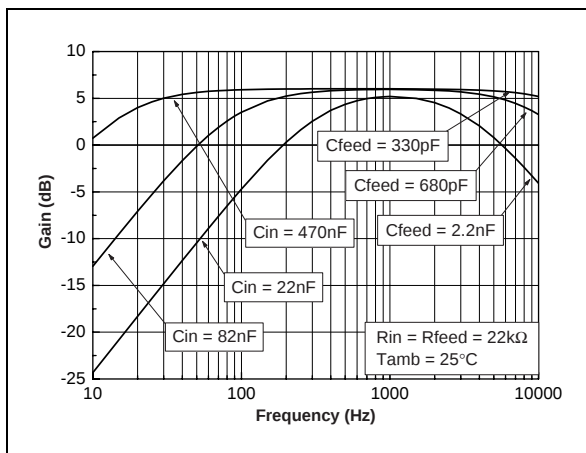


Fig. 74 : Current Consumption vs Power Supply Voltage

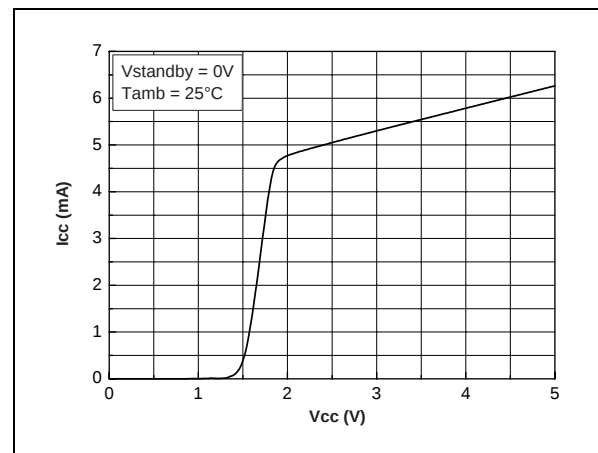


Fig. 75 : Current Consumption vs Standby Voltage @ $V_{CC} = 5V$

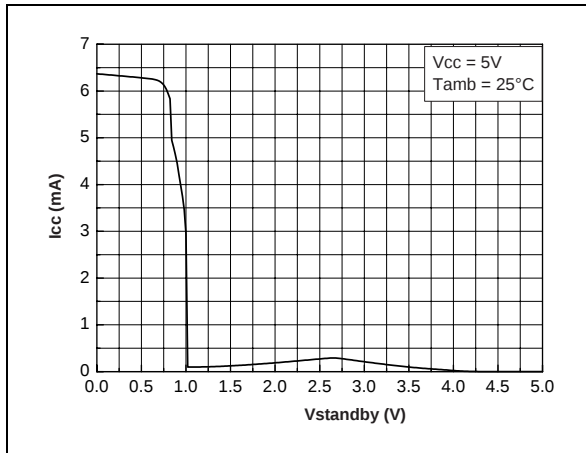


Fig. 76 : Current Consumption vs Standby Voltage @ $V_{CC} = 3.3V$

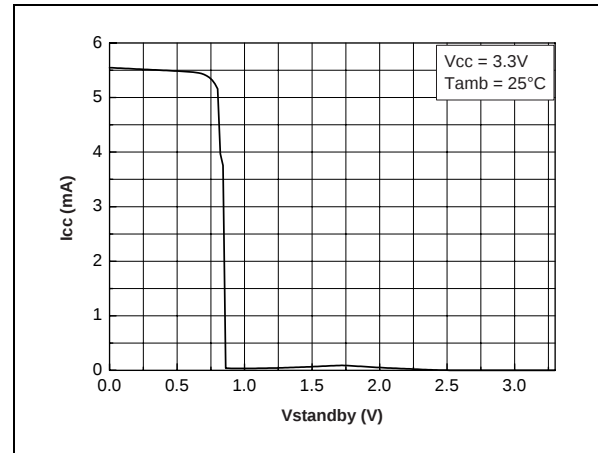


Fig. 77 : Current Consumption vs Standby Voltage @ $V_{CC} = 2.6V$

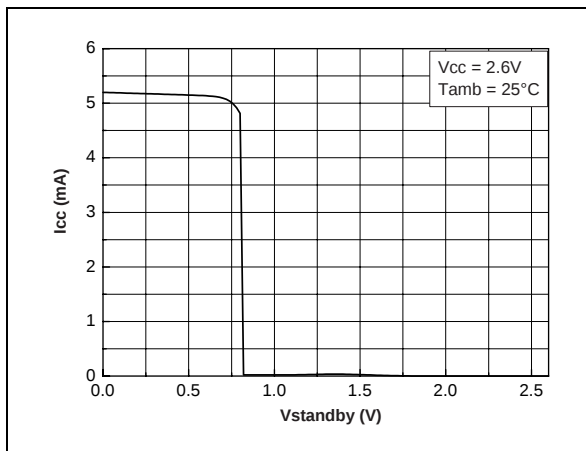


Fig. 78 : Clipping Voltage vs Power Supply Voltage and Load Resistor

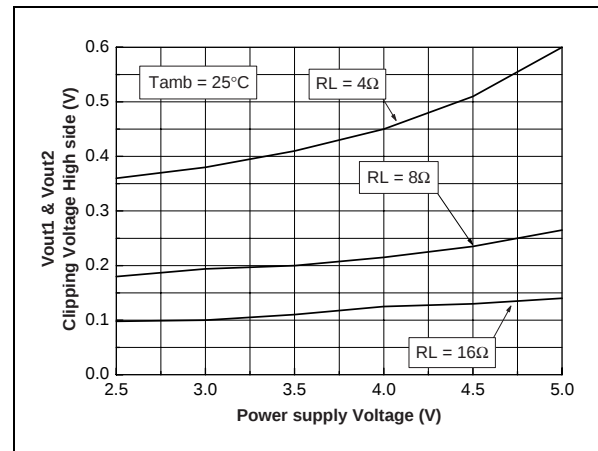
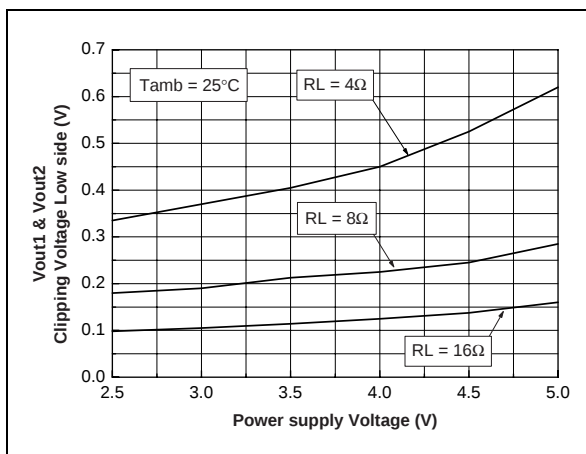


Fig. 79 : Clipping Voltage vs Power Supply Voltage and Load Resistor



APPLICATION INFORMATION

Fig. 80 : Demoboard Schematic

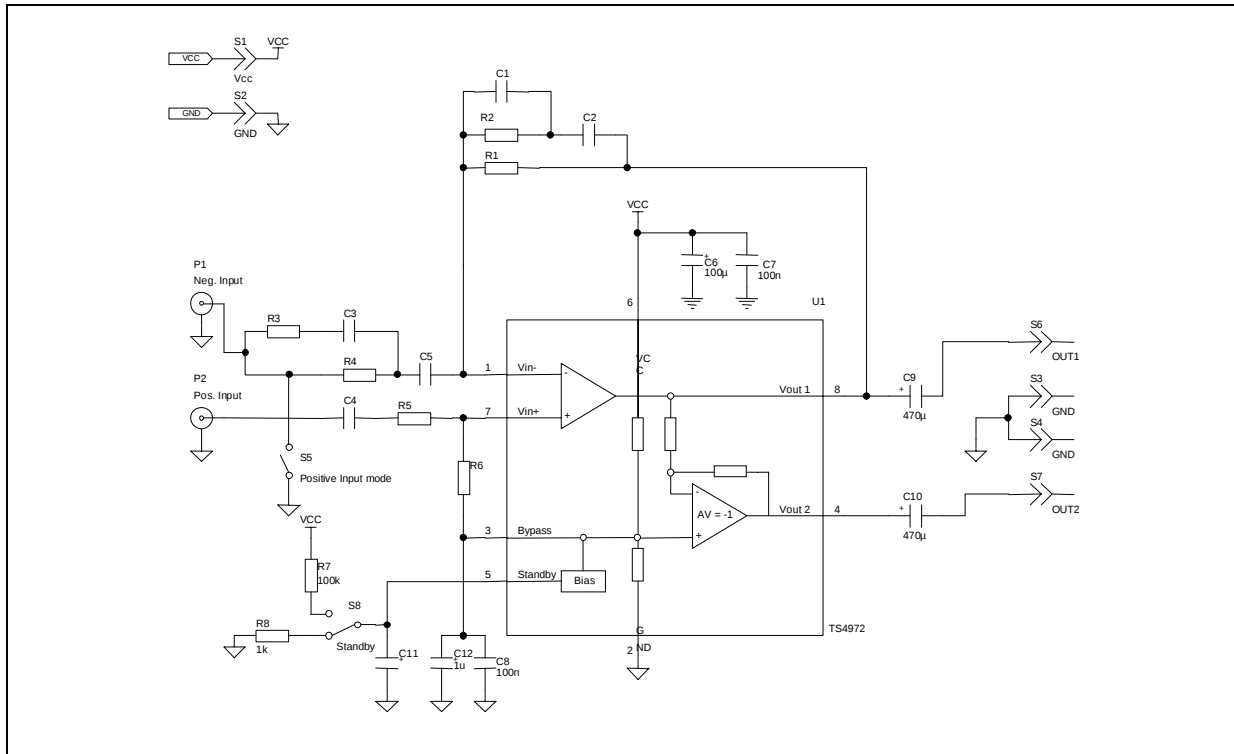


Fig. 81 : Flip-Chip 300µm Demoboard Components Side

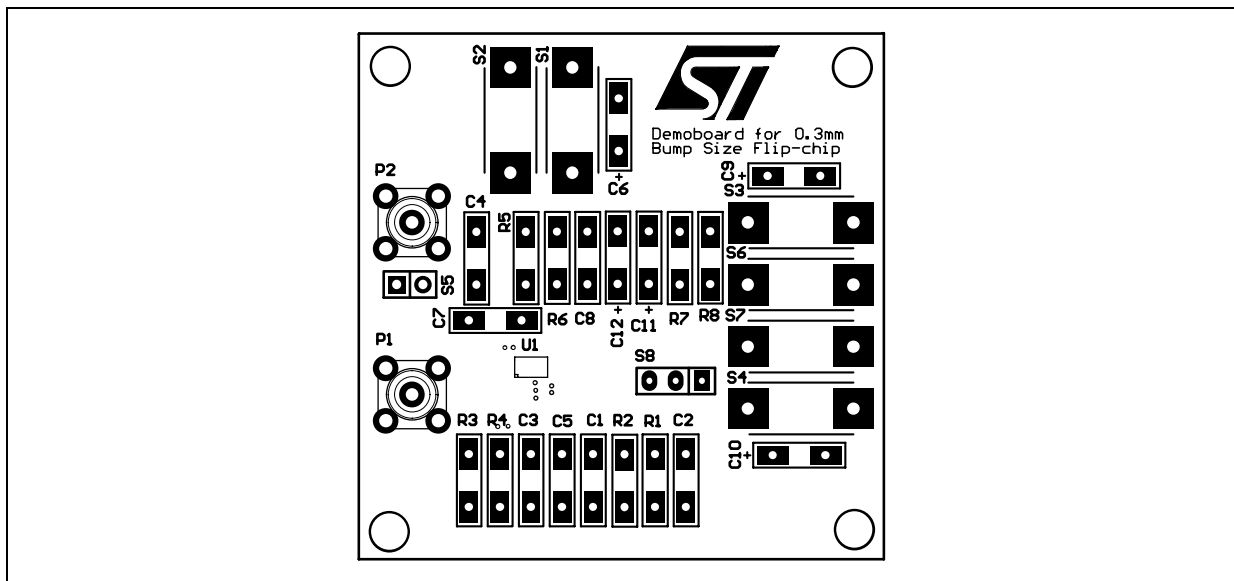


Fig. 82 : Flip-Chip 300µm Demoboard Top Solder Layer

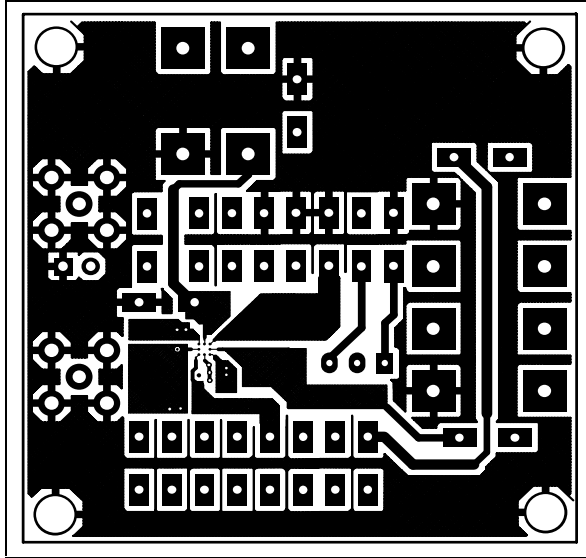
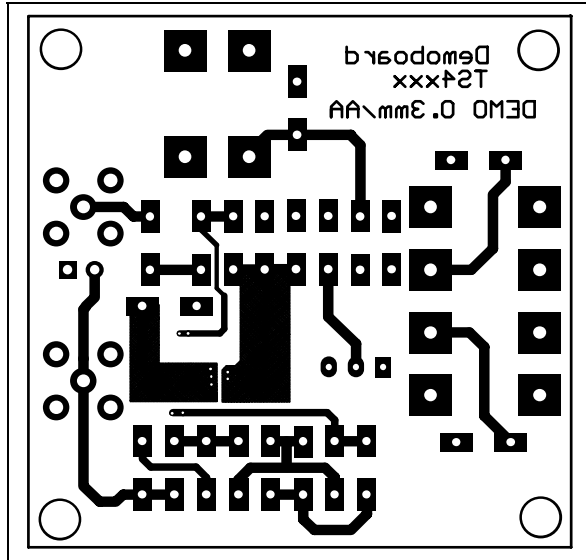


Fig. 83 : Flip-Chip 300µm Demoboard Bottom Solder Layer



■ BTL Configuration Principle

The TS4972 is a monolithic power amplifier with a BTL output type. BTL (Bridge Tied Load) means that each end of the load is connected to two single ended output amplifiers. Thus, we have :

Single ended output 1 = $V_{out1} = V_{out}$ (V)

Single ended output 2 = $V_{out2} = -V_{out}$ (V)

And $V_{out1} - V_{out2} = 2V_{out}$ (V)

The output power is:

$$P_{out} = \frac{(2 V_{out_{RMS}})^2}{R_L} (W)$$

For the same power supply voltage, the output power in BTL configuration is four times higher than the output power in single ended configuration.

■ Gain In Typical Application Schematic (cf. page 1)

In flat region (no effect of C_{in}), the output voltage of the first stage is:

$$V_{out1} = -V_{in} \frac{R_{feed}}{R_{in}} (V)$$

For the second stage : $V_{out2} = -V_{out1}$ (V)

The differential output voltage is:

$$V_{out2} - V_{out1} = 2V_{in} \frac{R_{feed}}{R_{in}} (V)$$

The differential gain named gain (G_v) for more convenient usage is:

$$G_v = \frac{V_{out2} - V_{out1}}{V_{in}} = 2 \frac{R_{feed}}{R_{in}}$$

Remark : V_{out2} is in phase with V_{in} and V_{out1} is 180 phased with V_{in} . It means that the positive terminal of the loudspeaker should be connected to V_{out2} and the negative to V_{out1} .

■ Low and high frequency response

In low frequency region, the effect of C_{in} starts. C_{in} with R_{in} forms a high pass filter with a -3dB cut off frequency.

$$F_{CL} = \frac{1}{2\pi R_{in} C_{in}} (Hz)$$

In high frequency region, you can limit the bandwidth by adding a capacitor (C_{feed}) in parallel on R_{feed} . Its form a low pass filter with a -3dB cut off frequency.

$$F_{CH} = \frac{1}{2\pi R_{feed} C_{feed}} (Hz)$$

■ Power dissipation and efficiency

Hypothesis :

- Voltage and current in the load are sinusoidal (V_{out} and I_{out})
- Supply voltage is a pure DC source (V_{cc})

Regarding the load we have:

$$V_{OUT} = V_{PEAK} \sin \omega t \text{ (V)}$$

and

$$I_{OUT} = \frac{V_{OUT}}{R_L} \text{ (A)}$$

and

$$P_{OUT} = \frac{V_{PEAK}^2}{2R_L} \text{ (W)}$$

Then, the average current delivered by the supply voltage is:

$$I_{CC \text{ AVG}} = 2 \frac{V_{PEAK}}{\pi R_L} \text{ (A)}$$

The power delivered by the supply voltage is
P_{supply} = V_{cc} I_{CC AVG} (W)

Then, the **power dissipated by the amplifier** is
P_{diss} = P_{supply} - P_{out} (W)

$$P_{diss} = \frac{2\sqrt{2}V_{CC}}{\pi\sqrt{R_L}} \sqrt{P_{OUT}} - P_{OUT} \text{ (W)}$$

and the maximum value is obtained when:

$$\frac{\partial P_{diss}}{\partial P_{OUT}} = 0$$

and its value is:

$$P_{diss \text{ max}} = \frac{2V_{CC}^2}{\pi^2 R_L} \text{ (W)}$$

Remark : This maximum value is only depending on power supply voltage and load values.

The **efficiency** is the ratio between the output power and the power supply

$$\eta = \frac{P_{OUT}}{P_{supply}} = \frac{\pi V_{PEAK}}{4V_{CC}}$$

The maximum theoretical value is reached when V_{peak} = V_{cc}, so

$$\frac{\pi}{4} = 78.5\%$$

■ Decoupling of the circuit

Two capacitors are needed to bypass properly the TS4972, a power supply bypass capacitor C_s and a bias voltage bypass capacitor C_b.

C_s has especially an influence on the THD+N in high frequency (above 7kHz) and indirectly on the power supply disturbances.

With 100μF, you can expect similar THD+N performances like shown in the datasheet.

If C_s is lower than 100μF, in high frequency increases, THD+N and disturbances on the power supply rail are less filtered.

To the contrary, if C_s is higher than 100μF, those disturbances on the power supply rail are more filtered.

C_b has an influence on THD+N in lower frequency, but its function is critical on the final result of PSRR with input grounded in lower frequency.

If C_b is lower than 1μF, THD+N increase in lower frequency (see THD+N vs frequency curves) and the PSRR worsens up

If C_b is higher than 1μF, the benefit on THD+N in lower frequency is small but the benefit on PSRR is substantial (see PSRR vs. C_b curve : fig.12).

Note that C_{in} has a non-negligible effect on PSRR in lower frequency. Lower is its value, higher is the PSRR (see fig. 13).

■ Pop and Click performance

Pop and Click performance is intimately linked with the size of the input capacitor C_{in} and the bias voltage bypass capacitor C_b.

Size of C_{in} is due to the lower cut-off frequency and PSRR value requested. Size of C_b is due to THD+N and PSRR requested always in lower frequency.

Moreover, C_b determines the speed that the amplifier turns ON. The slower the speed is, the softer the turn ON noise is.

The charge time of Cb is directly proportional to the internal generator resistance 50kΩ.

Then, the charge time constant for Cb is

$$\tau_b = 50k\Omega \times C_b \text{ (s)}$$

As Cb is directly connected to the non-inverting input (pin 2 & 3) and if we want to minimize, in amplitude and duration, the output spike on Vout1 (pin 5), Cin must be charged faster than Cb. The charge time constant of Cin is

$$\tau_{in} = (R_{in} + R_{feed}) \times C_{in} \text{ (s)}$$

Thus we have the relation

$$\tau_{in} \ll \tau_b \text{ (s)}$$

The respect of this relation permits to minimize the pop and click noise.

Remark : Minimize Cin and Cb has a benefit on pop and click phenomena but also on cost and size of the application.

Example : your target for the -3dB cut off frequency is 100 Hz. With $R_{in} = R_{feed} = 22 \text{ k}\Omega$, $C_{in} = 72 \text{ nF}$ (in fact 82nF or 100nF).

With $C_b = 1\mu\text{F}$, if you choose the one of the latest two values of Cin, the pop and click phenomena at power supply ON or standby function ON/OFF will be very small

$$50 \text{ k}\Omega \times 1\mu\text{F} \gg 44 \text{ k}\Omega \times 100 \text{ nF} \quad (50 \text{ ms} \gg 4.4 \text{ ms}).$$

Increasing Cin value increases the pop and click phenomena to an unpleasant sound at power supply ON and standby function ON/OFF.

Why Cs is not important in pop and click consideration ?

Hypothesis :

- $C_s = 100\mu\text{F}$
- Supply voltage = 5V
- Supply voltage internal resistor = 0.1Ω
- Supply current of the amplifier $I_{cc} = 6 \text{ mA}$

At power ON of the supply, the supply capacitor is charged through the internal power supply resistor. So, to reach 5V you need about five to ten times the charging time constant of Cs ($\tau_s = 0.1 \times C_s \text{ (s)}$).

Then, this time equal 50μs to 100μs $\ll \tau_b$ in the majority of application.

At power OFF of the supply, Cs is discharged by a constant current I_{cc} . The discharge time from 5V to 0V of Cs is:

$$t_{DischCs} = \frac{5C_s}{I_{cc}} = 83 \text{ ms}$$

Now, we must consider the discharge time of Cb. At power OFF or standby ON, Cb is discharged by a 100kΩ resistor. So the discharge time is about $\tau_{bDisch} \approx 3 \times C_b \times 100 \text{ k}\Omega \text{ (s)}$.

In the majority of application, $C_b = 1\mu\text{F}$, then $\tau_{bDisch} \approx 300 \text{ ms} \gg t_{dischCs}$.

■ Power amplifier design examples

Given :

- Load impedance : 8Ω
- Output power @ 1% THD+N : 0.5W
- Input impedance : 10kΩ min.
- Input voltage peak to peak : 1Vpp
- Bandwidth frequency : 20Hz to 20kHz (0, -3dB)
- Ambient temperature max = 50°C
- SO8 package

First of all, we must calculate the minimum power supply voltage to obtain 0.5W into 8Ω. With curves in fig. 15, we can read 3.5V. Thus, the power supply voltage value min. will be 3.5V.

Following the maximum power dissipation equation

$$P_{dissmax} = \frac{2V_{cc}^2}{\pi^2 R_L} \text{ (W)}$$

with 3.5V we have $P_{dissmax} = 0.31 \text{ W}$.

Refer to power derating curves (fig. 20), with 0.31W the maximum ambient temperature will be 100°C. This last value could be higher if you follow the example layout shown on the demoboard (better dissipation).

The gain of the amplifier in flat region will be:

$$G_v = \frac{V_{OUTPP}}{V_{INPP}} = \frac{2\sqrt{2R_L P_{OUT}}}{V_{INPP}} = 5.65$$

We have $R_{in} > 10 \text{ k}\Omega$. Let's take $R_{in} = 10 \text{ k}\Omega$, then $R_{feed} = 28.25 \text{ k}\Omega$. We could use for $R_{feed} = 30 \text{ k}\Omega$ in normalized value and the gain will be $G_v = 6$.

In lower frequency we want 20 Hz (-3dB cut off frequency). Then:

$$C_{IN} = \frac{1}{2\pi R_{in}F_{CL}} = 795nF$$

So, we could use for C_{in} a 1 μ F capacitor value which gives 16Hz.

In Higher frequency we want 20kHz (-3dB cut off frequency). The Gain Bandwidth Product of the TS4972 is 2MHz typical and doesn't change when the amplifier delivers power into the load.

The first amplifier has a gain of:

$$\frac{R_{feed}}{R_{in}} = 3$$

and the theoretical value of the -3dB cut-off higher frequency is 2MHz/3 = 660kHz.

We can keep this value or limit the bandwidth by adding a capacitor C_{feed} , in parallel on R_{feed} . Then:

$$C_{FEED} = \frac{1}{2\pi R_{FEED}F_{CH}} = 265pF$$

So, we could use for C_{feed} a 220pF capacitor value that gives 24kHz.

Now, we can calculate the value of C_b with the formula $\tau_b = 50k\Omega \times C_b \gg \tau_{in} = (R_{in} + R_{feed}) \times C_{in}$ which permits to reduce the pop and click effects. Then $C_b \gg 0.8\mu$ F.

We can choose for C_b a normalized value of 2.2 μ F that gives good results in THD+N and PSRR.

In the following tables, you could find three another examples with values required for the demoboard.

Application n°1 : 20Hz to 20kHz bandwidth and 6dB gain BTL power amplifier.

Components :

Designator	Part Type
R1	22k / 0.125W
R4	22k / 0.125W
R6	Short Circuit
R7	100k / 0.125W

Designator	Part Type
R8	Short Circuit
C5	470nF
C6	100 μ F
C7	100nF
C9	Short Circuit
C10	Short Circuit
C12	1 μ F
S1, S2, S6, S7	2mm insulated Plug 10.16mm pitch
S8	3 pts connector 2.54mm pitch
P1	SMB Plug

Application n°2 : 20Hz to 20kHz bandwidth and 20dB gain BTL power amplifier.

Components :

Designator	Part Type
R1	110k / 0.125W
R4	22k / 0.125W
R6	Short Circuit
R7	100k / 0.125W
R8	Short Circuit
C5	470nF
C6	100 μ F
C7	100nF
C9	Short Circuit
C10	Short Circuit
C12	1 μ F
S1, S2, S6, S7	2mm insulated Plug 10.16mm pitch
S8	3 pts connector 2.54mm pitch
P1	SMB Plug

Application n°3 : 50Hz to 10kHz bandwidth and 10dB gain BTL power amplifier.

Components :

Designator	Part Type
R1	33k / 0.125W
R2	Short Circuit
R4	22k / 0.125W
R6	Short Circuit
R7	100k / 0.125W
R8	Short Circuit
C2	470pF
C5	150nF
C6	100μF
C7	100nF
C9	Short Circuit
C10	Short Circuit
C12	1μF
S1, S2, S6, S7	2mm insulated Plug 10.16mm pitch
S8	3 pts connector 2.54mm pitch
P1	SMB Plug

Application n°4 : Differential inputs BTL power amplifier.

In this configuration, we need to place these components : R1, R4, R5, R6, R7, C4, C5, C12.

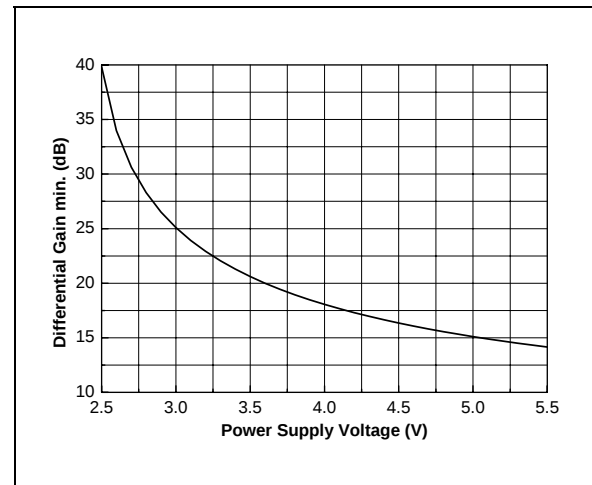
We have also : R4 = R5, R1 = R6, C4 = C5.

The differential gain of the amplifier is:

$$G_{VDIFF} = 2 \frac{R1}{R4}$$

Note : Due to the VICM range (see Operating Condition), G_{VDIFF} must have a minimum value shown in figure 84.

Fig. 84 : Minimum Differential Gain vs Power Supply Voltage



For V_{cc}=5V, a 20Hz to 20kHz bandwidth and 20dB gain BTL power amplifier you could follow the bill of material below.

Components :

Designator	Part Type
R1	110k / 0.125W
R4	22k / 0.125W
R5	22k / 0.125W
R6	110k / 0.125W
R7	100k / 0.125W
R8	Short circuit
C4	470nF
C5	470nF
C6	100μF
C7	100nF
C9	Short Circuit
C10	Short Circuit
C12	1μF
S1, S2, S6, S7	2mm insulated Plug 10.16mm pitch
S8	3 pts connector 2.54mm pitch
P1, P2	SMB Plug

■ Note on how to use the PSRR curves (page 7)

We have finished a design and we have chosen the components values :

- $R_{in}=R_{feed}=22k\Omega$
- $C_{in}=100nF$
- $C_b=1\mu F$

Now, on fig. 13, we can see the PSRR (input grounded) vs frequency curves. At 217Hz we have a PSRR value of -36dB.

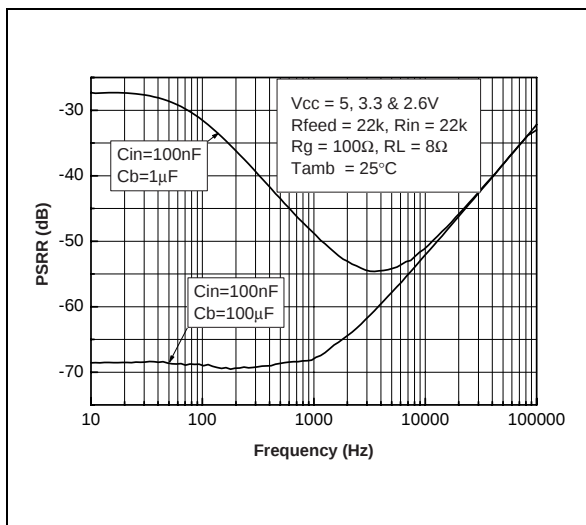
In reality we want a value about -70dB. So, we need a gain of 34dB !

Now, on fig. 12 we can see the effect of C_b on the PSRR (input grounded) vs. frequency. With $C_b=100\mu F$, we can reach the -70dB value.

The process to obtain the final curve ($C_b=100\mu F$, $C_{in}=100nF$, $R_{in}=R_{feed}=22k\Omega$) is a simple transfer point by point on each frequency of the curve on fig. 13 to the curve on fig. 12.

The measurement result is shown on the next figure.

Fig. 85 : PSRR changes with C_b



■ Note on PSRR measurement

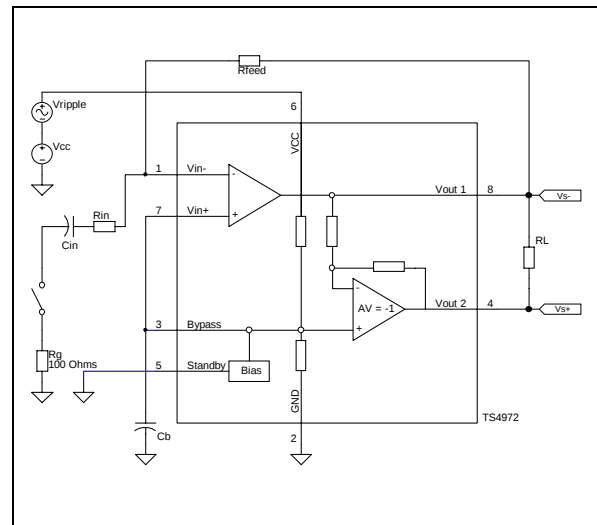
What is the PSRR ?

The PSRR is the Power Supply Rejection Ratio. It's a kind of SVR in a determined frequency range. The PSRR of a device, is the ratio between a power supply disturbance and the result on the output. We can say that the PSRR is the ability of a device to minimize the impact of power supply disturbances to the output.



How we measure the PSRR ?

Fig. 86 : PSRR measurement schematic



■ Principle of operation

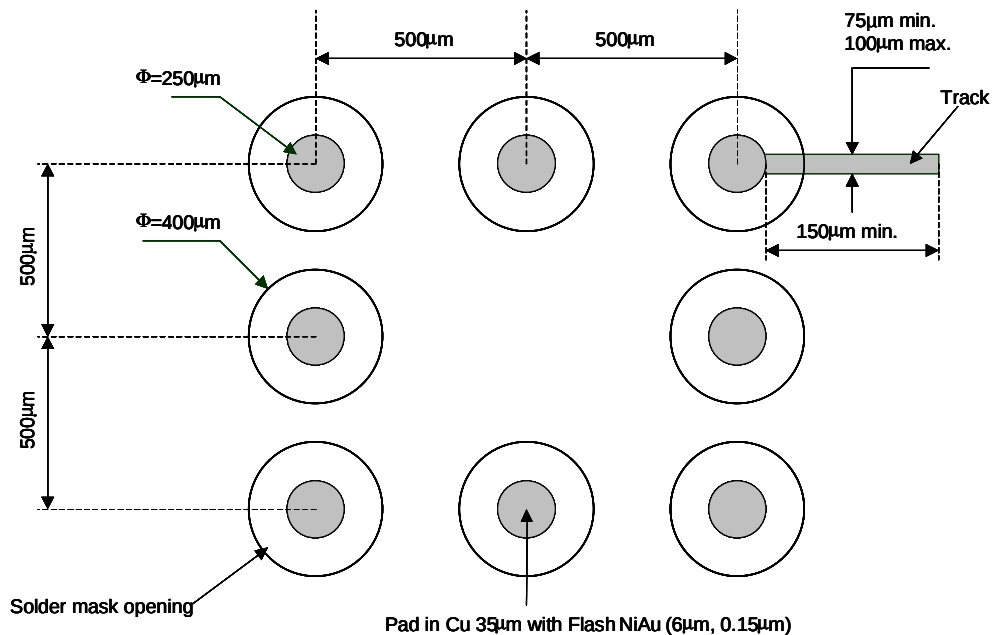
- We fixed the DC voltage supply (V_{cc})
- We fixed the AC sinusoidal ripple voltage (V_{ripple})
- No bypass capacitor C_s is used

The PSRR value for each frequency is:

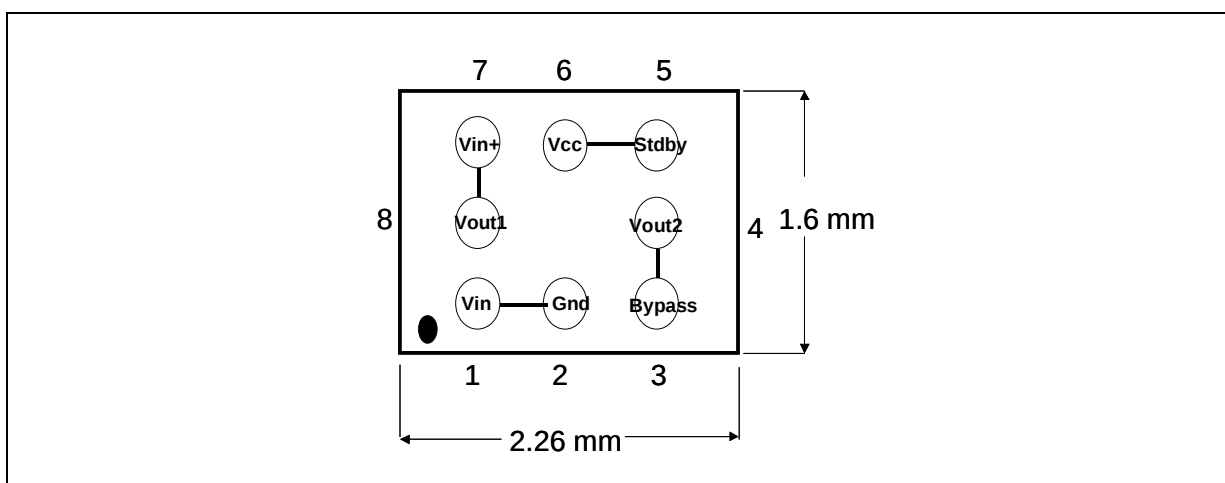
$$PSRR(dB) = 20 \times \log_{10} \left[\frac{Rms(V_{ripple})}{Rms(V_{s+} - V_{s-})} \right]$$

Remark : The measure of the Rms voltage is not a Rms selective measure but a full range (2 Hz to 125 kHz) Rms measure. It means that we measure the effective Rms signal + the noise.

Fig. 87 :TS4972 Footprint Recommendation (Non Solder Mask Defined)



TOP VIEW OF THE DAISY CHAIN MECHANICAL DATA (all drawings dimensions are in millimeters)



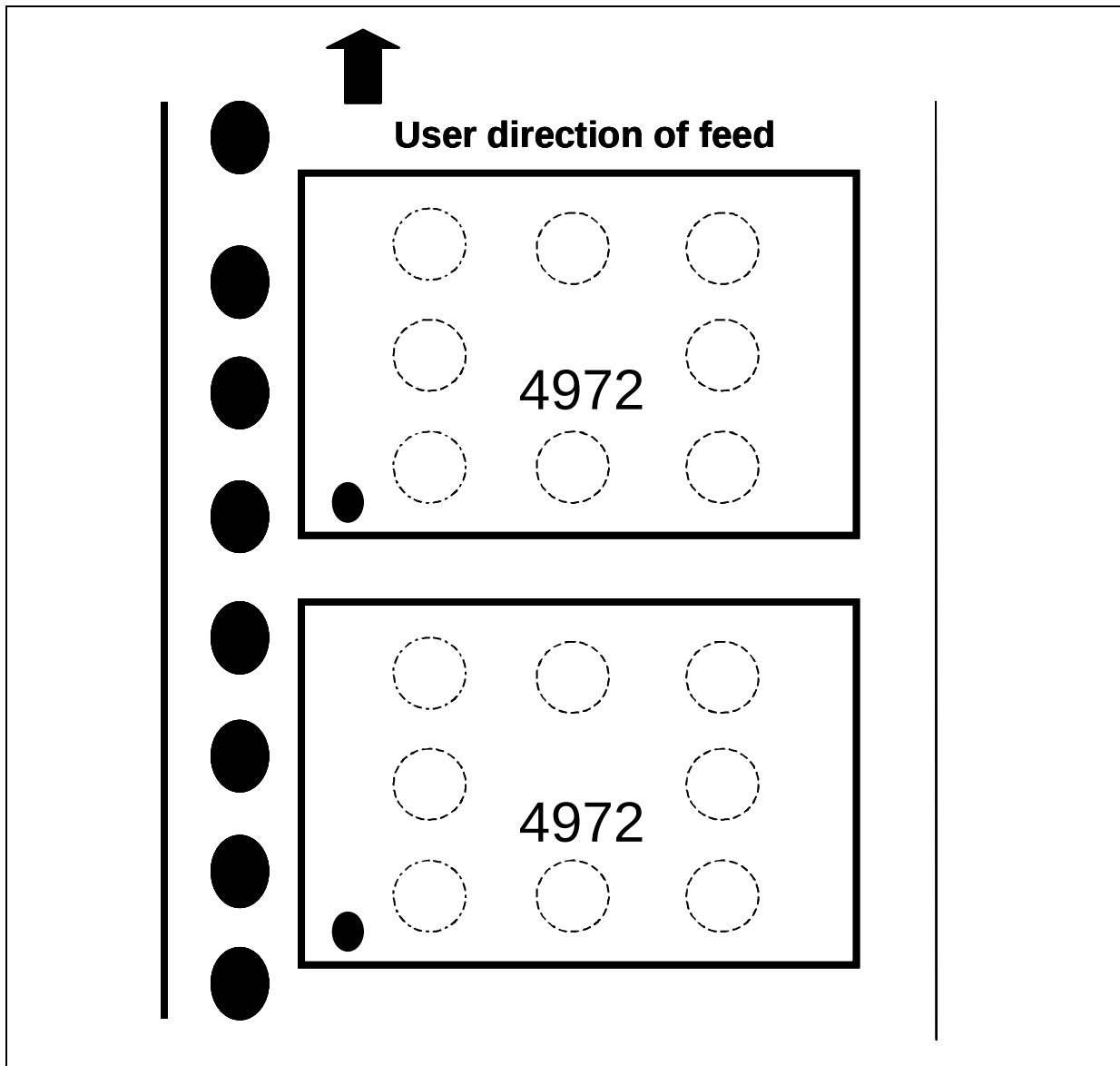
REMARKS

Daisy chain sample is featuring pins connection two by two. The schematic above is illustrating the way connecting pins each other. This sample is used for testing continuity on board. PCB needs to be designed on the opposite way, where pin connections are not done on daisy chain samples. By that way, just connecting an Ohmeter between pin 8 and pin 1, the soldering process continuity can be tested.

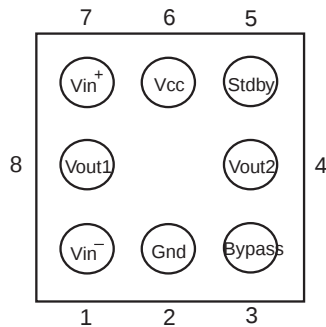
ORDER CODE

Part Number	Temperature Range	Package	Marking
		J	
TSDC03IJT	-40, +85°C	•	DC3

TAPE & REEL SPECIFICATION (top view)

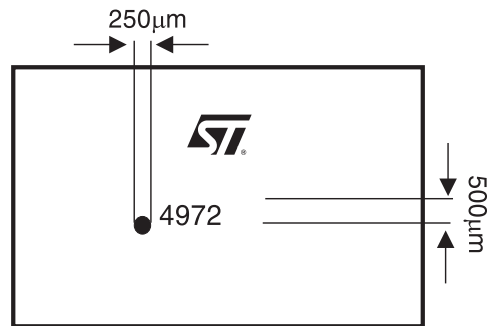


PIN OUT (Top View)



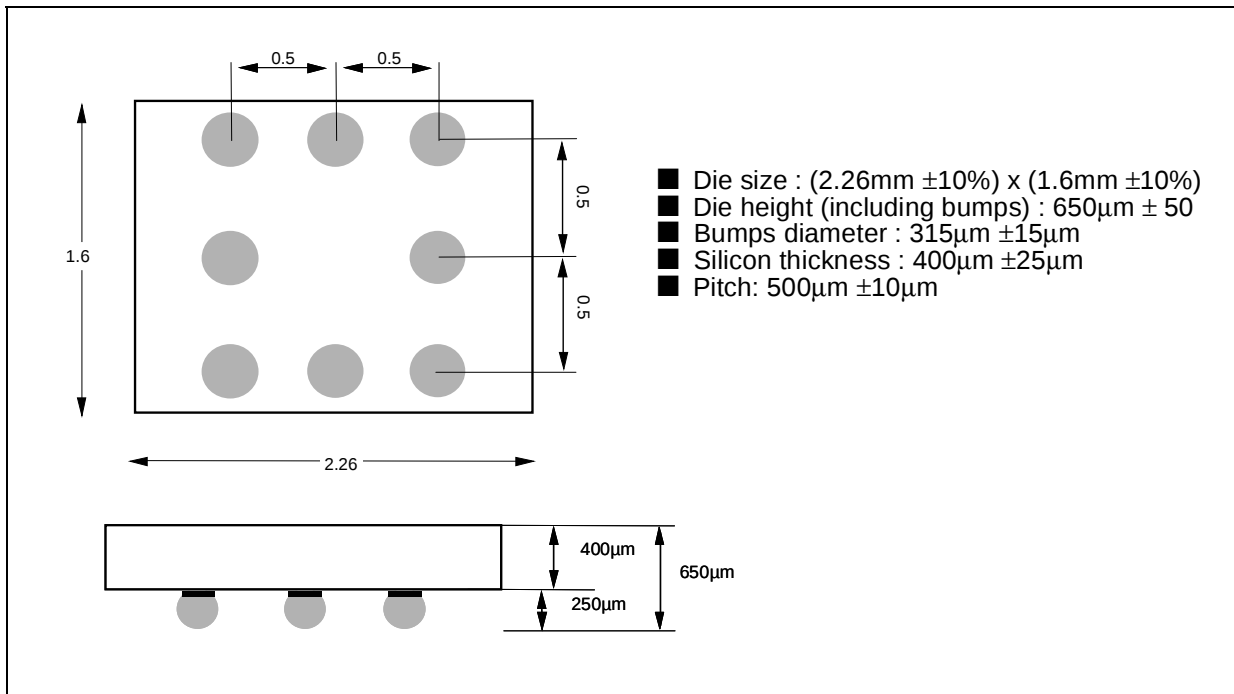
■ Balls are underneath

MARKING (Top View)



PACKAGE MECHANICAL DATA

FLIP CHIP - 8 BUMPS



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