TS486
TS487

100mW STEREO HEADPHONE AMPLIFIER WITH STANDBY MODE

- OPERATING FROM Vcc=2V to 5.5V
- **STANDBY MODE** ACTIVE LOW (TS486) or HIGH (TS487)
- OUTPUT POWER: 102mW @5V, 38mW @3.3V into 16Ω with 0.1% THD+N max (1kHz)
- **LOW CURRENT CONSUMPTION**: 2.5mA max
- High Signal-to-Noise ratio: 103dB(A) at 5V
- High Crosstalk immunity: 83dB (F=1kHz)
- PSRR: 58 dB (F=1kHz), inputs grounded
- ON/OFF click reduction circuitry
- Unity-Gain Stable
- **SHORT CIRCUIT LIMITATION**
- Available in SO8, MiniSO8 & DFN 3x3mm

DESCRIPTION

The TS486/7 is a dual audio power amplifier capable of driving, in single-ended mode, either a 16 or a 32Ω stereo headset.

Capable of descending to low voltages, it delivers up to 90mW per channel (into 16Ω loads) of continuous average power with 0.3% THD+N in the audio bandwitdth from a 5V power supply.

An externally-controlled standby mode reduces the supply current to 10nA (typ.). The unity gain stable TS486/7 can be configured by external gain-setting resistors or used in a fixed gain version.

APPLICATIONS

- Headphone Amplifier
- Mobile phone, PDA, computer motherboard
- High end TV, portable audio player

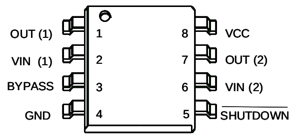
ORDER CODE

Part Number	Temperature Range: I	Package D	Package S	Package Q	Gain	Marking
TS486	-40, +85°C	•			external	TS486I
TS487		•			external	TS487I
TS486			•	•	external	K86A
TS486-1			tba	tba	x1/0dB	K86B
TS486-2			tba	tba	x2/6dB	K86C
TS486-4			tba	tba	x4/12dB	K86D
TS487			•	•	external	K87A
TS487-1			tba	tba	x1/0dB	K87B
TS487-2			tba	tba	x2/6dB	K87C
TS487-4			tba	tba	x4/12dB	K87D

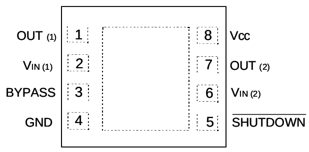
MiniSO & DFN only available in Tape & Reel with T suffix,
SO is available in Tube (D) and in Tape & Reel (DT)

PIN CONNECTIONS (top view)

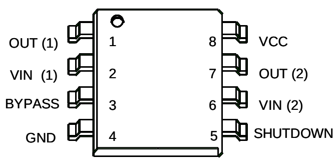
TS486IDT: SO8, TS486IST, TS486-1IST, TS486-2IST, TS486-4IST: MiniSO8



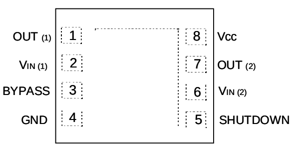
TS486-IQT, TS486-1IQT, TS486-2IQT, TS486-4IQT: DFN8



TS487IDT: SO8, TS487IST, TS487-1IST, TS487-2IST, TS487-4IST: MiniSO8



TS487-IQT, TS487-1IQT, TS487-2IQT, TS487-4IQT: DFN8



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage [1]	6	V
V_i	Input Voltage	-0.3v to V_{CC} +0.3v	V
T_{stg}	Storage Temperature	-65 to +150	°C
T_j	Maximum Junction Temperature	150	°C
R_{thja}	Thermal Resistance Junction to Ambient SO8 MiniSO8 DFN8	 175 215 70	°C/W
Pd	Power Dissipation [2] SO8 MiniSO8 DFN8	 0.71 0.58 1.79	W
ESD	Human Body Model (pin to pin): TS486, TS487[3]	1.5	kV
ESD	Machine Model - 220pF - 240pF (pin to pin)	100	V
Latch-up	Latch-up Immunity (All pins)	200	mA
	Lead Temperature (soldering, 10sec)	250	°C
	Output Short-Circuit to Vcc or GND	continous [4]	

1. All voltage values are measured with respect to the ground pin.
2. Pd has been calculated with Tamb = 25°C, Tjunction = 150°C.
3. TS487 stands 1.5KV on all pins except standby pin which stands 1KV.
4. Attention must be paid to continous power dissipation (V_{DD} x 300mA). Exposure of the IC to a short circuit for an extended time period is dramatically reducing product life expectancy.

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 5.5	V
R_L	Load Resistor	≥ 16	Ω
T_{oper}	Operating Free Air Temperature Range	-40 to + 85	°C
C_L	Load Capacitor R_L = 16 to 100Ω R_L > 100Ω	 400 100	pF
V_{STB}	Standby Voltage Input TS486 ACTIVE / TS487 in STANDBY TS486 in STANDBY / TS487 ACTIVE	 $1.5 \leq V_{STB} \leq V_{CC}$ $GND \leq V_{STB} \leq 0.4$ [1]	V
R_{THJA}	Thermal Resistance Junction to Ambient SO8 MiniSO8 DFN8[2]	 150 190 41	°C/W

1. The minimum current consumption ($I_{STANDBY}$) is guaranteed at GND (TS486) or V_{CC} (TS487) for the whole temperature range.
2. When mounted on a 4-layer PCB.

FIXED GAIN VERSION SPECIFIC ELECTRICAL CHARACTERISTICS

V_{CC} from **+5V to +2V**, GND = **0V**, T_{amb} = 25°C (unless otherwise specified)

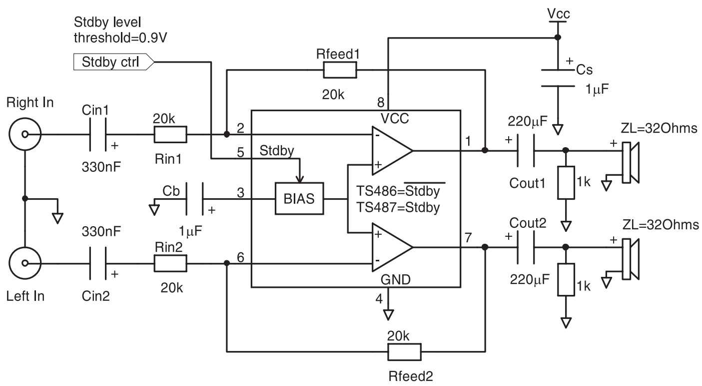
Symbol	Parameter	Min.	Typ.	Max.	Unit
$R_{IN\ 1,2}$	Input Resistance [1)]		20		kΩ
G	Gain value for Gain TS486/TS487-1 Gain value for Gain TS486/TS487-2 Gain value for Gain TS486/TS487-4		0dB 6dB 12dB		dB

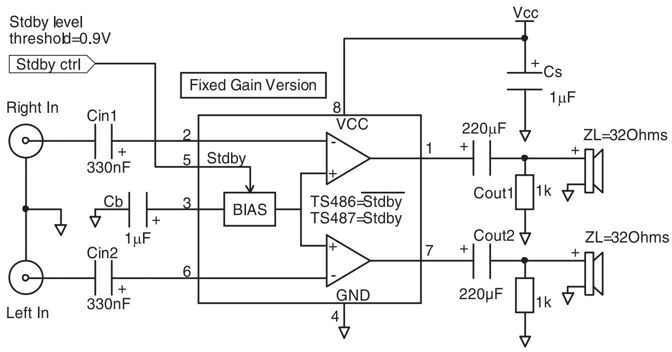
1. See figure 30 to establish the value of Cin vs. -3dB cut off frequency.

APPLICATION COMPONENTS INFORMATION

Components	Functional Description
$R_{IN1,2}$	Inverting input resistor which sets the closed loop gain in conjunction with R_{FEED}. This resistor also forms a high pass filter with C_{IN} (fc = 1 / (2 x Pi x R_{IN} x C_{IN})) . **Not needed in fixed gain versions.**
$C_{IN1,2}$	Input coupling capacitor which blocks the DC voltage at the amplifier's input terminal.
$R_{FEED1,2}$	Feedback resistor which sets the closed loop gain in conjunction with R_{IN}. A_V= Closed Loop Gain= -R_{FEED}/R_{IN}. **Not needed in fixed gain versions.**
C_S	Supply Bypass capacitor which provides power supply filtering.
C_B	Bypass capacitor which provides half supply filtering.
$C_{OUT1,2}$	Output coupling capacitor which blocks the DC voltage at the load input terminal. This capacitor also forms a high pass filter with RL (fc = 1 / (2 x Pi x R_L x C_{OUT})).

TYPICAL APPLICATION SCHEMATICS





ELECTRICAL CHARACTERISTICS

V_{CC} = **+5V**, GND = **0V**, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		1.8	2.5	mA
$I_{STANDBY}$	Standby Current No input signal, $V_{STANDBY}$=GND for TS486, R_L=32Ω No input signal, $V_{STANDBY}$=Vcc for TS487, R_L=32Ω		10	1000	nA
V_{IO}	Input Offset Voltage (V_{ICM} = V_{CC}/2)		1		mV
I_{IB}	Input Bias Current (V_{ICM} = V_{CC}/2) [1)]		90	200	nA
P_O	Output Power THD+N = 0.1% Max, F = 1kHz, R_L = 32Ω THD+N = 1% Max, F = 1kHz, R_L = 32Ω THD+N = 0.1% Max, F = 1kHz, R_L = 16Ω THD+N = 1% Max, F = 1kHz, R_L = 16Ω	60 95	64 65 102 108		mW
THD + N	Total Harmonic Distortion + Noise (A_V=-1) R_L = 32Ω, P_{out} = 60mW, 20Hz ≤ F ≤ 20kHz R_L = 16Ω, P_{out} = 90mW, 20Hz ≤ F ≤ 20kHz		0.3 0.3		%
PSRR	Power Supply Rejection Ratio, inputs grounded [2)] (A_V=-1), RL>=16Ω, C_B=1µF, F = 1kHz, Vripple = 200mVpp	53	58		dB
I_O	Max Output Current THD +N ≤ 1%, R_L = 16Ω connected between out and V_{CC}/2	106	115		mA
V_O	Output Swing V_{OL} : R_L = 32Ω V_{OH} : R_L = 32Ω V_{OL} : R_L = 16Ω V_{OH} : R_L = 16Ω	4.45 4.2	0.45 4.52 0.6 4.35	0.5 0.7	V
SNR	Signal-to-Noise Ratio (A weighted, A_V=-1) [2)] (R_L = 32Ω, THD +N < 0.4%, 20Hz ≤ F ≤ 20kHz)	80	103		dB
Crosstalk	Channel Separation, R_L = 32Ω, A_V=-1 F = 1kHz F = 20Hz to 20kHz Channel Separation, R_L = 16Ω, A_V=-1 F = 1kHz F = 20Hz to 20kHz		83 79 80 72		dB
C_I	Input Capacitance		1		pF
GBP	Gain Bandwidth Product (R_L = 32Ω)		1.1		MHz
SR	Slew Rate, Unity Gain Inverting (R_L = 16Ω)		0.4		V/µs

1. Only for external gain version.
2. Guaranteed by design and evaluation.

ELECTRICAL CHARACTERISTICS

V_{CC} = **+3.3V**, GND = **0V**, T_{amb} = 25°C (unless otherwise specified) [1)]

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		1.8	2.5	mA
$I_{STANDBY}$	Standby Current No input signal, $V_{STANDBY}$=GND for TS486, R_L=32Ω No input signal, $V_{STANDBY}$=Vcc for TS487, R_L=32Ω		10	1000	nA
V_{IO}	Input Offset Voltage ($V_{ICM} = V_{CC}/2$)		1		mV
I_{IB}	Input Bias Current ($V_{ICM} = V_{CC}/2$) [2)]		90	200	nA
P_O	Output Power THD+N = 0.1% Max, F = 1kHz, R_L = 32Ω THD+N = 1% Max, F = 1kHz, R_L = 32Ω THD+N = 0.1% Max, F = 1kHz, R_L = 16Ω THD+N = 1% Max, F = 1kHz, R_L = 16Ω	 23 36	 26 28 38 42		mW
THD + N	Total Harmonic Distortion + Noise (A_v=-1) R_L = 32Ω, P_{out} = 16mW, 20Hz ≤ F ≤ 20kHz R_L = 16Ω, P_{out} = 35mW, 20Hz ≤ F ≤ 20kHz		 0.3 0.3		%
PSRR	Power Supply Rejection Ratio, inputs grounded [3)] (A_v=-1), RL>=16Ω, C_B=1µF, F = 1kHz, Vripple = 200mVpp	53	58		dB
I_O	Max Output Current THD +N ≤ 1%, R_L = 16Ω connected between out and $V_{CC}/2$	64	75		mA
V_O	Output Swing V_{OL} : R_L = 32Ω V_{OH} : R_L = 32Ω V_{OL} : R_L = 16Ω V_{OH} : R_L = 16Ω	 2.85 2.68	 0.3 3 0.45 2.85	 0.38 0.52	V
SNR	Signal-to-Noise Ratio (A weighted, A_v=-1) [3)] (R_L = 32Ω, THD +N < 0.4%, 20Hz ≤ F ≤ 20kHz)	80	98		dB
Crosstalk	Channel Separation, R_L = 32Ω, A_v=-1 F = 1kHz F = 20Hz to 20kHz Channel Separation, R_L = 16Ω, A_v=-1 F = 1kHz F = 20Hz to 20kHz		 80 76 77 69		dB
C_I	Input Capacitance		1		pF
GBP	Gain Bandwidth Product (R_L = 32Ω)		1.1		MHz
SR	Slew Rate, Unity Gain Inverting (R_L = 16Ω)		0.4		V/µs

1. All electrical values are guaranted with correlation measurements at 2V and 5V.
2. Only for external gain version.
3. Guaranteed by design and evaluation.

ELECTRICAL CHARACTERISTICS

V_{CC} = **+2.5V**, GND = **0V**, T_{amb} = 25°C (unless otherwise specified)[1)]

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		1.7	2.5	mA
$I_{STANDBY}$	Standby Current No input signal, $V_{STANDBY}$=GND for TS486, R_L=32Ω No input signal, $V_{STANDBY}$=Vcc for TS487, R_L=32Ω		10	1000	nA
V_{IO}	Input Offset Voltage ($V_{ICM} = V_{CC}/2$)		1		mV
I_{IB}	Input Bias Current ($V_{ICM} = V_{CC}/2$) [2)]		90	200	nA
P_O	Output Power THD+N = 0.1% Max, F = 1kHz, R_L = 32Ω THD+N = 1% Max, F = 1kHz, R_L = 32Ω THD+N = 0.1% Max, F = 1kHz, R_L = 16Ω THD+N = 1% Max, F = 1kHz, R_L = 16Ω	 12.5 17.5	 13 14 21 22		mW
THD + N	Total Harmonic Distortion + Noise (A_V=-1) R_L = 32Ω, P_{out} = 10mW, 20Hz ≤ F ≤ 20kHz R_L = 16Ω, P_{out} = 16mW, 20Hz ≤ F ≤ 20kHz		 0.3 0.3		%
PSRR	Power Supply Rejection Ratio, inputs grounded [3)] (A_V=-1), RL>=16Ω, C_B=1µF, F = 1kHz, Vripple = 200mVpp	53	58		dB
I_O	Max Output Current THD +N ≤ 1%, R_L = 16Ω connected between out and $V_{CC}/2$	45	56		mA
V_O	Output Swing V_{OL} : R_L = 32Ω V_{OH} : R_L = 32Ω V_{OL} : R_L = 16Ω V_{OH} : R_L = 16Ω	 2.14 1.97	 0.25 2.25 0.35 2.15	 0.32 0.45	V
SNR	Signal-to-Noise Ratio (A weighted, A_V=-1) [3)] (R_L = 32Ω, THD +N < 0.4%, 20Hz ≤ F ≤ 20kHz)	80	95		dB
Crosstalk	Channel Separation, R_L = 32Ω, A_V=-1 F = 1kHz F = 20Hz to 20kHz Channel Separation, R_L = 16Ω, A_V=-1 F = 1kHz F = 20Hz to 20kHz		 80 76 77 69		dB
C_I	Input Capacitance		1		pF
GBP	Gain Bandwidth Product (R_L = 32Ω)		1.1		MHz
SR	Slew Rate, Unity Gain Inverting (R_L = 16Ω)		0.4		V/µs

1. All electrical values are guaranted with correlation measurements at 2V and 5V.
2. Only for external gain version.
3. Guaranteed by design and evaluation.

ELECTRICAL CHARACTERISTICS

V_{CC} = **+2V**, GND = **0V**, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		1.7	2.5	mA
$I_{STANDBY}$	Standby Current No input signal, $V_{STANDBY}$=GND for TS486, R_L=32Ω No input signal, $V_{STANDBY}$=Vcc for TS487, R_L=32Ω		10	1000	nA
V_{IO}	Input Offset Voltage (V_{ICM} = V_{CC}/2)		1		mV
I_{IB}	Input Bias Current (V_{ICM} = V_{CC}/2) [1)]		90	200	nA
P_O	Output Power THD+N = 0.1% Max, F = 1kHz, R_L = 32Ω THD+N = 1% Max, F = 1kHz, R_L = 32Ω THD+N = 0.3% Max, F = 1kHz, R_L = 16Ω THD+N = 1% Max, F = 1kHz, R_L = 16Ω	7 9.5	8 9 12 13		mW
THD + N	Total Harmonic Distortion + Noise (A_V=-1) R_L = 32Ω, P_{out} = 6.5mW, 20Hz ≤ F ≤ 20kHz R_L = 16Ω, P_{out} = 8mW, 20Hz ≤ F ≤ 20kHz		0.3 0.3		%
PSRR	Power Supply Rejection Ratio, inputs grounded [2)] (A_V=-1), RL>=16Ω, C_B=1µF, F = 1kHz, Vripple = 200mVpp	52	57		dB
I_O	Max Output Current THD +N ≤ 1%, R_L = 16Ω connected between out and V_{CC}/2	33	41		mA
V_O	Output Swing V_{OL} : R_L = 32Ω V_{OH} : R_L = 32Ω V_{OL} : R_L = 16Ω V_{OH} : R_L = 16Ω	 1.67 1.53	0.24 1.73 0.33 1.63	0.29 0.41	V
SNR	Signal-to-Noise Ratio (A weighted, A_V=-1) [2)] (R_L = 32Ω, THD +N < 0.4%, 20Hz ≤ F ≤ 20kHz)	80	93		dB
Crosstalk	Channel Separation, R_L = 32Ω, A_V=-1 F = 1kHz F = 20Hz to 20kHz Channel Separation, R_L = 16Ω, A_V=-1 F = 1kHz F = 20Hz to 20kHz		80 76 77 69		dB
C_I	Input Capacitance		1		pF
GBP	Gain Bandwidth Product (R_L = 32Ω)		1.1		MHz
SR	Slew Rate, Unity Gain Inverting (R_L = 16Ω)		0.4		V/µs

1. Only for external gain version.
2. Guaranteed by design and evaluation.

Index of Graphs

Fig. 1: Open Loop Gain and Phase vs Frequency

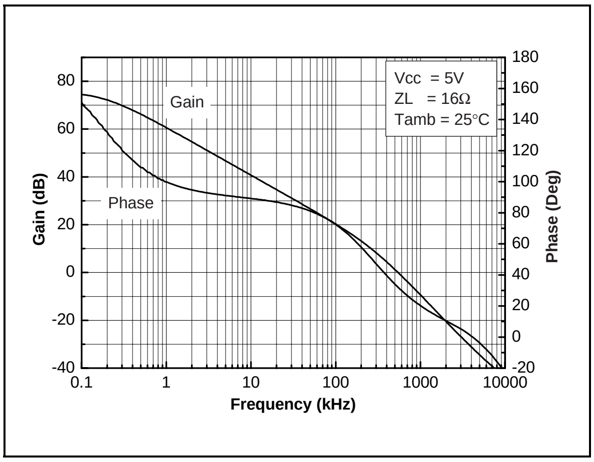


Fig. 2: Open Loop Gain and Phase vs Frequency

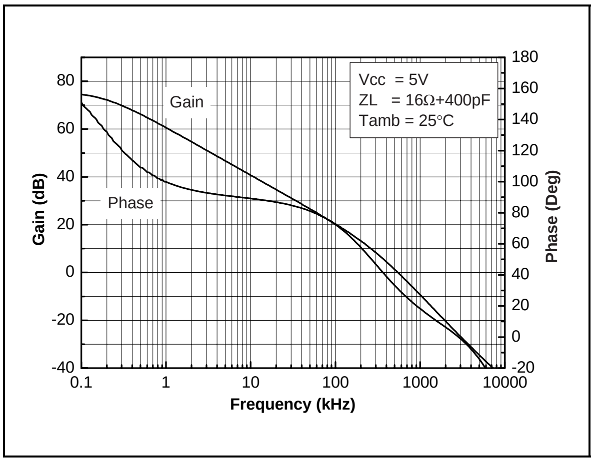


Fig. 3: Open Loop Gain and Phase vs Frequency

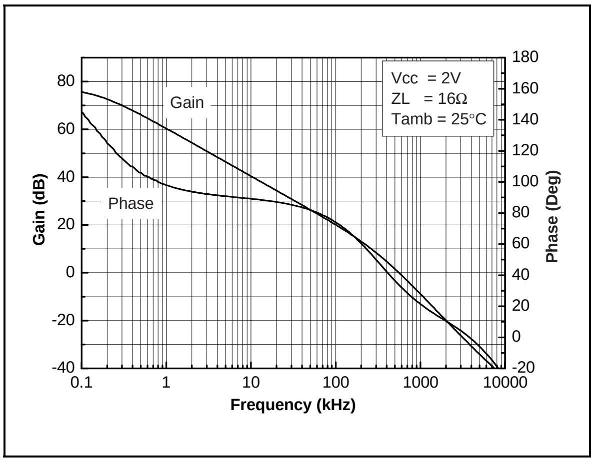


Fig. 4: Open Loop Gain and Phase vs Frequency

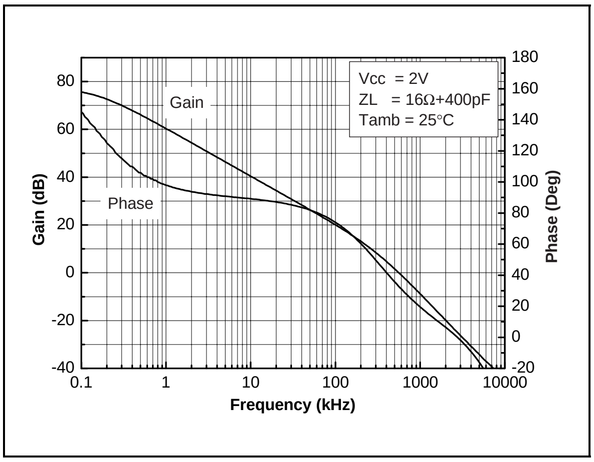


Fig. 5: Open Loop Gain and Phase vs Frequency

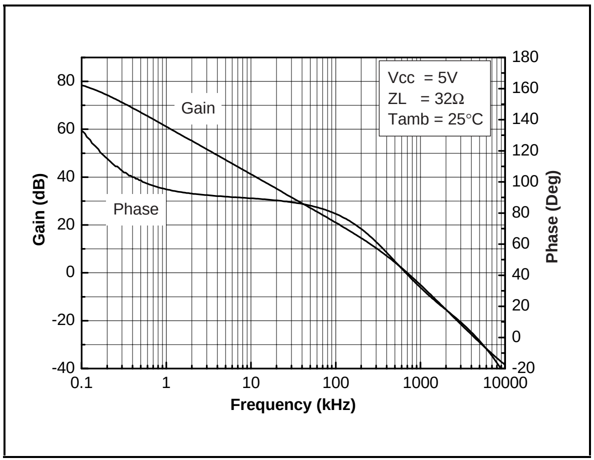


Fig. 6: Open Loop Gain and Phase vs Frequency

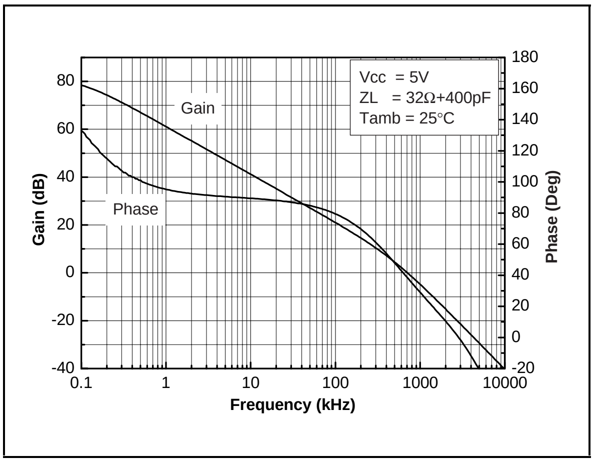


Fig. 7: Open Loop Gain and Phase vs Frequency

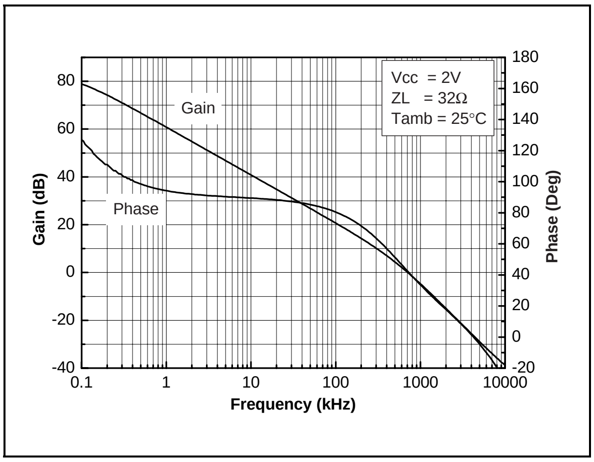


Fig. 8: Open Loop Gain and Phase vs Frequency

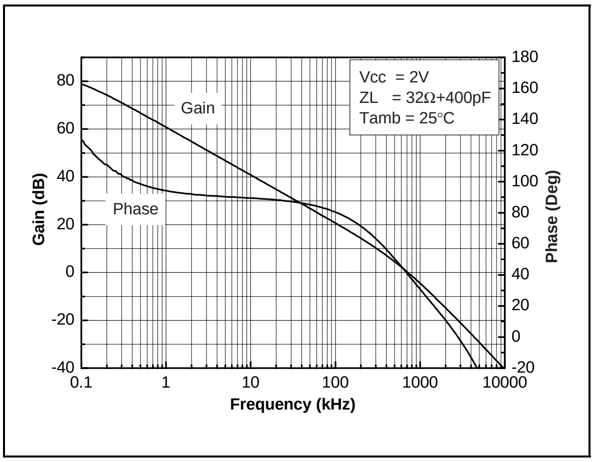


Fig. 9: Open Loop Gain and Phase vs Frequency

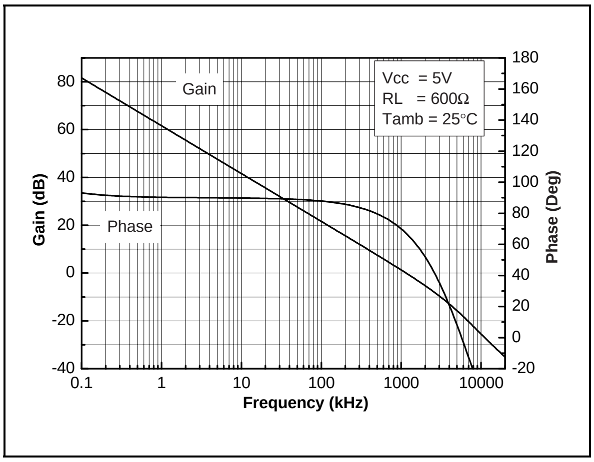


Fig. 10: Open Loop Gain and Phase vs Frequency

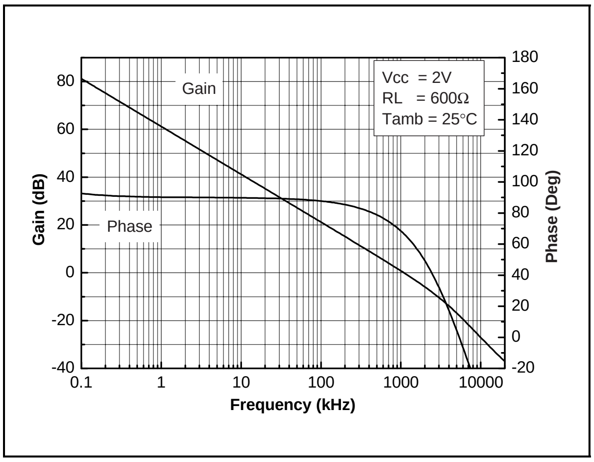


Fig. 11: Current Consumption vs Power Supply Voltage

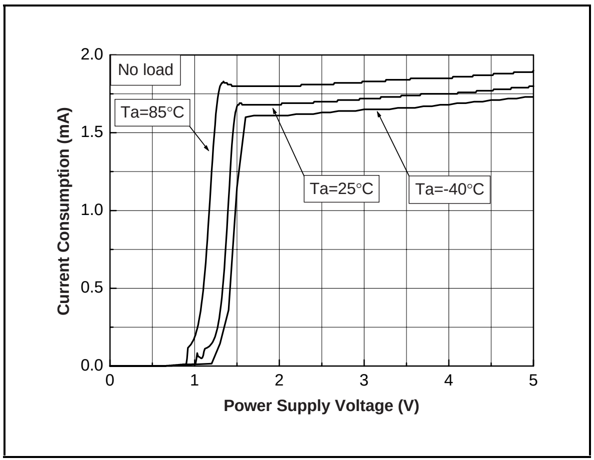


Fig. 12: Current Consumption vs Standby Voltage

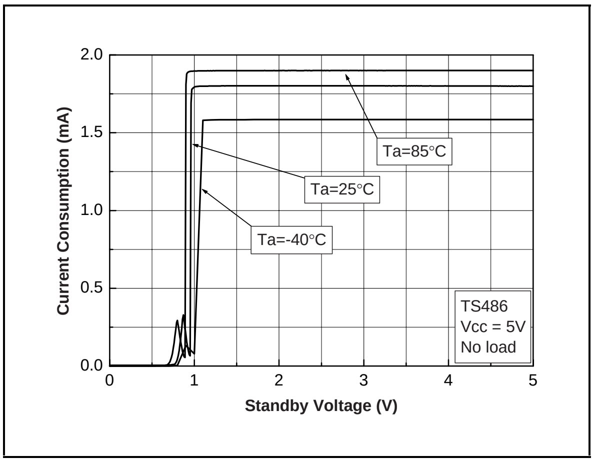


Fig. 13: Current Consumption vs Standby Voltage

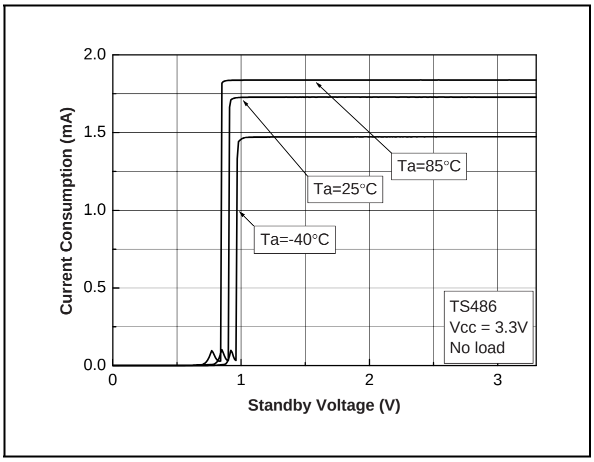


Fig. 14: Current Consumption vs Standby Voltage

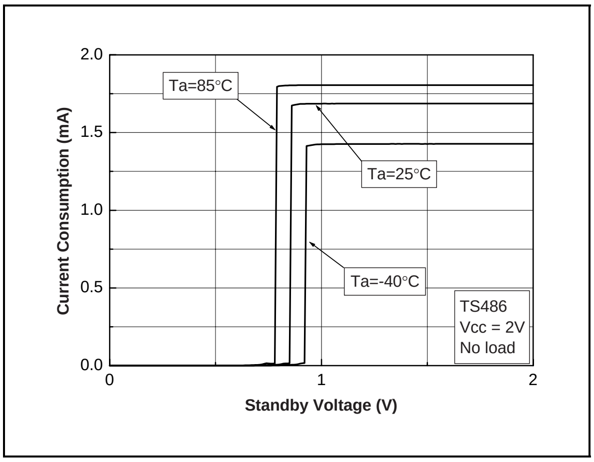


Fig. 15: Current Consumption vs Standby Voltage

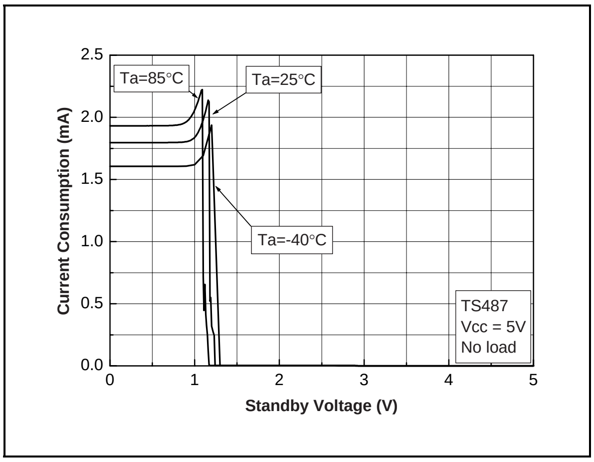


Fig. 16: Current Consumption vs Standby Voltage

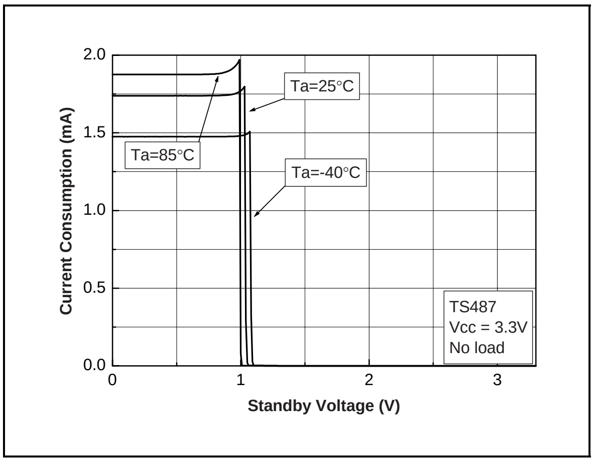


Fig. 17: Current Consumption vs Standby Voltage

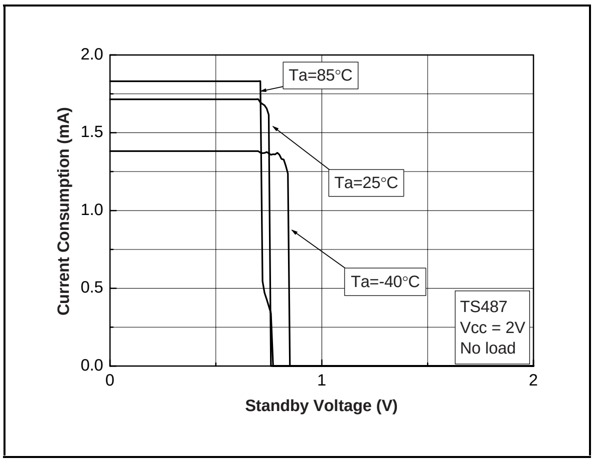


Fig. 18: Output Power vs Power Supply Voltage

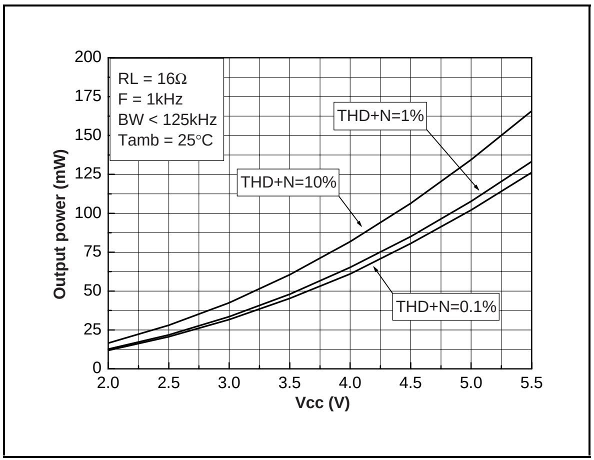


Fig. 19: Output Power vs Power Supply Voltage

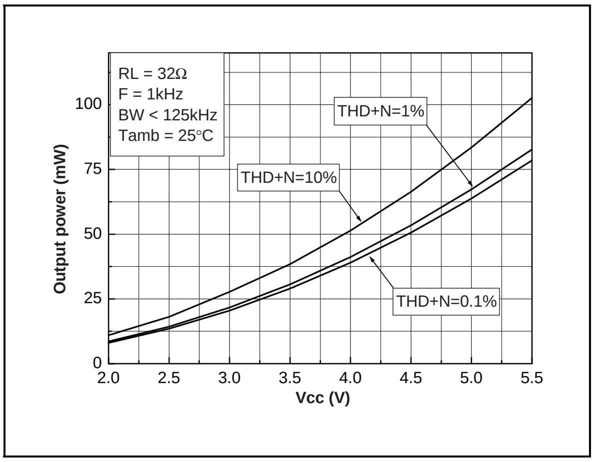


Fig. 20: Output Power vs Load Resistor

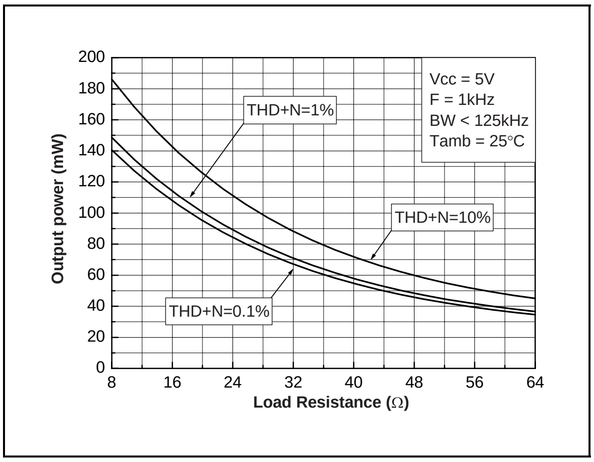


Fig. 21: Output Power vs Load Resistor

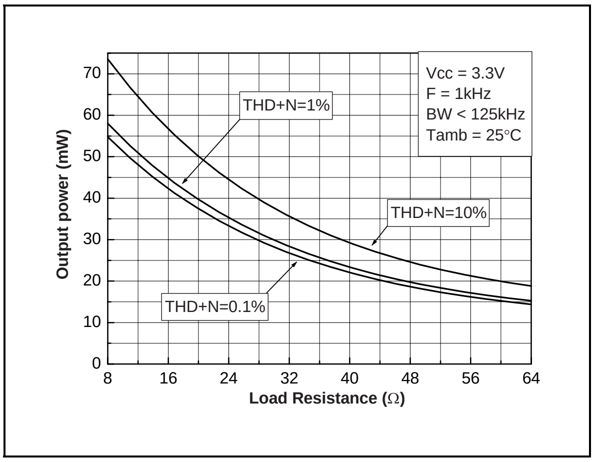


Fig. 22: Output Power vs Load Resistor

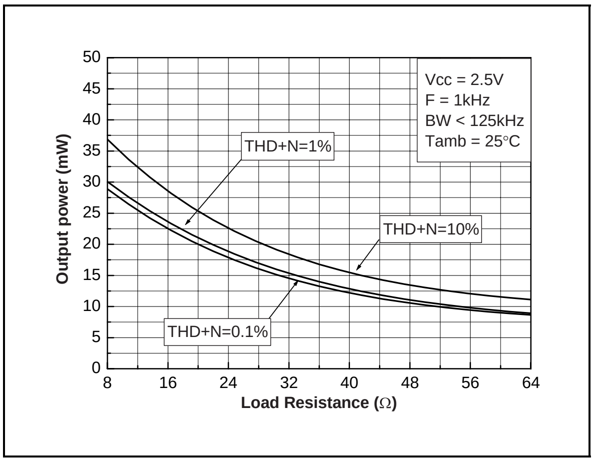


Fig. 23: Output Power vs Load Resistor

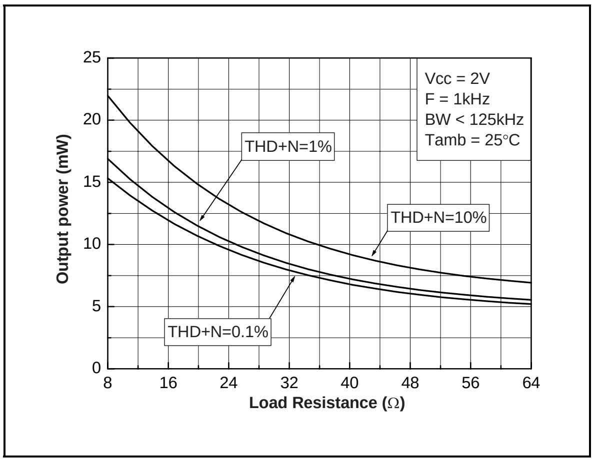


Fig. 24: Power Dissipation vs Output Power

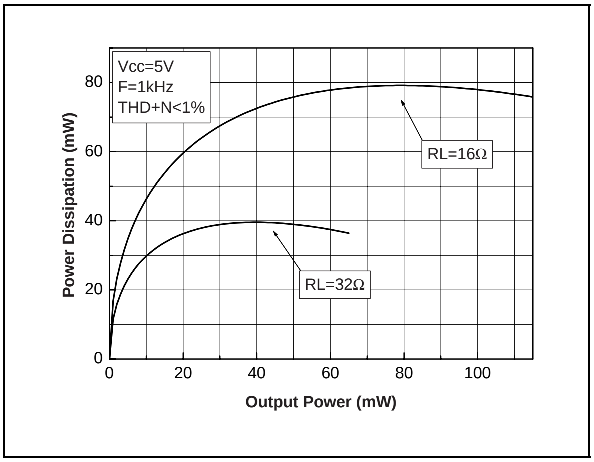


Fig. 25: Power Dissipation vs Output Power

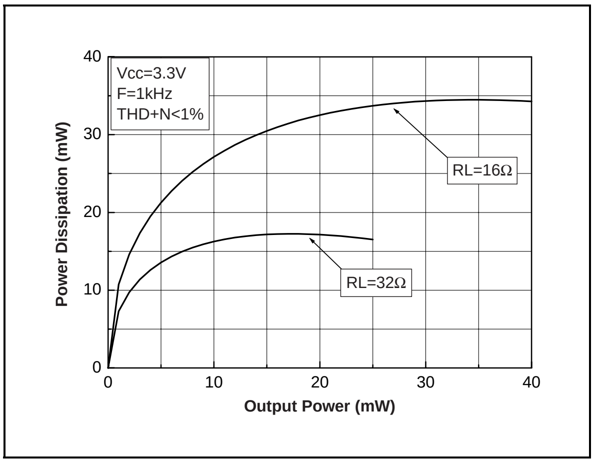


Fig. 26: Power Dissipation vs Output Power

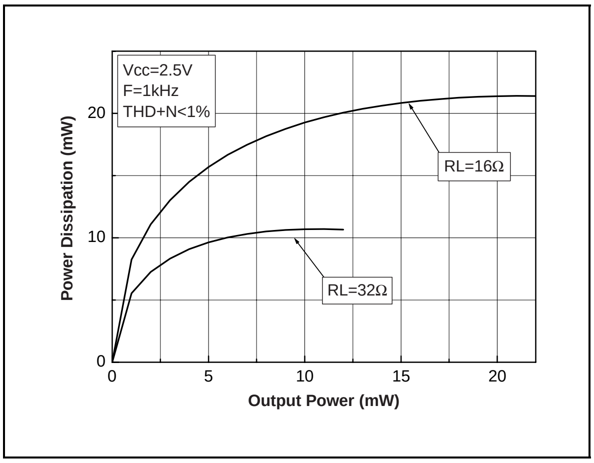


Fig. 27: Power Dissipation vs Output Power

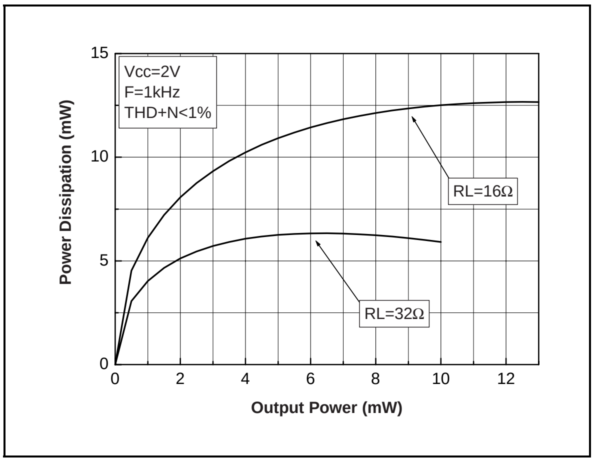


Fig. 28: Power Derating vs Ambiant Temperature

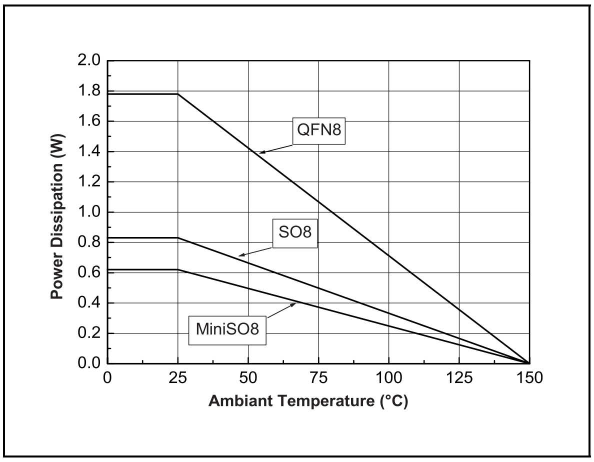


Fig. 29: Output Voltage Swing vs Power Supply Voltage

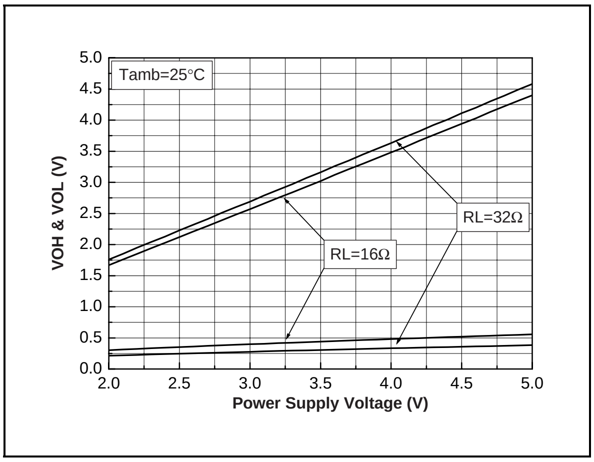


Fig. 30: Low Frequency Cut Off vs Input Capacitor for fixed gain versions.

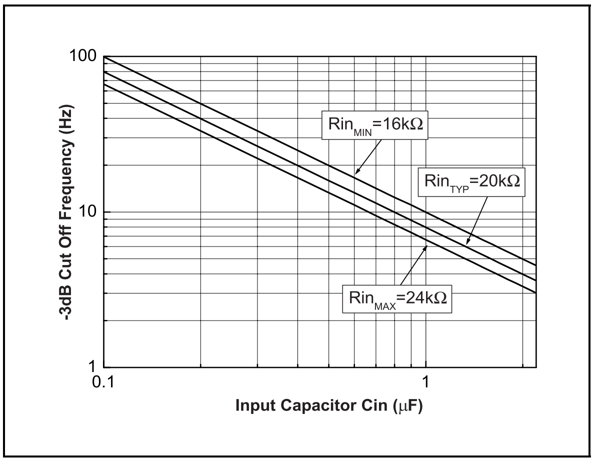


Fig. 31: THD + N vs Output Power

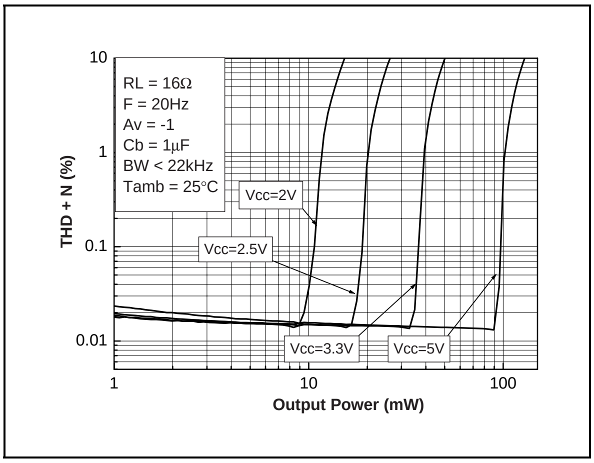


Fig. 32: THD + N vs Output Power

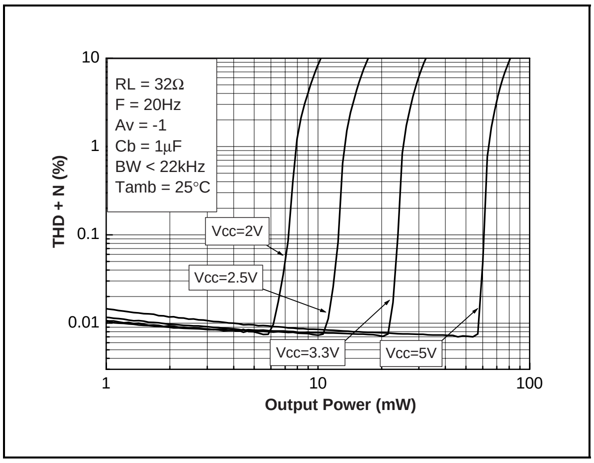


Fig. 33: THD + N vs Output Power

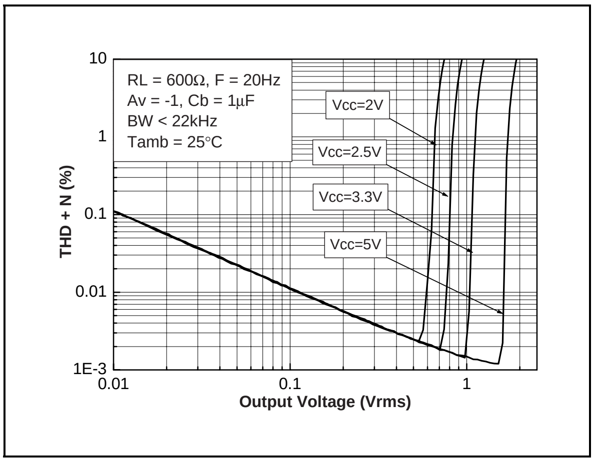


Fig. 34: THD + N vs Output Power

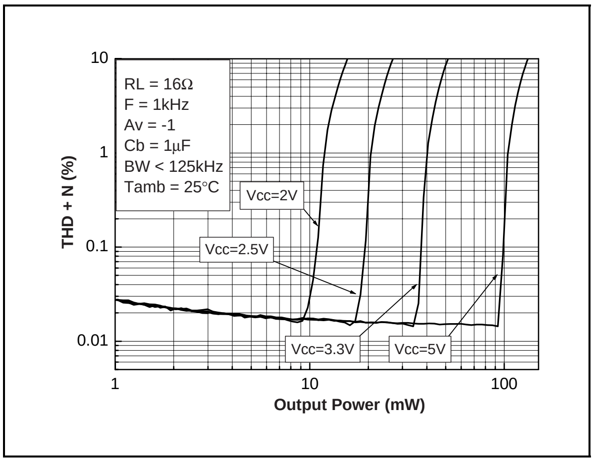


Fig. 35: THD + N vs Output Power

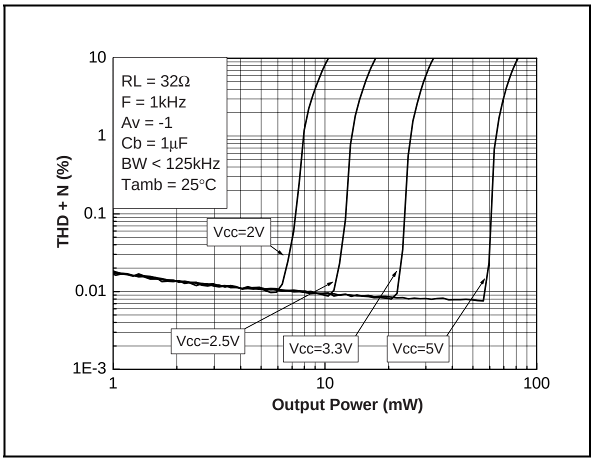


Fig. 36: THD + N vs Output Power

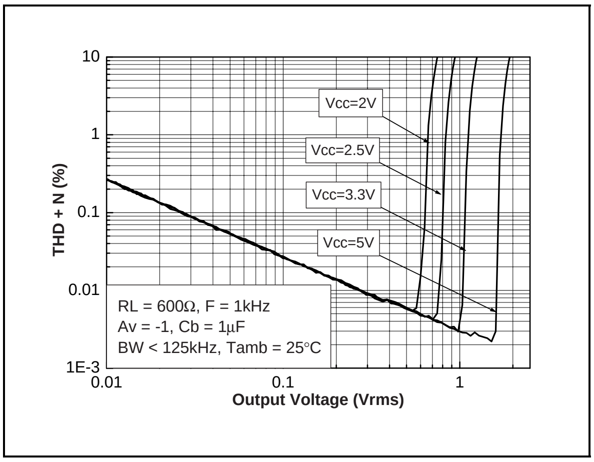


Fig. 37: THD + N vs Output Power

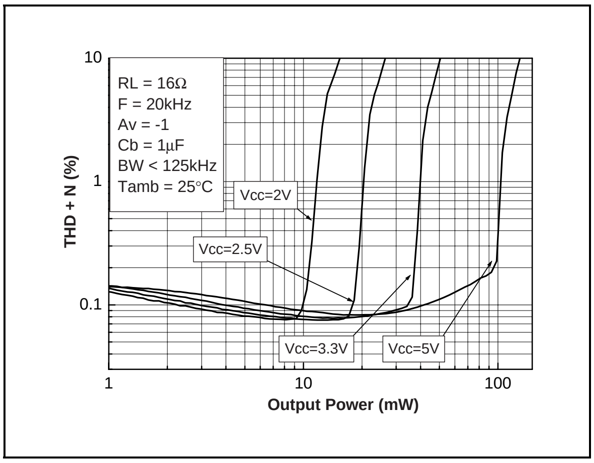


Fig. 38: THD + N vs Output Power

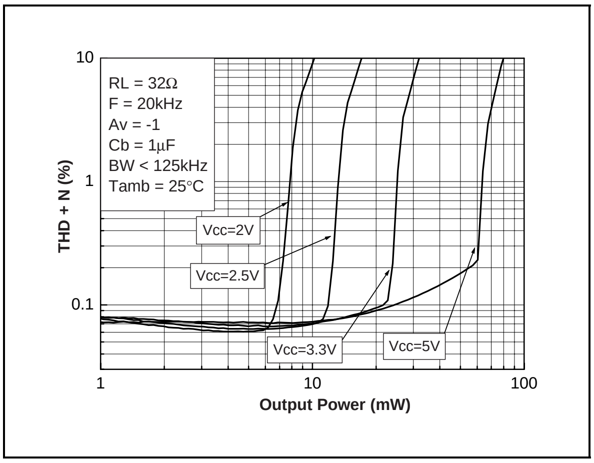


Fig. 39: THD + N vs Output Power

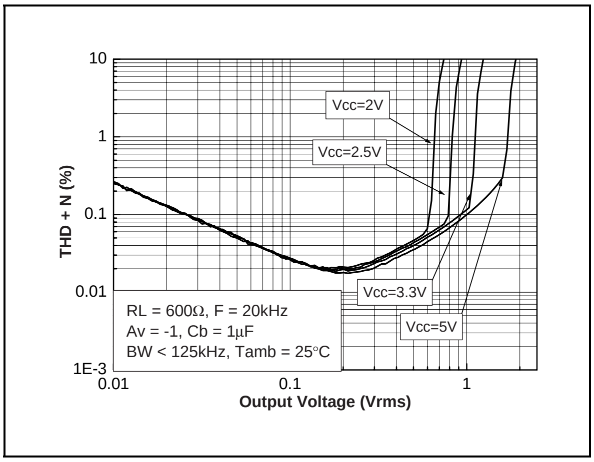


Fig. 40: THD + N vs Frequency

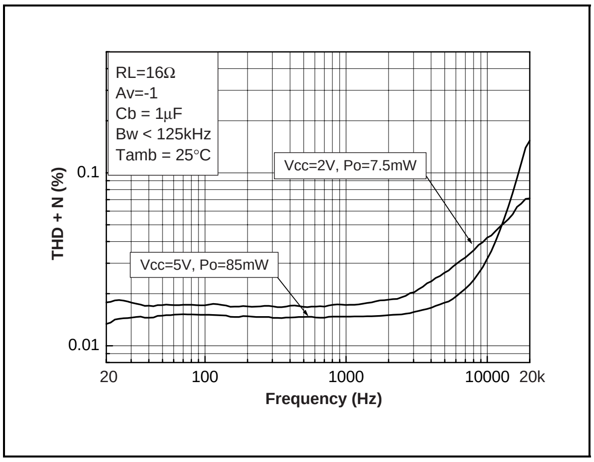


Fig. 41: THD + N vs Frequency

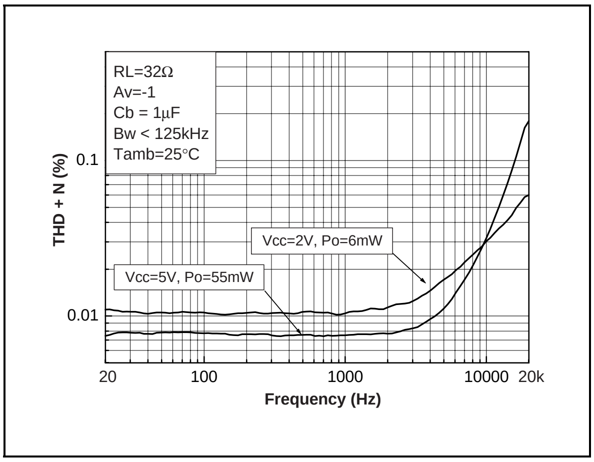


Fig. 42: THD + N vs Frequency

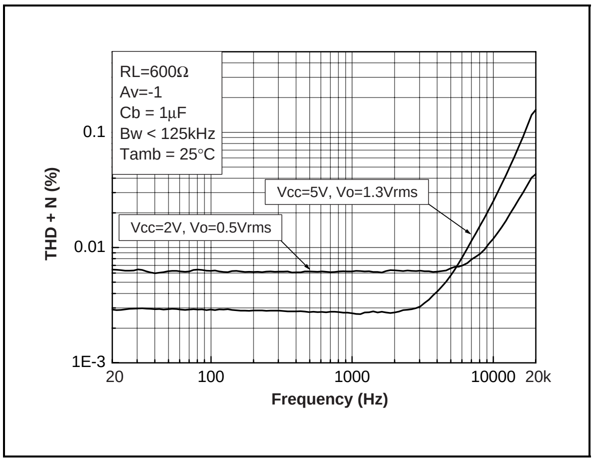


Fig. 43: Crosstalk vs Frequency

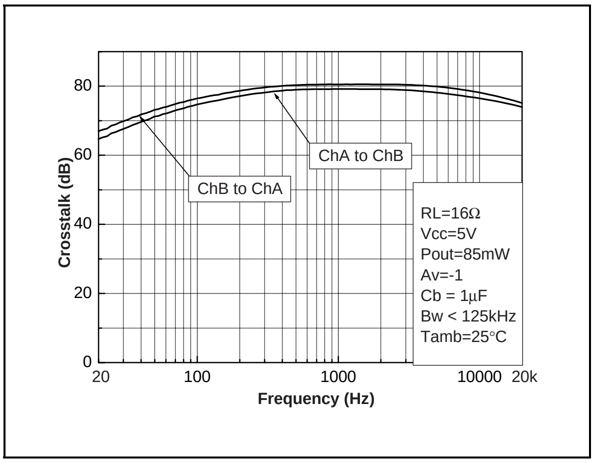


Fig. 44: Crosstalk vs Frequency

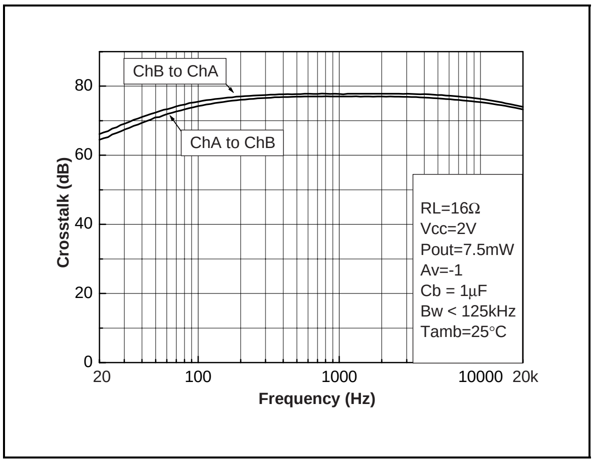


Fig. 45: Crosstalk vs Frequency

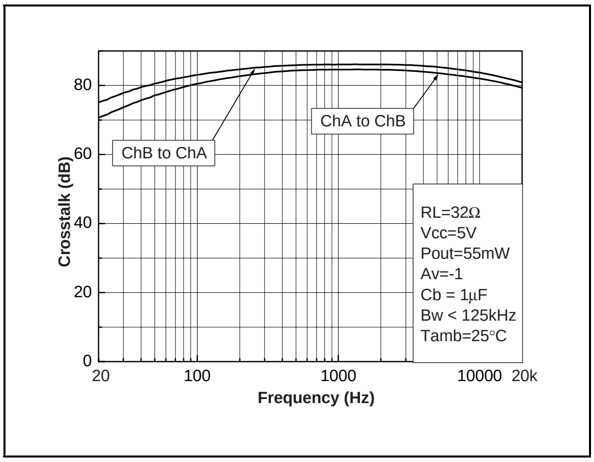


Fig. 46: Crosstalk vs Frequency

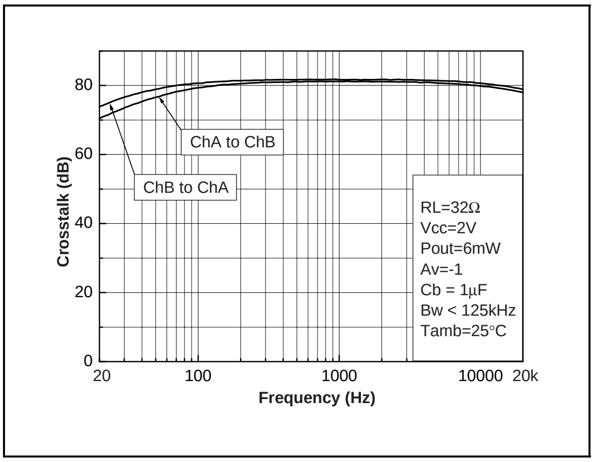


Fig. 47: Crosstalk vs Frequency

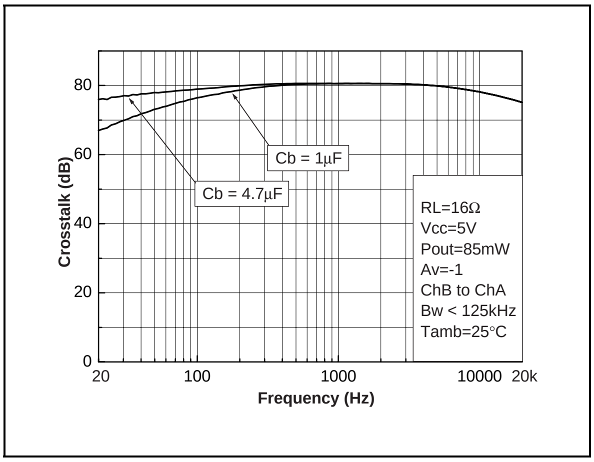


Fig. 48: Crosstalk vs Frequency

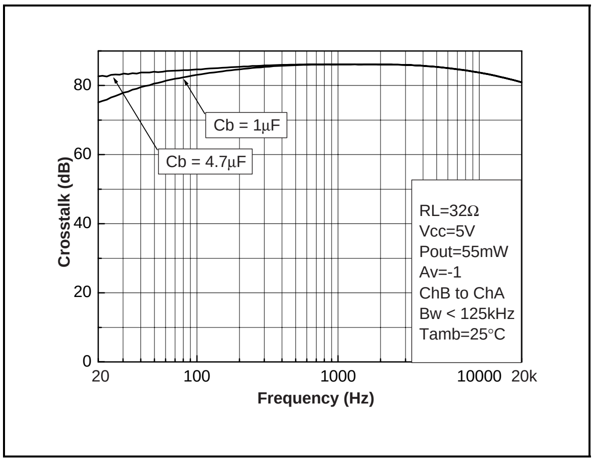


Fig. 49: Signal to Noise Ratio vs Power Supply Voltage with Unweighted Filter (20Hz to 20kHz)

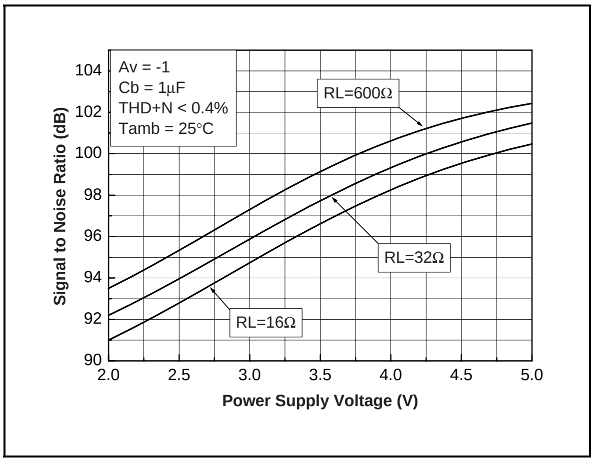


Fig. 50: Signal to Noise Ratio vs Power Supply Voltage with Weighted Filter Type A

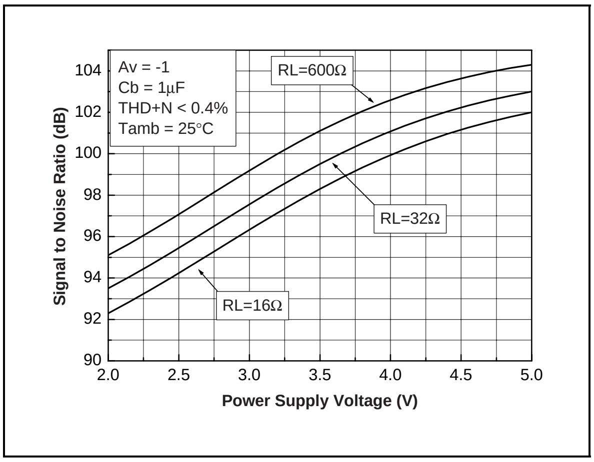


Fig. 51: PSRR vs Power Supply Voltage

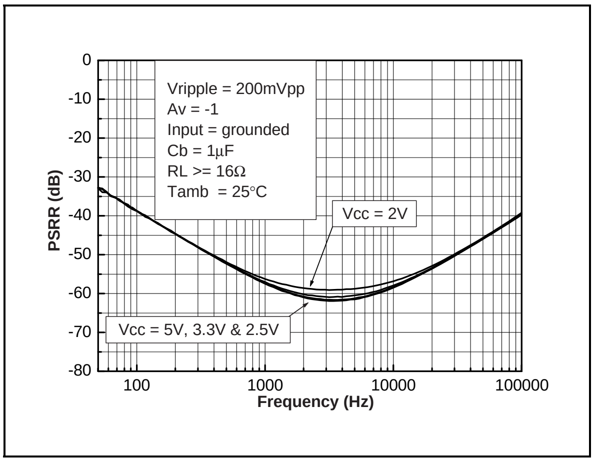


Fig. 52: PSRR vs Bypass Capacitor

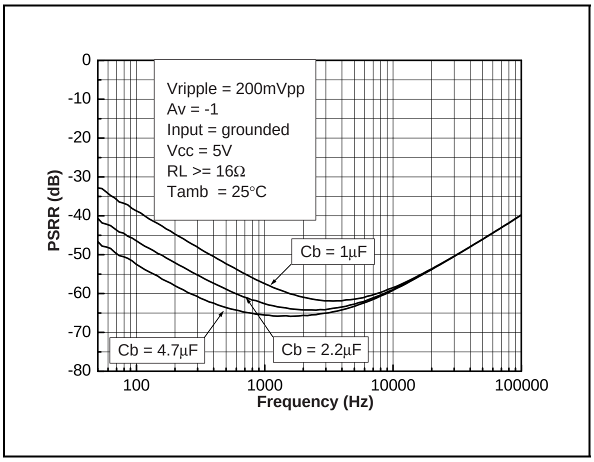


Fig. 53: PSRR vs Input Capacitor

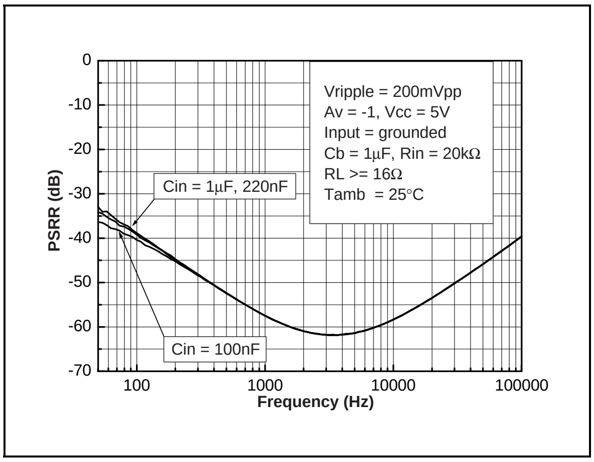


Fig. 54: PSRR vs Output Capacitor

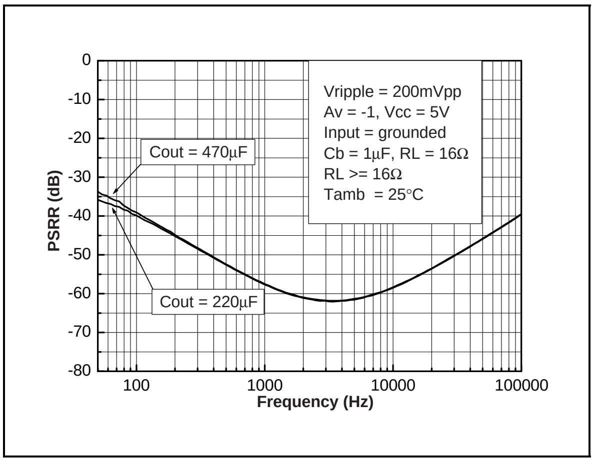


Fig. 55: PSRR vs Output Capacitor

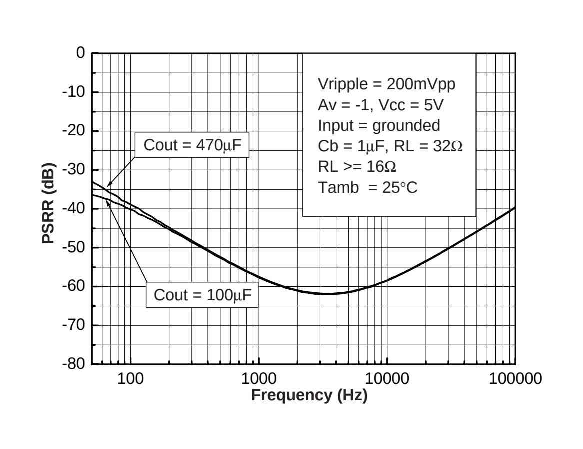


Fig. 56: PSRR vs Power Supply Voltage

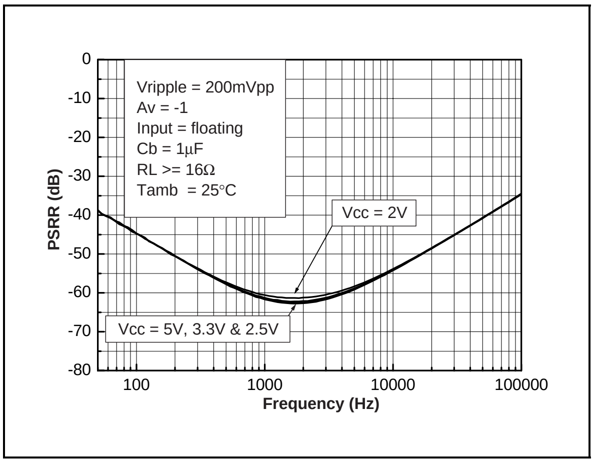


Fig. 57: THD + N vs Output Power

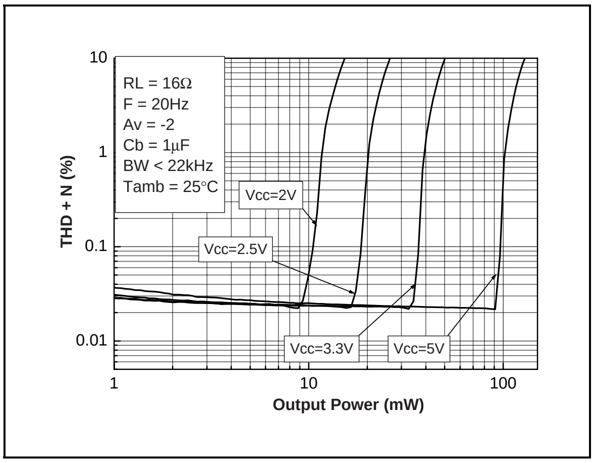


Fig. 58: THD + N vs Output Power

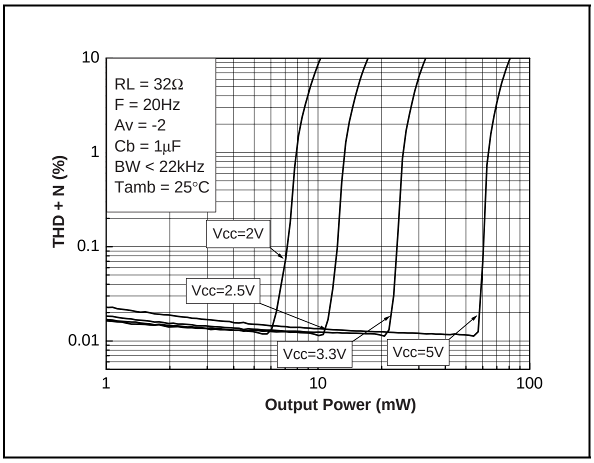


Fig. 59: THD + N vs Output Power

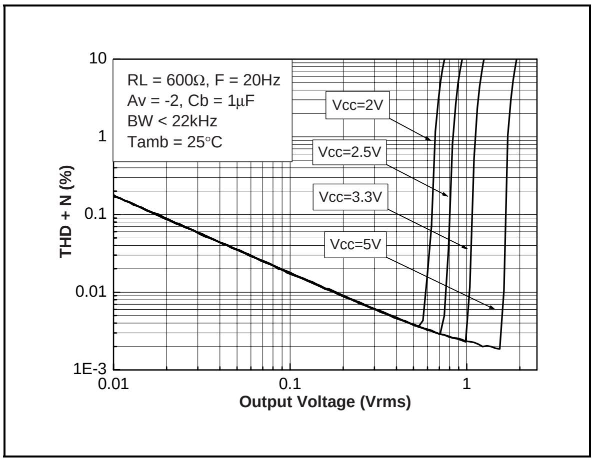


Fig. 60: THD + N vs Output Power

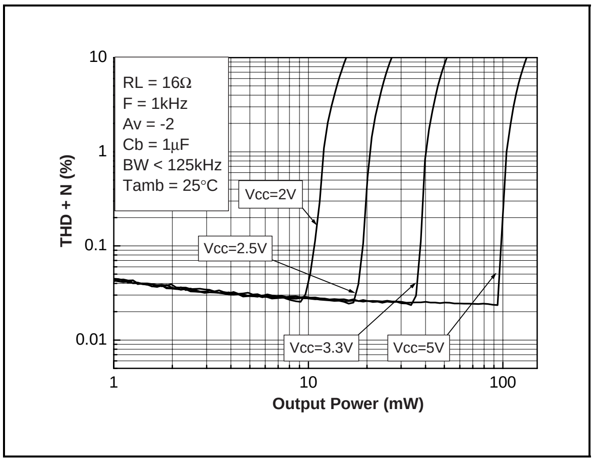


Fig. 61: THD + N vs Output Power

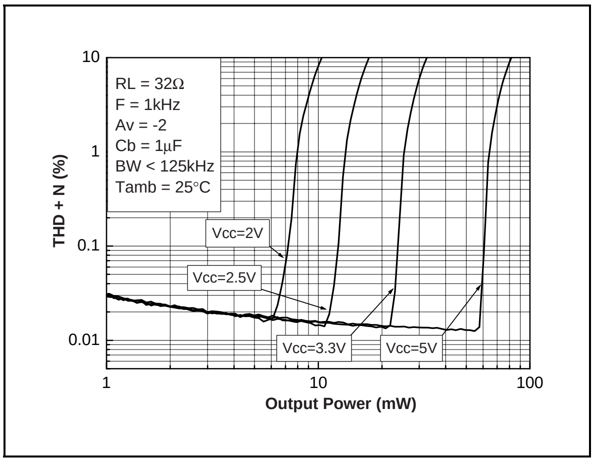


Fig. 62: THD + N vs Output Power

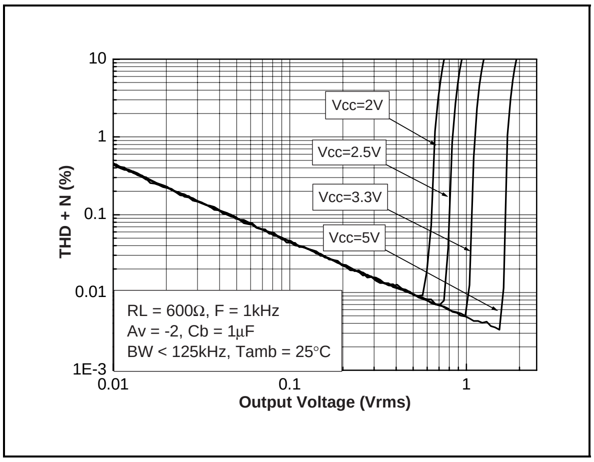


Fig. 63: THD + N vs Output Power

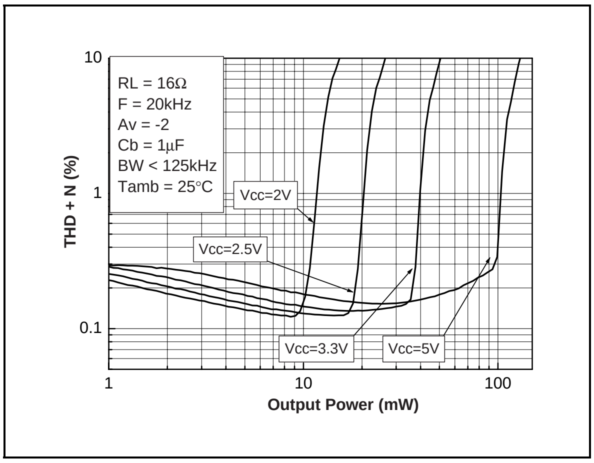


Fig. 64: THD + N vs Output Power

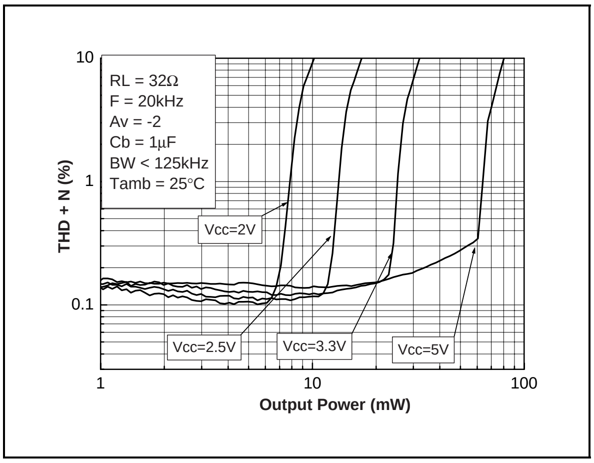


Fig. 65: THD + N vs Output Power

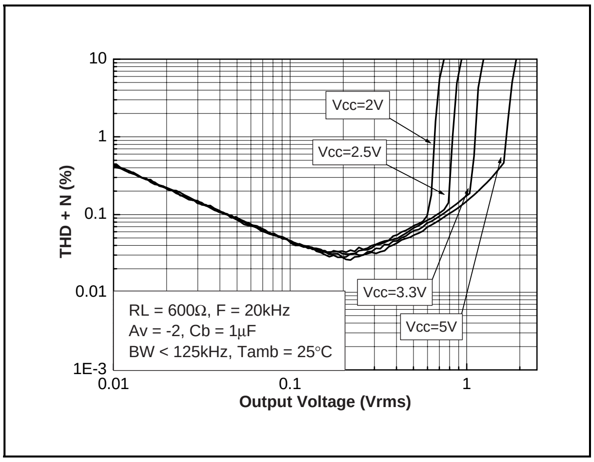


Fig. 66: THD + N vs Frequency

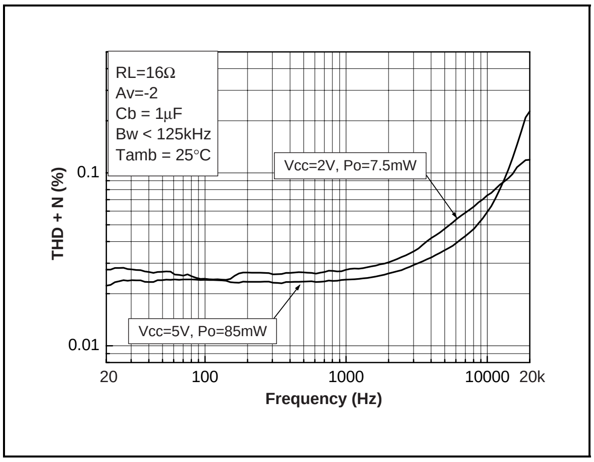


Fig. 67: THD + N vs Frequency

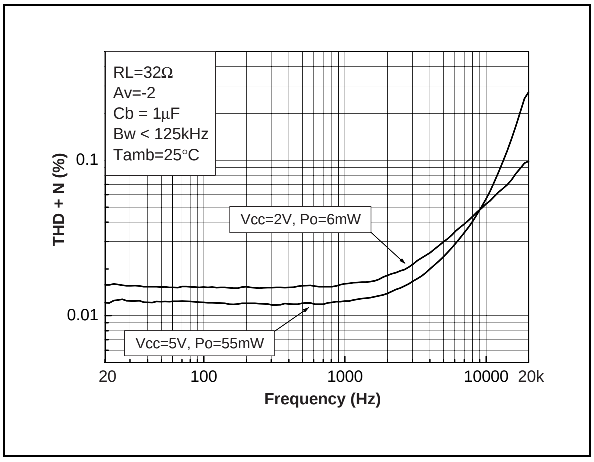


Fig. 68: THD + N vs Frequency

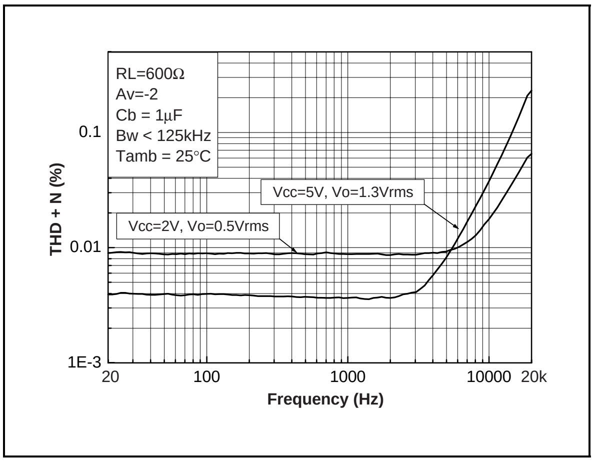


Fig. 69: Crosstalk vs Frequency

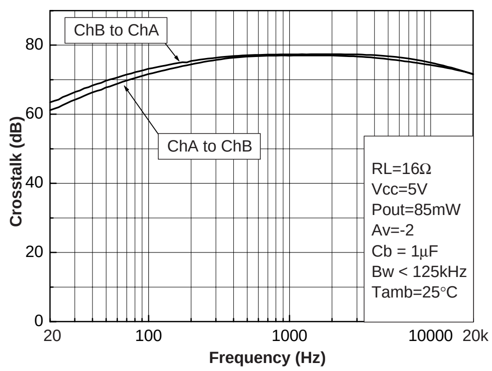


Fig. 70: Crosstalk vs Frequency

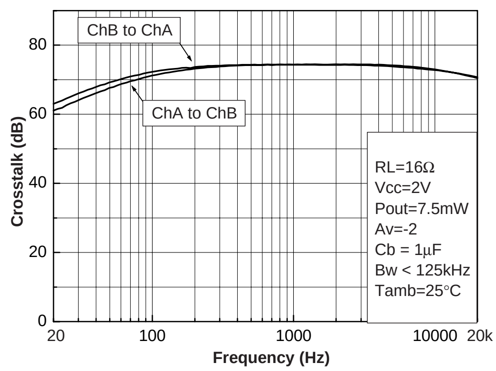


Fig. 71: Crosstalk vs Frequency

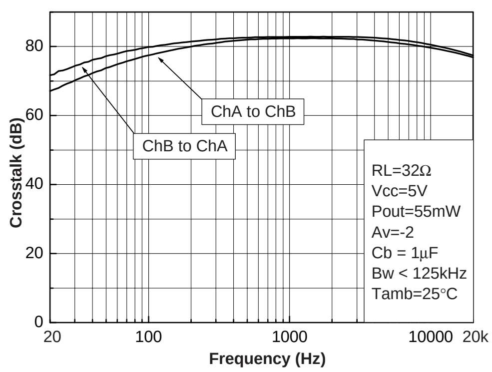


Fig. 72: Crosstalk vs Frequency

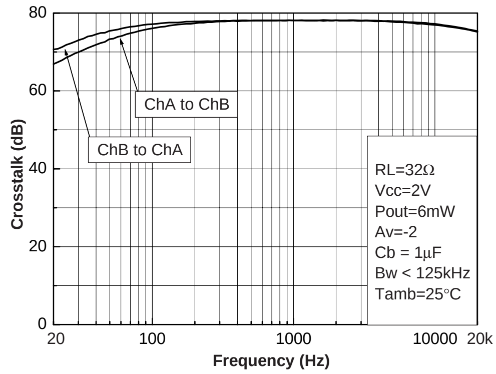


Fig. 73: Signal to Noise Ratio vs Power Supply Voltage with Unweighted Filter (20Hz to 20kHz)

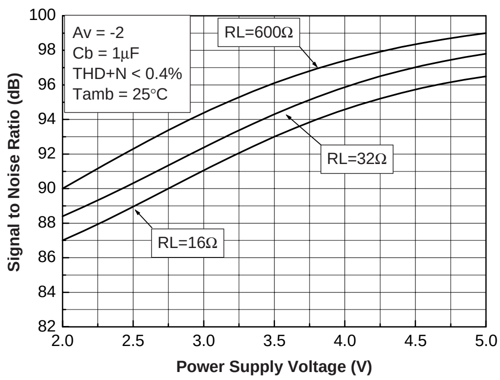


Fig. 74: Signal to Noise Ratio vs Power Supply Voltage with Weighted Filter Type A

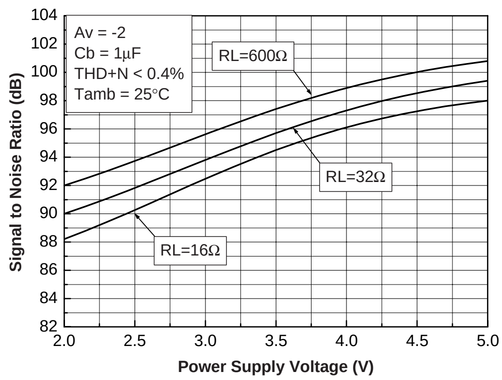


Fig. 75: PSRR vs Power Supply Voltage

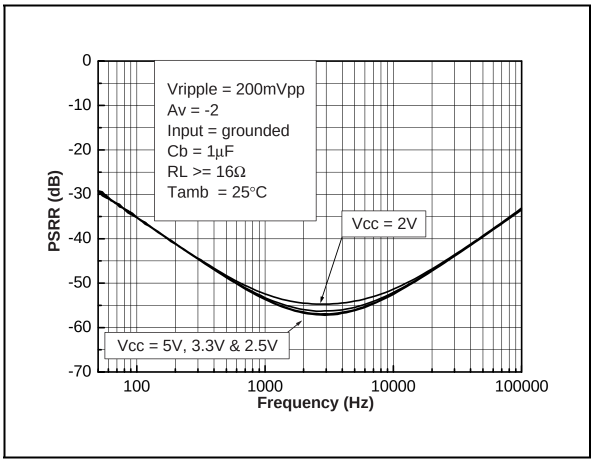


Fig. 76: PSRR vs Bypass Capacitor

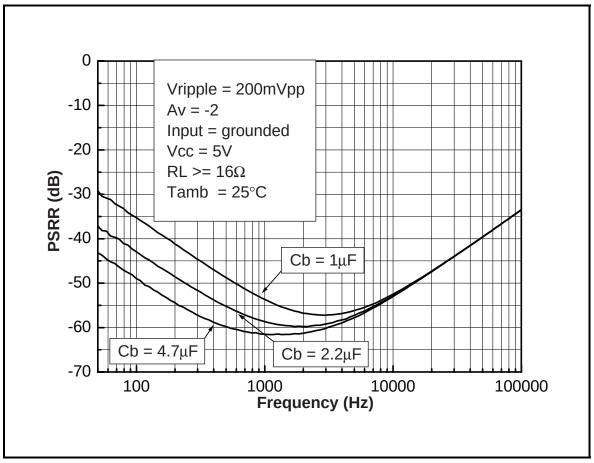


Fig. 77: PSRR vs Input Capacitor

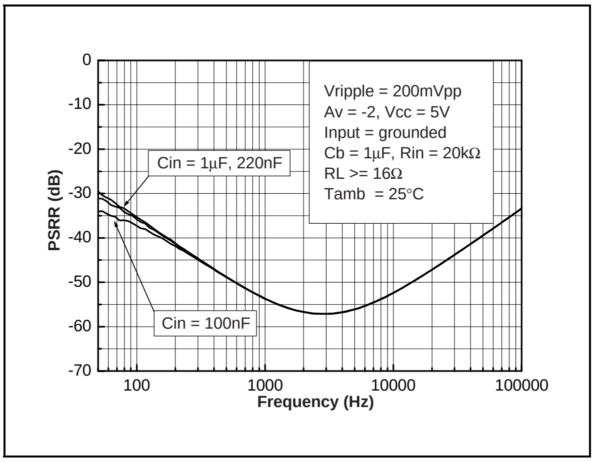


Fig. 78: PSRR vs Output Capacitor

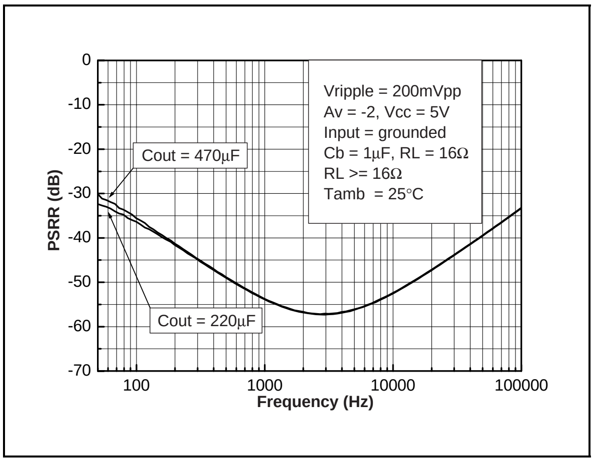


Fig. 79: PSRR vs Output Capacitor

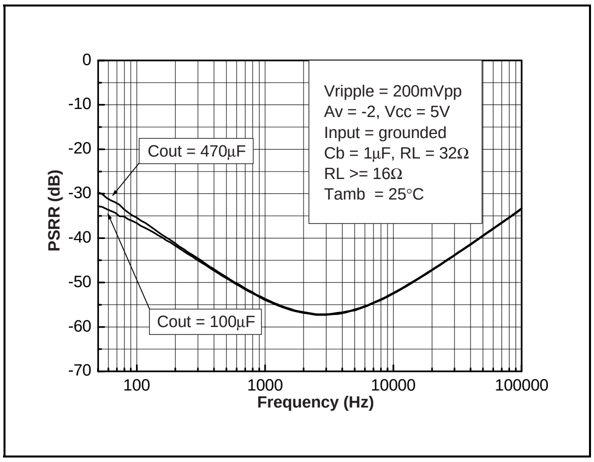


Fig. 80: THD + N vs Output Power

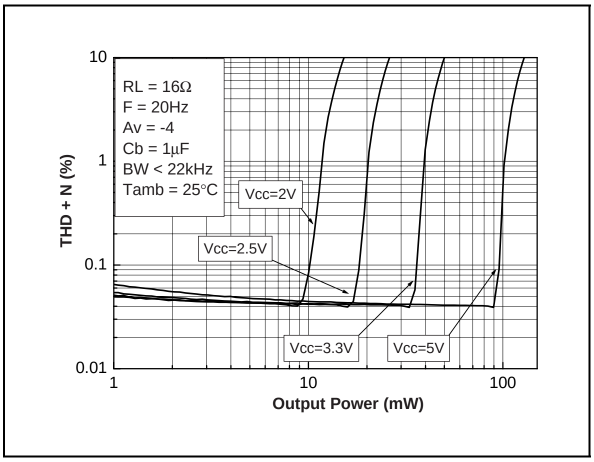


Fig. 81: THD + N vs Output Power

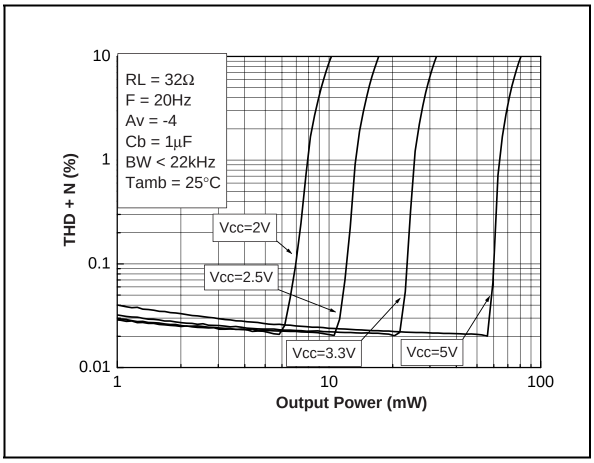


Fig. 82: THD + N vs Output Power

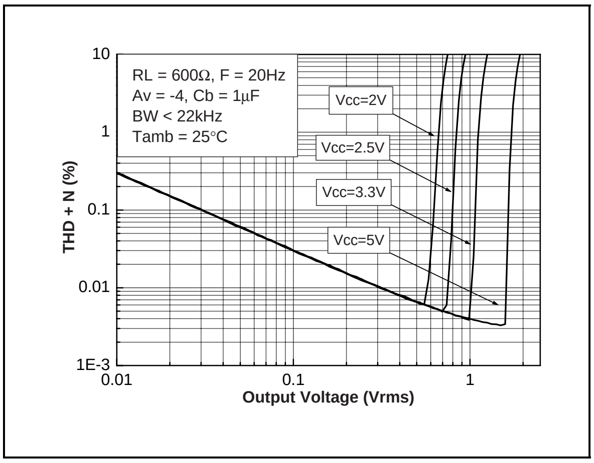


Fig. 83: THD + N vs Output Power

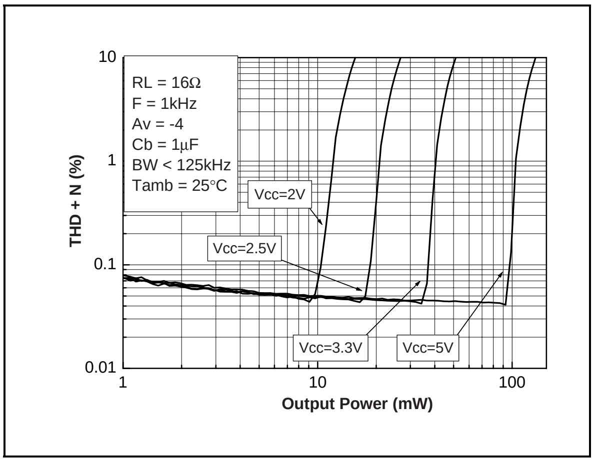


Fig. 84: THD + N vs Output Power

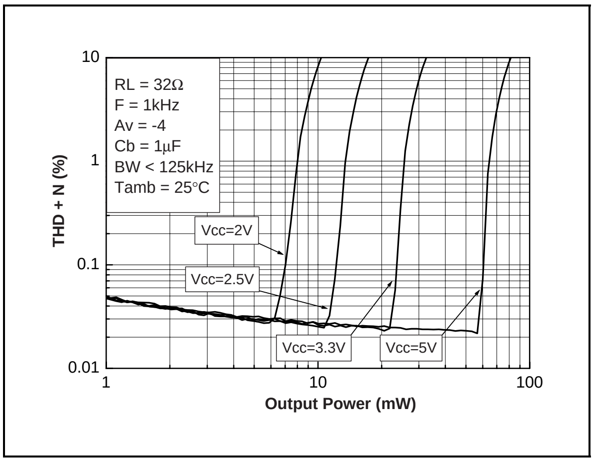


Fig. 85: THD + N vs Output Power

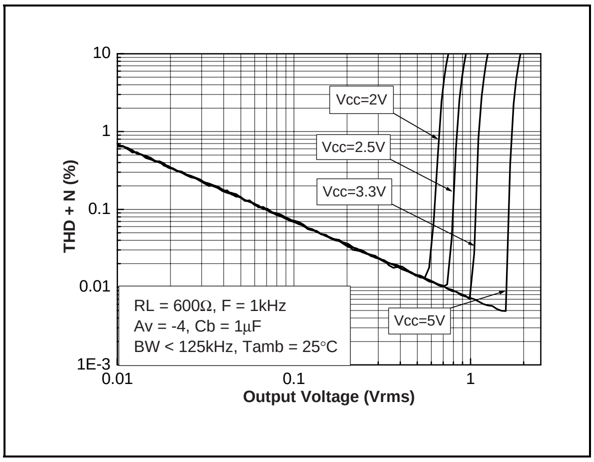


Fig. 86: THD + N vs Output Power

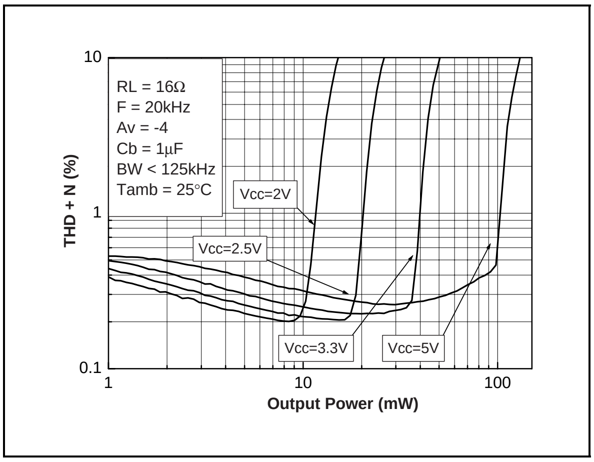


Fig. 87: THD + N vs Output Power

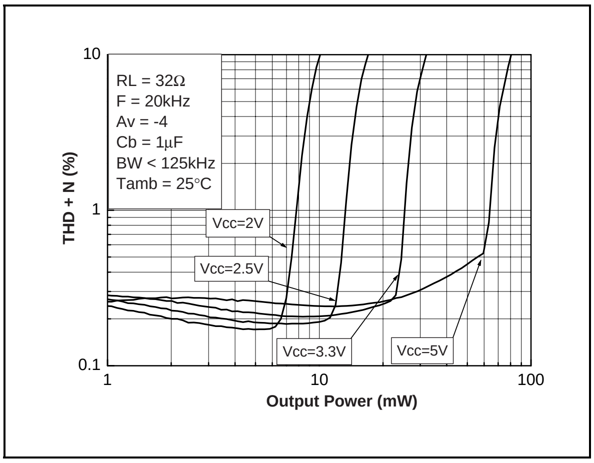


Fig. 88: THD + N vs Output Power

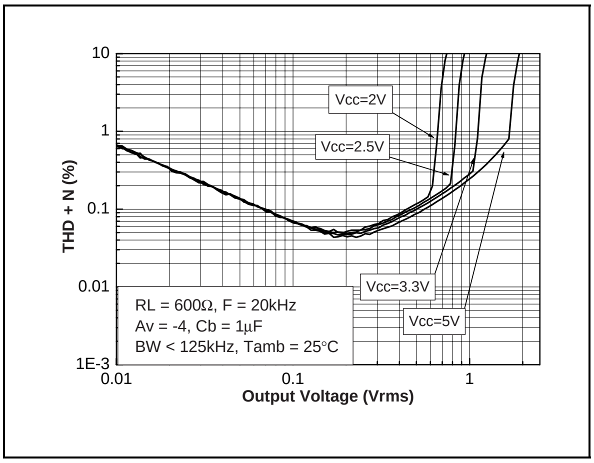


Fig. 89: THD + N vs Frequency

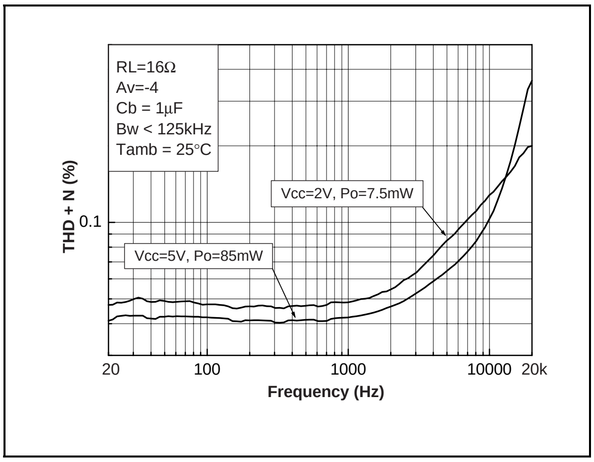


Fig. 90: THD + N vs Frequency

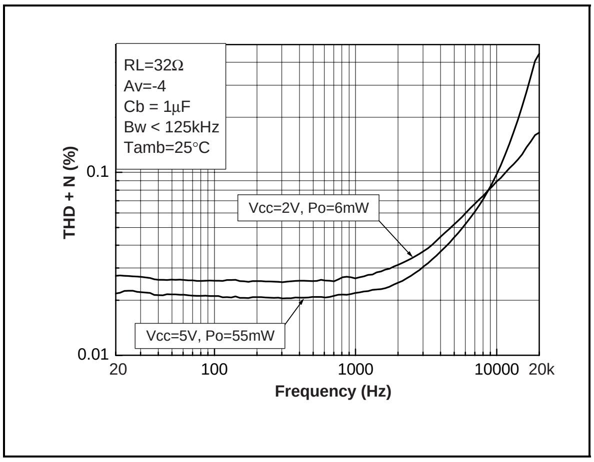


Fig. 91: THD + N vs Frequency

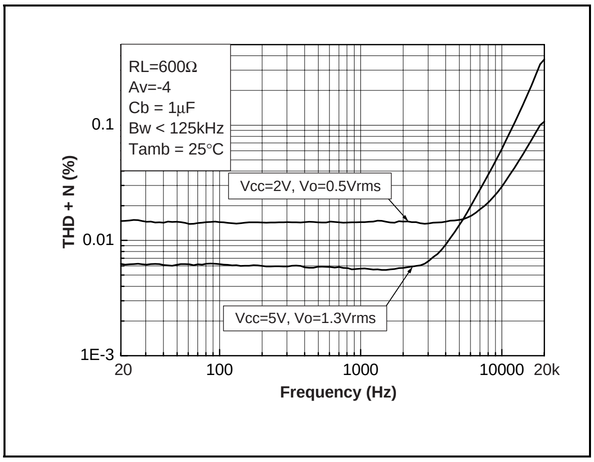


Fig. 92: Crosstalk vs Frequency

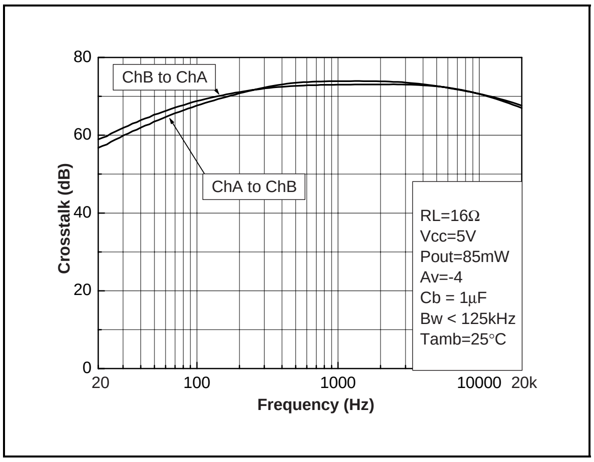


Fig. 93: Crosstalk vs Frequency

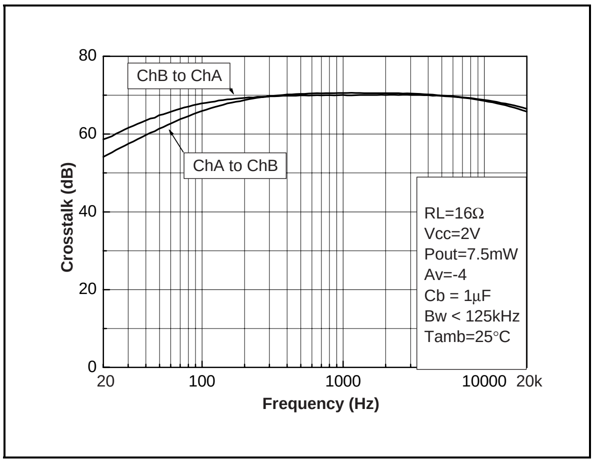


Fig. 94: Crosstalk vs Frequency

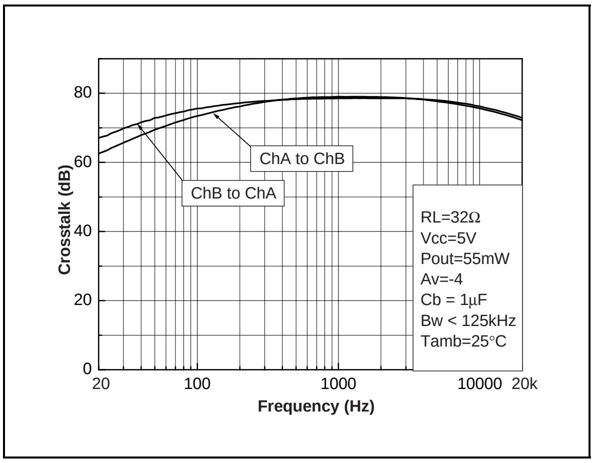


Fig. 95: Crosstalk vs Frequency

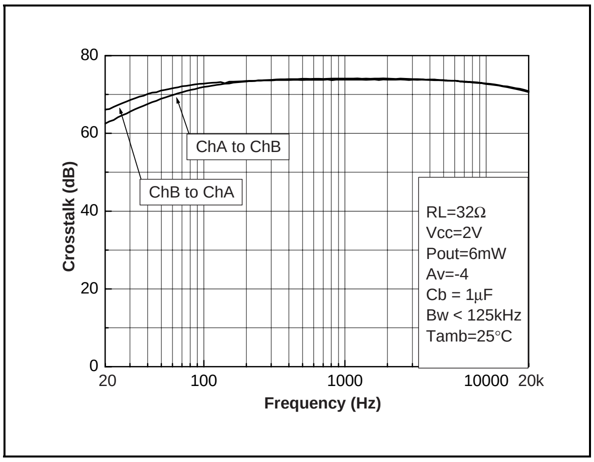


Fig. 96: Signal to Noise Ratio vs Power Supply Voltage with Unweighted Filter (20Hz to 20kHz)

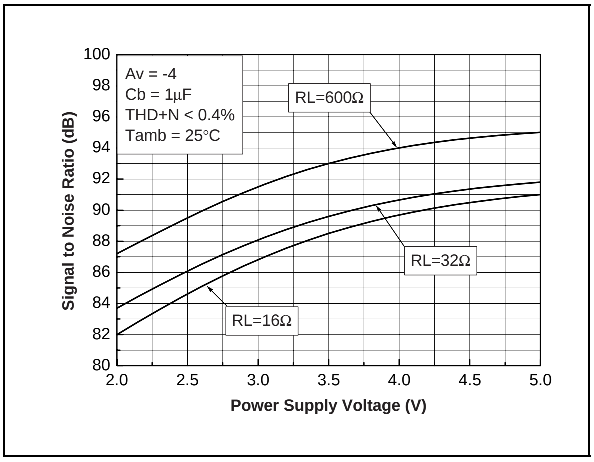


Fig. 97: Signal to Noise Ratio vs Power Supply Voltage with Weighted Filter Type A

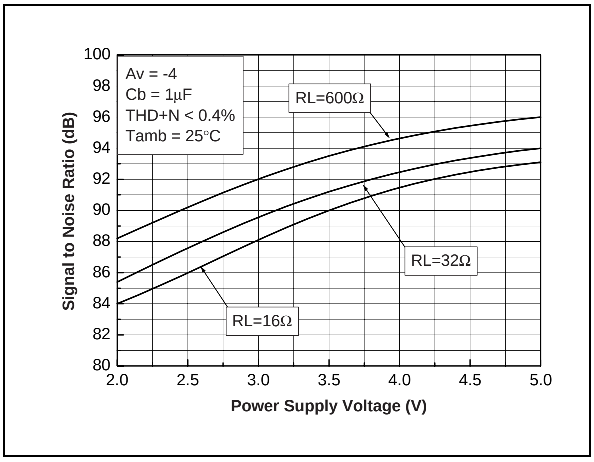


Fig. 98: PSRR vs Power Supply Voltage

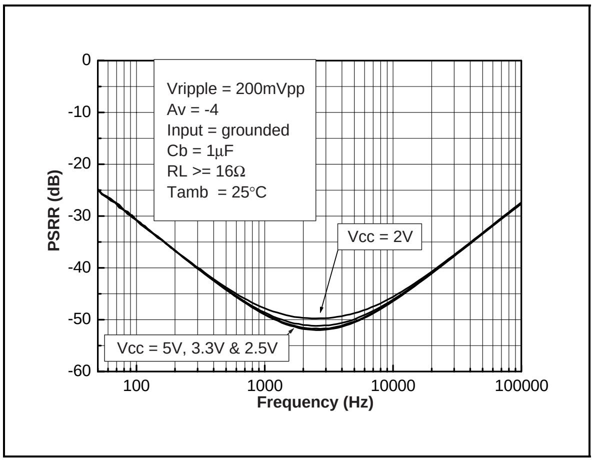


Fig. 99: PSRR vs Input Capacitor

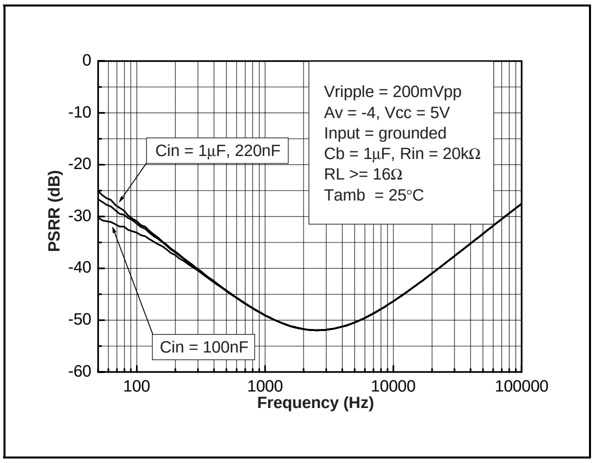


Fig. 100: PSRR vs Bypass Capacitor

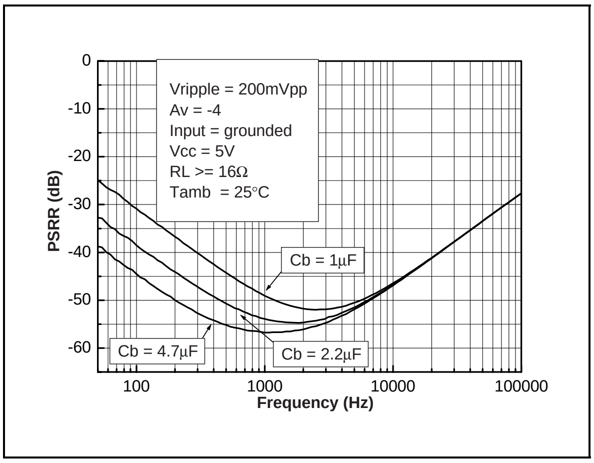


Fig. 101: PSRR vs Output Capacitor

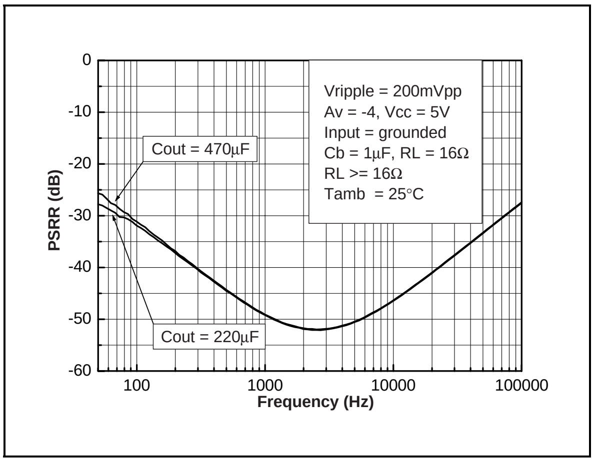
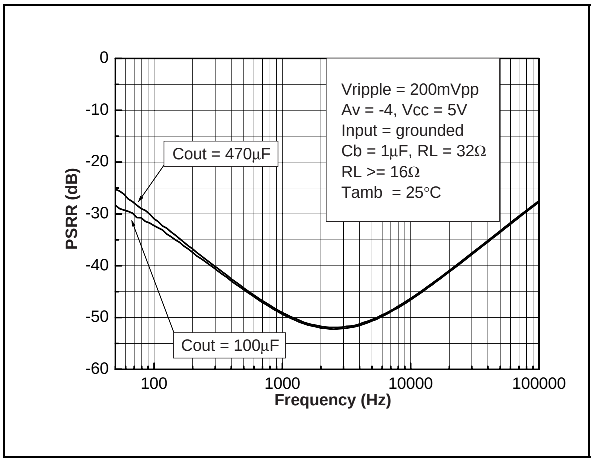
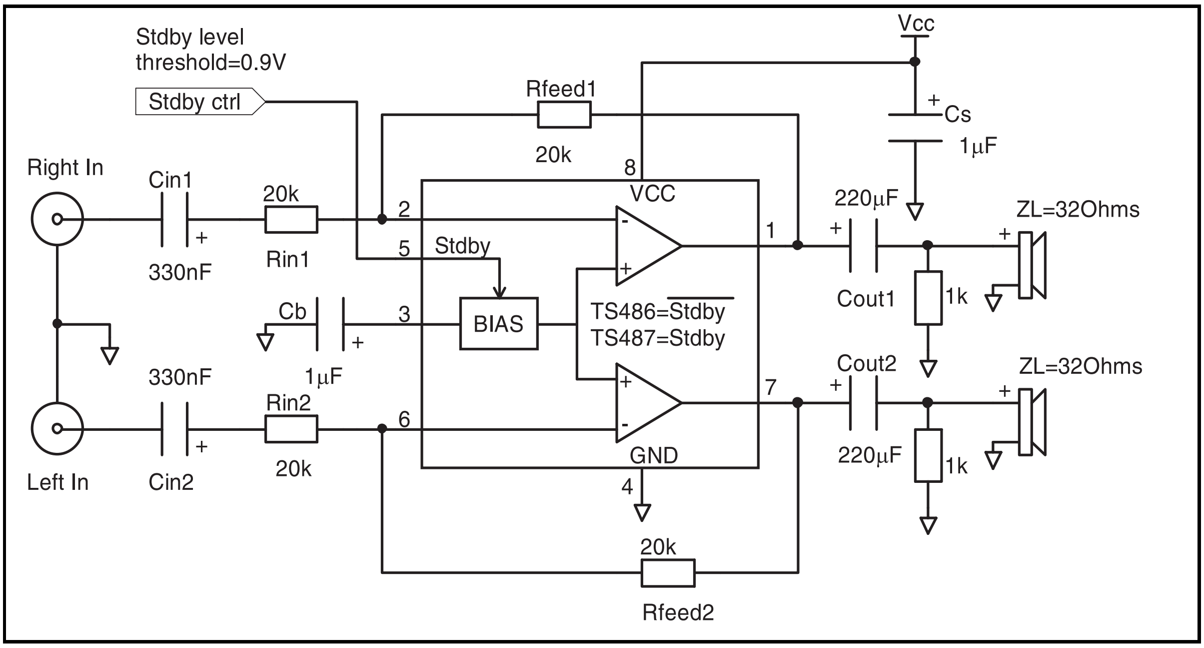


Fig. 102: PSRR vs Output Capacitor



APPLICATION NOTE:



TS486/487 GENERAL DESCRIPTION

TS486/487 is a family of dual audio amplifiers able to drive 16Ω or 32Ω headsets. Working in the 2V to 5.5V supply voltage range, they deliver 100mW at 5V and 12mW at 2V in a 16Ω load. An internal output current limitation, offers protection against short-circuits at the output over a limited time period.

Fixed gain versions of the TS486 and TS487 including the feedback resistor and the input resistors are also proposed to reduce the number of external parts.

The TS486 and TS487 exhibit a low quiescent current of typically 1.8mA, allowing usage in portable applications.

The standby mode is selected using the SHUTDOWN input. For TS486 (respectively TS487), the device is in sleep mode when PIN 5 is connected at GND (resp. V_{CC}).

GAIN SETTING

The gain of each inverter amplifier of the TS486 and TS487 is set by the resistors R_{IN} and R_{FEED}.

$Gain_{LINEAR} = -(R_{FEED}/R_{IN})$

$Gain_{dB} = 20\ Log(R_{FEED}/R_{IN})$

Fixed gain versions TS486-n and TS487-n including R_{IN} and R_{FEED} are proposed to reduce external parts.

LOW FREQUENCY ROLL-OFF WITH INPUT CAPACITORS

The low roll-off frequency of the headphone amplifiers depends on the input capacitors C_{IN1} and C_{IN2} and the input resistors R_{IN1} and R_{IN2}.

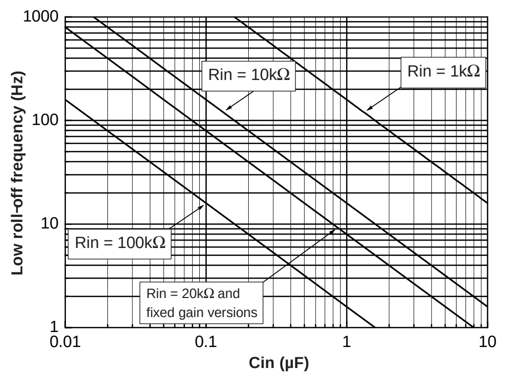
The C_{IN} capacitor in series with the input resistor R_{IN} of the amplifier is equivalent to a first order high pass filter.

Assuming that F_{min} is the lowest frequency to be amplified (with a 3dB attenuation), the minimum value of C_{IN} is:

$C_{IN} > 1 / (2*\pi*F_{min}*R_{IN})$

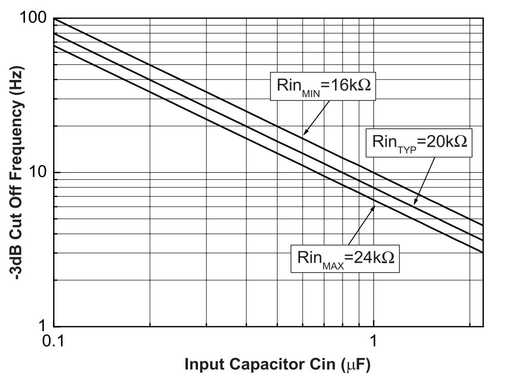
The following curve gives directly the low frequency roll-off versus the input capacitor C_{IN}

and for various values of the input resistor R_{IN} .



The input resistance of the fixed gain version is typically 20kΩ.

The following curve shows the limits of the roll off frequency depending on the min. and max. values of Rin:



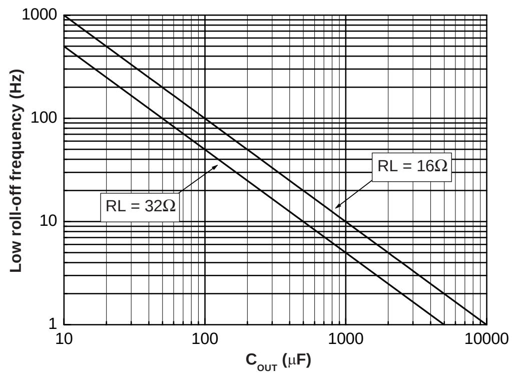
LOW FREQUENCY ROLL OFF WITH OUTPUT CAPACITORS

The DC voltage on the outputs of the TS486/487 is blocked by the output capacitors C_{OUT1} and C_{OUT2} . Each output capacitor C_{OUT} in series with the resistance of the load R_L is equivalent to a first order high pass filter.

Assuming that F_{min} is the lowest frequency to be amplified (with a 3dB attenuation), the minimum value of C_{OUT} is:

$$C_{OUT} > 1 / (2*\pi*F_{min}*R_L)$$

The following curve gives directly the low roll-off frequency versus the output capacitor C_{OUT} in µF and for the two typical 16Ω and 32Ω impedances:



DECOUPLING CAPACITOR C_B

The internal bias voltage at Vcc/2 is decoupled with the external capacitor C_B.

The TS486 and TS487 have a specified Power Supply Rejection Ratio parameter with C_B = 1µF. A higher value of C_B improves the PSRR, for example, a 4.7µF improves the PSRR by 15dB at 200Hz (please, refer to fig. 76 "PSRR vs Bypass Capacitor").

POP PRECAUTIONS

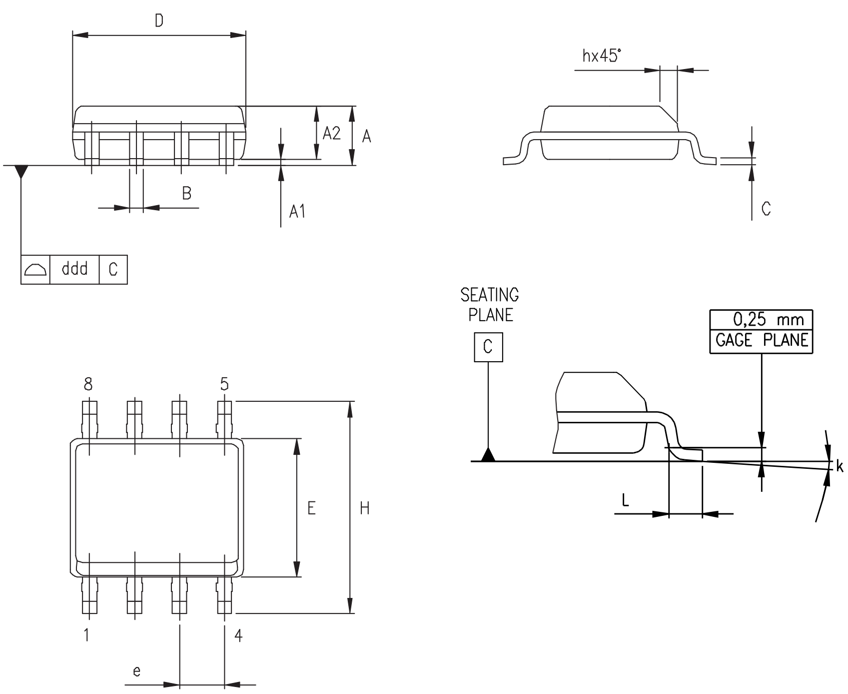
Generally headphones are connected using a connector as a jack. To prevent a pop in the headphones when plugged in the jack, a resistor should be connected in parallel with each headphone output. This allows the capacitors Cout to be charged even when no headphone is plugged.

A resistor of 1 kΩ is high enough to be a negligible load, and low enough to charge the capacitors Cout in less than one second.

PACKAGE MECHANICAL DATA

SO-8 MECHANICAL DATA

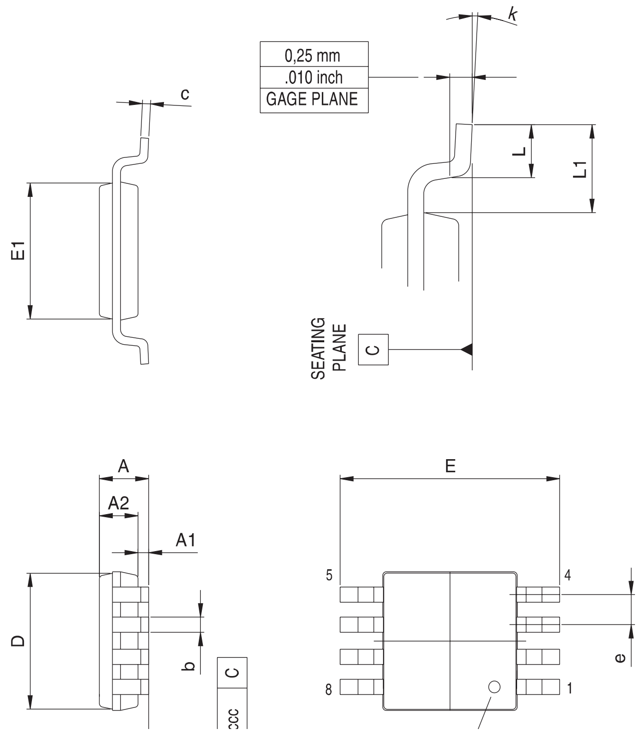
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.04		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	4.80		5.00	0.189		0.197
E	3.80		4.00	0.150		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	8° (max.)					
ddd			0.1			0.04



0016023/C

PACKAGE MECHANICAL DATA

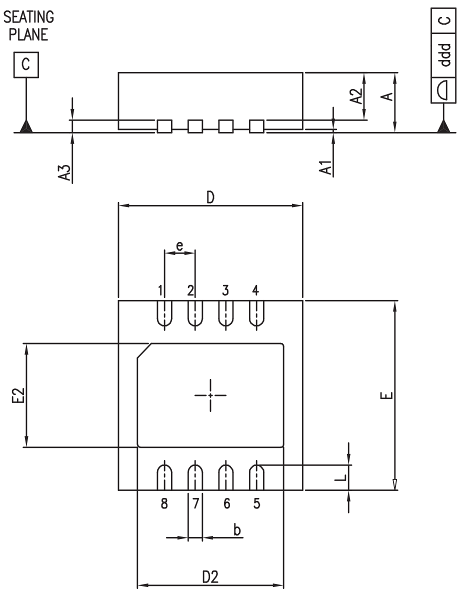
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.1			0.043
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.78	0.86	0.94	0.031	0.031	0.037
b	0.25	0.33	0.40	0.010	0.13	0.013
c	0.13	0.18	0.23	0.005	0.007	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.75	4.90	5.05	0.187	0.193	0.199
E1	2.90	3.00	3.10	.0114	0.118	0.122
e		0.65			0.026	
K	0°		6°	0°		6°
L	0.40	0.55	0.70	0.016	0.022	0.028
L1			0.10			0.004



PACKAGE MECHANICAL DATA

DFN8 (3x3) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.80	0.90	1.00	31.5	35.4	39.4
A1		0.02	0.05		0.8	2.0
A2		0.70			27.6	
A3		0.20			7.9	
b	0.18	0.23	0.30	7.1	9.1	11.8
D		3.00			118.1	
D2	2.23	2.38	2.48	87.8	93.7	97.7
E		3.00			118.1	
E2	1.49	1.64	1.74	58.7	64.6	68.5
e		0.50			19.7	
L	0.30	0.40	0.50	11.8	15.7	19.7



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