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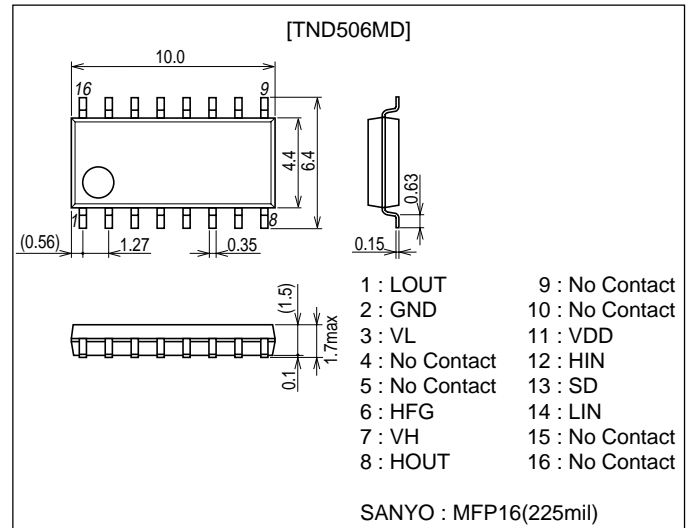
General Purpose Driver for Applications Including PDP Sustain Pulse Drive, DC / AC Motor Drive, Ballast, Battery Charger, High Frequency Switching Power Supply, Induction Heating, and Switching Amplifiers

Features

- Monolithic structure.
- Allows simplified configuration of driver circuit.
- Withstand voltage of 600V is assured.
- Shutdown protection function.
- Low-side output-watching circuit.
- Fully compatible input to LSTTL/CMOS.
- Fast switching time(120ns at 1000pF load).
- Propagation delay is about 150ns.
- Output current : 220mA Source, 450mA Sink.

Package Dimensions

unit : mm
2198



Specifications

Absolute Maximum Ratings at Ta=25°C (All voltage parameters are absolute voltage referenced to GND)

Parameter	Symbol	Conditions	Ratings	Unit
High Side Floating Supply Voltage	V _H		-0.3 to 625	V
High Side Floating Supply Offset Voltage	V _{HFG}		V _H -25 to V _H +0.3	V
High Side Output Voltage	V _{HOUT}		V _{HFG} -0.3 to V _H +0.3	V
Low Side Supply Voltage	V _L		-0.3 to 25	V
Low Side Output Voltage	V _{LOUT}		-0.3 to V _L +0.3	V
Logic Supply Voltage V _{DD}			-0.3 to 25	V
Logic Input Voltage(HIN, LIN, SD)	V _{IN}		-0.3 to V _{DD} +0.3	V
Allowable Power Dissipation	P _D	Mounted on a ceramic board	0.9	W
Junction Temperature	T _J		-55 to +150	°C
Storage Temperature	T _{stg}		-55 to +150	°C

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Recommended Operating Conditions at Ta=25°C

Parameter	Symbol	Conditions	Ratings	Unit
High Side Floating Supply Voltage	V _H		V _{HFG} +10 to V _{HFG} +20	V
High Side Floating Supply Offset Voltage	V _{HFG}		0 to 600	V
High Side Output Voltage	V _{HOUT}		V _{HFG} to V _H	V
Low Side Supply Voltage	V _L		10 to +20	V
Low Side Output Voltage	V _{LOUT}		0 to V _L	V
Logic Supply Voltage	V _{DD}		+5 to +20	V
Logic Input Voltage(HIN, LIN, SD)	V _{IN}		0 to V _{DD}	V
Ambient Temperature	Topr		-40 to +125	°C

AC Characteristics at Ta=25°C (V_{DD}=V_L=V_{HFG}=15V, C_L=1000pF)

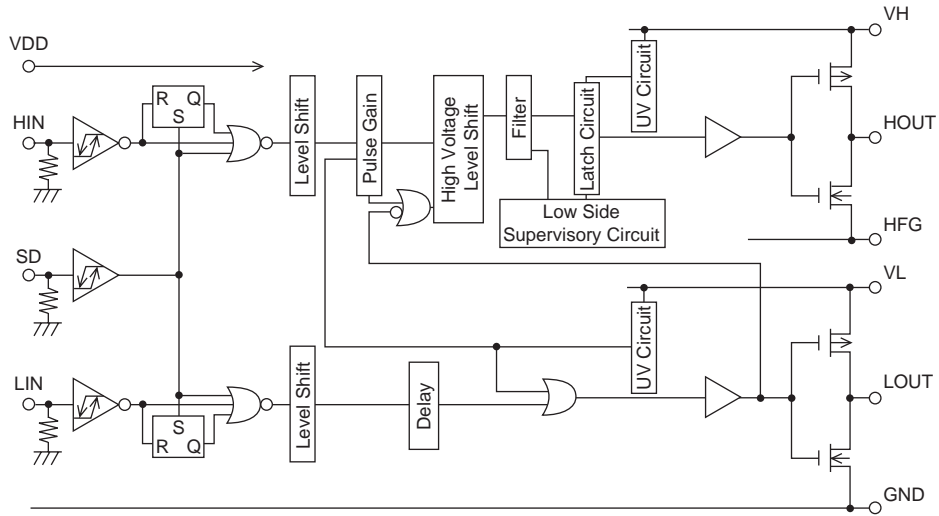
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Turn-ON Delay Time	t _{on}	V _{HFG} =0V	105	150	195	ns
Turn-OFF Delay Time	t _{off}	V _{HFG} =600V	84	120	156	ns
Shutdown Delay Time	t _{sd}	V _{HFG} =600V		120		ns
Turn-ON Rise Time	t _r			120		ns
Turn-OFF Fall Time	t _f			60		ns
Delay Matching, HS and LS Turn-ON	M _{t_{on}}	Ht _{on} -Lt _{on}		15		ns
Delay Matching, HS and LS Turn-OFF	M _{t_{off}}	Ht _{off} -Lt _{off}		15		ns

DC Characteristics at Ta=25°C, (V_{DD}=V_L=V_{HFG}=15V)

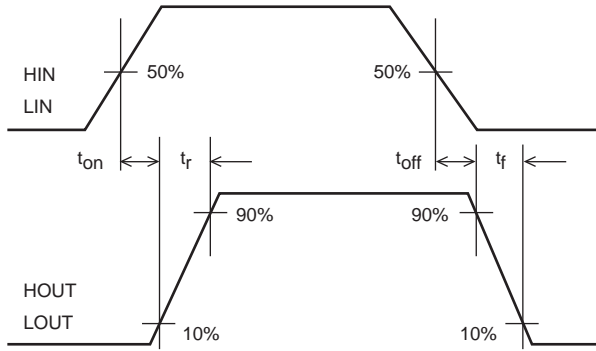
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Logic "1" Input Voltage	V _{IH}	V _{DD} =5V	3.2			V
		V _{DD} =10V	6.4			V
		V _{DD} =15V	9.5			V
		V _{DD} =20V	12.8			V
Logic "0" Input Voltage	V _{IL}	V _{DD} =5V			1.5	V
		V _{DD} =10V			3.7	V
		V _{DD} =15V			5.8	V
		V _{DD} =20V			7.7	V
High-level Output Voltage, V _{BIAS-VO}	V _{OH}	V _{IN} =V _{IH} , I _O =0A			0.1	V
Low-level Output Voltage, V _O	V _{OL}	V _{IN} =V _{IL} , I _O =0A			0.1	V
Offset Supply Leakage Current	I _{LK}	V _H =V _{HFG} =600V			10	μA
Quiescent V _H Supply Current	I _{QH}	V _{IN} =0V or V _{DD}		35	60	μA
Quiescent V _L Supply Current	I _{QL}	V _{IN} =0V or V _{DD}		120	200	μA
Quiescent V _{DD} Supply Current	I _{QDD}	V _{IN} =0V or V _{DD}		5	20	μA
Logic "1" Input Bias Current	I _{IN+}	V _{IN} =V _{DD}		20	55	μA
Logic "0" Input Bias Current	I _{IN-}	V _{IN} =0V			1	μA
V _H Supply Undervoltage Positive Going Threshold	V _{HUV+}		7.6	8.9	9.9	V
V _H Supply Undervoltage Negative Going Threshold	V _{HUV-}		6.7	8.1	9.5	V
V _L Supply Undervoltage Positive Going Threshold	V _{LUV+}		7.6	8.9	9.9	V
V _L Supply Undervoltage Negative Going Threshold	V _{LUV-}		6.7	8.1	9.5	V
Output High Short Circuit Pulsed Current	I _{O+}	V _{OUT} =0V, V _{IN} =15V, PW≤10μs	220	250		mA
Output Low Short Circuit Pulsed Current	I _{O-}	V _{OUT} =15V, V _{IN} =0V, PW≤10μs	450	500		mA

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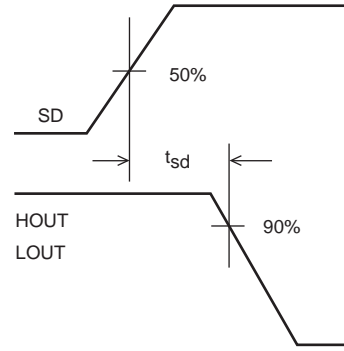
Functional Block Diagram



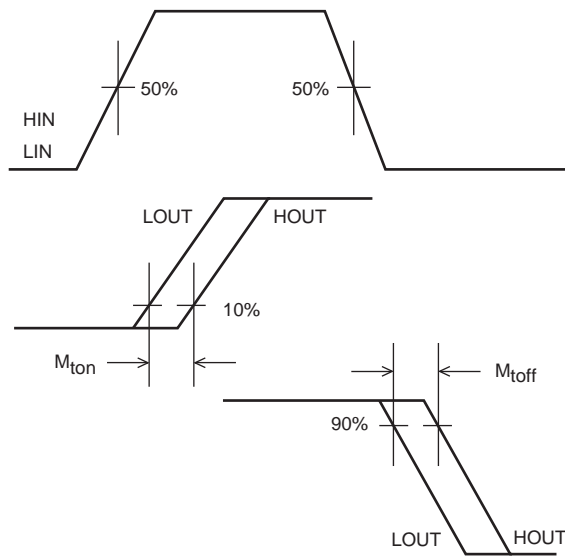
Switching Time Waveform Definition



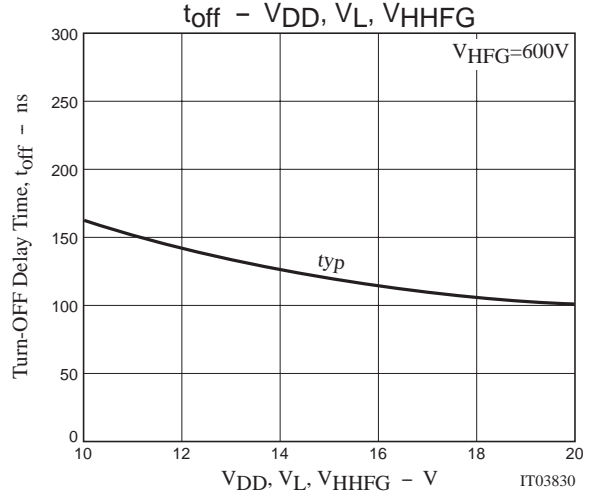
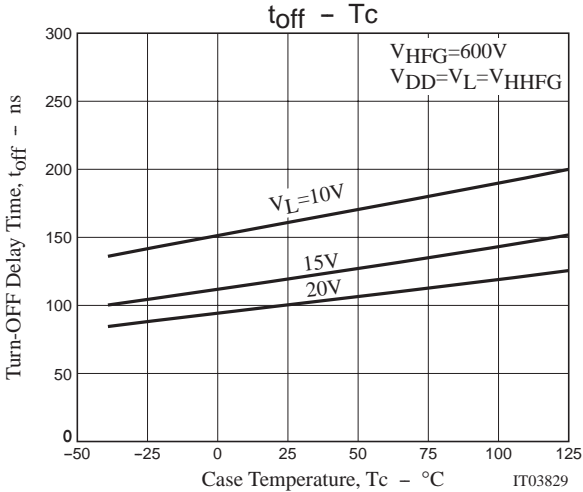
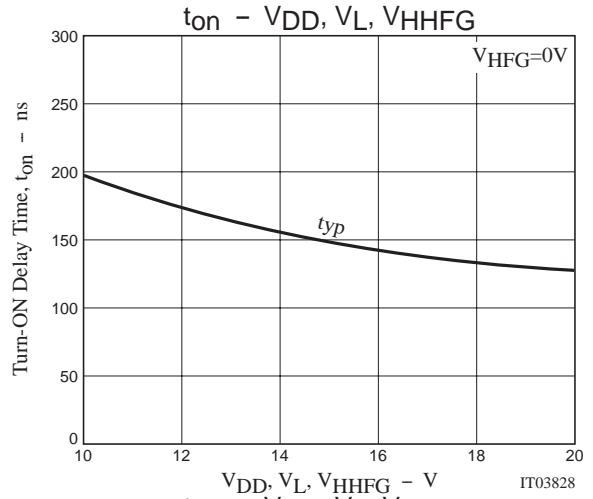
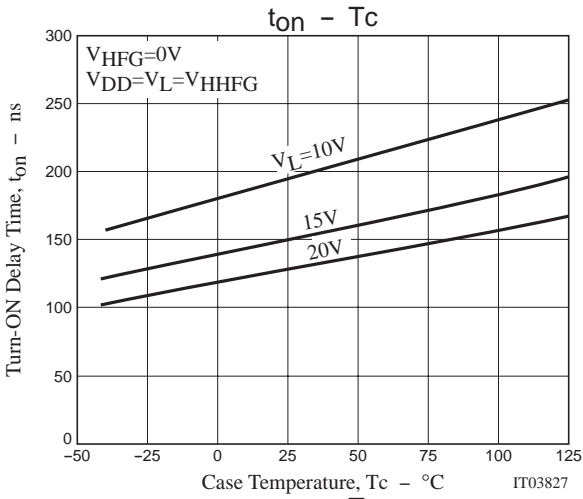
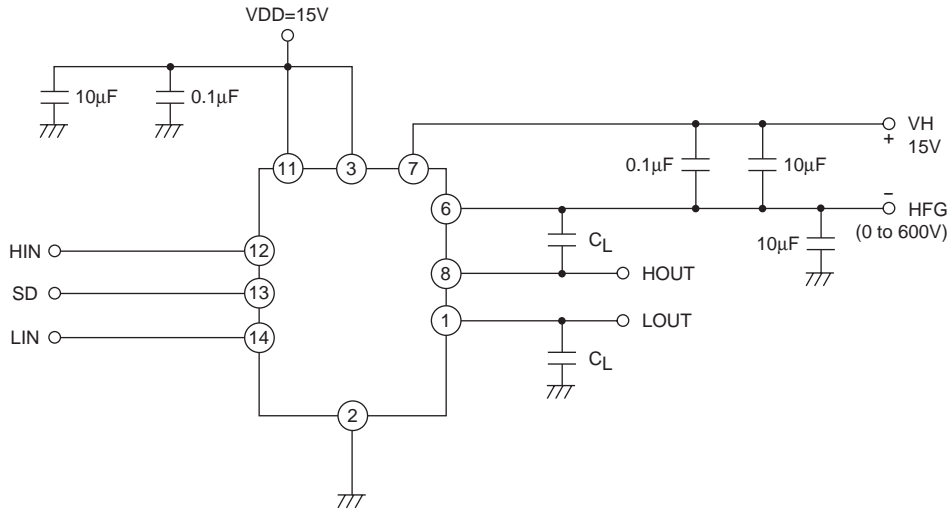
Shutdown Waveform Definition



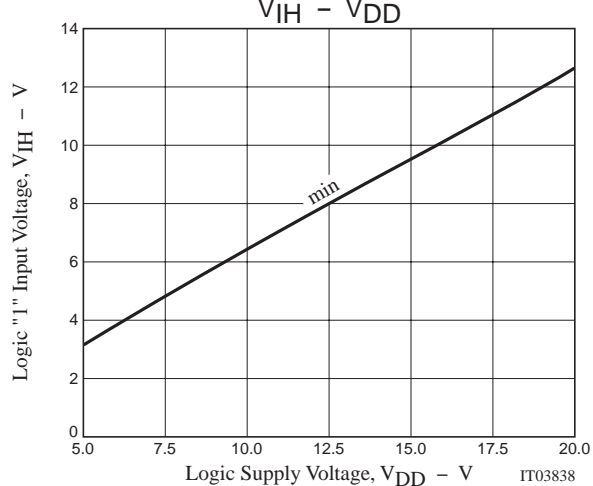
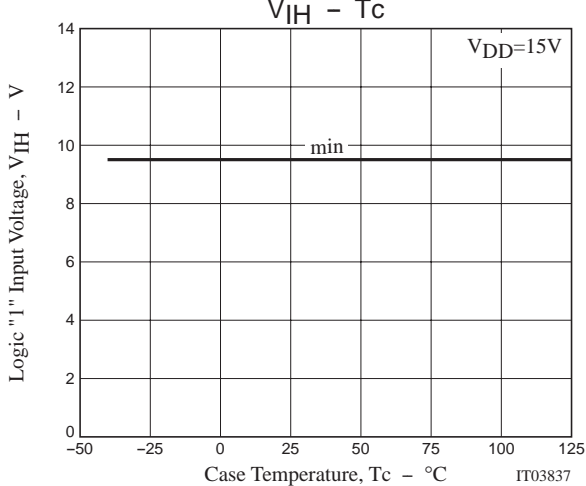
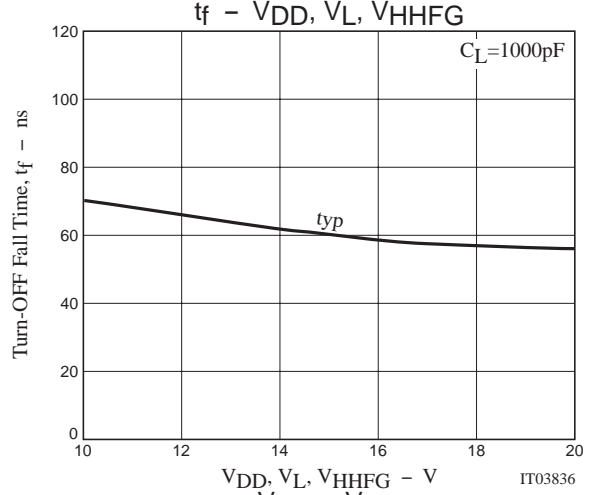
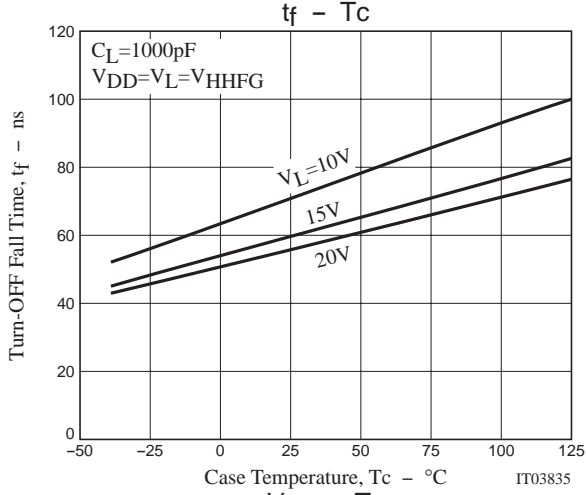
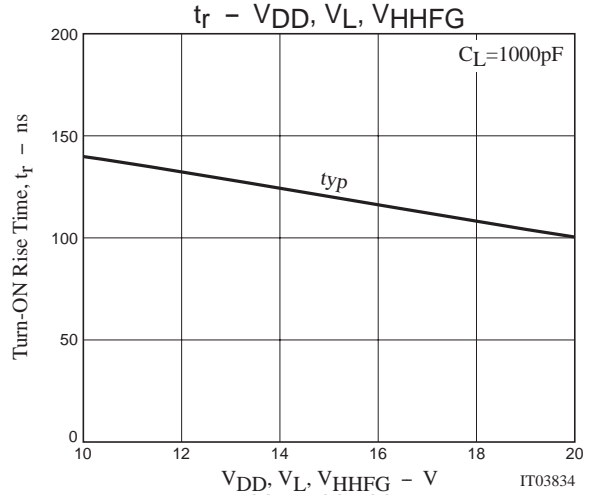
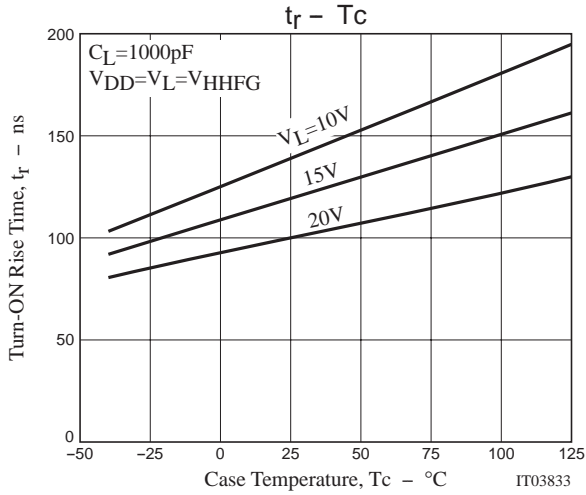
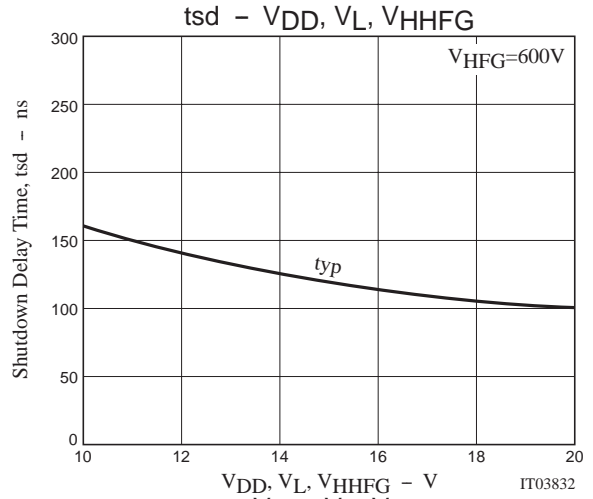
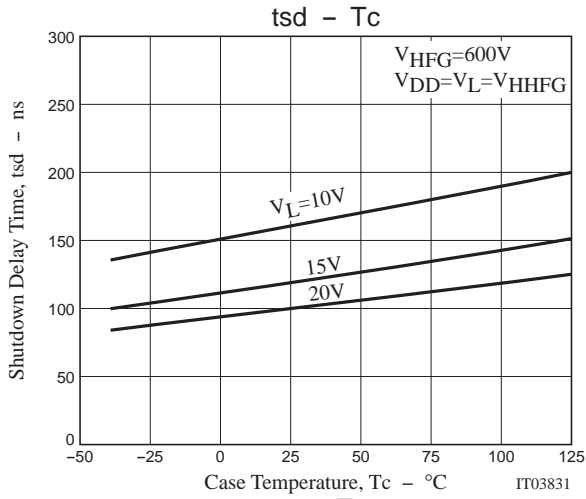
Delay Matching Waveform Definition



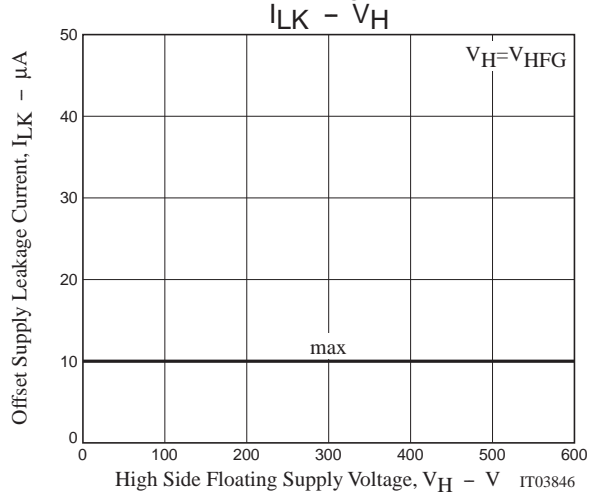
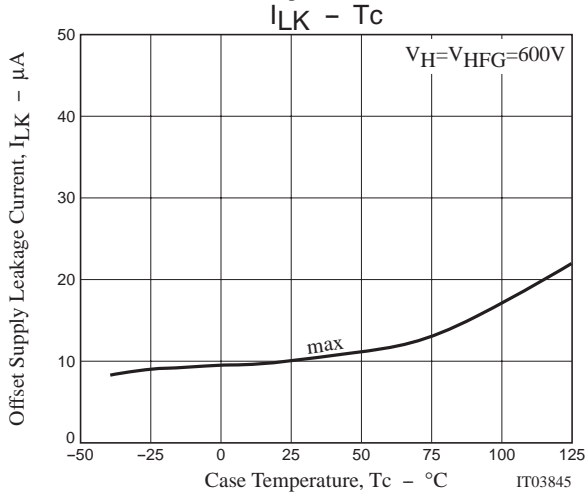
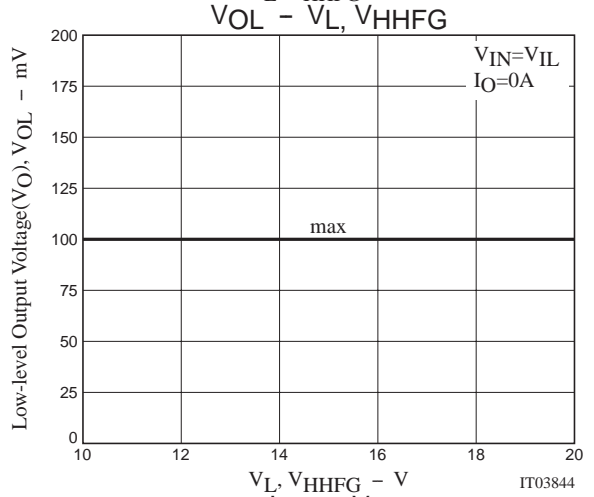
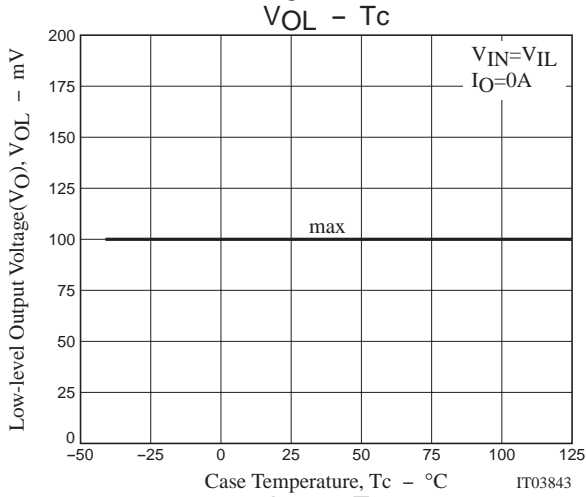
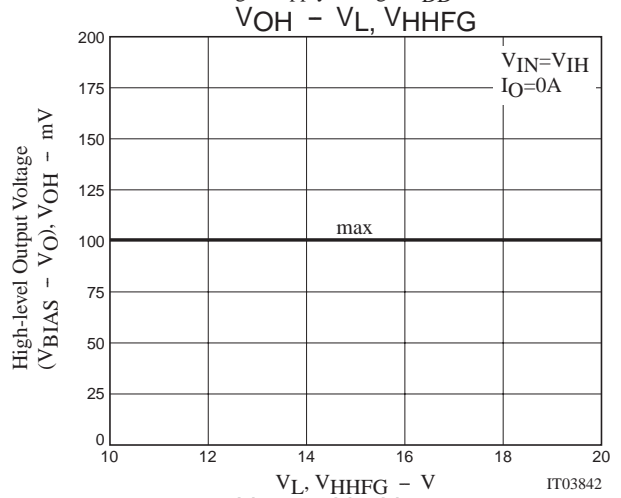
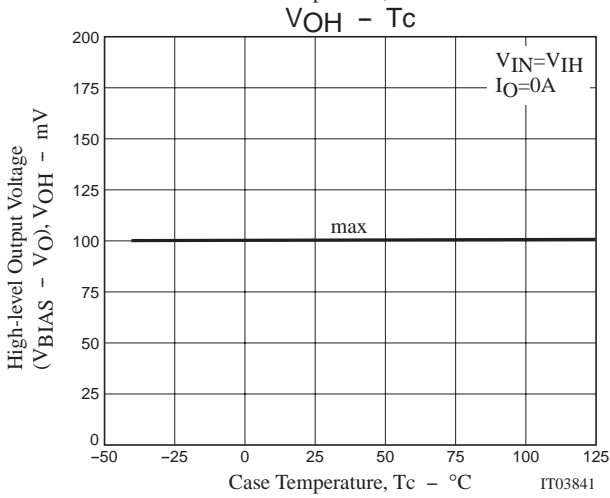
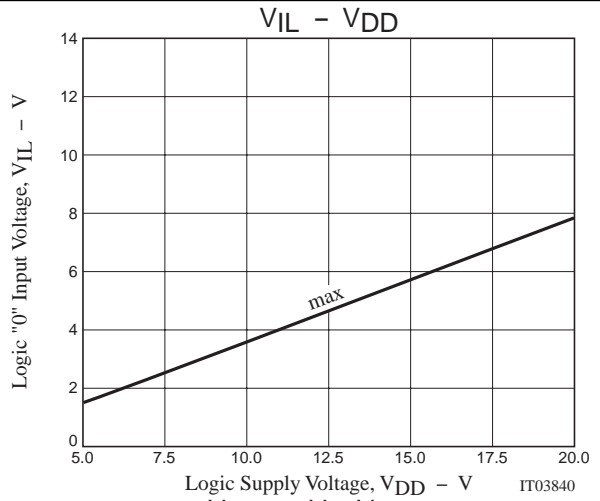
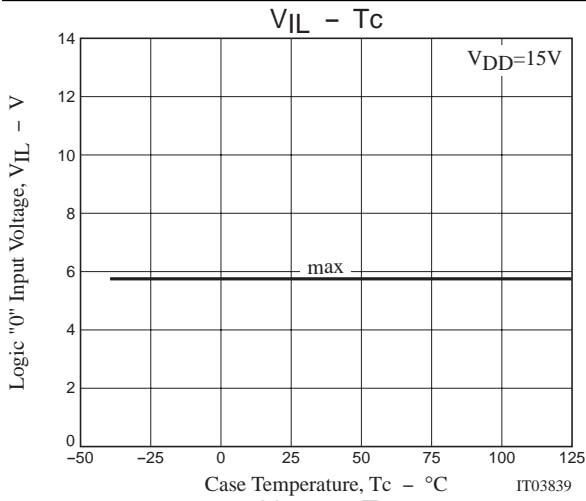
Switching Time Test Circuit



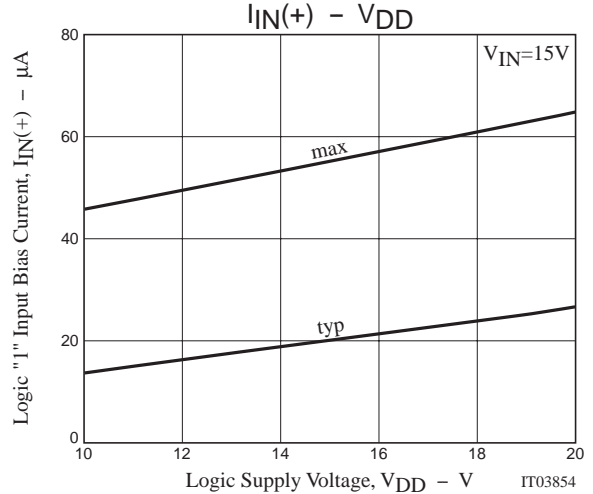
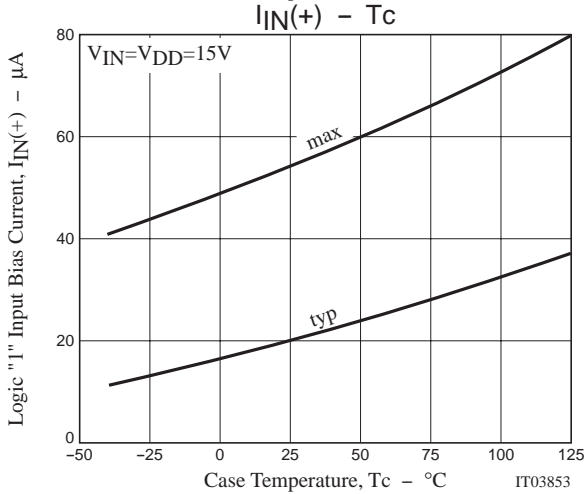
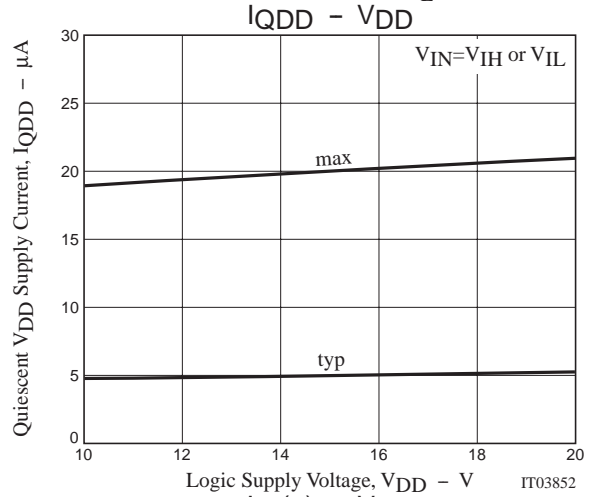
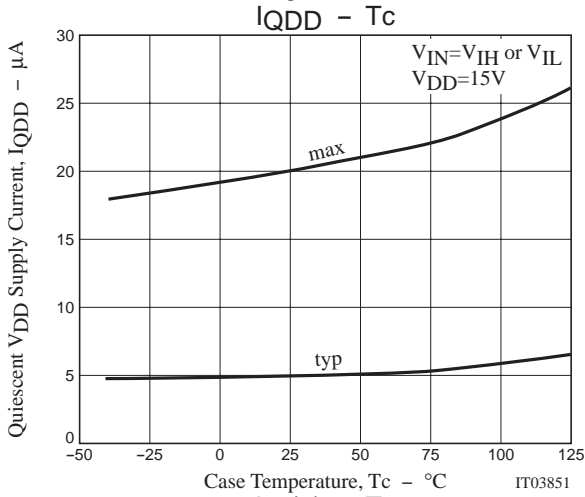
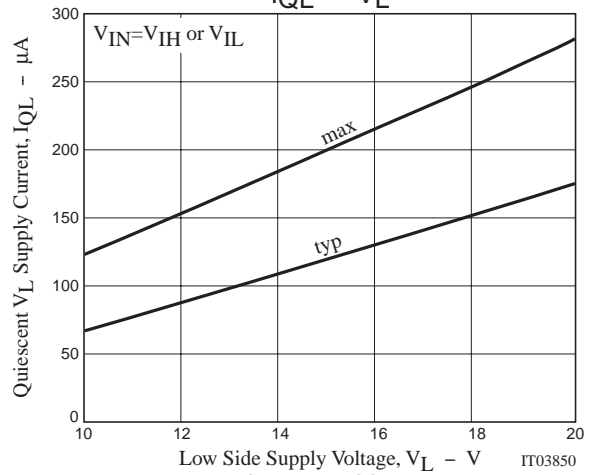
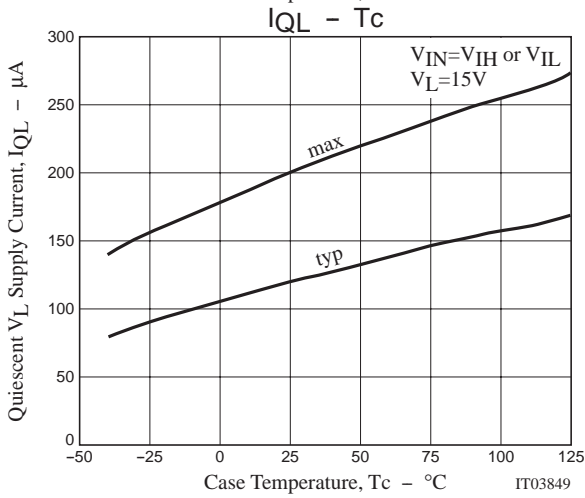
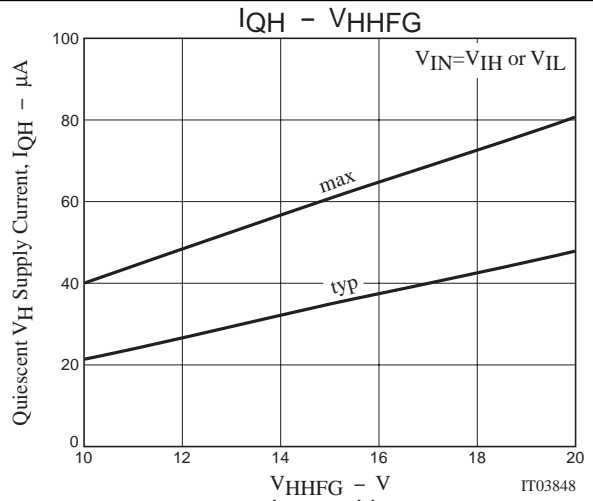
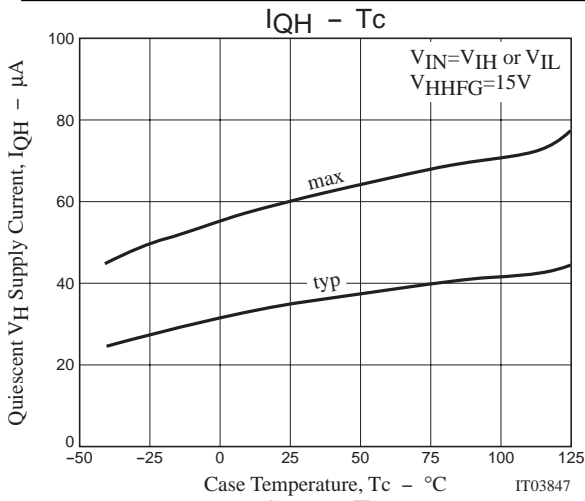
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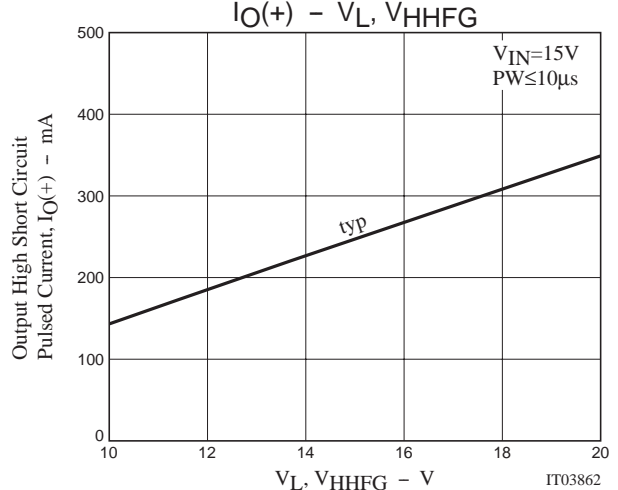
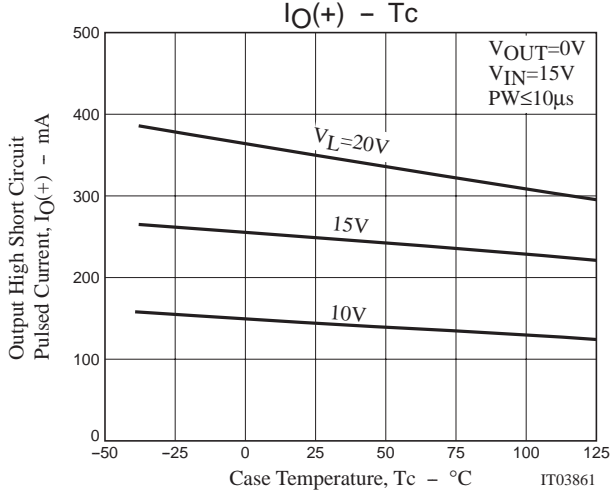
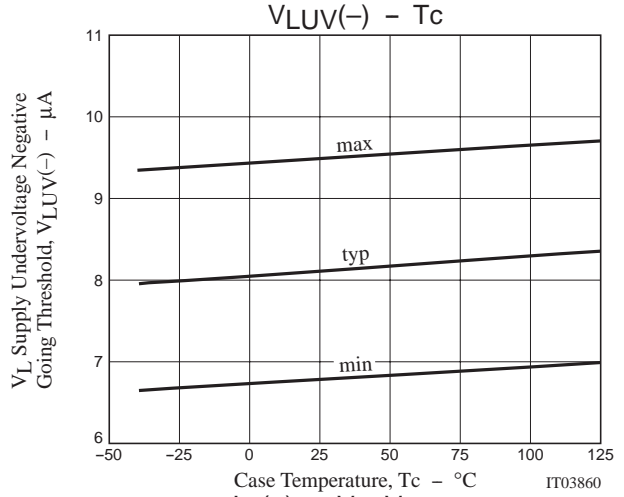
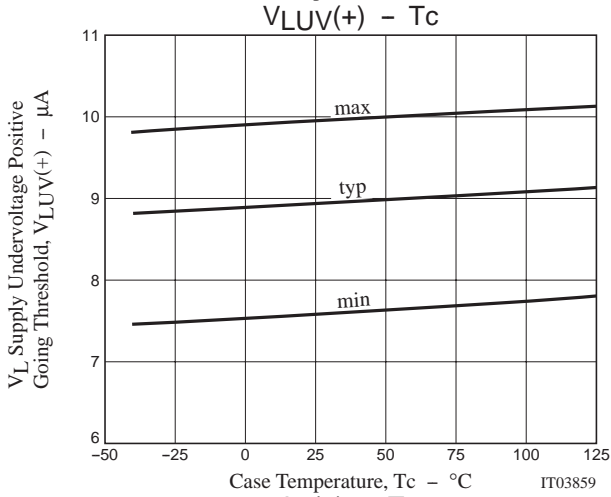
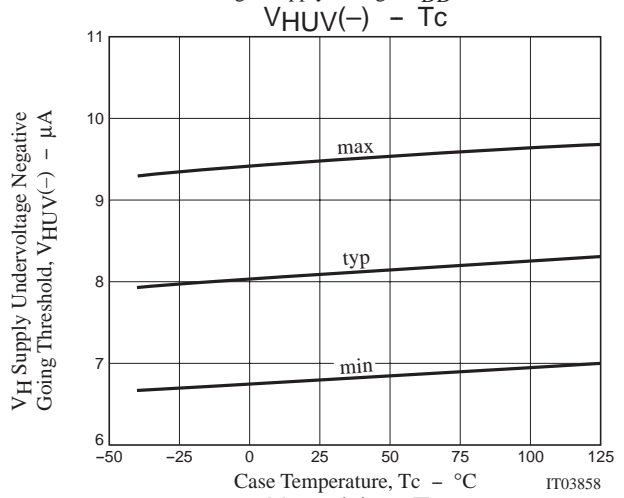
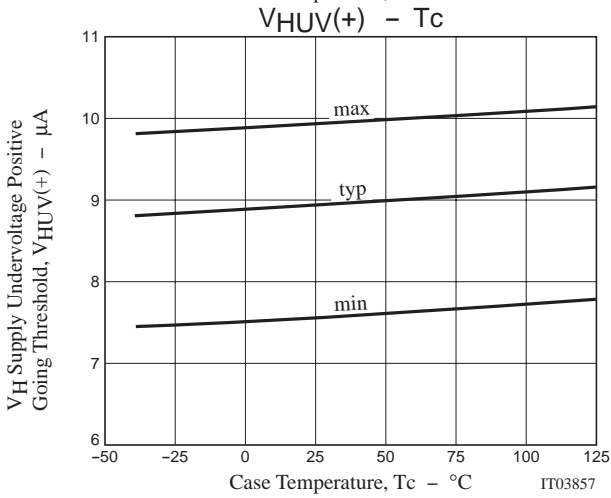
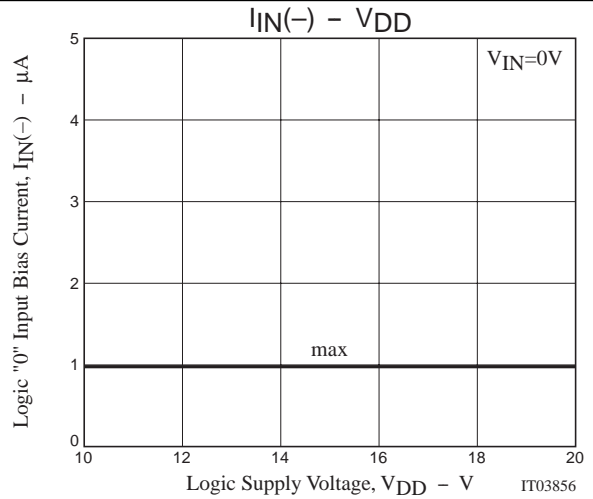
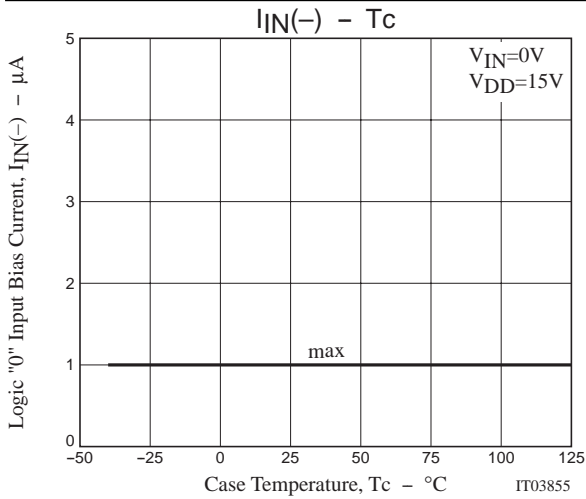
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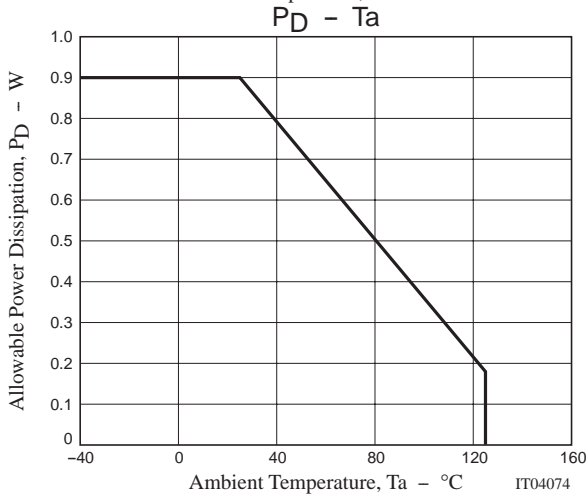
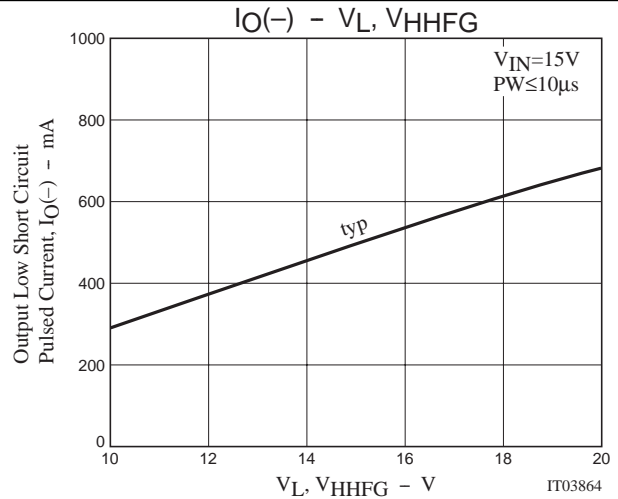
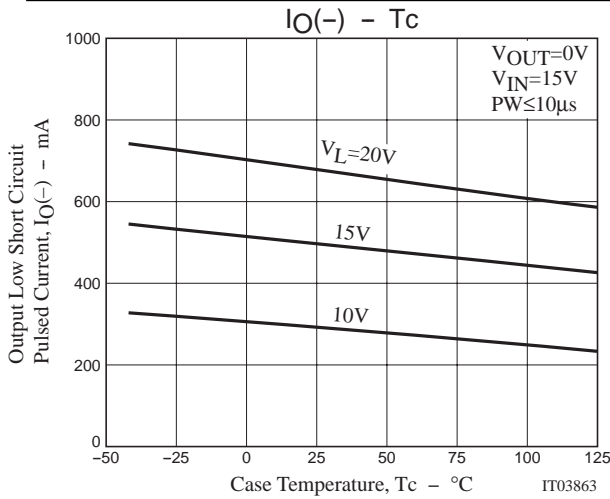
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