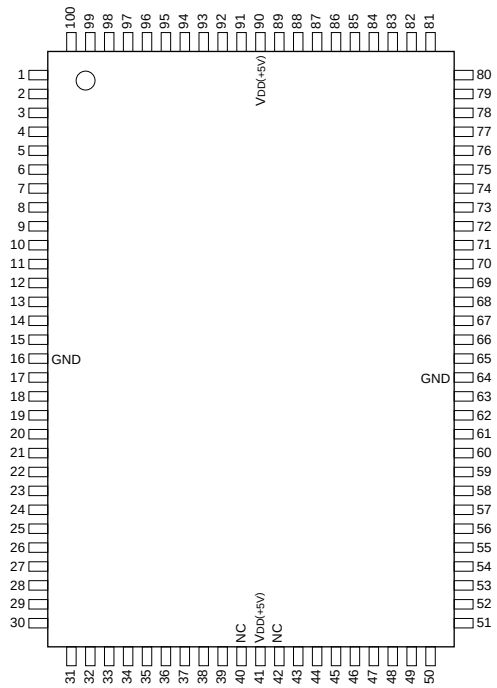
****

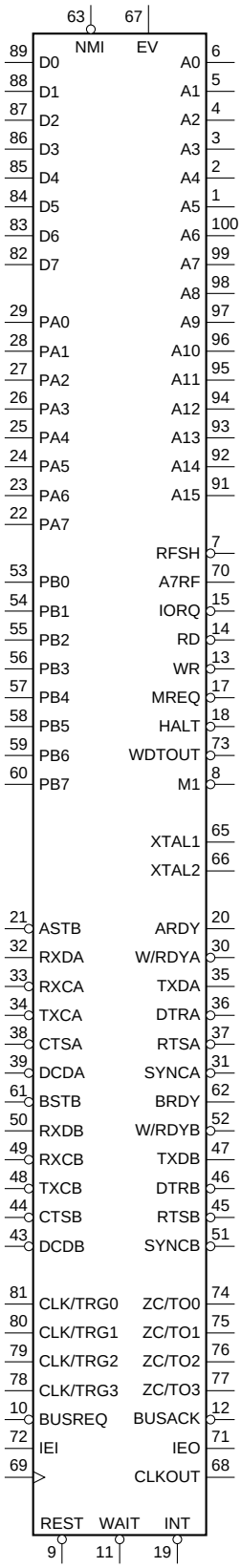
C-MOS 8-BIT MICROPROCCESSOR
-TOP VIEW-

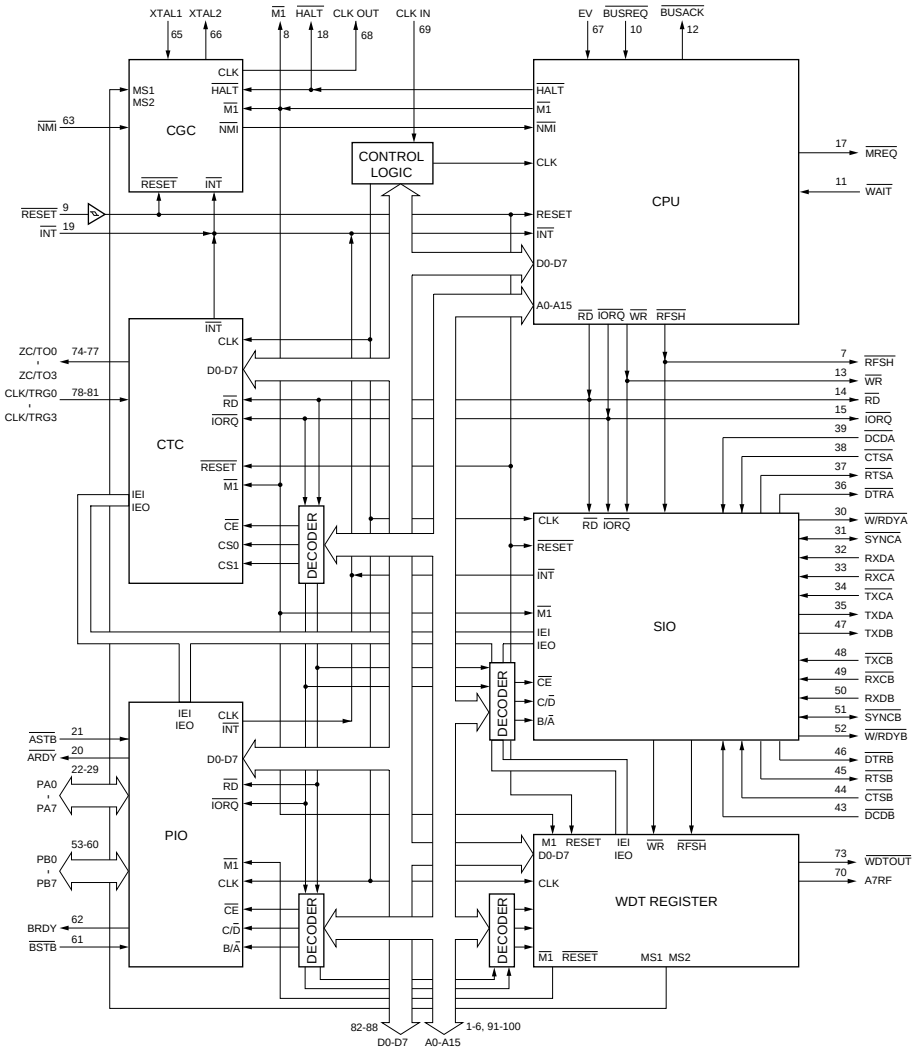


(V_{DD} = +5V)

NO.	I/O	SIGNAL	NO.	I/O	SIGNAL	NO.	I/O	SIGNAL	NO.	I/O	SIGNAL
1	O	A5	26	I/O	PA3	51	I/O	$\overline{\text{SYNCB}}$	76	O	ZC/TO2
2	O	A4	27	I/O	PA2	52	O	$\overline{\text{W/RDYB}}$	77	O	ZC/TO3
3	O	A3	28	I/O	PA1	53	I/O	PB0	78	I	CLK/TRG3
4	O	A2	29	I/O	PA0	54	I/O	PB1	79	I	CLK/TRG2
5	O	A1	30	O	$\overline{\text{W/RDYA}}$	55	I/O	PB2	80	I	CLK/TRG1
6	O	A0	31	I/O	$\overline{\text{SYNCA}}$	56	I/O	PB3	81	I	CLK/TRG0
7	O	$\overline{\text{RFSH}}$	32	I	RXDA	57	I/O	PB4	82	I/O	D7
8	O	$\overline{\text{M1}}$	33	I	$\overline{\text{RXCA}}$	58	I/O	PB5	83	I/O	D6
9	I	$\overline{\text{REST}}$	34	I	$\overline{\text{TXCA}}$	59	I/O	PB6	84	I/O	D5
10	I	$\overline{\text{BUSREQ}}$	35	O	TXDA	60	I/O	PB7	85	I/O	D4
11	I	$\overline{\text{WAIT}}$	36	O	$\overline{\text{DTRA}}$	61	I	$\overline{\text{BSTB}}$	86	I/O	D3
12	O	$\overline{\text{BUSACK}}$	37	O	$\overline{\text{RTSA}}$	62	O	BRDY	87	I/O	D2
13	O	$\overline{\text{WR}}$	38	I	$\overline{\text{CTSA}}$	63	I	$\overline{\text{NMI}}$	88	I/O	D1
14	O	$\overline{\text{RD}}$	39	I	$\overline{\text{DCDA}}$	64	—	GND	89	I/O	D0
15	O	$\overline{\text{IORQ}}$	40	—	NC	65	I	XTAL1	90	—	V_{DD}
16	—	GND	41	—	V_{DD}	66	O	XTAL2	91	O	A15
17	O	$\overline{\text{MREQ}}$	42	—	NC	67	I	EV	92	O	A14
18	O	$\overline{\text{HALT}}$	43	I	$\overline{\text{DCDB}}$	68	O	CLKOUT	93	O	A13
19	I	$\overline{\text{INT}}$	44	I	$\overline{\text{CTSB}}$	69	I	CLKIN	94	O	A12
20	O	ARDY	45	O	$\overline{\text{RTSB}}$	70	O	A7RF	95	O	A11
21	I	$\overline{\text{ASTB}}$	46	O	$\overline{\text{DTRB}}$	71	O	IEO	96	O	A10
22	I/O	PA7	47	O	TXDB	72	I	IEI	97	O	A9
23	I/O	PA6	48	I	$\overline{\text{TXCB}}$	73	O	$\overline{\text{WDTOUT}}$	98	O	A8
24	I/O	PA5	49	I	$\overline{\text{RXCB}}$	74	O	ZC/TO0	99	O	A7
25	I/O	PA4	50	I	RXDB	75	O	ZC/TO1	100	O	A6

TMPZ84C015AF (2/3)





A0 - A15	; 3-STATE ADDRESS BUS OUTPUTS	WR	; 3-STATE WRITE OUTPUT
BUSACK	; BUS ACKNOWLEDGE OUTPUT	ZC/TO0-3	; ZERO COUNT/TIME OUT 0-3 OUTPUT
BUSREQ	; BUS REQUEST INPUT	ASTB	; PORT A STROBE PULSE INPUT
CLK/TRIG0 - 3	; EXTERNAL CLOCK/TIMER TRIGGER 0-3 INPUTS	ARDY	; REGISTER A READY OUTPUT
D0 - D7	; 3-STATE DATA BUS INPUTS/OUTPUTS	BSTB	; PORT B STROBE PULSE INPUT
EV	; EVALUATER INPUT	BRDY	; REGISTER B READY OUTPUT
HALT	; HALT OUTPUT	SYNCA, SYNCB	; SYNC INPUT/OUTPUT
IEI/IEO	; CTC INTERRUPT ENABLE INPUT/OUTPUT	W/RDYA, W/RDYB	; WAIT/READY OUTPUT
INT	; MASKABLE INTERRUPT REQUEST/INPUT	RXDA, RXDB	; SERIAL DATA INPUT
IORQ	; 3-STATE I/O REQUEST OUTPUT	RXCA, RXCB	; RECEIVE CLOCK INPUT
M1	; 3-STATE MACHINE CYCLE 1 OUTPUT	TXCA, TXCB	; TRANSMISSION CLOCK INPUT
MREQ	; 3-STATE MEMORY REQUEST OUTPUT	TXDA, TXDB	; SERIAL DATA OUTPUT
NMI	; NON-MASKABLE INTERRUPT REQUEST INPUT	DTRA, DTRB	; DATA TERMINAL READY OUTPUT
PA0 - PA7, PB0 - PB7	; 3-STATE I/O PORT	RTSA, RTSB	; TRANSMISSION REQUEST OUTPUT
RD	; 3-STATE READ OUTPUT	CTSA, CTSB	; TRANSMISSION ENABLE INPUT
REST	; RESET INPUT	DCDA, DCDB	; DATA CARRIER DETECT OUTPUT
RFSH	; REFRESH OUTPUT	WDTOUT	; WATCH DOG TIMER OUTPUT
WAIT	; WAIT REQUEST INPUT		