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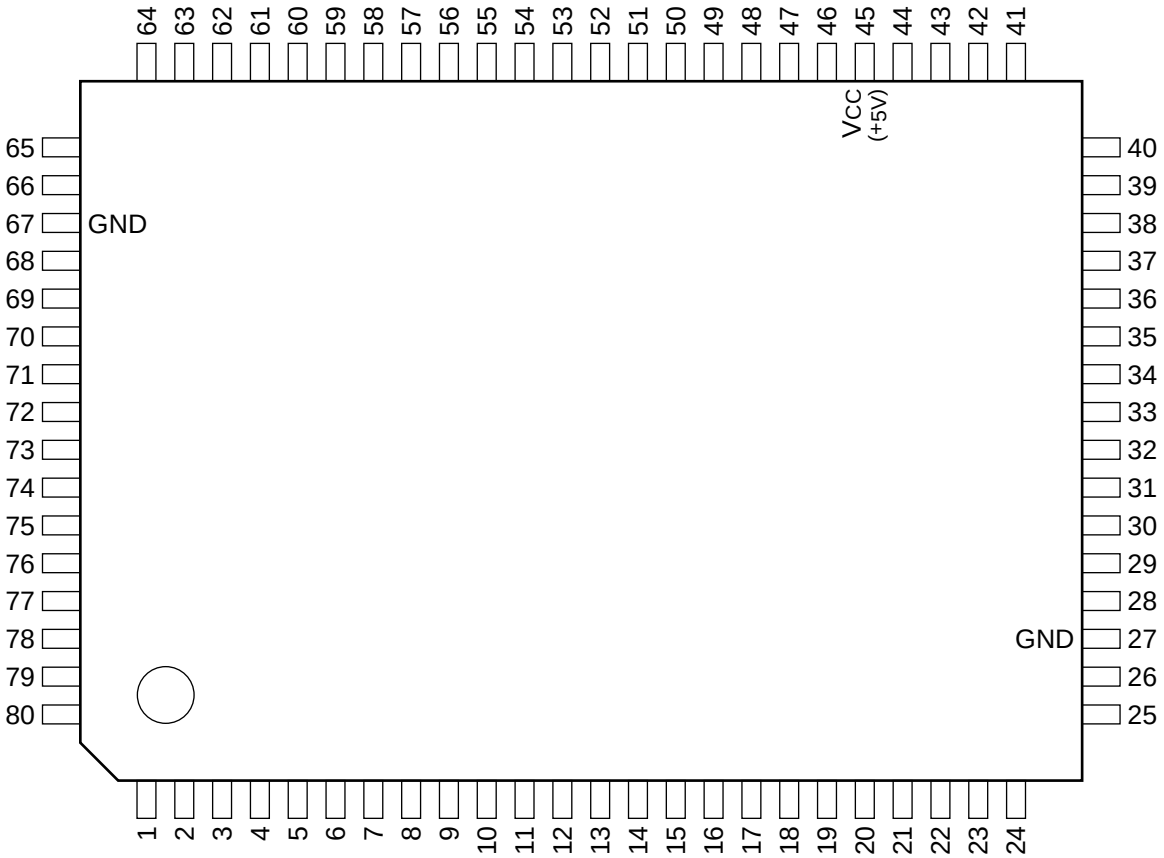
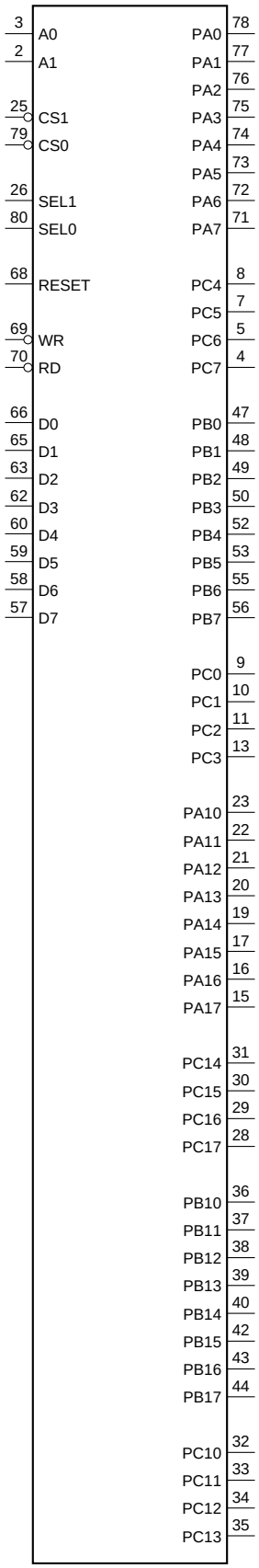
C-MOS PROGRAMMABLE PERIPHERAL INTERFACE

-TOP VIEW-



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	–	NC	21	I/O	PA12	41	–	NC	61	–	NC
2	I	A1	22	I/O	PA11	42	I/O	PB15	62	I/O	D3
3	I	A0	23	I/O	PA10	43	I/O	PB16	63	I/O	D2
4	I/O	PC07	24	–	NC	44	I/O	PB17	64	–	NC
5	I/O	PC06	25	I	$\overline{CS1}$	45	–	VCC	65	I/O	D1
6	–	NC	26	I	SEL1	46	–	NC	66	I/O	D0
7	I/O	PC05	27	–	GND	47	I/O	PB00	67	–	GND
8	I/O	PC04	28	I/O	PC17	48	I/O	PB01	68	I	RESET
9	I/O	PC00	29	I/O	PC16	49	I/O	PB02	69	I	$\overline{WR}$
10	I/O	PC01	30	I/O	PC15	50	I/O	PB03	70	I	$\overline{RD}$
11	I/O	PC02	31	I/O	PC14	51	–	NC	71	I/O	PA7
12	–	NC	32	I/O	PC10	52	I/O	PB04	72	I/O	PA6
13	I/O	PC03	33	I/O	PC11	53	I/O	PB05	73	I/O	PA5
14	–	NC	34	I/O	PC12	54	–	NC	74	I/O	PA4
15	I/O	PA17	35	I/O	PC13	55	I/O	PB06	75	I/O	PA3
16	I/O	PA16	36	I/O	PB10	56	I/O	PB07	76	I/O	PA2
17	I/O	PA15	37	I/O	PB11	57	I/O	D7	77	I/O	PA1
18	–	NC	38	I/O	PB12	58	I/O	D6	78	I/O	PA0
19	I/O	PA14	39	I/O	PB13	59	I/O	D5	79	I	$\overline{CS0}$
20	I/O	PA13	40	I/O	PB14	60	I/O	D4	80	I	SEL0

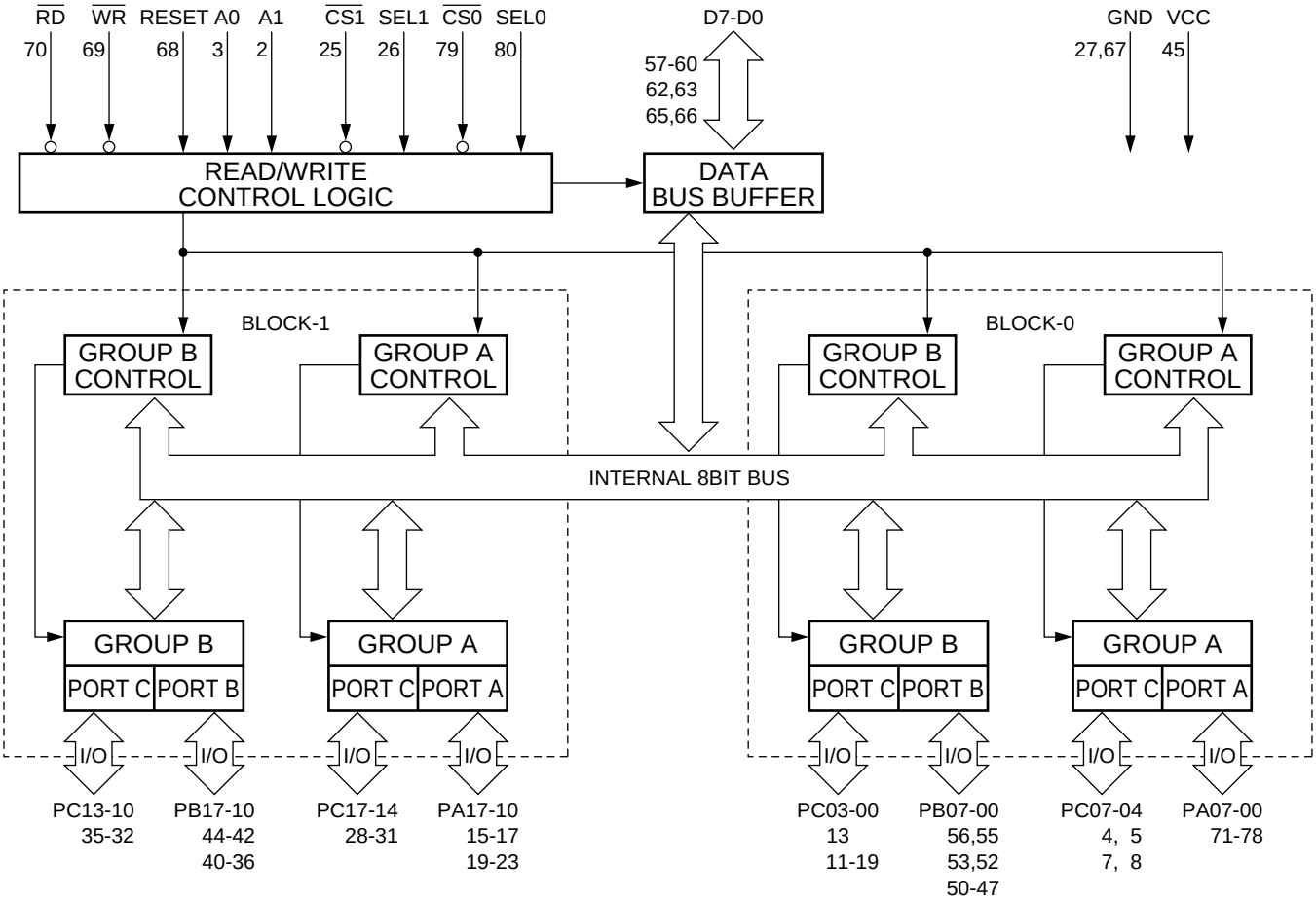


INPUT

A0-A1	;	ADDRESS LINE
$\overline{CS0}$-$\overline{CS1}$	;	CHIP SELECT
$\overline{RD}$	;	READ CONTROL
R/$\overline{W}$	;	READ/WRITE CONTROL
RESET	;	RESET
SEL	;	GENERAL MODE/OUTPUT MODE SELECT CONTROL
$\overline{WR}$	;	WRITE CONTROL

INPUT/OUTPUT

D0-D7	;	DATA BUS
PA0-PA17	;	INPUT/OUTPUT PORT A
PB0-PB17	;	INPUT/OUTPUT PORT B
PC0-PC17	;	INPUT/OUTPUT PORT C


RD
70
WR
69
RESET
68
A0
3
A1
2
CS1
25
SEL1
26
CS0
79
SEL0
80
D7-D0
57-60
62,63
65,66
GND
27,67
VCC
45
READ/WRITE
CONTROL LOGIC
DATA
BUS BUFFER
BLOCK-1
BLOCK-0
GROUP B
CONTROL
GROUP A
CONTROL
INTERNAL 8BIT BUS
GROUP B
PORT C
PORT B
GROUP A
PORT C
PORT A
I/O
PC13-10
35-32
PB17-10
44-42
40-36
PC17-14
28-31
PA17-10
15-17
19-23
PC03-00
13
11-19
PB07-00
56,55
53,52
50-47
PC07-04
4, 5
7, 8
PA07-00
71-78