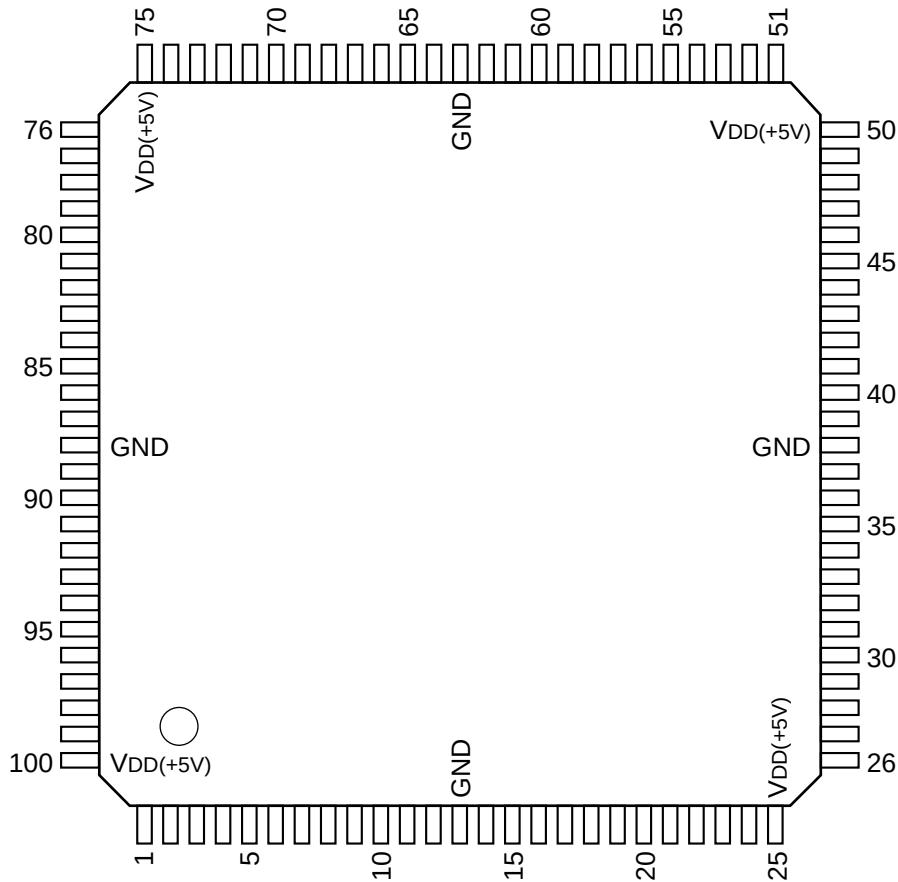

C-MOS 16-BIT MICRO PROCESSOR

—TOP VIEW—



(V_{DD} = +5 V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I/O	A19	21	I/O	D1	41	I/O	M11/P11	61	I/O	LDS	81	I/O	A1
2	I/O	A20	22	I/O	D0	42	I/O	M10/P10/ TOUT4	62	I/O	R/W	82	I/O	A2
3	I/O	A21	23	I/O	CTS0/P21	43	I/O	M03/P03	63	—	GND	83	I/O	A3
4	I/O	A22	24	I/O	RTS0/P20	44	I/O	M02/P02	64	I	CLK	84	I/O	A4
5	I/O	A23	25	—	V _{DD}	45	I/O	M01/P01	65	O	TOUT2	85	I/O	A5
6	I/O	D15	26	O	TXD1	46	I/O	M00/P00/ TOUT3	66	O	TOUT1	86	I/O	A6
7	I/O	D14	27	O	TXD0	47	O	IACK2	67	I	TIN	87	I/O	A7
8	I/O	D13	28	I	RXD1	48	O	IACK1	68	O	BG	88	—	GND
9	I/O	D12	29	I	RXD0	49	O	IACK0	69	I/O	BGACK	89	I/O	A8
10	I/O	D11	30	I	BCLK	50	—	V _{DD}	70	I/O	BR	90	I/O	A9
11	I/O	D10	31	I/O	DTEND	51	I	INT2	71	I/O	DTACK	91	I/O	A10
12	I/O	D9	32	O	DACK2	52	I	INT1	72	I/O	HALT	92	I/O	A11
13	—	GND	33	O	DACK1	53	I	INT0	73	I/O	RESET	93	I/O	A12
14	I/O	D8	34	O	DACK0	54	O	CAS/CS1	74	I/O	BERR	94	I/O	A13
15	I/O	D7	35	I	DREQ2	55	O	RAS/CS0	75	—	V _{DD}	95	I/O	A14
16	I/O	D6	36	I	DREQ1	56	I/O	IPL2	76	I	NOR/EMU	96	I/O	A15
17	I/O	D5	37	I	DREQ0	57	I/O	IPL1	77	I	BGIN	97	I/O	A16
18	I/O	D4	38	—	GND	58	I/O	IPL0	78	I/O	FC2	98	I/O	A17
19	I/O	D3	39	I/O	M13/P13	59	I/O	AS	79	I/O	FC1	99	I/O	A18
20	I/O	D2	40	I/O	M12/P12	60	I/O	UDS	80	I/O	FC0	100	—	V _{DD}

5	A23	D15	6
4	A22	D14	7
3	A21	D13	8
2	A20	D12	9
1	A19	D11	10
99	A18	D10	11
98	A17	D9	12
97	A16	D8	14
96	A15	D7	15
95	A14	D6	16
94	A13	D5	17
93	A12	D4	18
92	A11	D3	19
91	A10	D2	20
90	A9	D1	21
89	A8	D0	22
87	A7		
86	A6	DACK0	34
85	A5	DACK1	33
84	A4	DACK2	32
83	A3	IACK0	49
82	A2	IACK1	48
81	A1	IACK2	47
			46
	M00/P00/TOUT3		
29	RXD0	M01/P01	45
28	RXD1	M02/P02	44
23	CTS0/P21	M03/P03	43
53	INT0	M10/P10/TOUT4	42
52	INT1	M11/P11	41
51	INT2	M12/P12	40
37	DREQ0	M13/P13	39
36	DREQ1	TOUT1	66
35	DREQ2	TOUT2	65
30	BCLK		
64	CLK	DTEND	31
77	BGIN	TXD0	27
76	NOR/EMU	TXD1	26
67	TIN	BG	68
58	IPL0	CAS/CS1	54
57	IPL1	RAS/CS0	55
56	IPL2	RTS0/P20	24
59	AS		
60	UDS	BGACK	69
61	LDS	BR	70
62	R/W	DTACK	71
80	FC0	HALT	72
79	FC1	RESET	73
78	FC2	BERR	74

INPUT

BCLK	; BAUD RATE CLOCK
BGIN	; BUS GRANT
CLK	; CLOCK
CTS0	; CLEAR TO SEND
DREQ0 - 2	; DMA REQUESTS
INT0 - 2	; INTERRUPT REQUESTS
NOR/EMU	; MODE SELECT
RXD0, 1	; RECEIVE SERIAL DATA
TIN	; TIMER INPUT

OUTPUT

BG	; BUS GRANT
CAS	; COLUMN ADDRESS STROBE
CS0, 1	; CHIP SELECTS
DACK0 - 2	; DMA ACKNOWLEDGE
IACK0 - 2	; INTERRUPT ACKNOWLEDGE
M00 - 03, 10 - 13	; MOTOR CONTROL
RTS0	; REQUEST TO SEND
RAS	; ROW ADDRESS STROBE
TOUT1 - 4	; TIMER OUTPUTS
TXD0, 1	; TRANSFER SERIAL DATA

INPUT/OUTPUT

A1 - 23	; ADDRESS BUS
AS	; ADDRESS STROBE
BERR	; BUS ERROR
BGACK	; BUS GRANT ACKNOWLEDGE
BR	; BUS REQUEST
D0 - 15	; DATA BUS
DTACK	; DATA TRANSFER ACKNOWLEDGE
DTEND	; DMA FORCED END / TRANSFER END
FC0 - 2	; FUNCTION CORDS
HALT	; HALT
IPL0 - 2	; INTERRUPT CONTROLS
LDS	; LOWER DATA STROBE
P00 - 03	; PORT 0
P10 - 13	; PORT 1
P20, 21	; PORT 2
RESET	; RESET
R/W	; READ/WRITE
UDS	; UPPER DATA STROBE

