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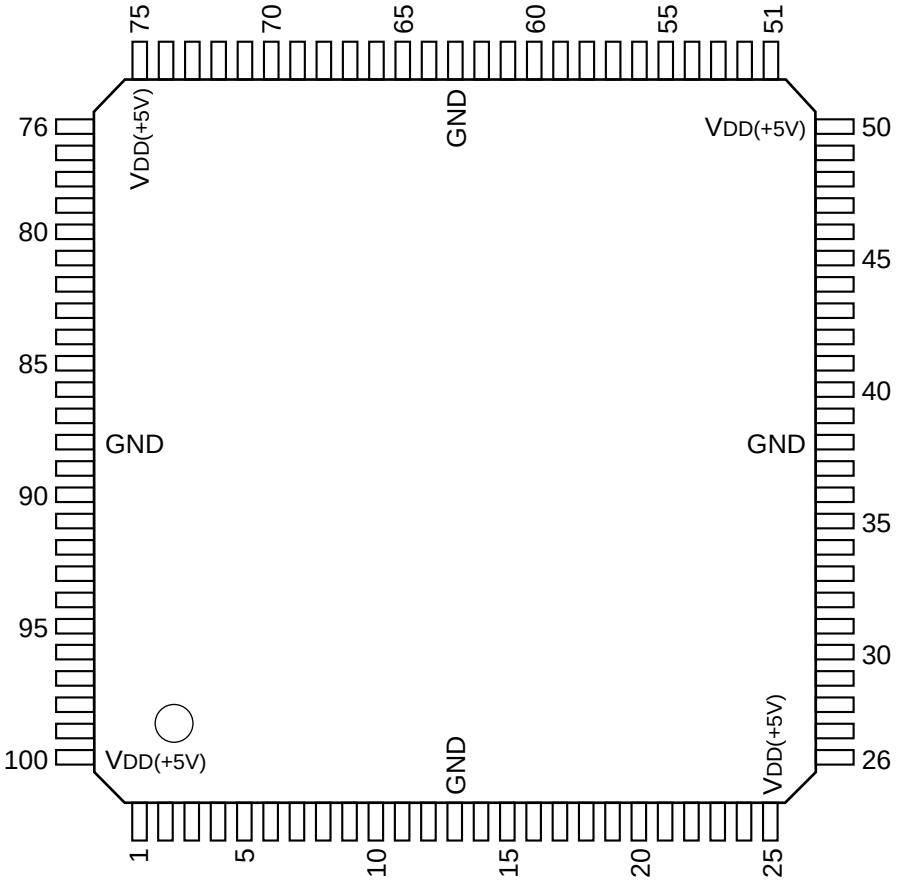
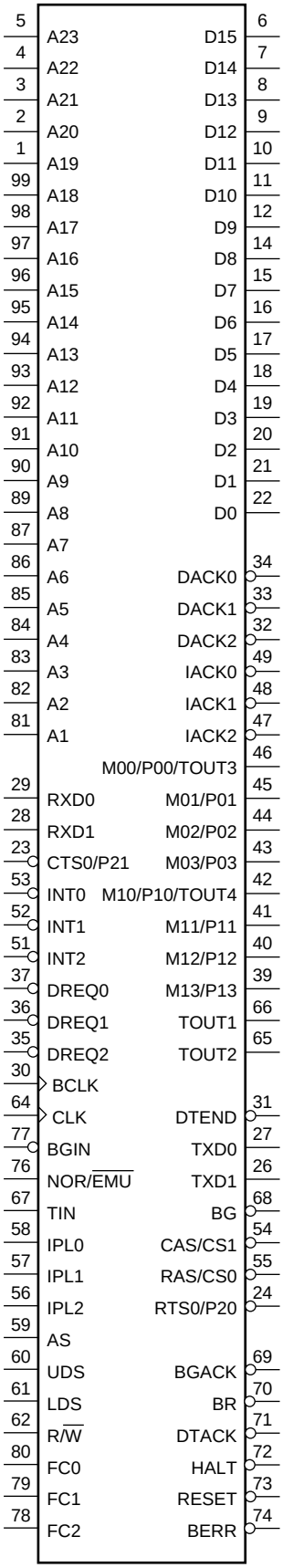
C-MOS 16-BIT MICRO PROCESSOR

—TOP VIEW—



(V_{DD} = +5 V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I/O	A19	21	I/O	D1	41	I/O	M11/P11	61	I/O	$\overline{LDS}$	81	I/O	A1
2	I/O	A20	22	I/O	D0	42	I/O	M10/P10/ TOUT4	62	I/O	R/$\overline{W}$	82	I/O	A2
3	I/O	A21	23	I/O	$\overline{CTS0}$/P21				63	—	GND	83	I/O	A3
4	I/O	A22	24	I/O	$\overline{RTS0}$/P20	43	I/O	M03/P03	64	I	CLK	84	I/O	A4
5	I/O	A23	25	—	V_{DD}	44	I/O	M02/P02	65	O	TOUT2	85	I/O	A5
6	I/O	D15	26	O	TXD1	45	I/O	M01/P01	66	O	TOUT1	86	I/O	A6
7	I/O	D14	27	O	TXD0	46	I/O	M00/P00/ TOUT3	67	I	TIN	87	I/O	A7
8	I/O	D13	28	I	RXD1	47	O	$\overline{IACK2}$	68	O	$\overline{BG}$	88	—	GND
9	I/O	D12	29	I	RXD0	48	O	$\overline{IACK1}$	69	I/O	$\overline{BGACK}$	89	I/O	A8
10	I/O	D11	30	I	BCLK	49	O	$\overline{IACK0}$	70	I/O	$\overline{BR}$	90	I/O	A9
11	I/O	D10	31	I/O	$\overline{DTEND}$	50	—	VDD	71	I/O	$\overline{DTACK}$	91	I/O	A10
12	I/O	D9	32	O	$\overline{DACK2}$	51	I	INT2	72	I/O	$\overline{HALT}$	92	I/O	A11
13	—	GND	33	O	$\overline{DACK1}$	52	I	INT1	73	I/O	$\overline{RESET}$	93	I/O	A12
14	I/O	D8	34	O	$\overline{DACK0}$	53	I	INT0	74	I/O	$\overline{BERR}$	94	I/O	A13
15	I/O	D7	35	I	$\overline{DREQ2}$	54	O	$\overline{CAS}$/$\overline{CS1}$	75	—	V_{DD}	95	I/O	A14
16	I/O	D6	36	I	$\overline{DREQ1}$	55	O	$\overline{RAS}$/$\overline{CS0}$	76	I	NOR/$\overline{EMU}$	96	I/O	A15
17	I/O	D5	37	I	$\overline{DREQ0}$	56	I/O	$\overline{IPL2}$	77	I	$\overline{BGIN}$	97	I/O	A16
18	I/O	D4	38	—	GND	57	I/O	$\overline{IPL1}$	78	I/O	FC2	98	I/O	A17
19	I/O	D3	39	I/O	M13/P13	58	I/O	$\overline{IPL0}$	79	I/O	FC1	99	I/O	A18
20	I/O	D2	40	I/O	M12/P12	59	I/O	$\overline{AS}$	80	I/O	FC0	100	—	V_{DD}
						60	I/O	$\overline{UDS}$						



INPUT

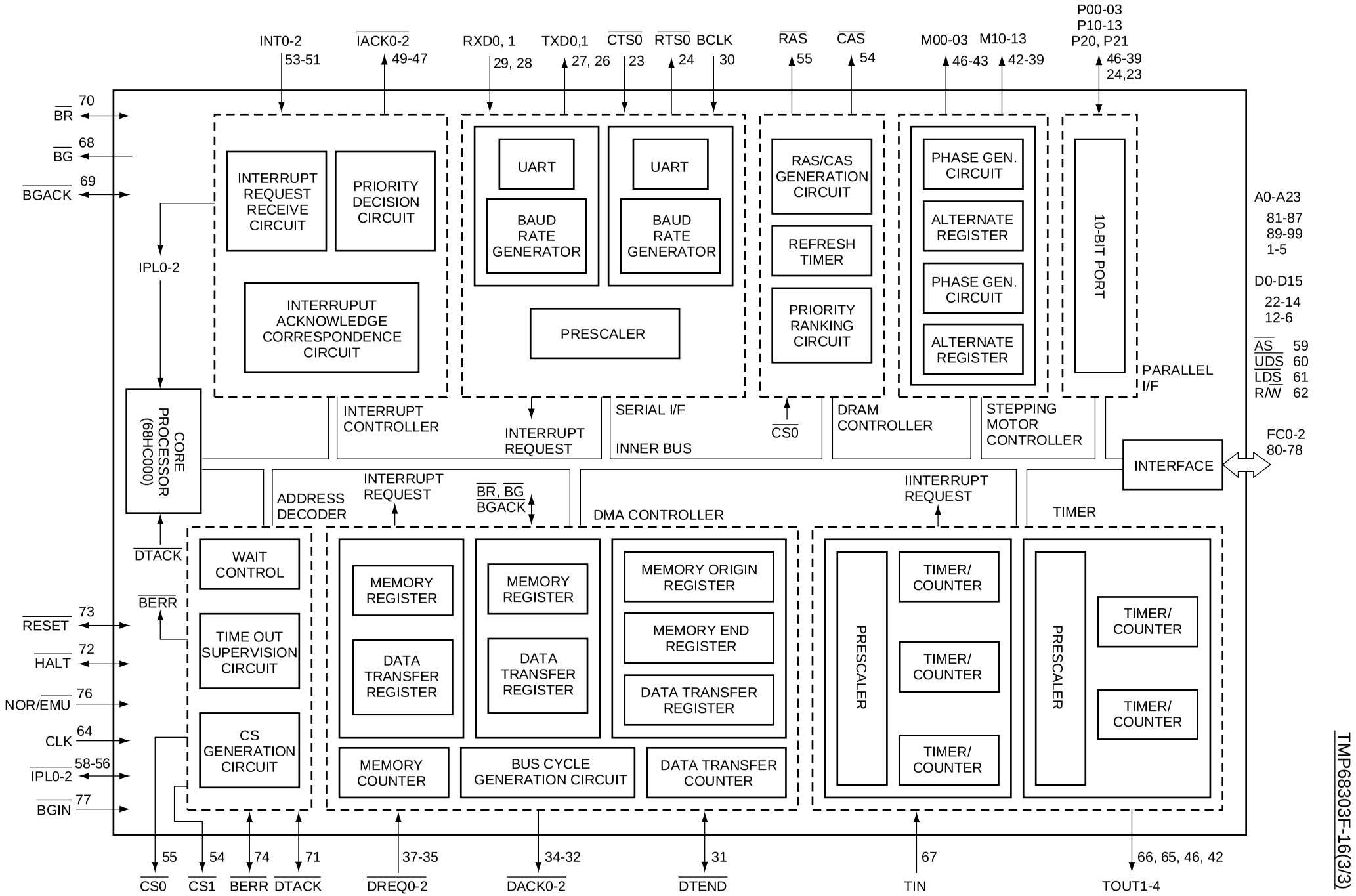
BCLK	;	BAUD RATE CLOCK
BGIN	;	BUS GRANT
CLK	;	CLOCK
CTS0	;	CLEAR TO SEND
DREQ0 - 2	;	DMA REQUESTS
INT0 - 2	;	INTERRUPT REQUESTS
NOR/EMU	;	MODE SELECT
RXD0, 1	;	RECEIVE SERIAL DATA
TIN	;	TIMER INPUT

OUTPUT

BG	;	BUS GRANT
CAS	;	COLUMN ADDRESS STROBE
CS0, 1	;	CHIP SELECTS
DACK0 - 2	;	DMA ACKNOWLEDGE
IACK0 - 2	;	INTERRUPT ACKNOWLEDGE
M00 - 03, 10 - 13	;	MOTOR CONTROL
RTS0	;	REQUEST TO SEND
RAS	;	ROW ADDRESS STROBE
TOUT1 - 4	;	TIMER OUTPUTS
TXD0, 1	;	TRANSFER SERIAL DATA

INPUT/OUTPUT

A1 - 23	;	ADDRESS BUS
AS	;	ADDRESS STROBE
BERR	;	BUS ERROR
BGACK	;	BUS GRANT ACKNOWLEDGE
BR	;	BUS REQUEST
D0 - 15	;	DATA BUS
DTACK	;	DATA TRANSFER ACKNOWLEDGE
DTEND	;	DMA FORCED END / TRANSFER END
FC0 - 2	;	FUNCTION CORDS
HALT	;	HALT
IPL0 - 2	;	INTERRUPT CONTROLS
LDS	;	LOWER DATA STROBE
P00 - 03	;	PORT 0
P10 - 13	;	PORT 1
P20, 21	;	PORT 2
RESET	;	RESET
R/W	;	READ/WRITE
UDS	;	UPPER DATA STROBE



TMP68303F-16(3/3)