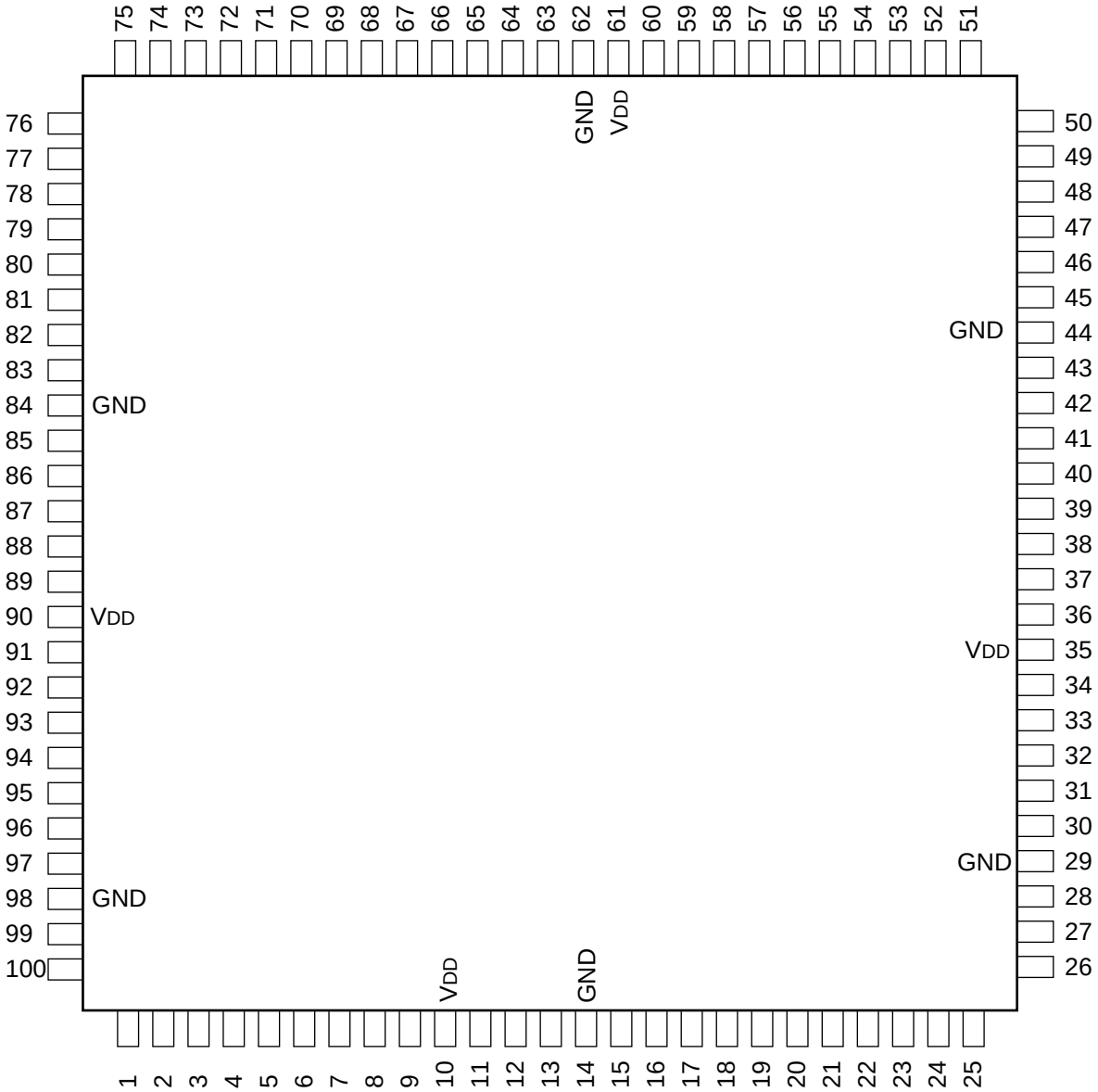
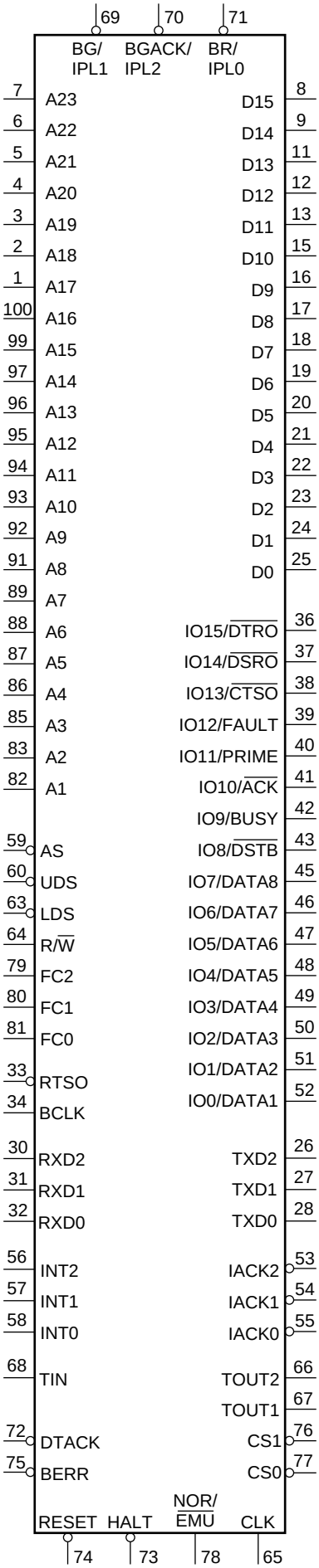
-TOP VIEW-



(V_{DD} = +5.0V)



INPUT

BCLK	;	BAUD RATE CLOCK
$\overline{\text{BERR}}$	;	BUS ERROR
CLK	;	CLOCK
$\overline{\text{DTACK}}$	;	DATA TRANSFER ACKNOWLEDGE
INT0-2	;	INTERRUPT REQUESTS
NOR/$\overline{\text{EMU}}$	;	MODE SELECT
RXD0-2	;	RECEIVE DATA
TIN	;	TIMER INPUT

OUTPUT

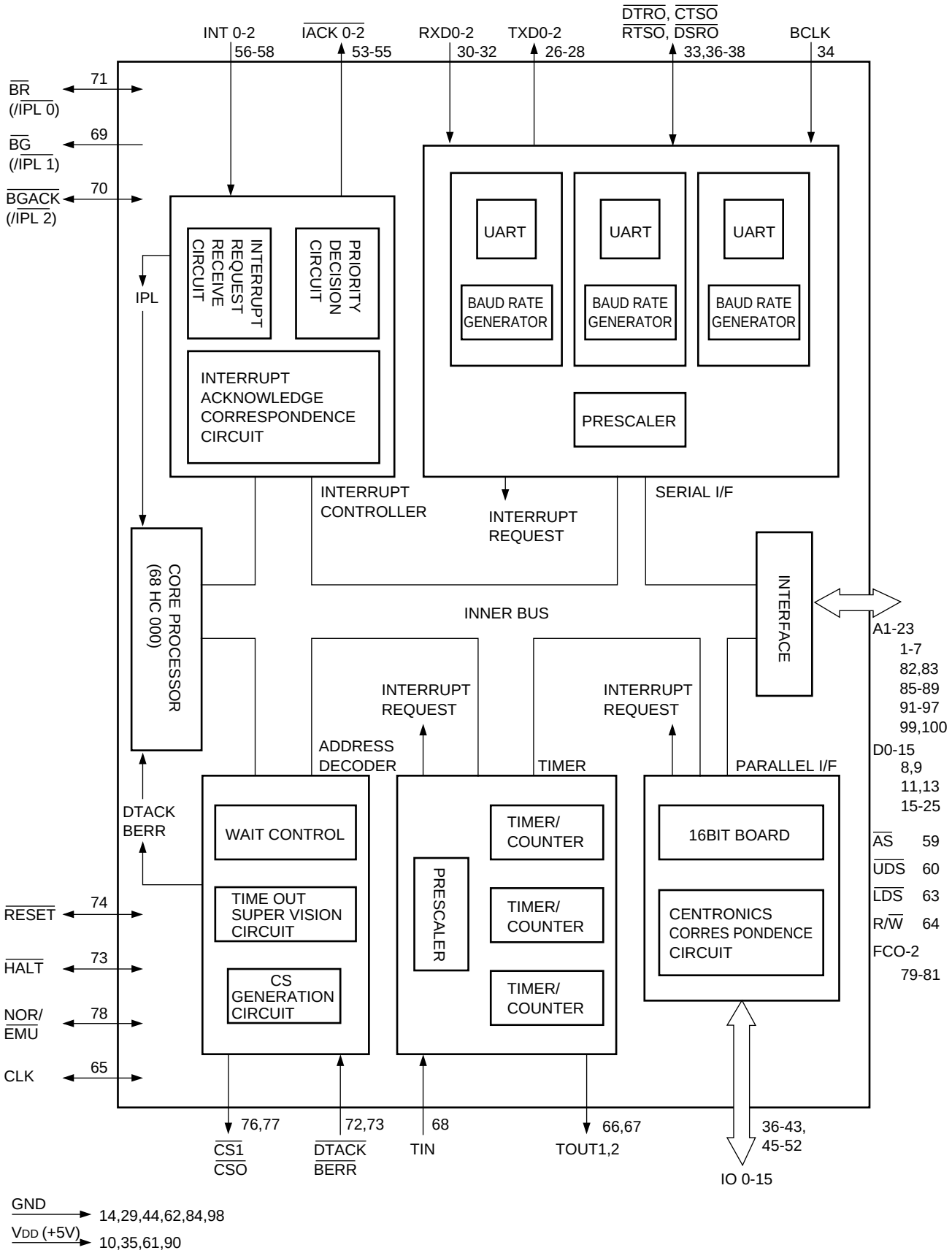
$\overline{\text{BG}}$(/$\overline{\text{IPL1}}$)	;	BUS GROUND
$\overline{\text{CS0,1}}$	;	CHIP SELECTS
$\overline{\text{IACK0-2}}$	;	INTERRUPT ACKNOWLEDGE
TOUT1,2	;	TIMER OUTPUTS
TXD0-2	;	TRANSFER DATA

INPUT/OUTPUT

A1-23	;	ADDRESS BUS
$\overline{\text{ACK}}$	;	I/O PORT
$\overline{\text{AS}}$	;	ADDRESS STROBE
$\overline{\text{BGACK}}$(/$\overline{\text{IPL2}}$)	;	BUS GROUND ACKNOWLEDGE
$\overline{\text{BR}}$(/$\overline{\text{IPL0}}$)	;	BUS REQUEST
BUSY	;	I/O PORT
$\overline{\text{CTSO}}$,$\overline{\text{DSRO}}$,$\overline{\text{DTRO}}$,$\overline{\text{DSTB}}$	;	I/O PORTS
D0-15	;	DATA BUS
DATA1-8	;	I/O PORTS
FAULT	;	I/O PORT
FC0-2	;	FUNCTION CORDS
$\overline{\text{HALT}}$	;	HALT
IO0-15	;	I/O PORT
$\overline{\text{LDS}}$	;	LOWER DATA STROBE
PRIME	;	I/O PORT
$\overline{\text{RESET}}$	;	RESET
$\overline{\text{RTSO}}$	;	TRANSFER REQUEST
R/$\overline{\text{W}}$	;	READ/WRITE
$\overline{\text{UDS}}$	;	UPPER DATA STROBE

(V_{DD} = +5.0V)

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	I/O	A17	26	O	TXD2	51	I/O	IO1/DATA2	76	O	$\overline{CS1}$
2	I/O	A18	27	O	TXD1	52	I/O	IO0/DATA1	77	O	$\overline{CS0}$
3	I/O	A19	28	O	TXD0	53	O	$\overline{IACK2}$	78	I	NOR/$\overline{EMU}$
4	I/O	A20	29	—	GND	54	O	$\overline{IACK1}$	79	I/O	FC2
5	I/O	A21	30	I	RXD2	55	O	$\overline{IACK0}$	80	I/O	FC1
6	I/O	A22	31	I	RXD1	56	I	INT2	81	I/O	FC0
7	I/O	A23	32	I	RXD0	57	I	INT1	82	I/O	A1
8	I/O	D15	33	I/O	$\overline{RTSO}$	58	I	INT0	83	I/O	A2
9	I/O	D14	34	I	BCLK	59	I/O	$\overline{AS}$	84	—	GND
10	—	V_{DD} (+5.0V)	35	—	V_{DD} (+5.0V)	60	I/O	$\overline{UDS}$	85	I/O	A3
11	I/O	D13	36	I/O	IO15/$\overline{DTRO}$	61	—	V_{DD} (+5.0V)	86	I/O	A4
12	I/O	D12	37	I/O	IO14/$\overline{DSRO}$	62	—	GND	87	I/O	A5
13	I/O	D11	38	I/O	IO13/$\overline{CTSO}$	63	I/O	$\overline{LDS}$	88	I/O	A6
14	—	GND	39	I/O	IO12/FAULT	64	I/O	R/$\overline{W}$	89	I/O	A7
15	I/O	D10	40	I/O	IO11/PRIME	65	I	CLK	90	—	V_{DD} (+5.0V)
16	I/O	D9	41	I/O	IO10/$\overline{ACK}$	66	O	TOUT2	91	I/O	A8
17	I/O	D8	42	I/O	IO9/BUSY	67	O	TOUT1	92	I/O	A9
18	I/O	D7	43	I/O	IO8/$\overline{DSTB}$	68	I	TIN	93	I/O	A10
19	I/O	D6	44	—	GND	69	O	$\overline{BG}$/$\overline{IPL1}$	94	I/O	A11
20	I/O	D5	45	I/O	IO7/DATA8	70	I/O	$\overline{BGACK}$/$\overline{IPL2}$	95	I/O	A12
21	I/O	D4	46	I/O	IO6/DATA7	71	I/O	$\overline{BR}$/$\overline{IPL0}$	96	I/O	A13
22	I/O	D3	47	I/O	IO5/DATA6	72	I	$\overline{DTACK}$	97	I/O	A14
23	I/O	D2	48	I/O	IO4/DATA5	73	I/O	$\overline{HALT}$	98	—	GND
24	I/O	D1	49	I/O	IO3/DATA4	74	I/O	$\overline{RESET}$	99	I/O	A15
25	I/O	D0	50	I/O	IO2/DATA3	75	I	$\overline{BERR}$	100	I/O	A16


INT 0-2
56-58
IACK 0-2
53-55
RXD0-2
30-32
TXD0-2
26-28
DTRO, CTSO
RTSO, DSRO
33,36-38
BCLK
34
BR
(/IPL 0)
71
BG
(/IPL 1)
69
BGACK
(/IPL 2)
70
IPL
INTERRUPT REQUEST RECEIVE CIRCUIT
PRIORITY DECISION CIRCUIT
INTERRUPT ACKNOWLEDGE CORRESPONDENCE CIRCUIT
INTERRUPT CONTROLLER
UART
BAUD RATE GENERATOR
UART
BAUD RATE GENERATOR
UART
BAUD RATE GENERATOR
PRESCALER
SERIAL I/F
INTERRUPT REQUEST
CORE PROCESSOR (68 HC 000)
INNER BUS
INTERFACE
A1-23
1-7
82,83
85-89
91-97
99,100
D0-15
8,9
11,13
15-25
AS 59
UDS 60
LDS 63
R/W 64
FCO-2
79-81
INTERRUPT REQUEST
ADDRESS DECODER
INTERRUPT REQUEST
TIMER
PARALLEL I/F
DTACK
BERR
WAIT CONTROL
TIME OUT SUPER VISION CIRCUIT
CS GENERATION CIRCUIT
PRESCALER
TIMER/ COUNTER
TIMER/ COUNTER
TIMER/ COUNTER
16BIT BOARD
CENTRONICS CORRES PONDENCE CIRCUIT
RESET
74
HALT
73
NOR/ EMU
78
CLK
65
76,77
CS1
CSO
72,73
DTACK
BERR
68
TIN
66,67
TOUT1,2
36-43,
45-52
IO 0-15
GND
14,29,44,62,84,98
VDD (+5V)
10,35,61,90