CMOS 4-BIT MICROCONTROLLER

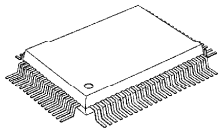
TMP47C647F, TMP47C847F

The 47C647/847 are high speed and high performance 4-bit single chip microcomputers based on the TLCS-470 series with a LCD driver, A/D converter and the pulse output circuit used for drive of the buzzer and so on. The 47C647/847 is possible to stop the CPU at the standby period and decrease the power consumption in the Home electric appliance.

PART No.	ROM	RAM	PACKAGE	EPROM
TMP47C647F	6144 × 8-bit	384 × 4-bit	QFP80-P-1420-0.80B	TMP47P847VF
TMP47C847F	8192 × 8-bit	512 × 4-bit		

FEATURES

QFP80-P-1420-0.80B



TMP47C647F
TMP47C847F
TMP47P847VF

◆4-bit signal chip mocrocomputer
◆Instruction execution time:
1.3 μs (at 6 MHz), 244 μs (at 32.8 kHz)
◆92 basic instrutions
- Table look-up instructions
- 5-bit to 8-bit data conversion instruction

◆Subroutine nesting: 15 levels max.
◆6 interrupt sources (External: 2, Internal: 4)
All sources have independent latchs each, and multiple interrupt control is available.
◆I/O port (35 pins)
- Input 2 ports 5 pins
- Output 2 ports 8 pins
- I/O 6 ports 22 pins

◆Interval Timer
◆Two 12-bit Timer/Counters
Timer, event counter, and pulse width measurement mode
◆Watchdog Timer
◆Serial Interface with 8-bit buffer
- Simutltaneous transmission and reception is available.
- External/internal clock, leading/trailing edge, and 4/8-bit mode

◆8-bit successive approximate type A/D converter
- With sample and hold
- 8 analog inputs
- Conversion time : 32 μs (at 6 MHz)

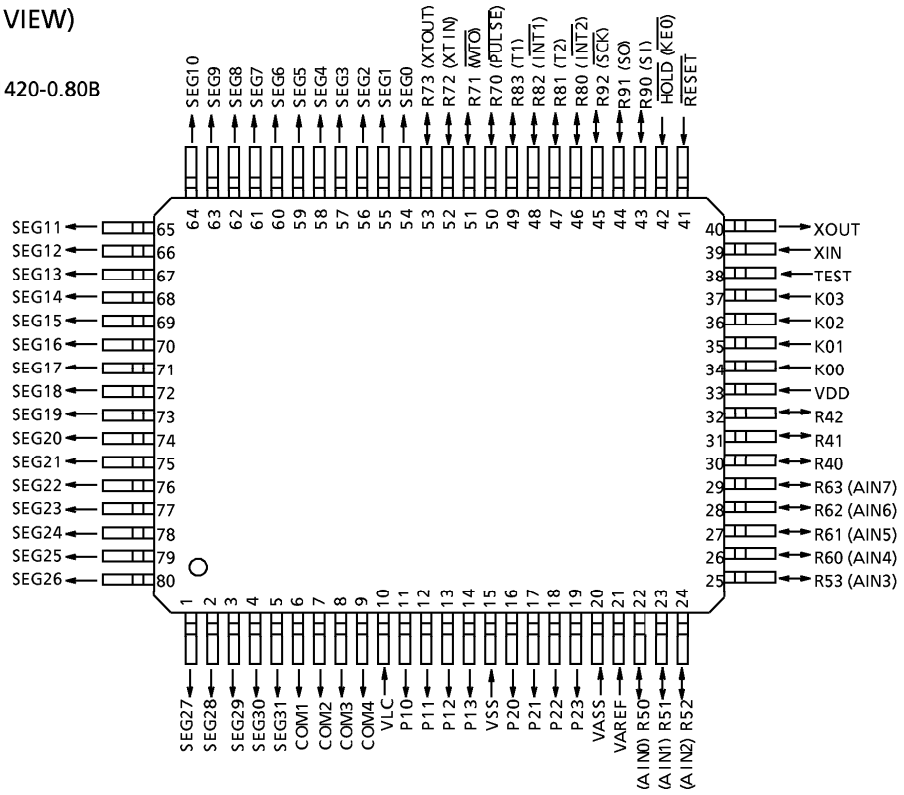
◆Pluse Output
Output frequency select
◆High current outputs
LED direct drive is available (typ. 10 mA × 8 bits)
◆LCD driver
- LCD direct drive is available (max. 12-digit display at 1/4 duty LCD)
- 1/4, 1/3, 1/2 duties or static drive are programmably selectable.

◆Dual-clock operation
High-speed/Low-power-consumption operating mode
◆Hold function
Battery/Capacitor back-up
◆SLEEP function
- Battery/Capacitor back-up
- LCD is displaying

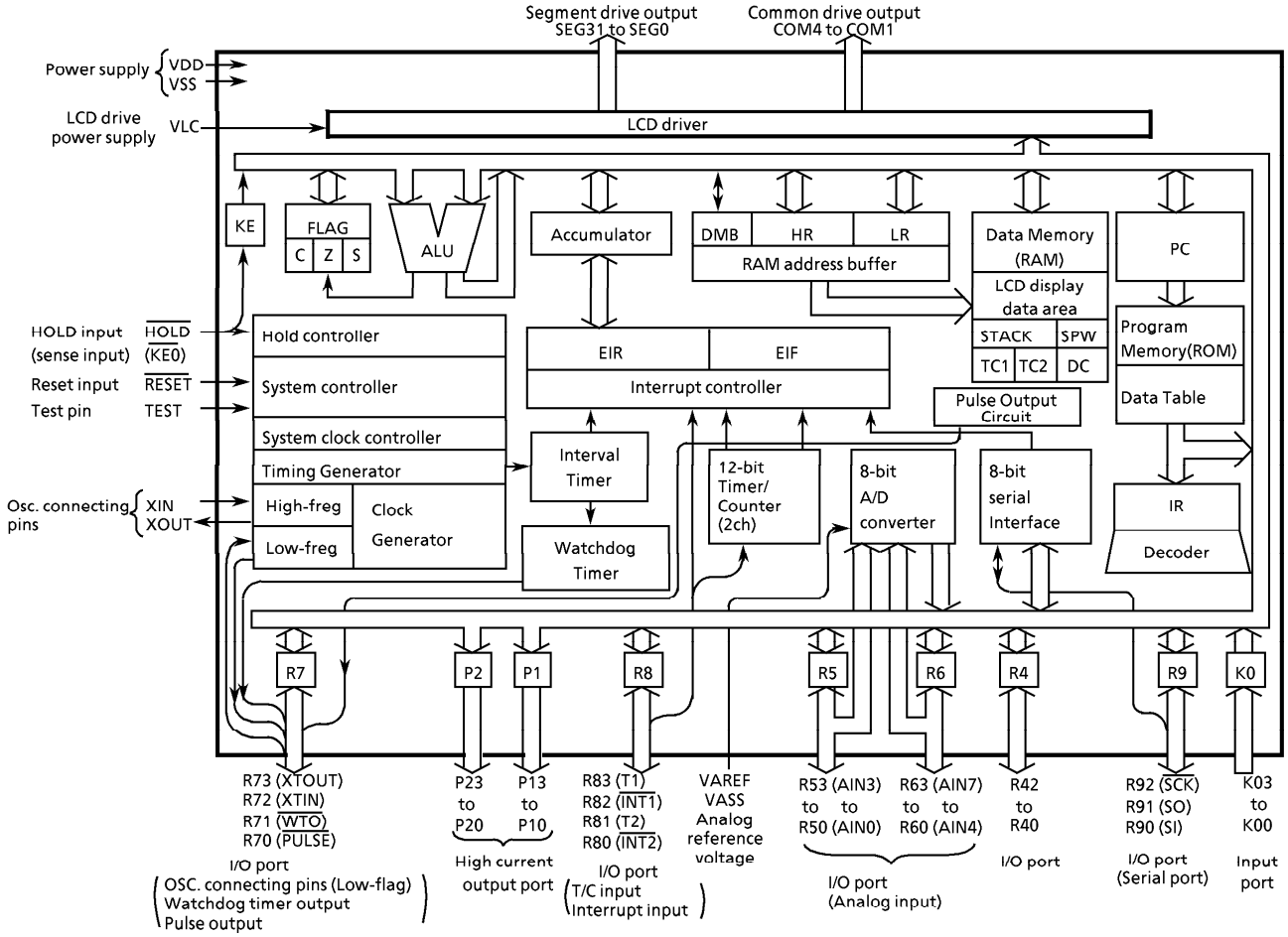
◆Real Time Emulator : BM47C847F0A

PIN ASSIGNMENTS (TOP VIEW)

QFP80-P-1420-0.80B



BLOCK DIAGRAM



PIN FUNCTION

PIN NAME	Input/Output	FUNCTIONS	
K03 to K00	Input	4-bit input port	
P13 to P10	Output	4-bit output port with latch. 8-bit data are output by the 5-bit to 8-bit data conversion instruction [OUTB @HL].	
P23 to P20			
P42 to P40	I/O	3-bit I/O port with latch When used as input port, the latch must be set to "1".	
R63 (AIN7) to R50 (AIN0)	I/O (Input)	4-bit I/O port with latch. When used as input port, the latch must be set to "1".	A/D converter analog input
R73 (XTOUT)	I/O (Output)	4-bit I/O port with latch. When used as input port, watchdog timer output, the latch must be set to "1".	Resonator connecting pin (Low-freq.). For inputting external clock, XTIN is used and XTOUT is opened.
R72 (XTIN)	I/O (Input)		
R71 ($\overline{WTO}$)	I/O (Output)		Watchdog timer output
R70 ($\overline{PULSE}$)	I/O (Output)		Pulse output
R83 (T1)	I/O (Input)	4-bit I/O port with latch. When used as input port, external interrupt input pin, or timer/counter external input pin, the latch must be set to "1".	Timer/Counter 1 external input
R82 ($\overline{INT1}$)			External interrpt 1 input
R81 (T2)			Timer/Counter 2 external input
R80 ($\overline{INT2}$)			External interrpt 2 input
R92 ($\overline{SCK}$)	I/O(I/O)	3-bit I/O port with latch. When used as input port or serial port, the latch must be set to "1".	Serial clock I/O
R91 (SO)	I/O (Output)		Serial data output
R90 (SI)	I/O (Input)		Serial data input
SEG31 to SEG0	Output	LCD Segment drive output	
COM4 to COM1		LCD Common drive output	
XIN	Input	Resonator connecting pin (High-frequency) . For inputting external clock, XIN is used and XOUT is opened.	
XOUT	Output		
$\overline{RESET}$	Input	Reset signal input	
$\overline{HOLD}$ ($\overline{KE0}$)	Input (Input)	HOLD request/release signal input	Sence input
TEST	Input	Test pin for out-going test. Be opened or fixed to low level.	
VDD	Power supply	+ 5 V	
VSS		0V (GND)	
VLC		LCD drive power supply	
VAREF		A/D converter analog reference voltage (High)	
VASS		A/D converter analog reference voltage (Low)	

OPERATIONAL DESCRIPTION

Concerning the 47C647/847 the configuration and functions of hardwares are described. As the description has been provided with priority on those parts differing from the 47C660/860, the technical data sheets for the 47C660/860 shall also be referred to.

1. SYSTEM CONFIGURATION

◆ INTERNAL CPU FUNCTION

Except for the system control circuit, the CPU core functions are the same as those of the 47C660/860.

◆ PERIPHERAL HARDWARE FUNCTION

① I/O Ports
② Interval Timer
③ Timer/Counter
④ Watchdog Timer
⑤ Pulse Output
⑥ LCD Driver
⑦ A/D Converter
⑧ Serial Interface

The following are explanations of functions (①, ⑤, ⑥ and ⑦) which have been added to the 47C647/847 or which are different from those of the 47C660/860, and the system clock control circuit.

2. CPU CORE FUNCTIONS

2.1 SYSTEM CONTROL CIRCUIT

It is possible to switch from SLOW operating mode to SLEEP operating mode which maintains the internal status under low power consumption, and also to HOLD operating mode which reduces power consumption. In SLEEP operating mode, all operations except a timing generator (TG) binary counter and a LCD driver are suspended.

2.1.1 System Clock Controller

The system clock controller starts or stops the high-frequency and low-frequency clock oscillator and switches between the basic clocks. The operating mode is generally divided into the single-clock mode and the dual-clock mode, which are controlled by command.

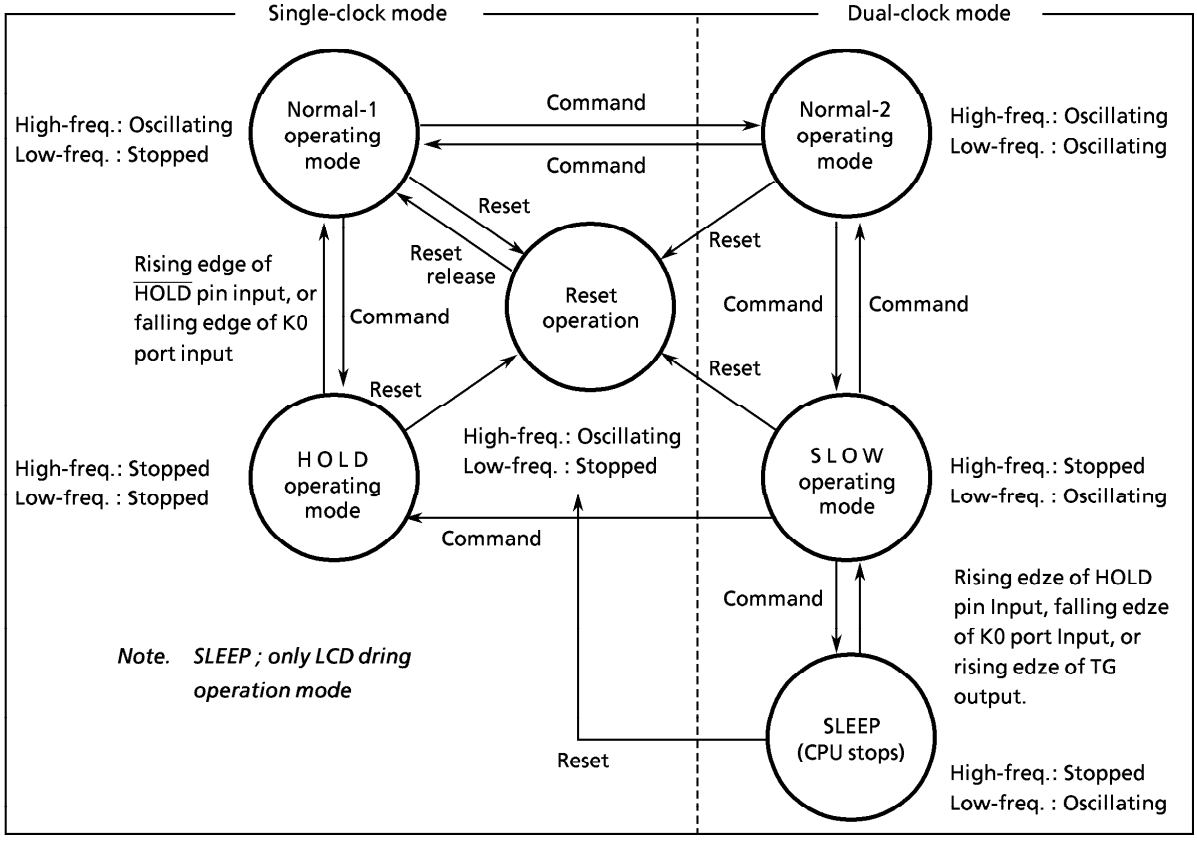


Figure 2-1. Operating Mode Transition Diagram

(1) System clock control

System clock control is performed by the command register (OP16). During reset, this register is initialized to "0" and the single-clock mode is selected. Each state at operating mode switching can be read from the status register (IP0E).

System clock control command register
(Port address OP16) (Initial value 0000)

3	2	1	0
DCLK3	SLCK	DCLK1	DWUT

DCLK3 / DCLK1	Selects operation mode	(Note2)

0 0 : Single clock mode (Normal-1 operation mode)
0 1 : Reserved
1 0 : Dual clock mode (Normal-2 operation mode)
1 1 : Dual clock mode (SLOW operation mode)

SLCK	Selects input clock for the interval timer	(Note3)

0 : $fc / 2^7$ [Hz]
1 : fs

DWUT	Sets the warm-up time	(Note4)

Example At fc = 4.19 MHz
fs = 32.8 kHz

0 : $2^8 / fs + 2^9 / fc$ [s] …… 7.9 [ms]
1 : $2^{11} / fs + 2^9 / fc$ …… 62.6

System clock control command register
(Port address IP0E)

3	2	1	0
(SIOF)	(SEF)	SMF	HOLD/SLS

SMF	Low-frequency clock oscillating state

Status of binary counter
(output of the seventeenth stage of TG)

HOLD / SLS	$\overline{HOLD}$ pin state/operation state monitor

	Single clock mode	Dual clock mode
0 :	$\overline{HOLD}$ pin at "H" level	In normal operation
1 :	$\overline{HOLD}$ pin at "L" level	In SLOW operation

Note 1. fc ; High-frequency clock [Hz]
fs ; High-frequency clock [Hz]
Note 2. Note that the configuration of bits.
Note 3. Only Normal-2 operation mode
Note 4. Only switching from SLOW to Normal-2

Figure 2-2. System Clock Control Command Register / Status Register

(2) Instruction cycle

The instruction execution and on-chip peripheral hardware operations are performed in synchronization with the basic clock. The smallest unit of instruction execution is called the "instruction cycle". The TLCS-470 series instruction set has 3 kinds of instructions, 1-cycle instruction to 3-cycle instruction. Each instruction cycle consists of 4 states (S1 through S4). Each state consists of 2 basic clock pulses.

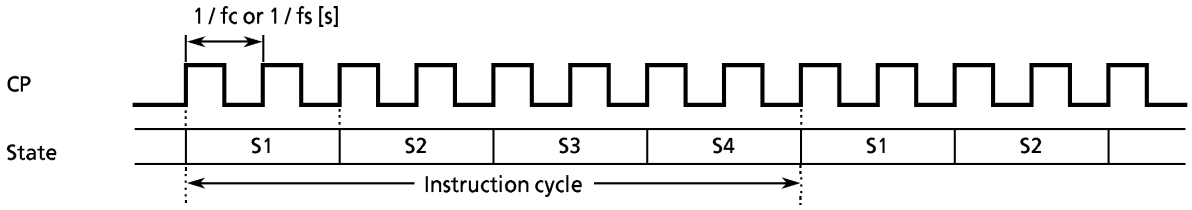


Figure 2-3. Instruction Cycle

2.1.2 Operating Mode

There are two operating mode: the single-clock and the Dual-clock mode.

(1) Dual-clock mode

In this mode, the Normal-2 operation is generally performed by generating the instruction cycle from the high-frequency clock (fc). As required, the instruction cycle is generated by the low-frequency clock (fs), and the lower consumption power operation is performed by transferring SLOW operation to HOLD operation. The following describes the switching between the Normal-2, SLOW and HOLD operations in the dual clock mode. At reset, the command register is initialized to the single-clock mode. Since the low-frequency clock is not oscillated, Normal-2 operation in the dual clock mode must be set first. The low frequency clock starts oscillating by transferring to Normal-2 operation.

a. Switching from Normal-2 operation to SLOW operation

Setting DCLK1 (bit 1 of OP16) to "1" switches Normal-2 operation to SLOW operation. However it takes a few seconds to get a stable oscillation of the low-frequency clock. Therefore if there is possible to switch from Normal-2 operation to SLOW operation, wait until the low-frequency clock is stable or check the oscillation state by a program. SMF status (bit 1 of 1P0E) is available to check it.

When the high-frequency clock ($fc/2^7$) is input to the 8th stage of TG, first sets SLCK (bit 2 of OP16) to "1" and input the low-frequency clock (fs). Then, SMF is monitored by a program. After confirming that SMF is changed "1" to "0" to "1" or "0" to "1" to "0", set DCLK1 to "1". At this time, the high-frequency clock oscillator stops.

b. Returning from SLOW operation to Normal-2 operation

Bit 1 of the command register is cleared to "0" and, at the same time,the warm-up time for return is set to DWUT. When the warm-up time has passed, the Normal-2 operation takes place. By monitoring SLS (bit 0 of the status register), the current operating mode can be known.

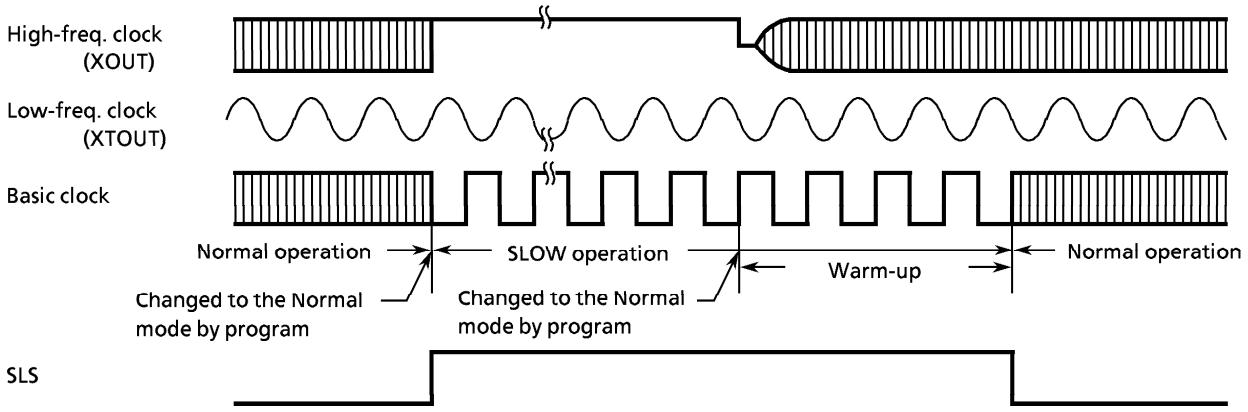


Figure 2-4. System Clock Switching Timing

c. Shifting from the SLOW operation to the HOLD operation

By setting the command in the command register (OP10), the low-frequency clock oscillation stops and the HOLD operation starts.

After being released the HOLD operation, the operation mode is NORMAL-1.

d. Shifting from the SLOW operation to the SLEEP operation

After selecting the return conditions using the return conditions selection register (OP17), shift to SLEEP operation (refer to the SLEEP operation mode explanation) by setting the command in the command register (OP10). Occurrence of the selected condition returns to SLOW operation.

Note1. The command register (OP10) is used for both HOLD operation control and SLEEP operation control. This register is used for HOLD operation control when accessed during Normal-1 operation and for SLEEP operation control when accessed during SLOW operation.

Note2. The SLOW operating mode can be switched to either the SLEEP or the HOLD mode, it is necessary to select which mode to be switched by the bit 7 of command register (OP17).

Note3. During SLOW operation and SLEEP operation, oscillation of the high-frequency clock is automatically halted to enable low power supply voltage operation and low power consumption operation. However, while less power is consumed by the oscillator and internal hardware, the amount of power consumed by the pin interface (dependent on external circuitry and programs) is not directly related to the low power consumption operation mode; therefore, caution is required during system design and interface circuit design. Also, the execution of instructions is not interrupted by switching to SLOW operation but, in some cases, there is influence on some of the peripheral hardware functions; therefore, refer to the explanations of the various operations.

(2) Single-clock mode

In this mode, only the high-frequency clock oscillator is used. Pins R72 (XTIN) and R73 (XTOUT) become the ordinary I/O port. The HOLD operating mode is available for reducing power consumption. It is controlled by the command register (OP10). In this mode,therefore, the system clock control command register (OP16) need not be manipulated.

2.1.3 SLEEP Operation Mode

The SLEEP operation mode suspends all SLOW operation operations except for the low-frequency clock, TG binary counter and LCD driver, and retains the internal status with low power consumption without stopping the clock function and LCD display.

SLEEP mode control
(Port address : OP10) (Initial value : ****)

3	2	1	0
SLPMS	1	1	1

SLPMS	Mode selection and SLEEP operation starts

0 : Starts SLEEP operation in edge sensitive release mode
1 : Starts SLEEP operation in level sensitive release mode
The other codes are reserved

Note 1. When Normal-1 and -2 mode is operated and SLPEN is set to 1, the SLEEP operation is not started.
Note 2. fs ; Low frequency clock [Hz].

Return conditions selection register
(Port address : OP17) (Initial value : 0000)

3	2	1	0
SLPEN	SWU		SK0IN

SLPEN	HOLD/SLEEP mode selection

0: Starts SLEEP operation mode
1: Starts HOLD operation mode

SWU	Return conditions selection

00: HOLD and K0 pin input
01: HOLD, K0 pin and fs/2^{15} [Hz] signal
1*: HOLD, K0 pin and fs/2^{9} [Hz] signal

SK0IN	Release HOLD/SLEEP by K0

0: Release disable by K0 pin input (Only HOLD valid)
1: Release enabled by K0 pin input (HOLD and K0 valid)

Figure 2-6. Command Register, Return Conditions Selection register

The operation in edge release mode and level release mode are the same as in HOLD operating mode. In order to start SLEEP operation, select the return condition by the selection register (OP17) during SLOW operation. Then, set the start command in the command register (OP10). In addition, SLEEP operation can be controlled by K0 pin input. This is also selected by the command register (OP17).
For switching from SLOW to HOLD or SLEEP operating mode, select the upper bit of Port address (OP17). SLEEP operation is then return to SLOW operation when the conditions selected with the return conditions selection register occur.

Example : Starting SLEEP operation using the HOLD and K0 pin input, and the 1 sec signal as return condition.

```
LD      A, #0DH      ; Selects HOLD, K0 pin input and 1 sec signal
OUT     A, %OP17
LD      A, #7H       ; Starts SLEEP operation
OUT     A, %OP10
```

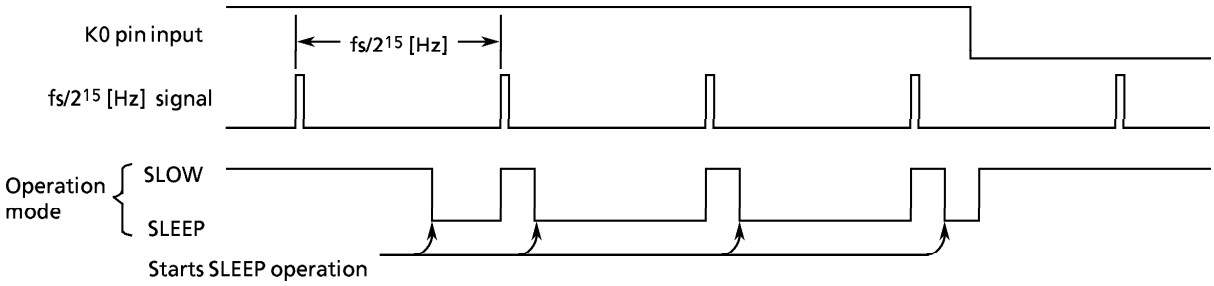


Figure 2-7. Return Conditions and operation Mode

2.1.4 HOLD Operation Mode

The HOLD feature stops the system and holds the systems internal states active before stop with a low power. The $\overline{\text{HOLD}}$ operation is controlled by the command register (OP10) and the $\overline{\text{HOLD}}$ pin input. The $\overline{\text{HOLD}}$ pin input state can be known by the status register (IP0E or IP10).

HOLD operating mode can be controlled by HOLD pin as well as by K0 port, selected by the command register (OP17). Figure 2.9 shows the connection between HOLD pin input and HOLD control signal.

HOLD operation mode command register
(Port address : OP10) (Initial value : *0**)

3	2	1	0
HLDMS		HWUT	

HLDMS	Mode select/HOLD operation start

01 : Starts HOLD operation in edge release mode
11 : Starts HOLD operation in level release mode
*0 : Reserved

HWUT	Warm-up time selection

Example: At fc = 4 MHz

00 : 2^{18} / fc [s] ····· 65.5 [ms]
01 : 2^{14} / fc ····· 4.1
10 : Reserved
11 : 2^{6} / fc ····· 0.016

HOLD operation mode status register
(Port address IP0E)

3	2	1	0
(SIOF)	(SEF)	(SMF)	HOLD (KE0)

(Port address IP10)

3	2	1	0
HOLD (K103)			

HOLD	$\overline{\text{HOLD}}$ pin input state

0 : $\overline{\text{HOLD}}$ pin is high
1 : $\overline{\text{HOLD}}$ pin is low (HOLD operation request)

(Note 1) * ; don't care

Figure 2-8. HOLD Operation Mode Command Register/Status Register

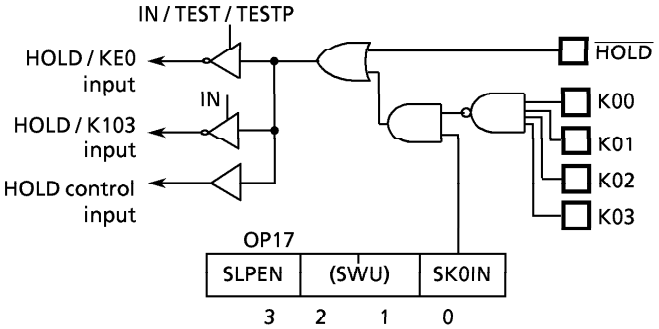


Figure 2-9. $\overline{\text{HOLD}}$ Pin Input and $\overline{\text{HOLD}}$ Control Signal

Return conditions selections register
(Port address : OP17) (Initial value : 0000)

3	2	1	0
(SLPEN)		(SWU)	SK0IN

SK0IN	Release HOLD/SLEEP by K0

0 : Release disabled by K0 pin input (Only HOLD valid)
1 : Release enabled by K0 pin input (HOLD and K0 valid)

Figure 2-10. Return Conditions Selection Command Register

Other than that, the HOLD operation mode is the same as for the 47C860. For details, refer to the 47C860 technical data.

3. PERIPHERAL HARDWARE FUNCTION

3.1 Input / Output Ports

The 47C647 / 847 have 10 built-in input/output ports as follows:

① K0 ; 4-bit input
② P1, P2 ; 4-bit output
③ R4 ; 3-bit input / output
④ R5, R6 ; 4-bit input / output (also used for A/D converter analog inputs)
⑤ R7 ; 4-bit input / output (also used for resonator connection, watchdog timer output, pulse output)
⑥ R8 ; 4-bit input / output (also used for external interrupt input, timer/counter input)
⑦ R9 ; 3-bit input / output (also used as a serial port)
⑧ KE ; 1-bit sense input (also used for hold request / release signal input)

This section describes ports of ③~⑤, ⑧ which are changed from 47C660/860. Table 3-1 lists the port address assignments and the I/O 'instructions that can access the ports.

(1) Port R4 (R42-R40)

These ports are 3-bit I/O ports with latch. The latch is initialized to "1" during reset.
When used as input port, the latch should be set to "1".

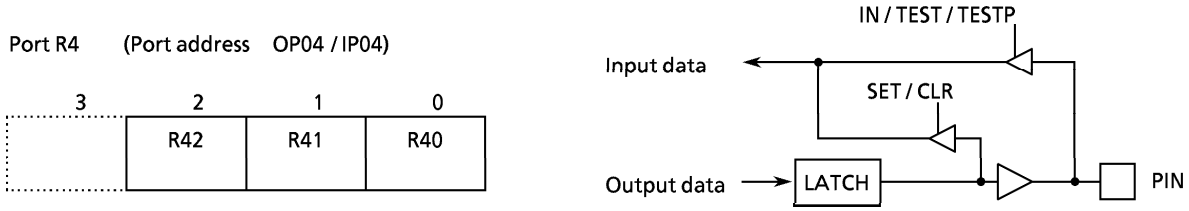


Figure 3-1. Port R4

(2) R5 (R53-R50), R6 (R63-R60)

These ports are 4-bit I/O ports with a latch. When used as an input port, the latch must be set to "1". The latch is initialized to "1" during reset.
Ports R5 and R6 are 4-bit I/O ports with latch shared by the analog inputs for A/D converter. When used as an input ports or analog inputs, the latch should be set to "1".
If other port is used as an output, be careful not to execute the output instruction for any port during A/D conversion in order to keep accuracy of conversion.
The latch is initialized to "1" and analog input is selected R50 (AIN0) pin during reset.

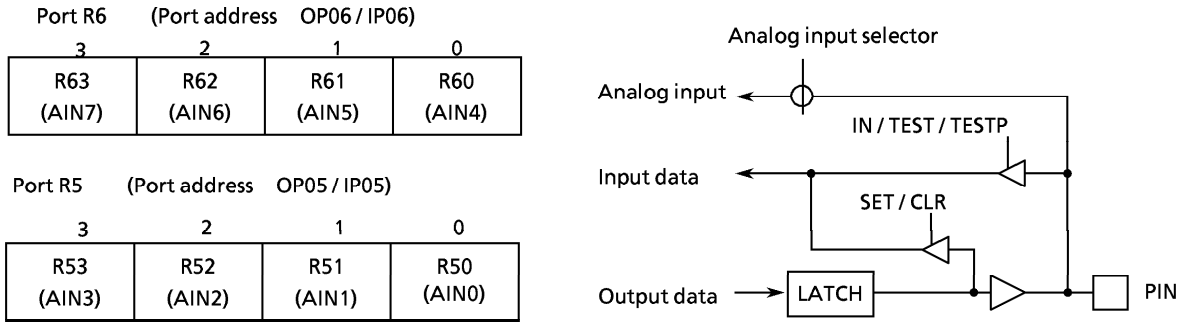


Figure 3-2. Ports R5, R6

(3) Port R7 (R73-R70)

Port R7 is shared by the low-frequency resonator connection pins (XTIN, XTOUT), pulse output pin ($\overline{PULSE}$) and the watchdog timer output pin ($\overline{WTO}$). For the dual-clock mode operation, the low-frequency resonator (32.768 kHz), is connected to R72 (XTIN) and R73 (XTOUT) pins. For the single-clock mode operation, R72 and R73 pins are used for the ordinary I/O ports. When the watchdog timer is used, R71 ($\overline{WTO}$) becomes the watchdog timer output pin.

The watchdog timer output is the logical AND output with the port R71 output latch. To use the R71 pin for an ordinary I/O port, the watchdog timer must be disabled (with the watchdog timer output set to "1"). When the pulse output is used, R70 ($\overline{PULSE}$) becomes the pulse output pin. The pulse output is the logical AND output with the port R70 output latch. To use the R70 pin for an ordinary I/O port, the pulse output must be disabled (with the pulse output set to "1").

Port R7 (Port address OP07/IP07)

3	2	1	0
R73 (XTOUT)	R72 (XTIN)	R71 ($\overline{WTO}$)	R70 ($\overline{PULSE}$)

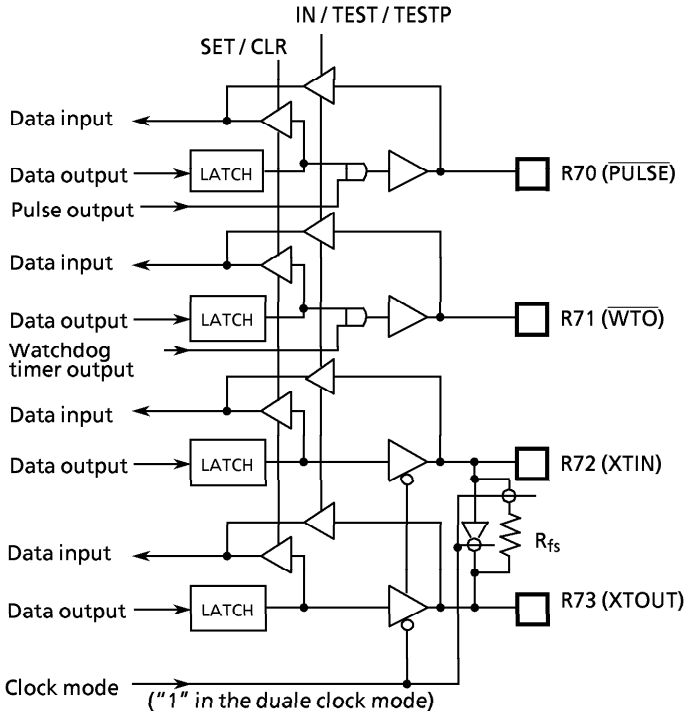


Figure 3-3. Port R7

(4) In the 47C647 and 847, the KE port functions as follows.

The logic arithmetic results of KE0 pin input and K0 port input are set into the least significant bit of IP0E and the most significant bit of IP10. For details, see HOLD operation mode in section 2.1.4.

Table 3-1. Port Address Assignments and Available I/O Instructions

Port address (**)	Port		Input/Output instruction						
	Input (IP**)	Output (OP**)	IN %p, A IN %p, @HL	OUT A, %p OUT @HL,%p	OUT #k, %p	OUTB @HL	SET %p, b CLR %p, b	TEST %p, b TESTP %p, b	SET @L CLR @L TEST @L
00_H	K0 input port	——	○	–	–	–	–	○	–
01	P1 output latch	P1 output port	○	○	○	○ (Note2)	○	○	–
02	P2 output latch	P2 output port	○	○	○		○	○	–
03	——	——	–	–	–	–	–	–	–
04	R4 input port	R4 output port	○	○	○	–	○	○	○
05	R5 input port (Analog input)	R5 output port	○	○	○	–	○	○	○
06	R6 input port (Analog input)	R6 output port	○	○	○	–	○	○	○
07	R7 input port	R7 output port (Pulse output)	○	○	○	–	○	○	○
08	R8 input port	R8 output port	○	○	○	–	○	○	–
09	R9 input port	R9 output port	○	○	○	–	○	○	–
0A	——	——	–	–	–	–	–	–	–
0B	——	——	–	–	–	–	–	–	–
0C	——	——	–	–	–	–	–	–	–
0D	——	——	–	–	–	–	–	–	–
0E	Status input (Note 3)	——	○	–	–	–	–	○	–
0F	Serial receive buffer	Serial transmit buffer	○	○	○	–	–	–	–
10_H	$\overline{HOLD}$ pin status	Hold/SLEEP operating mode control	○	○	–	–	–	–	–
11	——	——	–	–	–	–	–	–	–
12	A / D converted value	A / D analog input selector	○	○	–	–	–	–	–
13	A / D status input	A / D start register	○	○	–	–	–	–	–
14	——	——	–	–	–	–	–	–	–
15	——	Watchdog timer control	–	○	–	–	–	–	–
16	——	System clock control	–	○	–	–	–	–	–
17	——	Hold/SLEEP operation control	–	○	–	–	–	–	–
18	——	Pulse output control	–	○	–	–	–	–	–
19	——	Interval Timer interrupt control	–	○	–	–	–	–	–
1A	——	LCD driver control 1	–	○	–	–	–	–	–
1B	——	LCD driver control 2	–	○	–	–	–	–	–
1C	——	Timer/Counter 1 control	–	○	–	–	–	–	–
1D	——	Timer/Counter 2 control	–	○	–	–	–	–	–
1E	——	Serial interface control 1	–	○	–	–	–	–	–
1F	——	Serial interface control 2	–	○	–	–	–	–	–

Note 1 : "——" means the reserved state. Unavailable for the user programs.
Note 2 : The 5-bit to 8-bit data conversion instruction [OUTB @HL], automatic access to ports P1 and P2.
Note 3 : The status input of serial interface, clock generator, and $\overline{HOLD}$ ($\overline{KE0}$) pin.

3.2 Pulse output circuit

The 47C647/847 has a built-in one-channel pulse output to use in driving, for example, a buzzer. Eight different pulse output frequencies can be selected by command. Pulses are output from the PULSE pin. The PULSE pin is also used as the R70 pin. When used as the PULSE pin, the R70 output latch is set to "1".

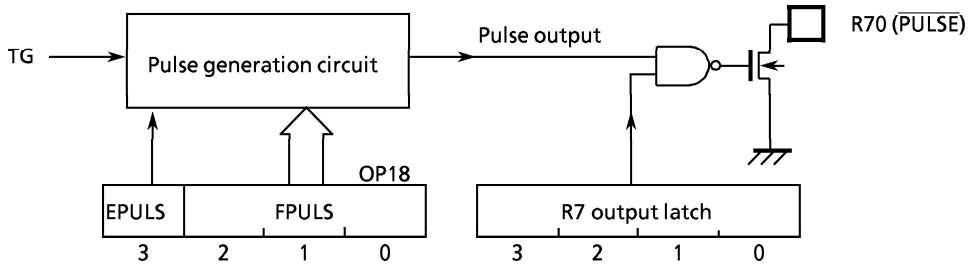


Figure 3-4. Pulse output circuit

3.2.1 Control of pulse output circuit

The pulse output circuit is controlled by the command register (OP18). Pulses are output by setting EPULS to "1". Pulse output is disabled (by clearing OP18 to"0") during hold operation.

Pulse output control command resister (Port address OP18)

3	2	1	0	
EPULS	FPULS			(Initial value 0000)

EPULS	Pulse output control
0 :	Disable
1 :	Enable

FPULS	Pulse output frequency select	Example:At fc = 4.19 MHz
000:	fc / (2^9 × 8) [Hz]	1.024 [kHz]
001:	fc / (2^9 × 7)	1.170
010:	fc / (2^9 × 6)	1.365
011:	fc / (2^9 × 5)	1.638
100:	fc / (2^9 × 4)	2.048
101:	fc / (2^9 × 3)	2.731
110:	fc / (2^9 × 2)	4.096
111:	fc / (2^9 × 1)	8.192

Note. fc : Basic clock frequency [Hz]

Figure 3-5. Pulse output command resister

3.3 LCD Driver

The 47C647/847 have the circuit that directly drives the liquid crystal display (LCD) and its control circuit.

The 47C647/847 have following connecting pins with LCD.

① Segment output port 32 pins (SEG31-SEG0)
② Common output port 4 pins (COM4-COM1)

In addition, VLC pin is provided as the drive power pin.

The devices that can be directly driven is selectable from LCD of following drive methods.

① 1 / 4 Duty (1 / 3 Bias) LCD …… Max. 128 Segment (16 disits × 8 segments)
② 1 / 3 Duty (1 / 3 Bias) LCD …… Max. 96 Segment (12 disits × 8 segments)
③ 1 / 3 Duty (1 / 2 Bias) LCD …… Max. 96 Segment (12 disits × 8 segments)
④ 1 / 2Duty (1 / 2 Bias) LCD …… Max. 64 Segment (8 disits × 8 segments)
⑤ Static LCD …… Max. 32 Segment (4 disits × 8 segments)

3.3.1 Configruation of LCD driver

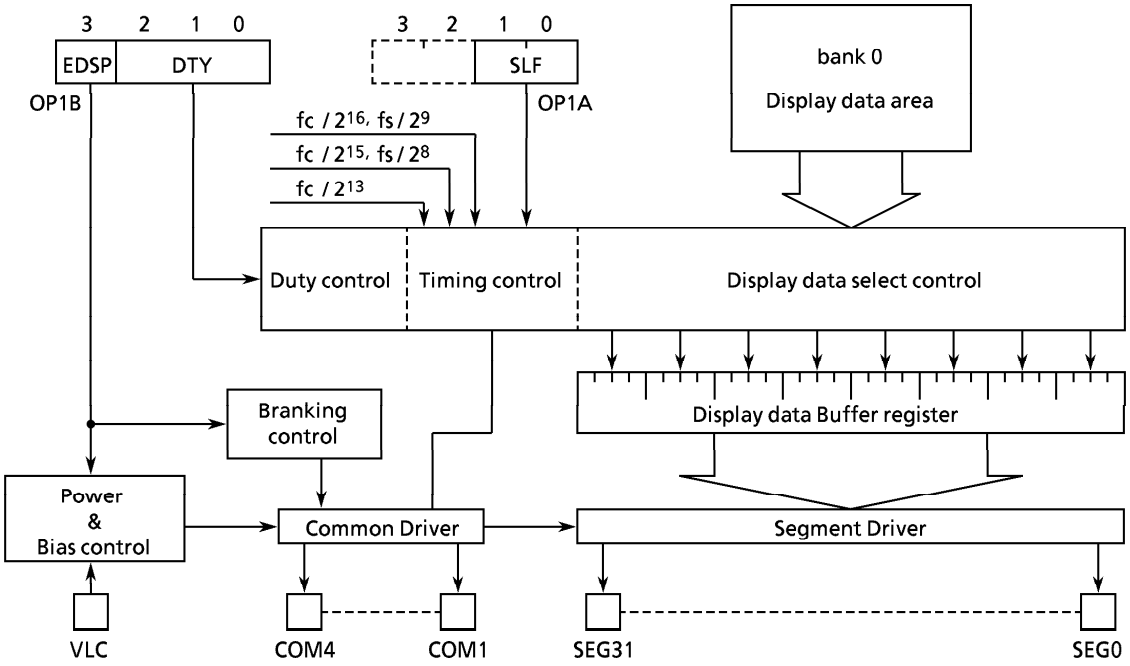


Figure 3-6. LCD Driver

3.3.2 Control of LCD driver circuit

The LCD driver is controlled by the command register 1,2 (OP1A, OP1B). Further, when the command register 1 is accessed, the most significant bit of the command register 2 must be set to "0" (Blanking).

LCD Driver control command register 1
(Port address OP1A) (Initial value 0000)

3	2	1	0
		SLF	

SLF	Selection of LCD drive frequency	
	Single Clock Mode	Dual Clock Mode
00:	fc / 2^{13} [Hz]	Unused
01:	fc / 2^{15}	fs / 2^{8} [Hz]
10:	fc / 2^{16}	fs / 2^{9}
11:	Unused	Unused

Note. fc ; High-frequency clock [Hz]
fs ; Low-frequency clock [Hz]
** ; don't care*

LCD Driver control command register 2
(Port address OP1B) (Initial value 0000)

3	2	1	0
EDSP	DTY		

EDSP	LCD Display Control
0:	Blanking
1:	Enables LCD display (Blanking is released)

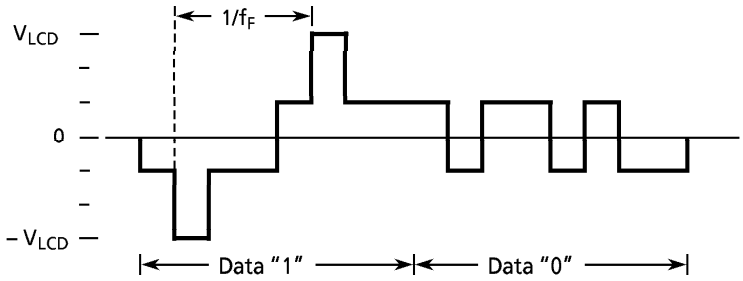
DTY	Selection of driving methods	
000:	1 / 4 Duty	(1 / 3 Bias)
001:	1 / 3 Duty	(1 / 3 Bias)
010:	1 / 3 Duty	(1 / 2 Bias)
011:	1 / 2 Duty	(1 / 2 Bias)
100:	Static	
101:	Reserved	
11*:	Reserved	

Figure 3-7. LCD Driver control Command Register

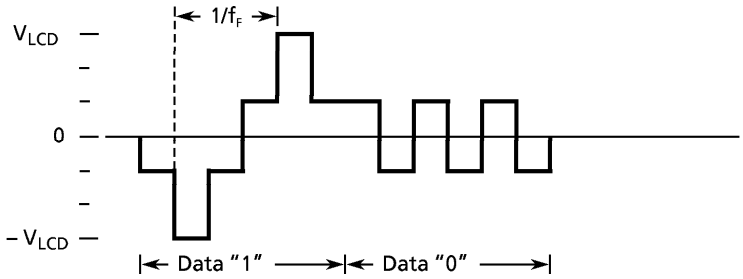
(1) Driving methods of LCD driver

Driving methods of LCD is selected 5 kind of DTY (bit 2-0 of command register 2). The drive method is initialized according to LCD used in the initial program.

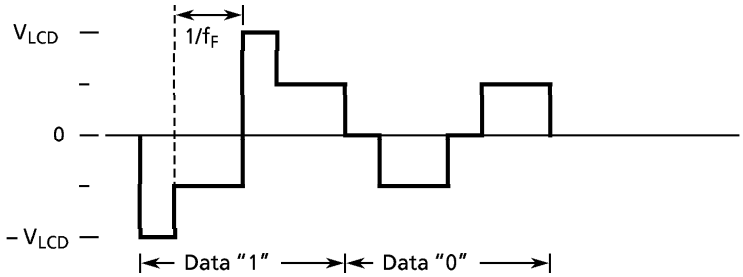
① 1 / 4 Duty (1 / 3 Bias)



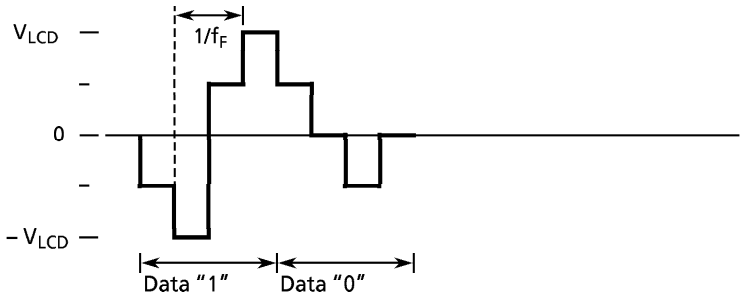
② 1 / 3 Duty (1 / 3 Bias)



③ 1 / 3 Duty (1 / 2 Bias)



④ 1 / 2 Duty (1 / 2 Bias)



⑤ Static

Note 1. f_F : Fram frequency
Note 2. V_{LCD} : LCD drive voltage ($= V_{DD} - V_{LC}$)

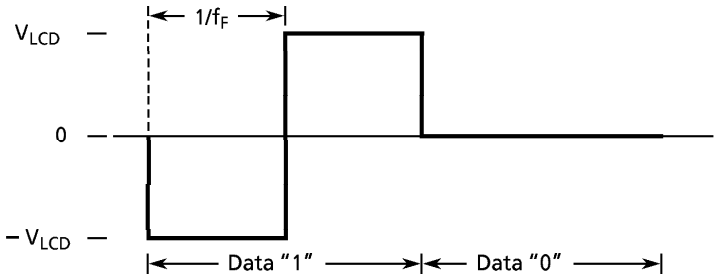


Figure 3-8. LCD drive waveform (COM-SEG pins)

(2) Frame frequency

Frame frequency (f_F) is set according to the drive method and base frequency as shown in the following table 3-2.

The base frequency is selected by SLF (the lower 2 bits of the command register) according to the reference clock frequency fc and fs.

Table 3-2. Setting of LCD Frame Frequency

a. At the single clock mode

SLF	BASE FREQUENCY [Hz]	FRAME FREQUENCY [Hz]			
		1 / 4 DUTY	1 / 3 DUTY	1 / 2 DUTY	STATIC
10	$\frac{fc}{2^{16}}$	$\frac{fc}{2^{16}}$	$\frac{4}{3} \cdot \frac{fc}{2^{16}}$	$\frac{4}{2} \cdot \frac{fc}{2^{16}}$	$\frac{fc}{2^{16}}$
	fc = 4 MHz	61	81	122	61
01	$\frac{fc}{2^{15}}$	$\frac{fc}{2^{15}}$	$\frac{4}{3} \cdot \frac{fc}{2^{15}}$	$\frac{4}{2} \cdot \frac{fc}{2^{15}}$	$\frac{fc}{2^{15}}$
	fc = 4 MHz	122	163	244	122
00	$\frac{fc}{2^{13}}$	$\frac{fc}{2^{13}}$	$\frac{4}{3} \cdot \frac{fc}{2^{13}}$	$\frac{4}{2} \cdot \frac{fc}{2^{13}}$	$\frac{fc}{2^{13}}$
	fc = 1 MHz	122	163	244	122

Note . fc ; High-frequency clock [Hz]

b. At the dual clock mode

SLF	BASE FREQUENCY [Hz]	FRAME FREQUENCY [Hz]			
		1 / 4 DUTY	1 / 3 DUTY	1 / 2 DUTY	STATIC
10	$\frac{fs}{2^{9}}$	$\frac{fs}{2^{9}}$	$\frac{4}{3} \cdot \frac{fs}{2^{9}}$	$\frac{4}{2} \cdot \frac{fs}{2^{9}}$	$\frac{fs}{2^{9}}$
	fs = 32 KHz	61	83	125	61
01	$\frac{fs}{2^{8}}$	$\frac{fs}{2^{8}}$	$\frac{4}{3} \cdot \frac{fs}{2^{8}}$	$\frac{4}{2} \cdot \frac{fs}{2^{8}}$	$\frac{fs}{2^{8}}$
	fs = 32 KHz	125	167	250	125

Note . fs ; Low-frequency clock [Hz]

(3) LCD drive voltage

The LCD drive voltage (V_{LCD}) is given by the difference in potential (V_{DD}-V_{LC}) between pins VDD and VLC. Therefore, when the CPU operating voltage and LCD drive voltage are the same, the VLC pin is connected to the VSS pin.

The LCDs light only when the difference in potential between the segment output and common output is $\pm V_{LCD}$, and turn off at all other times.

During reset, the power switch of the LCD driver is turned off automatically, shutting off the VLC voltage.

Both the segment output and common output become V_{DD} level at this time and the LCDs turn off.

The power switch is turned on to supply VLC voltage to the LCD driver by setting EDSP (bit 3 of the command register 2) to "1_B". After that, the power switch will not turn off even during blanking (setting EDSP to "01_B") and the VLC voltage continues to flow.
The power switch is turned off during hold operation low power consumption by turning off the LCD. When hold operation is released the status in effect immediately before the hold operation is reinstated.

3.3.3 LCD display operation

(1) Display data setting

Display data are stored to the display data area (Max 32 words) in the data memory (bank0).
The display data stored to the display data area (address 20-3F_H) are read automatically and sent to the LCD driver by the hardware.
The LCD driver generates the segment signals and common signals in accordance with the display data and drive method. Therefore, display patterns can be changed by only overwriting the contents of the display data area with a program. The table look up instruction is mainly used for this overwriting.
Figure 3-9 shows the correspondence between the display data area and the SEG/COM pins. The LCD light when the display data is "1" and turn off when "0".
The number of segment which can be driven differs depending on the LCD drive method therefore, the number of display data area bits used to store the data also differs. Consequently, data memory not used to store display data and data memory for which the addresses are not connected to LCD can be used to store ordinary user's processing data.

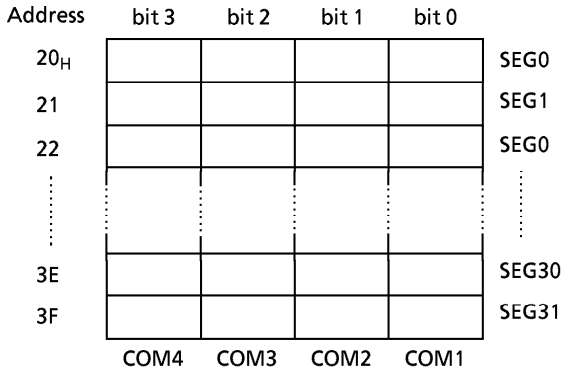


Figure 3-9. LCD Display Data Area (Bank 0)

Table 3-3. Drivinig Method and Bit for Display Data

Driving methods	bit 3	bit 2	bit 1	bit 0
1 / 4 Duty	COM4	COM3	COM2	COM1
1 / 3 Duty	–	COM3	COM2	COM1
1 / 2 Duty	–	–	COM2	COM1
Static	–	–	–	COM1

Note. – ; This bit is not used for display data.

(2) Blanking

Blanking is applied by setting EDSP to "0" and turns off the LCD by outputting the non light operation level to the COM pin.
The SEG pin continuously outputs the signal level in accordance with the display data and drive method.
With static drive, no voltage is applied between the COM and SEG pins when the LCD is turned off by data (display data cleared to "0"), but the COM pin output becomes constant at the $V_{LCD}/2$ level when turning off the LCD by blanking, so the COM and SEG pins are then driven by $V_{LCD}/2$.

3.3.4 Control method of LCD driver

(1) Initial Setting

Flow chart of intial setting are as shown in Figure 3-10.

Example : When operating the 47C647/847 with 1/4 duty LCD using a from frequency of fc/2^{16} [HZ] .

```
LD      A, #0000B  ;  Sets the 1/4 duty drive
OUT     A, %OP1B
LD      A, #0010B  ;  Setting of base frequency
OUT     A, %OP1A
  ⋮                ;  Setting of clear or intial value of
  ⋮                   display area in the memory
LD      A, #1000B  ;  Display enable
OUT     A, %OP1B
  ⋮
```

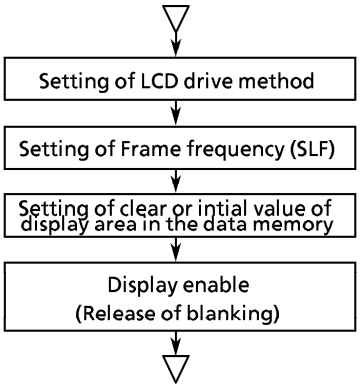


Figure 3-10. Intial setting of LCD driver

(2) Store of display data

Normally, display data are kept permantly in the program memory and then stored to the display data area by the table look-up instruction.

Example of numeric display data using the 1/4 duty LCD are given inTable 3-4.
The COM pin and SEG pin connection method is as shown in Figure 3-11.

```
        LD      HL, #0FCH          ; To set the DC
        LD      A,  10H
        ST      A,  @HL+
        ST      #DTBL/16, @HL+
        ST      #DTBL/256, @HL+
        LD      HL, #20H           ; Store of clisplay data
        LDL     A, @DC
        ST      A, @HL+
        LDH     A, @DC+
        ST      A, @HL+
        ⋮
DTBL :  DATA    11011111B, 00000110B,
                11100011B, 10100111B,
                00110110B, 10110101B,
                11110101B, 00010111B,
                11110111B, 10110111B
```

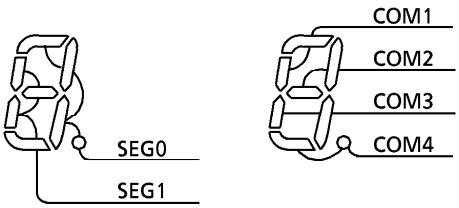


Figure 3.11 Example of COM. and SEG connection

Table 3-4. Example of display data (1/4 Duty LCD)

Numeric	Display	Display data memory		Numeric	Display	Display data memory	
		High order address	Low order address			High order address	Low order address
0	0.	1101	1111	5	5	1011	0101
1	1	0000	0110	6	6	1111	0101
2	2	1110	0011	7	7	0001	0111
3	3	1010	0111	8	8	1111	0111
4	4	0011	0110	9	9	1011	0111

Futher, example numeric display data (in the same way as in Table 3-4) using the 1/3 duty LCD are given in Table 3-5. The COM pin and SEG pin connection method is as shown in Figure 3-12.

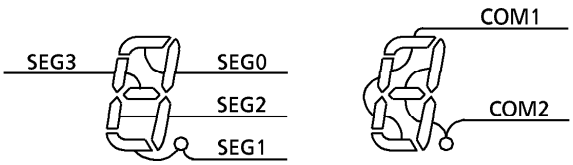


Figure 3.12 Example of COM and SEG connection.

Table 3-5. Example of display data (1/3 Duty LCD)

Numeric	Display data memory			Numeric	Display data memory		
	High order address	Middle order address	Low order address		High order address	Middle order address	Low order address
0	**11	*101	*111	5	**01	*111	*010
1	**00	*000	*011	6	**11	*111	*010
2	**10	*111	*001	7	**01	*001	*011
3	**00	*111	*011	8	**11	*111	*011
4	**01	*101	*011	9	**01	*111	*011

*Note. * ; don't care*

(2) Example of LCD drive output

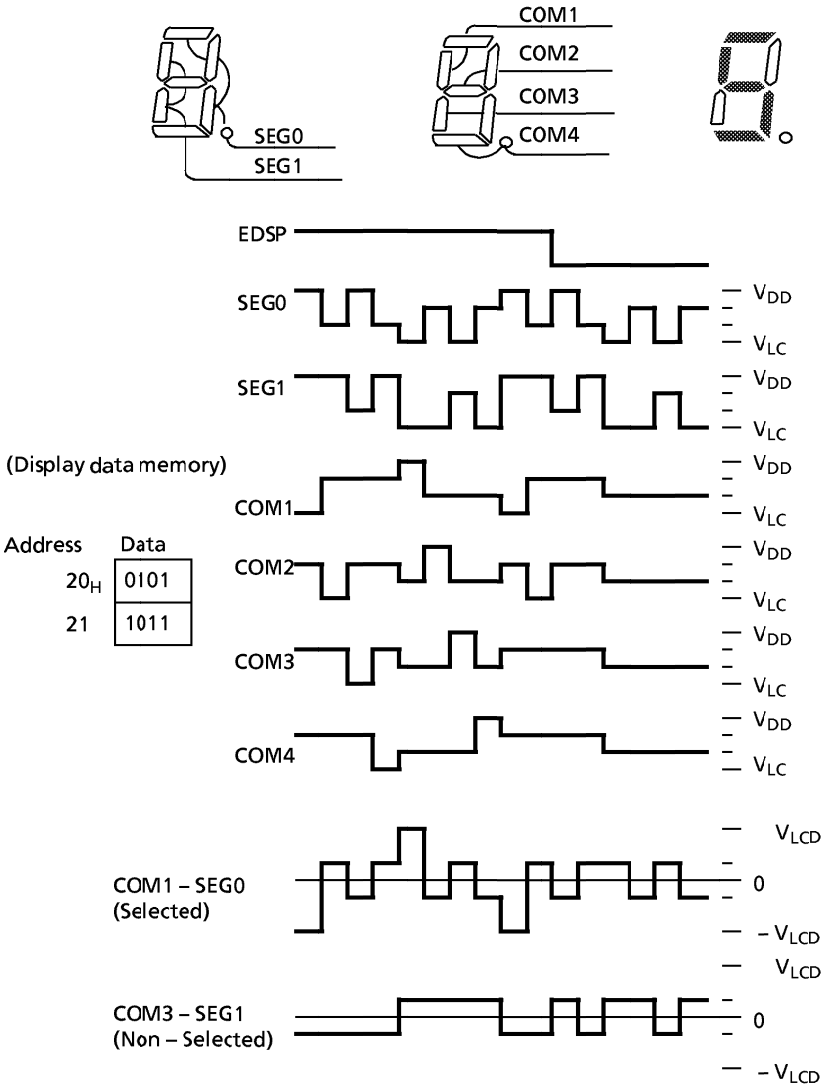


Figure 3-13. 1/4 Duty (1/3 Bias) Drive

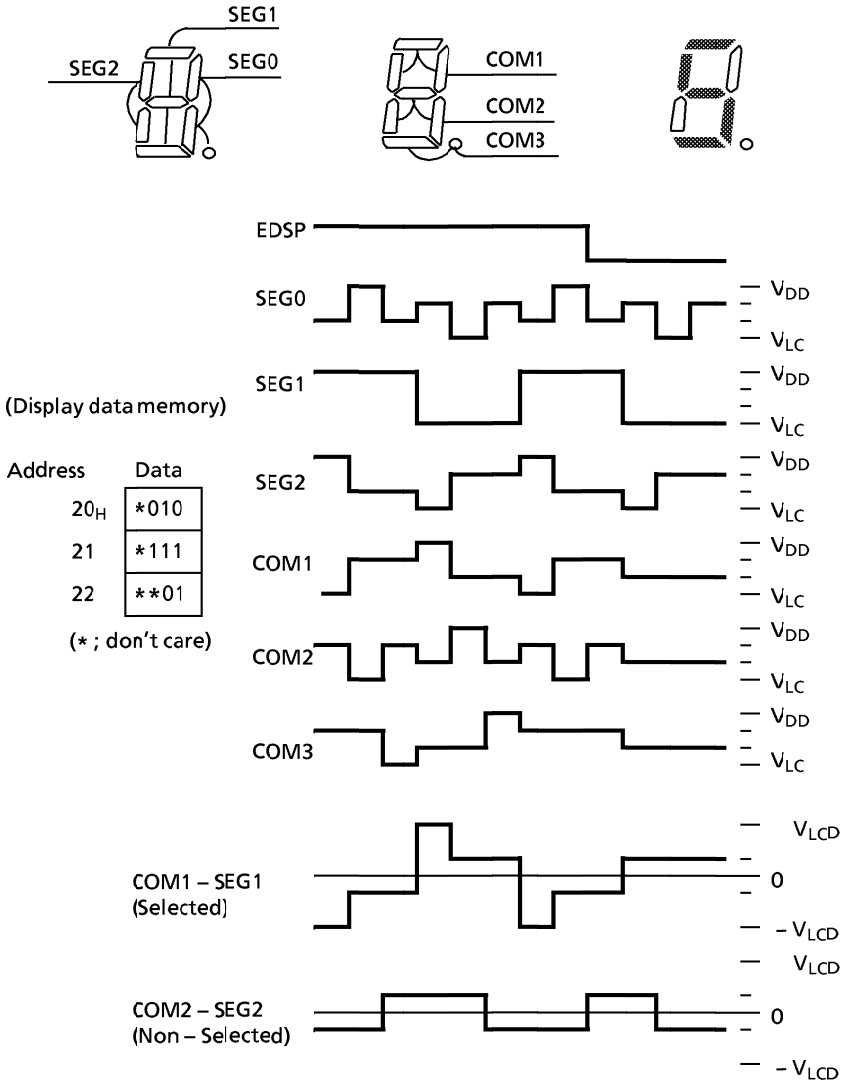


Figure 3-14. 1/3 Duty (1/3 Bias) Drive

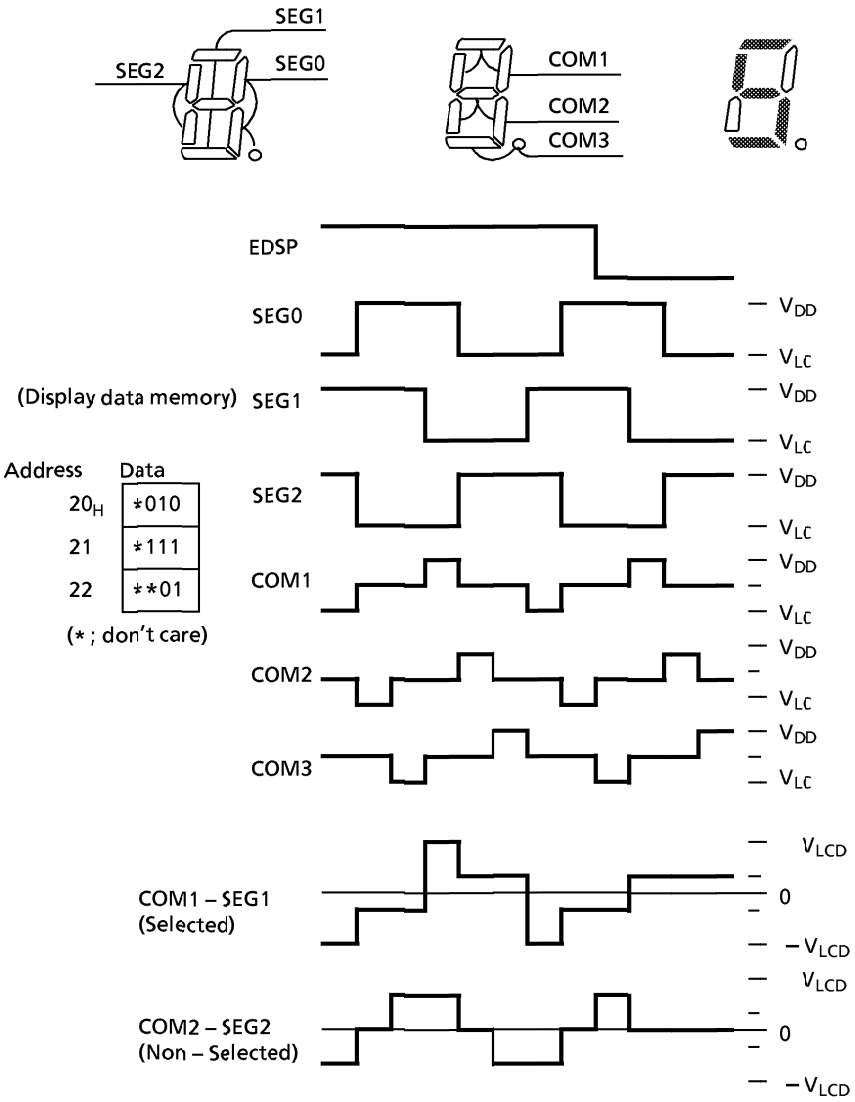


Figure 3-15. 1/3 Duty (1/2 Bias) Drive

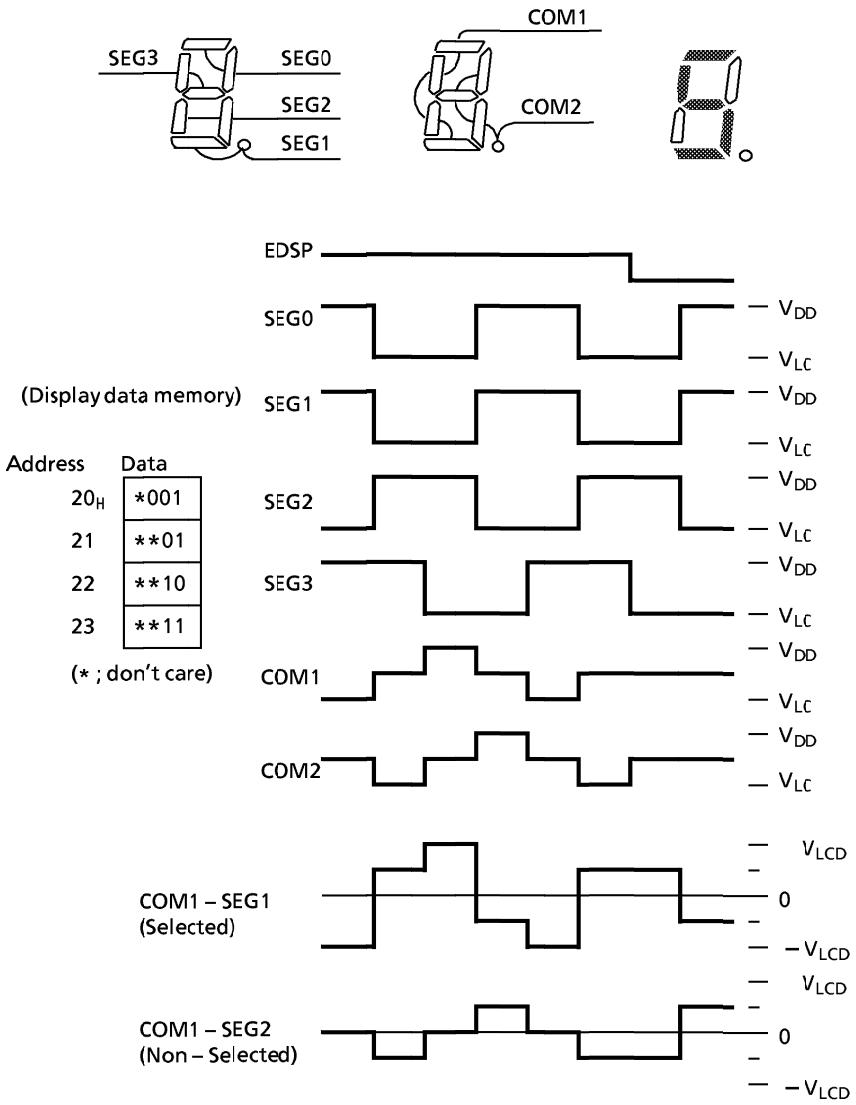


Figure 3-16. 1/2 Duty (1/2 Bias) Drive

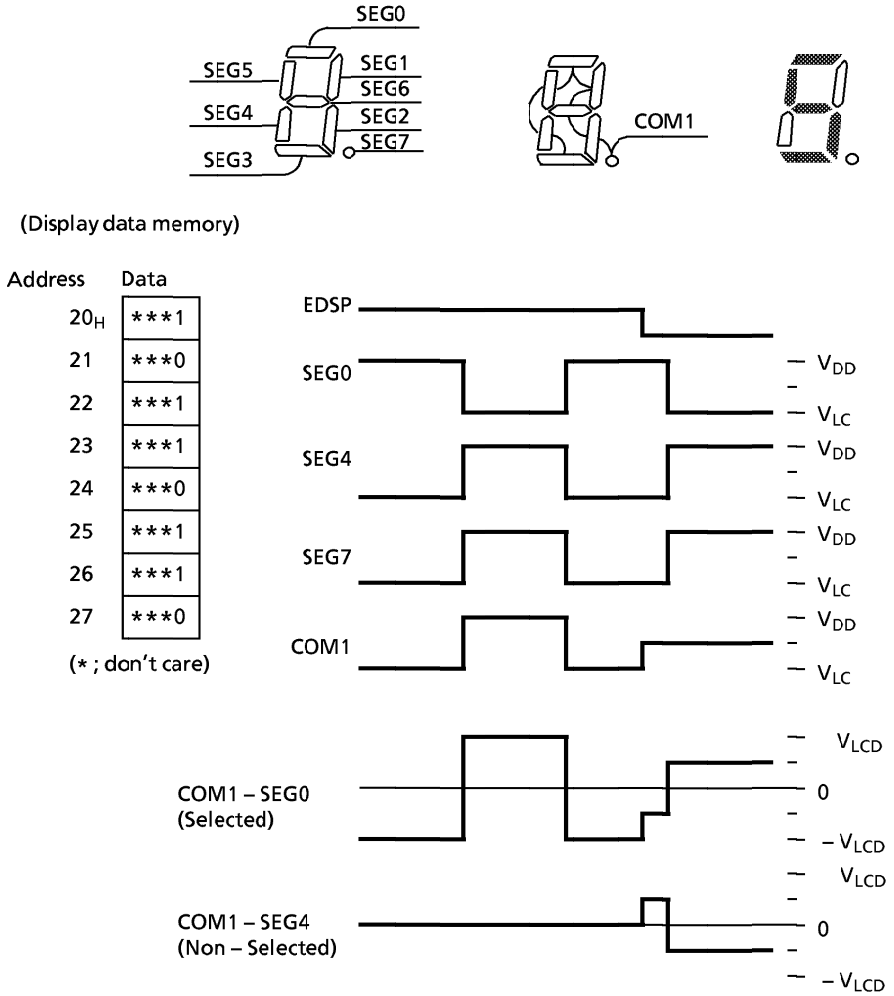


Figure 3-17. Static Drive

3.4 A/D Converter

47C647/847 have a 8-bit successive approximate type A/D converter and is capable of processing 8 analog inputs.

3.4.1 Circuit Configuration

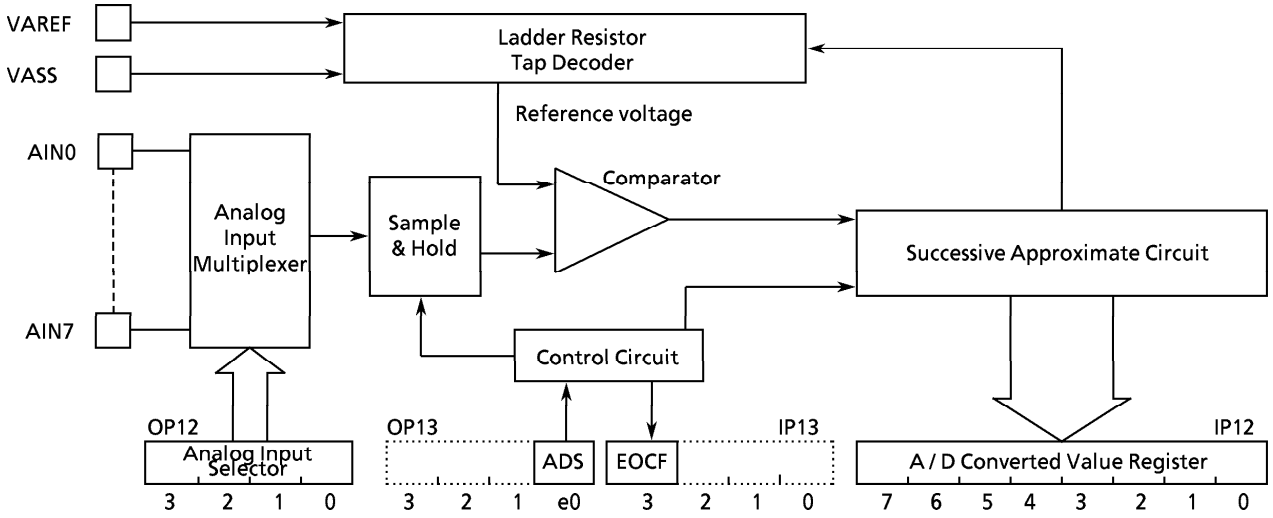


Figure 3-18. Block Diagram of A/D Converter

3.4.2 Control of A/D converter

The operation of A/D converter is controlled by a command. The command register is accessed as port addresses OP12, OP13, IP12 and IP13.

(1) Analog input selector (OP12)
Analog inputs (AIN0 through AIN7) are selected by this register.

Analog input select command register
(Port address OP12)

3	2	1	0
SAIN			

(Initial value 0000)

SAIN	Analog input selection
0000 :	R40 (AIN0)
0001 :	R41 (AIN1)
0010 :	R42 (AIN2)
0011 :	R43 (AIN3)
0100 :	R50 (AIN4)
0101 :	R51 (AIN5)
0110 :	R52 (AIN6)
0111 :	R53 (AIN7)
1*** :	Analog input is not selected.

*Note. * ; don't care*

Figure 3-19. Analog input selector

(2) Start of A/D conversion (OP13)

A/D conversion is started when ADS is set to "1". After the conversion is started, ADS is cleared by hardware. If the restart is requested during the conversion, the conversion is started again at the time.

Analog input voltage is hold by the sample hole circuit.

A/D conversion start command register
(Port address OP13)

3	2	1	0	
			ADS	(Initial value ***0)

ADS	A / D conversion enable

1 : A / D conversion is started (clears after starting)

Figure 3-20. A/D conversion start register

(3) A/D converter end frag (IP13)

End of conversion flag (EOCF) is a single bit flag showing the end of conversion and is set to "1" when conversion ended. When both upper 4 bits and lower 4 bits of a converted value are read or A/D conversion is started, EOCF is cleared to "0".

A/D converter status register
(Port address IP13)

3	2	1	0
EOCF			

EOCF	End of conversion flag

0 : Under A/D conversion or before A/D conversion

1 : End of A/D conversion

Figure 3-21. A/D converter status register

(4) A/D converted value register (IP12)

An A/D converted value is read by accessing port address IP12. An A/D converted value is read by splitting into upper 4 bits and lower 4 bits by a value of LR_0 (LSB of the L registers).

A / D converted value register
(Port address IP12)

3	2	1	0
D3	D2	D1	D0
D7	D6	D5	D4

D7 to D0	Reading of an A/D conversion

When LR_0 = 0, lower 4 bits of the converted value is read.

When LR_0 = 1, upper 4 bits of the converted value is read.

Figure 3-22. A/D converted value register

3.4.3 How to use A/D converter

Apply positive of analog reference voltage to the VAREF pin and negative to the VASS pin. The A/D conversion is carried out by splitting reference voltage between VAREF and VASS to bit corresponding voltage by a ladder resistor and making a judgement by comparing it with analog input voltage.

(1) Start of A/D conversion

Prior to conversion, select one of the analog input AIN0 througn AIN7 by the analog input selector. Place output of the analog input, which is to be A/D converted, in the high impedance state by setting "1". If other port is used as an output port, be careful not to execute the output instruction for any port during conversion in order to keep accuracy of conversion.

A/D conversion is started by setting ADS (bit1 of the A/D conversion start register). When conversion ends after 24 instruction cycles, EOCF showing the end of conversion is set to "1".

Analog input voltage is sampled during the following 2 instruction cycles after setting conversion enable ADS.

Note. The sample and hold circuit has capacitor (C_A = 12 pF typ.) with resistor (RA = 5 kΩ typ.). See I/O circuitry table. This capacitor should be charged or discharged within 2 instruction cycles.

(2) Reading of an A/D converted value

After the end of conversion, read an A/D converted value is read by splitting into lower 4 bits and upper 4 bits by the A/D converted value register (IP12). Lower 4 bits of the A/D converted value can be read when LR_0 = 0 and upper 4 bits when LR_0 = 1. Usually an A/D converted value is stored in RAM by an instruction [IN %p, @HL]. Further, if an A/D converted value is read during conversion, it becomes an indefinite value.

(3) A/D conversion with HOLD operation

When the HOLD operation is started during the conversion, the conversion is terminated and an A/D converted value becomes indefinite. Therefore, EOCF is kept clear to "0" after release from the HOLD operation. However, if the HOLD operation is started after the end of conversion (after EOCF has been set), A/D converted value and status of EOCF are held.

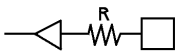
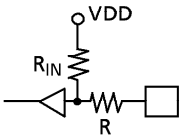
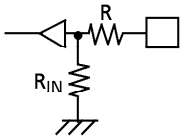
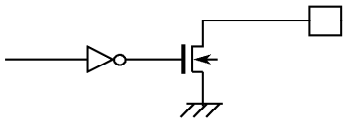
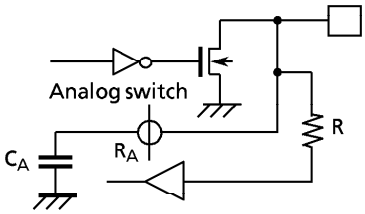
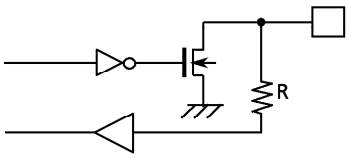
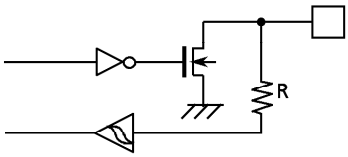
Example: Selecting analog input (AIN4), starting A/D conversion, monitoring EOCF, and storing lower 4 bits and upper 4 bits of a converted value to RAM [10_H] and RAM [11_H] respectively.

```
                                    ; AIN SELECT
        LD      A, #4H
        OUT     A, %OP12            ; A/D START
        LD      A, #1H
        OUT     A, %OP13            ; EOCF = 1?
SLOOP : IN      %IP13, A
        TEST    A, 3
        B       SLOOP               ; DATA READ
        LD      HL, #10H
        IN      %IP12, @HL
        INC     L
        IN      %IP12, @HL
```

INPUT/OUTPUT CIRCUITRY

(1) Control pins
The input/output circuitries of the 47C647/847 control pins are similar to those of the 47C660/860.

(2) I/O Ports
The input/output circuitries of the 47C647/847 I/O ports are shown as belows, any one of the circuitries can be chosen by a code (GA to GC) as a mask option.

PORT	I/O	IINPUT/OUTPUT CIRCUITRY and CODE			REMARKS
		GA	GB	GC	
K0	Input				Pull-up/pull-down resistor R_{IN} = 70 kΩ (typ.) R = 1 kΩ (typ.)
P1 P2	Output				Sink open drain output Initial "Hi-Z" High current I_{OL} = 10 mA (typ.)
R5 R6	I/O				Sink open darin output Initial "Hi-Z" R = 1 kΩ (typ.) Analog input (R4, R5) R_A = 5 kΩ (typ.) C_A = 12 pF (typ.)
R4 R7	I/O				Sink open drain output Initial "Hi-Z" R = 1 kΩ (typ.)
R8 R9	I/O				Sink open drain output Initial "Hi-Z" Hysteresis input R = 1 kΩ (typ.)

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V)

PARAMETER	SYMBOL	PINS	RATINGS	UNIT
Supply Voltage	V_{DD}		– 0.3 to 7	V
Supply Voltage (LCD drive)	V_{LC}		– 0.3 to V_{DD} + 0.3	V
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT1}	Except sink open drain pin	– 0.3 to V_{DD} + 0.3	V
	V_{OUT2}	Sink open drain pin	– 0.3 to 10	
Output Current (Per 1 pin)	I_{OUT1}	Ports P1, P2	15	mA
	I_{OUT2}	Ports R4 to R9	3.2	
Output Current (Total)	ΣI_{OUT1}	Ports P1, P2	60	mA
Power Dissipation [T_{opr} = 70 °C]	PD		600	mW
Soldering Temperature (time)	T_{sld}		260 (10 s)	°C
Storage Temperature	T_{stg}		– 55 to 125	°C
Operating Temperature	T_{opr}		– 40 to 70	°C

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V, T_{opr} = – 40 to 70 °C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
Supply Voltage	V_{DD}		In the Normal mode	4.5	6.0	V
			In the SLOW mode	2.7		
			In the SLEEP mode			
			In the HOLD mode	2.0		
Input High Voltage	V_{IH1}	Except Hysteresis Input	$V_{DD} \geqq 4.5V$	$V_{DD} \times 0.7$	V_{DD}	V
	V_{IH2}	Hysteresis Input		$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5V$	$V_{DD} \times 0.9$		
Input Low Voltage	V_{IL1}	Except Hysteresis Input	$V_{DD} \geqq 4.5V$	0	$V_{DD} \times 0.3$	V
	V_{IL2}	Hysteresis Input			$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5V$		$V_{DD} \times 0.1$	
Clock Frequency	fc	XIN, XOUT		0.4	6.0	MHz
	fs	XTIN, XTOUT		30.0	34.0	kHz

Note. Input Voltage V_{IH3}, V_{IL3} : in the SLOW, SLEEP and HOLD mode.

D.C. CHARACTERISTICS (V_{SS} = 0V, T_{opr} = – 40 to 70°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis Input		—	0.7	—	V
Input Current	I_{IN1}	Port K0, TEST, $\overline{RESET}$, $\overline{HOLD}$	V_{DD} = 5.5 V,	—	—	± 2	μA
	I_{IN2}	Open drain R port	V_{IN} = 5.5 V / 0 V				
Input Low Current	I_{IL}	Push-pull R port	V_{DD} = 5.5 V, V_{IN} = 0.4 V	—	—	– 2	mA
Input Resistance	R_{IN1}	Port K0 with pull-up/pull-down resistor		30	70	150	kΩ
	R_{IN2}	$\overline{RESET}$		100	220	450	
Output Leakage Current	I_{LO}	Open drain ports P, R	V_{DD} = 5.5 V, V_{OUT} = 5.5 V	—	—	2	μA
Output High Voltage	V_{OH}	Push-pull R port	V_{DD} = 4.5 V, I_{OH} = – 200 μA	2.4	—	—	V
Output Low Voltage	V_{OL2}	Except XOUT XOUT and ports P1, P2	V_{DD} = 4.5 V, I_{OL} = 1.6 mA	—	—	0.4	V
Output Low Current	I_{OL1}	Ports P1, P2	V_{DD} = 4.5 V, I_{OL} = 1.0V	—	10	—	mA
Segment Output Low Resistance	R_{OS1}	SEG pin	V_{DD} = 5 V, V_{DD} – V_{LC} = 3 V	—	20	—	kΩ
Common Output Low Resistance	R_{OC1}	COM pin					
Segment Output High Resistance	R_{OS2}	SEG pin		—	200	—	
Common Output High Resistance	R_{OC2}	COM pin					
Segment / Common Output Voltage	$V_{O2/3}$	SEG / COM pin		3.8	4.0	4.2	V
	$V_{O1/2}$			3.3	3.5	3.7	
	$V_{O1/3}$			2.8	3.0	3.2	
Supply Current (in the Normal mode)	I_{DD}		V_{DD} = 5.5 V, V_{LC} = V_{SS} fc = 4 MHz	—	3	6	mA
Supply Current (in the SLOW mode)	I_{DDS}		V_{DD} = 3.0 V, V_{LC} = V_{SS} fs = 32.768 kHz	—	30	60	μA
				—	15	30	
Supply Current (in the HOLD mode)	I_{DDH}		V_{DD} = 5.5 V	—	0.5	10	μA

Note 1. Typ. values show those at T_{opr} = 25 °C, V_{DD} = 5 V.

Note 2. Input Current IIN1 ; The current through resistor is not included, when the input resistor (pull-up / pull-down) is contained.

Note 3. Output Resistance R_{OS}, R_{OC} ; Shows on-resistance at the level switching.

Note 4. $V_{O2/3}$; Shows 2/3 level output voltage, when the 1/4 or 1/3 duty LCD is used.

Note 5. $V_{O1/2}$; Shows 1/2 level output voltage, when the 1/2 duty or static LCD is used.

Note 6. $V_{O1/3}$; Shows 1/3 level output voltage, when the 1/4 or 1/3 duty LCD is used.

Note 7. Supply Current I_{DD}, I_{DDH} ; V_{IN} = 5.3 V / 0.2 V
The K0 port is open when the input resistor is contained.
The voltage applied to the R port is within the valid range.
Supply Current I_{DDS} ; VIN = 2.8 V/0.2 V Only low frequency clock is only oscillated (connecting XTIN, XTOUT).

Note 8. When using LCD, it is necessary to consider values of $R_{OS1/2}$ and $R_{OC1/2}$.

Note 9. Times for SEG / COM output switching on ; R_{OS1}, R_{OC1} : 2/fs (s)
R_{OS2}, R_{OC2} : 1/(n · f_F)
(1/n : duty, f_F : frame frequency)

A / D CONVERSION CHARACTERISTICS

(T_{opr} = – 40 to 70 °C)

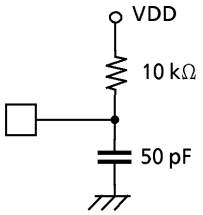
PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Analog Reference Voltage	V_{AREF}		V_{DD} – 1.5	–	V_{DD}	V
	V_{ASS}		V_{SS}	–	1.5	
Analog Reference Voltage Range	ΔV_{AREF}	$V_{AREF} - V_{ASS}$	2.5	–	–	V
Analog Input Voltage	V_{AIN}		V_{ASS}	–	V_{AREF}	V
Analog Supply Current	I_{REF}		–	0.5	1.0	mA
Nonlinearity Error		V_{DD} = 4.5 to 6.0V, V_{SS} = 0.0V V_{AREF} = V_{DD} ± 0.001V V_{ASS} = 0.000V	–	–	± 1	LSB
Zero Point Error			–	–	± 1	
Full Scale Error			–	–	± 1	
Total Error			–	–	± 2	

A.C. CHARACTERISTICS

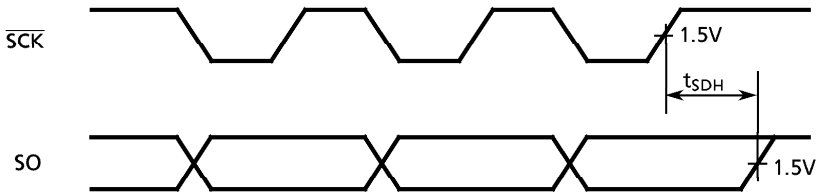
(V_{SS} = 0V, V_{DD} = 4.5 to 6.0V, T_{opr} = – 40 to 70 °C)

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Instruction Cycle Time	t_{cy}	in the Normal mode	1.3	–	20	μs
		in the SLOW mode	235	–	267	μs
High Level Clock Pulse Width	t_{WCH}	For external clock operation	80	–	–	ns
Low Level Clock Pulse Width	t_{WCL}					
Shift data Hold Time	t_{SDH}		0.5 t_{cy} – 300	–	–	ns
A/D Sampling Time	t_{AIN}	fc = 4 MHz	–	4	–	μs

Note. Shift data Hold time :
External circuit for $\overline{SCK}$ pin and SO pin



Serial port (completion of transmission)

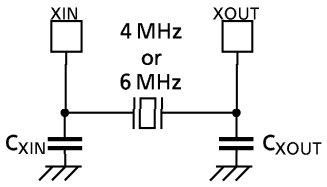


RECOMMENDED OSCILLATING CONDITIONS (V_{SS} = 0V, V_{DD} = 4.5 to 6.0V, T_{opr} = − 40 to 70 °C)

(1) 6 MHz

Ceramic Resonator

CSA6.00MGU	(MURATA)	$C_{XIN} = C_{XOUT}$ = 30 pF
KBR-6.00MS	(KYOCERA)	$C_{XIN} = C_{XOUT}$ = 30 pF



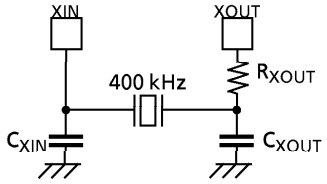
(2) 4 MHz

Ceramic Resonator

CSA4.00MG	(MURATA)	$C_{XIN} = C_{XOUT}$ = 30 pF
KBR-4.00MS	(KYOCERA)	$C_{XIN} = C_{XOUT}$ = 30 pF
FCR4.0M5	(TDK)	$C_{XIN} = C_{XOUT}$ = 33 pF

Crystal Oscillator

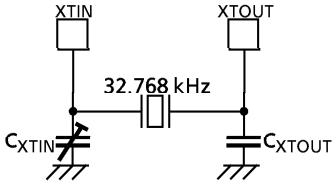
204B-6F 4.0000	(TOYOCOM)	$C_{XIN} = C_{XOUT}$ = 20 pF



(3) 400 kHz

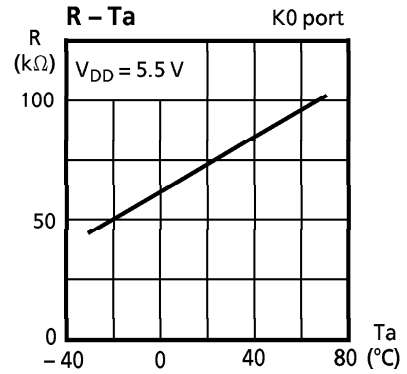
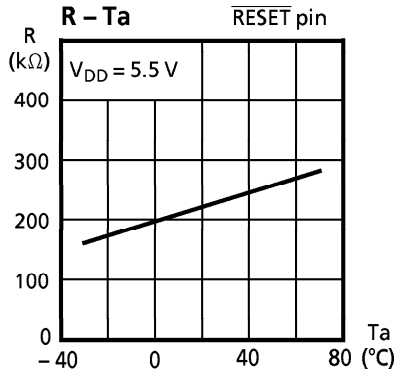
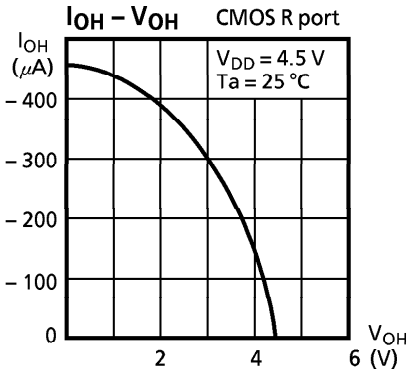
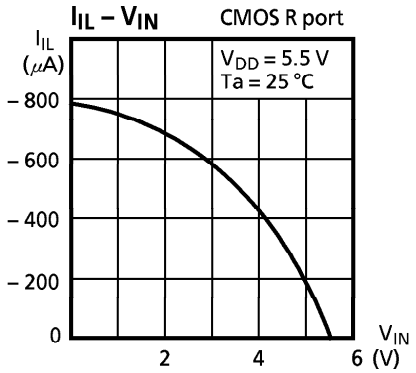
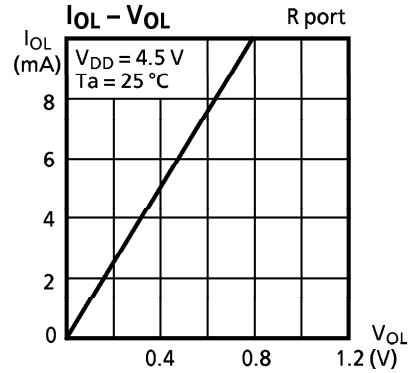
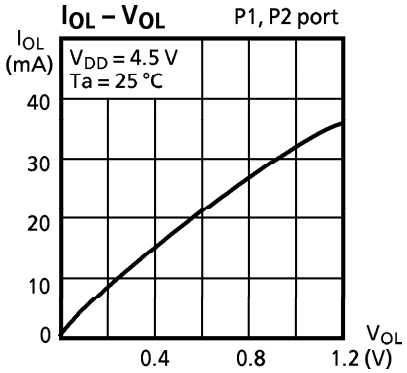
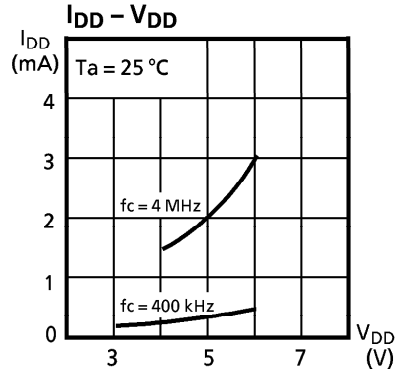
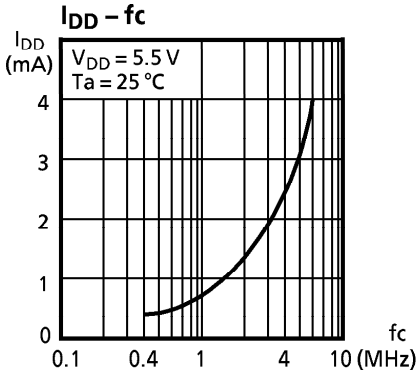
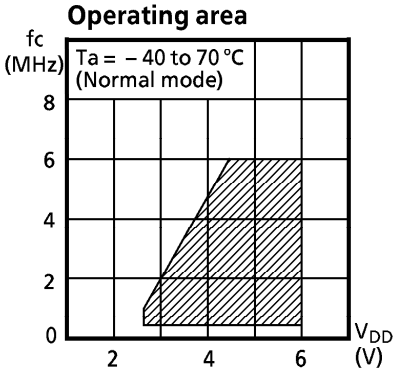
Ceramic Resonator

CSB400B	(MURATA)	$C_{XIN} = C_{XOUT}$ = 220 pF, R_{XOUT} = 6.8 kΩ
KBR-400B	(KYOCERA)	$C_{XIN} = C_{XOUT}$ = 100 pF, R_{XOUT} = 10 kΩ



(4) 32.768 kHz (Vss = 0V, V_{DD} = 2.7 to 6.0V, T_{opr} = − 30 to 70 °C)

Crystal Oscillator C_{XTIN}, C_{XTOUT} ; 10 to 33 pF

Note : In order to get the accurate oscillation frequency, the adjustment of capacitors must be required.

TYPICAL CHARACTERISTICS