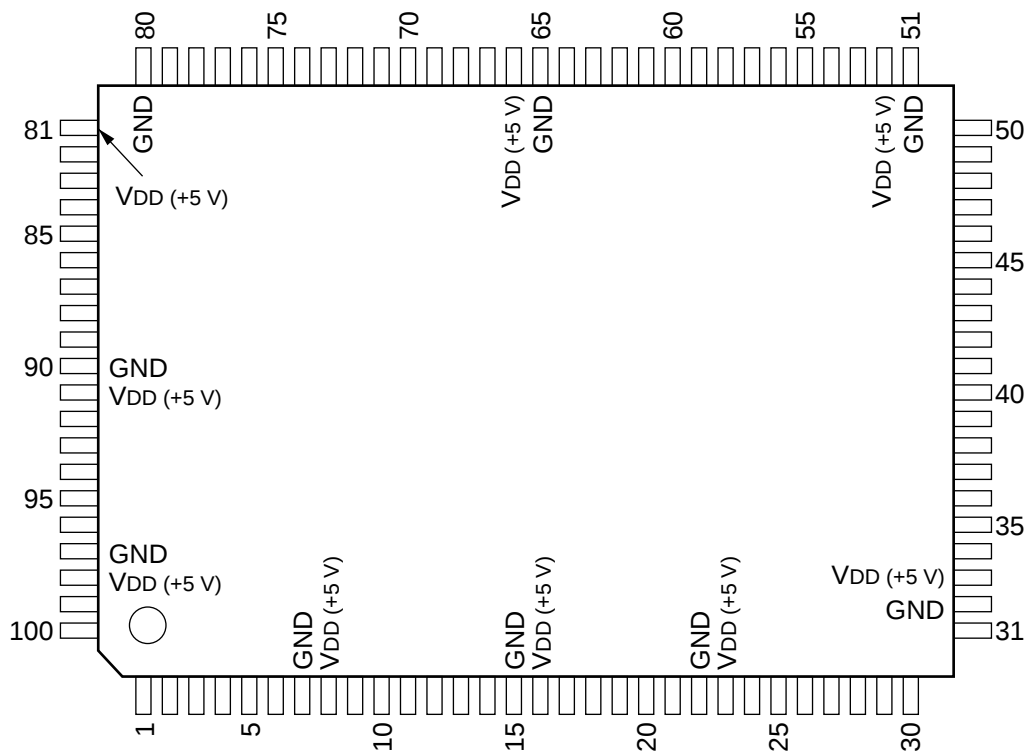

C-MOS 24-BIT DIGITAL AUDIO SIGNAL PROCESSOR

- TOP VIEW -



(VDD = +5 V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I/O	EA6/ED18	21	I/O	ED3	41	I	TEST3	61	I	HXBCK	81	—	VDD
2	I/O	EA7/ED19	22	—	GND	42	I	BIO	62	I	HXS	82	I	HDIR
3	I/O	EA8/ED20	23	—	VDD	43	I	INT1	63	I	CS	83	I	SEL5V3V
4	I/O	EA9/ED21	24	I/O	ED4	44	I	INT2	64	I	HBCKS	84	I	MUTE
5	I/O	EA10/ED22	25	I/O	ED5	45	I	INT3	65	—	GND	85	I	TRST
6	I/O	EA11/ED23	26	I/O	ED6	46	I	ARBC1	66	—	VDD	86	I	RS
7	—	GND	27	I/O	ED7	47	I	ARBC2	67	I	AXBC1	87	O	IOE
8	—	VDD	28	I/O	ED8	48	O	AX1	68	I	AXBC2	88	O	RAS
9	I	CLKM0	29	I/O	ED9	49	O	AX2	69	I	AXLR1	89	O	CAS
10	I	CLKM1	30	I/O	ED10	50	O	AX3	70	O	DIV8	90	—	GND
11	I	TMS	31	I/O	ED11	51	—	GND	71	O	LAV	91	—	VDD
12	I	TDI	32	—	GND	52	—	VDD	72	O	LMV	92	O	WE
13	I	TCK	33	—	VDD	53	O	HX	73	O	DRDY	93	I/O	EA0
14	I	CLKIN	34	I/O	ED12	54	O	EMPTY	74	I/O	EMU0	94	I/O	EA1
15	—	GND	35	I/O	ED13	55	I	AXLR2	75	I/O	EMU1	95	I/O	EA2
16	—	VDD	36	I/O	ED14	56	I	AR1	76	O	TDO	96	I/O	EA3
17	O	CLKO	37	I/O	ED15	57	I	AR2	77	O	DIV512	97	—	GND
18	I/O	ED0	38	I	TEST0	58	I	HRBCK	78	I	ARLR1	98	—	VDD
19	I/O	ED1	39	I	TEST1	59	I	HR	79	I	ARLR2	99	I/O	EA4/ED16
20	I/O	ED2	40	I	TEST2	60	I	HRS	80	—	GND	100	I/O	EA5/ED17

INPUT

AR1, AR2	; AUDIO DATA RECEIVER 1, 2 DATA RECEIVE
ARBC1, ARBC2	; AUDIO DATA RECEIVER 1, 2 BIT CLOCK
ARLR1, ARLR2	; AUDIO DATA RECEIVER 1, 2 CHANNEL FRAMING SYNC
AXBC1, AXBC2	; AUDIO DATA TRANSMITTER 1, 2/3 BIT CLOCK
AXLR1, AXLR2	; AUDIO DATA TRANSMITTER 1, 2/3 CHANNEL FRAMING SYNC
BIO	; BRANCH CONTROL
CLKIN	; CLOCK INPUT
CLKM0, CLKM1	; CLOCK MODE
CS	; HOST INTERFACE CHIP SELECT
HBCKS	; HRBCK/HXBCK ACTIVE EDGE SELECT
HDIR	; HOST INTERFACE DATA DIRECTION SELECT
HR	; HOST INTERFACE SERIAL PORT DATA RECEIVE
HRBCK	; HOST INTERFACE SERIAL PORT RECEIVER CLOCK
HRS	; HOST INTERFACE SERIAL PORT RECEIVE FRAME SYNC
HXBCK	; HOST INTERFACE SERIAL PORT TRANSMITTER CLOCK
HXS	; HOST INTERFACE SERIAL PORT TRANSMITTER FRAME SYNC
INT1, INT2, INT3	; INTERRUPT #1, #2, #3
MUTE	; AUDIO RECEIVE/TRANSMIT MUTING
RS	; DEVICE RESET
SEL5V3V	; BUFFER CONTROL
TCK	; TEST ACCESS PORT CLOCK
TDI	; TEST ACCESS PORT SCAN INPUT
TEST0 - TEST3	; TEST MODE
TMS	; TEST ACCESS PORT MODE
TRST	; TEST ACCESS PORT RESET

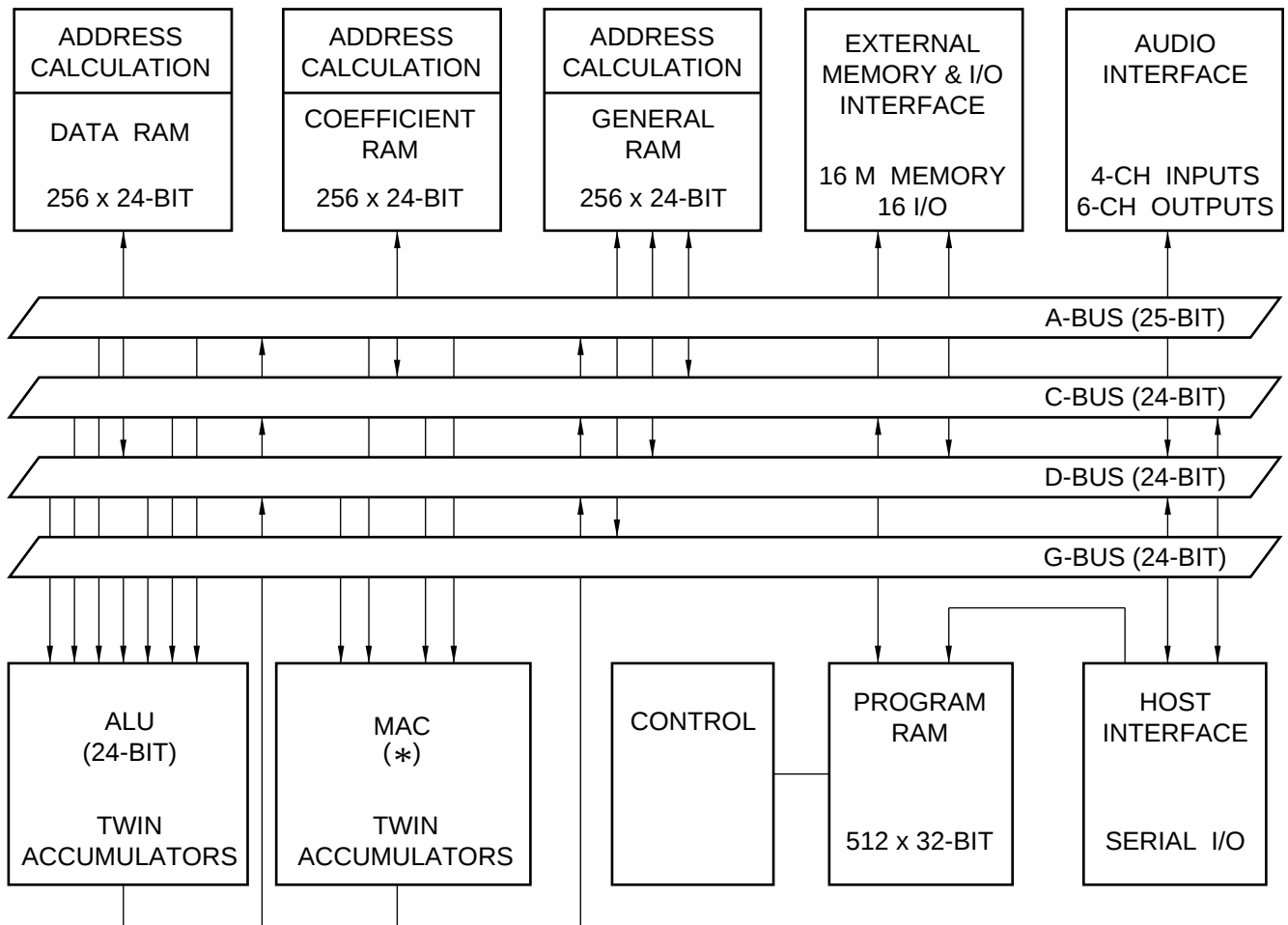
OUTPUT

AX1 - AX3	; AUDIO DATA TRANSMITTER 1-3 DATA OUTPUT
CAS	; EXTERNAL MEMORY I/F COLUMN ADDRESS STROBE
CLKO	; MACHINE CLOCK OUTPUT
DIV8	; DIVIDE-BY-8 MACHINE CLOCK OUTPUT
DIV512	; DIVIDE-BY-215 MACHINE CLOCK OUTPUT
DRDY	; UPLOAD DATA READY
EMPTY	; CMEM/PMEM UPDATE BUFFER EMPTY
HX	; HOST INTERFACE SERIAL PORT TRANSMITTER OUTPUT
IOE	; EXTERNAL I/O ENABLE
LAV	; LATCHED ALU OVERFLOW FLAG
LMV	; LATCHED MAC OVERFLOW FLAG
RAS	; EXTERNAL MEMORY I/F ROW ADDRESS STROBE
TDO	; TEST ACCESS PORT SCAN OUTPUT
WE	; EXTERNAL MEMORY & I/O I/F WRITE ENABLE

INPUT/OUTPUT

EA0 - EA3	; EXTERNAL MEMORY & I/O ADDRESS (LOWER 4-BIT)
EA4 - EA11	; EXTERNAL MEMORY & I/O ADDRESS (HIGHER 8-BIT)
ED0 - ED15	; EXTERNAL MEMORY DATA (16-BIT)/EXTERNAL I/O DATA (LOWER 16-BIT)
ED16 - ED23	; EXTERNAL I/O DATA (HIGHER 8-BIT)
EMU0, EMU1	; EMULATOR INTERRUPT 0, 1

18	ED0	AX1	48
19	ED1	AX2	49
20	ED2	AX3	50
21	ED3	CAS	89
24	ED4	CLKO	17
25	ED5	DIV8	70
26	ED6	DIV512	77
27	ED7	DRDY	73
28	ED8	EMPTY	54
29	ED9	HX	53
30	ED10	IOE	87
31	ED11	LAV	71
34	ED12	LMV	72
35	ED13	RAS	88
36	ED14	TDO	76
37	ED15	WE	92
93	EA0		
94	EA1		
95	EA2		
96	EA3		
99	EA4/ED16		
100	EA5/ED17		
1	EA6/ED18		
2	EA7/ED19		
3	EA8/ED20		
4	EA9/ED21		
5	EA10/ED22		
6	EA11/ED23		
56	AR1		
57	AR2		
46	ARBC1		
47	ARBC2		
78	ARLR1		
79	ARLR2		
67	AXBC1		
68	AXBC2		
69	AXLR1		
55	AXLR2		
42	BIO		
14	CLKIN		
9	CLKM0	EMU0	74
10	CLKM1	EMU1	75
63	CS		
64	HBCKS		
82	HDIR		
59	HR		
58	HRBCK		
60	HRS		
61	HXBCK		
62	HXS		
43	INT1		
44	INT2		
45	INT3		
84	MUTE		
86	RS		
83	SEL5V3V		
13	TCK		
12	TDI		
38	TEST0		
39	TEST1		
40	TEST2		
41	TEST3		
11	TMS		
85	TRST		



*; 25-BIT x 25-BIT + 52-BIT