TH6503

USB Low-Speed Interface

Description

The TH6503 is an integrated circuit which enables the Universal Serial Bus (USB) to be connected to a microcontroller. The interface module contains all the components required to transmit data via the USB.

The TH6503 has been developed for applications requiring a low speed interface to the USB. Any microcontroller can be used for control purposes. In addition to the default endpoint 0 for control transfer up to two endpoints can be supported by TH6503. The TH6503 has been developed in conformity with USB Specifications 1.0.

Features

- ❑ Supports up to two programmable endpoints for interrupt transfer
- ❑ Data transfer at USB low speed
- ❑ Supports suspend mode
- ❑ Universal serial microcontroller interface
- ❑ Register programmable
- ❑ Programmable 1.5 MHz to 6 MHz out clock for microcontroller
- ❑ Provides power supply for the microcontroller (3.3 volts or 5 volts)
- ❑ Integrated oscillator for clock generation, supports 6 MHz quartz, ceramic resonator or external clock input
- ❑ Simple external circuitry
- ❑ Supports low voltage

TH6503 Sample Application

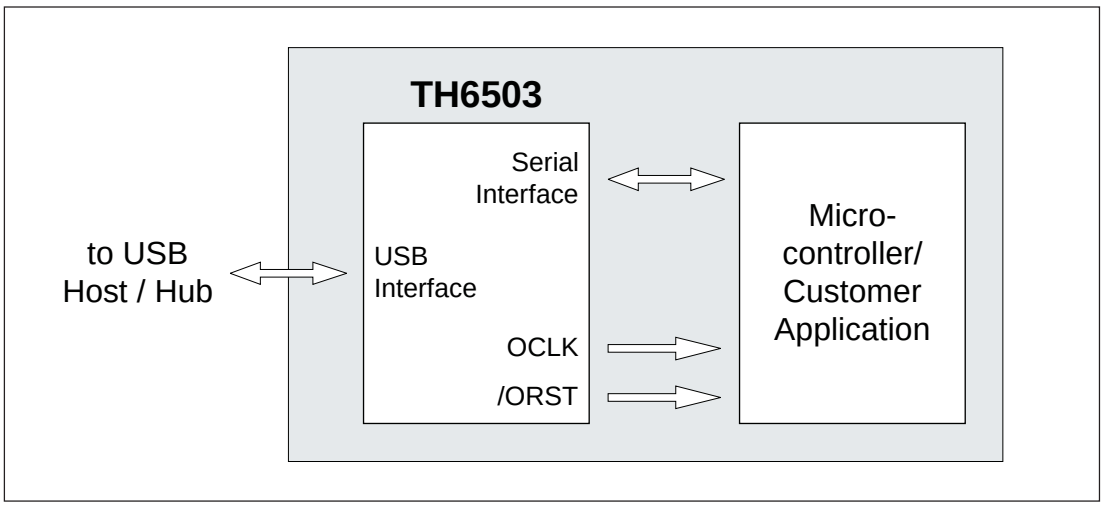


Figure 1. Typical TH6503 Sample Application

Figure 1 demonstrates a typical TH6503 application. The TH6503 translates the data and control signals received from the USB in a serial format which can be read by the microcontroller. The data is stored in a FIFO buffer and can be called up from a standard microcontroller via a register programmable serial interface at any time and processed further. Data generated by peripheries is passed to the TH6503 with the same protocol and stored in a FIFO buffer until it is collected by the USB. The TH6503 translates all the data in the USB-specific format and generates the necessary control signals. The TH6503 requires a minimum number of external elements and can easily be implemented in a circuitry. It provides an external clock which can be used to activate a microcontroller.

Rev. 3.0

August 1997

Function

USB Data Transmission

The TH6503 supports the USB Specification 1.0 data model.

Data from the USB host to the device and vice versa is transmitted serially. The data are NRZI coded to increase transmission reliability; bit stuffing (inserting an extra 0 bit after any 6 consecutive 1 bits) is performed and a CRC check carried out. Bit stuffing, NRZI coding/decoding and CRC checks or generation are performed within the TH6503.

The data is transmitted in packets. Three types of packets are defined for the USB: token, data and handshake.

The token is always passed on by the host. It contains a PID (packet identifier) which defines the direction of the following data transmission and the address of the device and endpoints to be addressed.

Depending on the previous token command, data is transferred from the USB host to the TH6503 (OUT transfer) or transferred from the TH6503 to the USB host (IN transfer). In the process the respective FIFOs are written (OUT) or read (IN).

The data transfer is concluded with a handshake. If the data has been received successfully, an ACK is sent to the data source. If no data is ready for an IN transfer out of the TH6503, it sends an NAK handshake instead of the data (if endpoint is enabled).

TH6503/ Microcontroller Cooperation

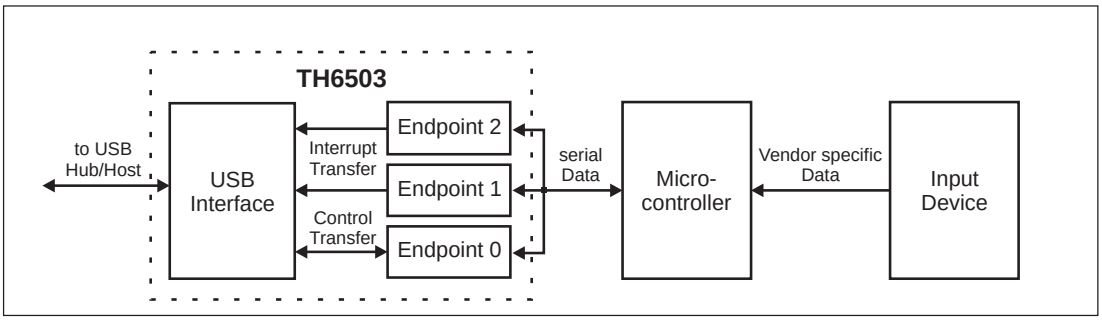


Figure 2. Data Flow

The TH6503 is responsible for the data flow between the USB and the microcontroller. It ensures that the USB transfers the data in line with the protocol. All information in the protocol layer is decoded by the TH6503 and carried out accordingly.

The data arriving from the USB host is stored in a FIFO buffer until it is collected by the microcontroller. Data transmitted to the USB host are imported from a FIFO buffer which has previously been filled by the microcontroller. A /INT signal signals to the microcontroller that the FIFO status has been changed by USB.

Data is transferred between the microcontroller and the TH6503 via a software-emulating serial interface controlled by the microcontroller.

As the TH6503 cannot interpret the content of the data, it must be evaluated within the microcontroller. This also applies to USB-specific control information. All USB-typical descriptors and the associated requests must be created and managed by the microcontroller.

The setting of the USB address serves here as an example. After resetting the USB, the address is set to the default value 0 (USBAddressRegister). A specific address is transferred from the USB host software to the device with the SET_ADDRESS command. This command, like all SET and GET commands, can only be decoded by the microcontroller. The USB address is decoded in the TH6503 with the aid of the USBAddressRegister. For this reason the microcontroller must write the USB address determined in this register.

The TH6503 supports the USB suspend mode. Control takes place via the microcontroller. The ACT bit can be used in the StatusRegister <5> which is set on the USB for each activity. If this bit has been inactive for a longer period of time (3 ms), the microcontroller can set the TH6503 and itself in the suspend mode using the SUS bit in the BridgeConfigRegister <4>. The suspend mode can be ended using the software or an external signal. Apart from the suspend mode, the TH6503 also supports a number of other power saving modes which either stop the microcontroller by switching off the clock or set the whole USB bridge in a power saving mode.

The TH6503 provides the clock pulse for the microcontroller. It can be programmed with the OCR1-OCR0 bits in the BridgeConfigRegister <1-0>.

The TH6503 supplies 3.3V voltage to power the microcontroller; this is produced by the adjacent 5V bus power supply connection.

TH6503/ Microcontroller Cooperation (continued)

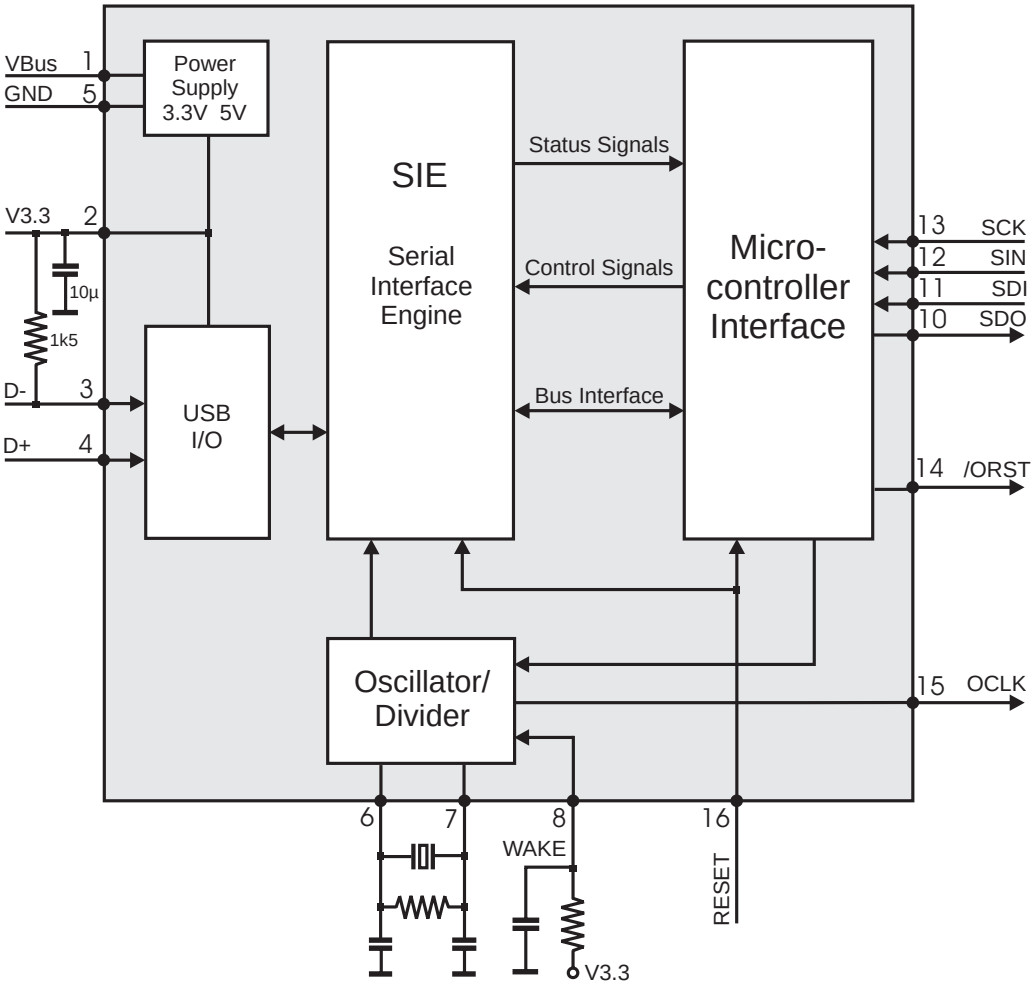


Figure 3. TH6503 Block Diagram

Microcontroller Interface

The data is transferred between the microcontroller and the USB bridge using the clock (SCK) generated by the microcontroller asynchronous to the USB clock.

Data IN Transfer

(from the microcontroller to the TH6503)

Data IN transfer is initiated with rising SIN edge (IN packet sync). Data is transferred via the SDI pin. Initially the Adr/CntInRegister which indicates the internal address in the TH6503 is transferred. Data is subsequently transferred beginning with byte 0 to Byte n. Bits IC3-IC0 in the Adr/CntInRegister <3-0> contain the information on the number of bytes to be transferred to the USB host if the target of the data transfer was an IN FIFO.

A zero data transfer is identified with reset of IC3-IC0 bits after writing the Adr/CntInRegister one additional clock on SCK must be generated.

If a register is the target of the data transfer the bits IC3-IC0 and TI have no meaning.

With falling SCK edge the microcontroller transmit the bits to SDI and the bits are imported from the bridge with increasing SCK edge. After each transmission of 8 bits the respective IN FIFO value is increased by 1. If the microcontroller writes more data than indicated in the Adr/CntInRegister, the oldest data are overwritten. After the final falling edge of SCK first SDI and then SIN must be reset to 0 to terminate the transfer. The associated IN Done bit in the StatusRegister is reset automatically to enable USB IN transfer.

Microcontroller Interface (continued)

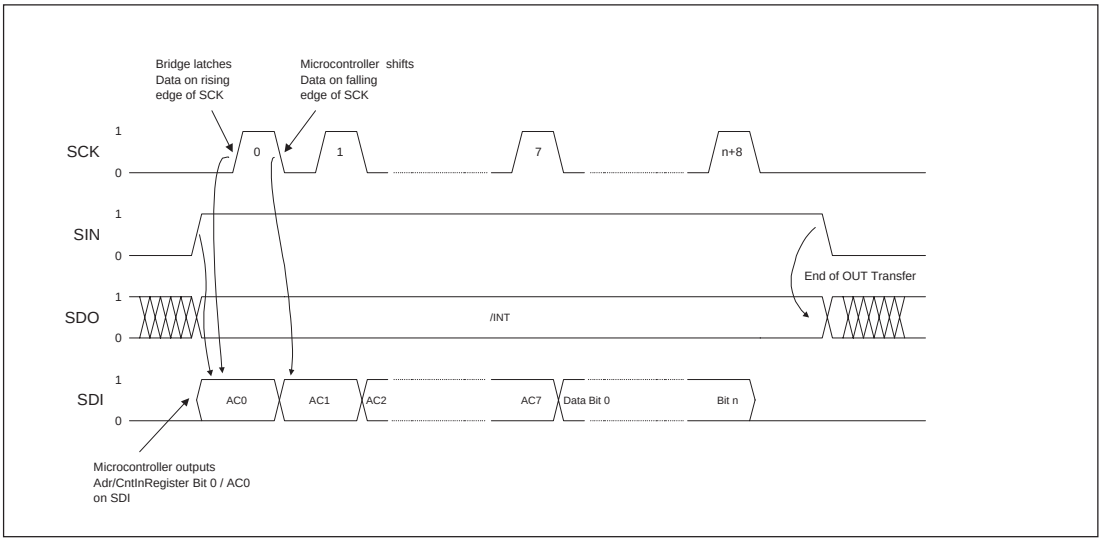


Figure 4. Serial Data IN

Data OUT Transfer

(from the TH6503 to the microcontroller)

An impulse on the SDI link at SIN = 0 represents the OUT packet sync for an OUT transfer. With the falling SCK edge the data (LSB first) is shifted to SDO and with rising SCK edge accepted by the microcontroller. The StatusRegister is transferred initially followed by the CntOutRegister and finally the OUT FIFO data. If the transfer is terminated after less than 8 clock pulses, only single StatusRegister bits are read. Linear transfer is interrupted by SIN = 1 and must be initiated with a new OUT packet sync at SIN = 0. Two impulses on the SDI link initiate a transfer of the CntOutRegisters and of the following OUT FIFO bytes without the StatusRegister. A zero data transfer is identified by an OUT Count Byte value of 0. The end of a Data OUT transfer clears the SET bit in the CntOutRegister and the OD bit in the StatusRegister to make the next USB OUT or Setup transfer possible.

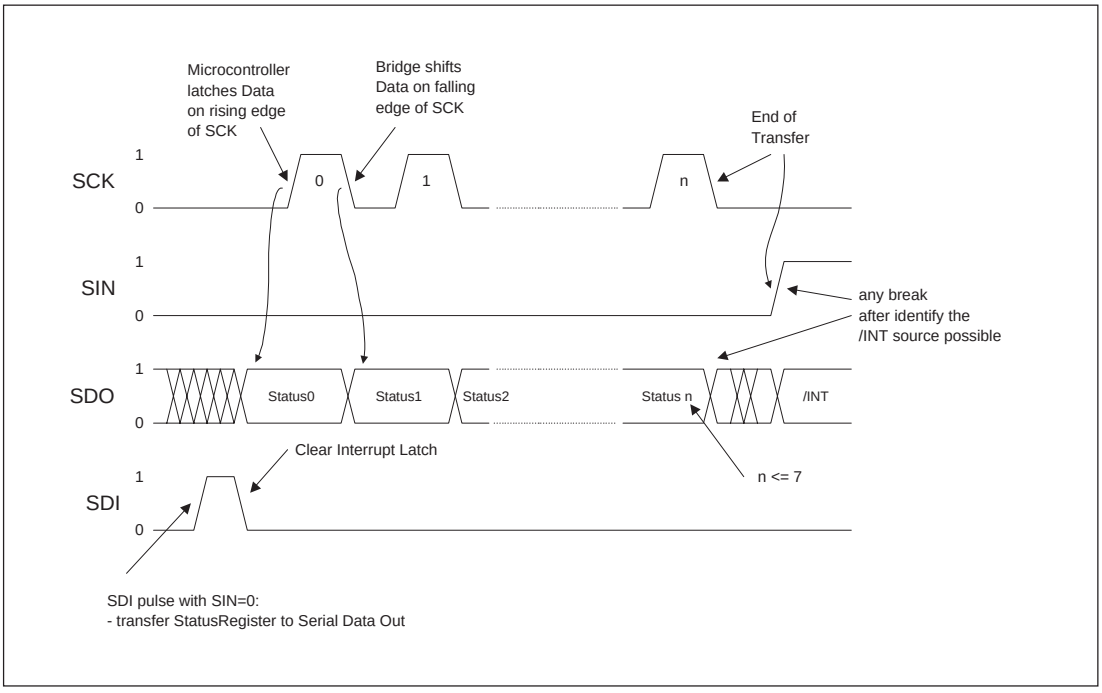


Figure 5. OUT Transfer of StatusRegister

Microcontroller Interface (continued)

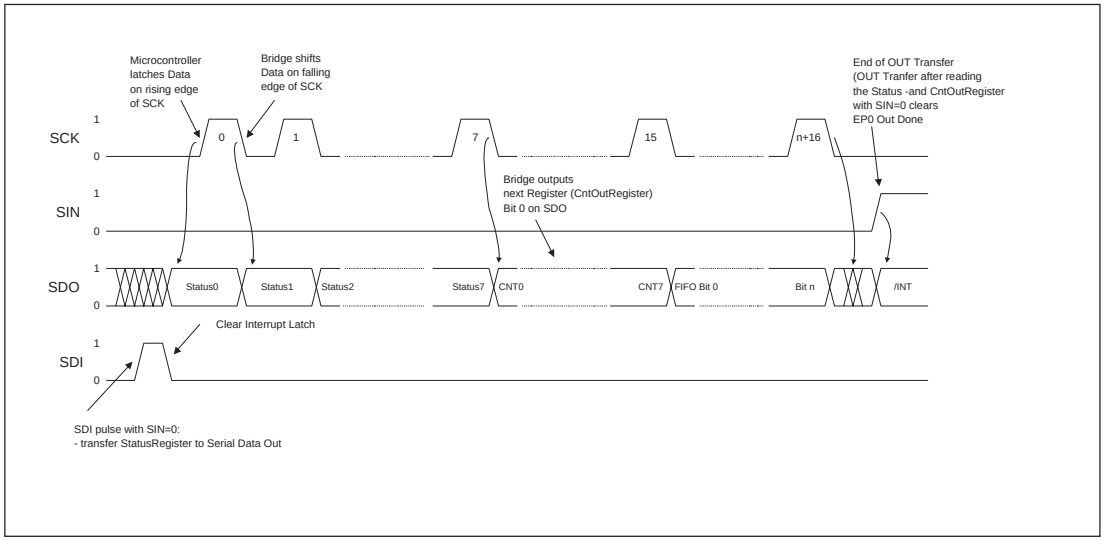


Figure 6. Complete Data OUT Transfer

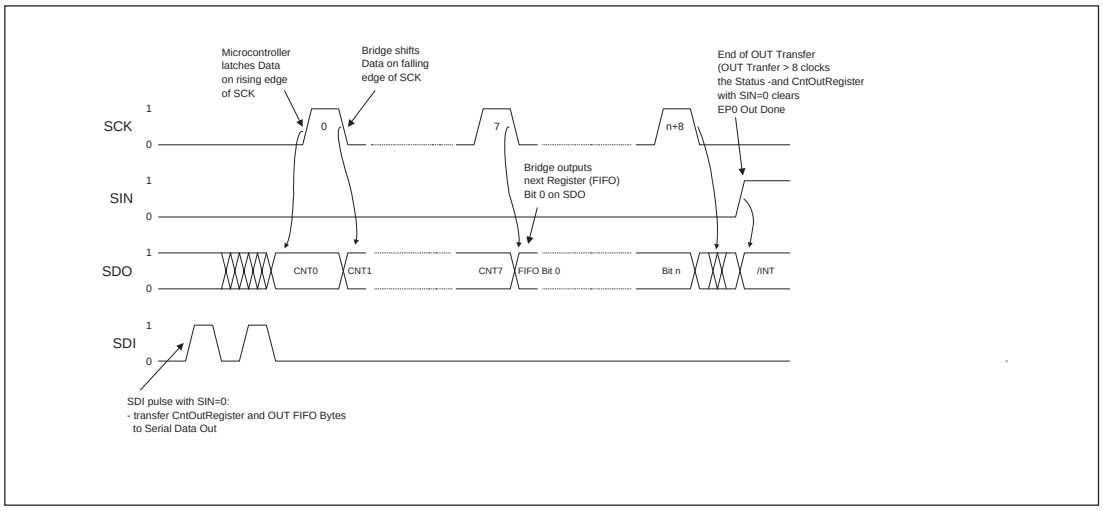


Figure 7. OUT Transfer, only CntOutRegister and OUT FIFO Bytes

Interrupt Function

If SIN = 1, the SDO pin can be used to generate an interrupt signal. The interrupt is low active. It is triggered if a control transfer is made from the USB host or a control or interrupt transfer is made to the USB host and one of the ID12, ID0 or OD bits has been set in the StatusRegister <3-1> or at high level of the WAKE pin. An interrupt signal is also triggered on RESUME and USB_RESET.

The interrupt latch is reset on reading the status register. If an interrupt is generated during reading StatusRegister, this interrupt is latched and after reading visible.

A WAKE interrupt is only generated during the stop state (bits SO and/or SMC in the BridgeConfig Register are set).

Timing Serial Interface

Figure 8 and Figure 9 show the timing of the serial interface of the TH6503. The serial interface is controlled by a standard microcontroller. It can be connected with any microcontroller port.

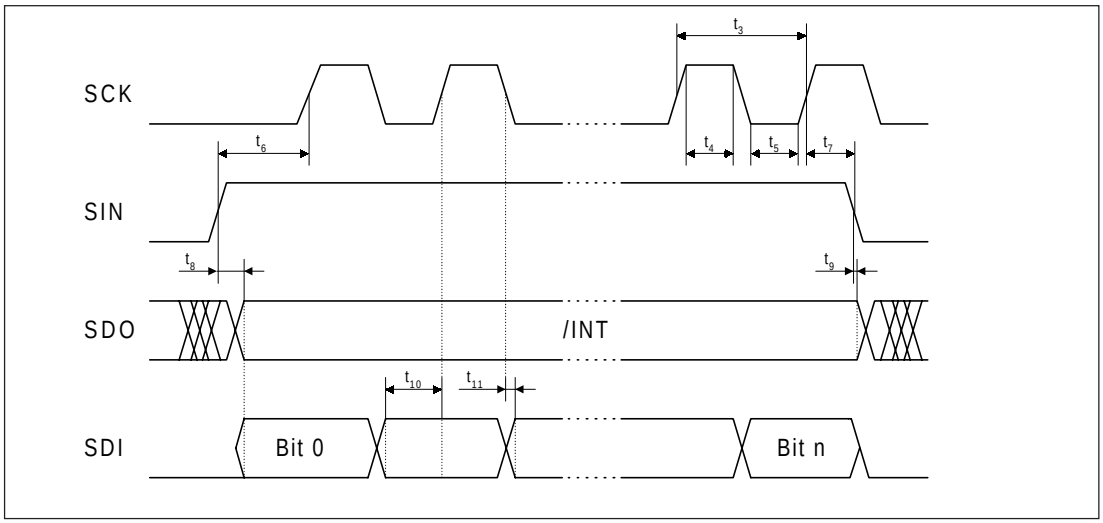


Figure 8. Timing Serial Data IN

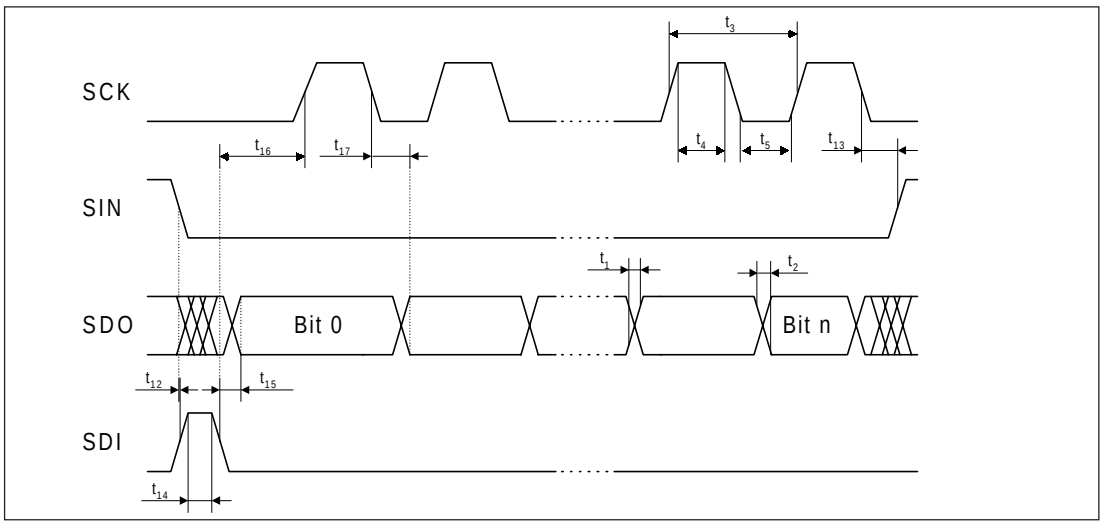


Figure 9. Timing Serial Data OUT

Timing Serial Interface (continued)

Description [1]	Symbol	Unit	min	typ	max
General					
Oscillator Input period on OSC1		ns	164		170
Rising time of SDO	t1	ns		20	
Falling time of SDO	t2	ns		7	
SCK period	t3	ns	600		Step
High time SCK [2]	t4	ns	345		
Low time SCK [2, 3]	t5	ns	255		
Data IN					
Setup time of SCK after rising edge of SIN	t6	ns	170		
Hold time of SIN after last rising edge of SCK	t7	ns	170		
Setup time of INT-Signal after rising edge of SIN	t8	ns			200
Hold time of INT-Signal after falling edge of SIN	t9	ns	165		
Setup time of Data on SDI before rising edge of SCK	t10	ns	170		
Hold time of Data on SDI after falling edge of SCK	t11	ns	0		
Data OUT					
Setup time of SDI-pulse after falling edge of SIN	t12	ns	170		
Setup time of SIN after last falling edge of SCK	t13	ns	170		
High time of SDI-pulse	t14	ns	255		
Setup time of Data on SDO after falling edge of SDI-pulse	t15	ns			280
Setup time of SCK after falling edge of SDI-pulse	t16	ns	170		
Setup time of Data on SDO after falling edge of SCK	t17	ns			365

Notes:
1 Capacitive load of 50 pF
2 Can be asymmetrical
3 The low time of SCK between the last bit of a byte and the first bit of the next byte must be at least 510 ns.

Input signals are double buffered and digital filtered. Therefore all spikes with a width < 255 ns are suppressed.

Connecting the TH6503 with a Microcontroller

The TH6503 can be connected with any micro-controller via a serial interface. The serial outputs can be connected with any microcontroller ports. The TH6503 out clock can be used to provide the clock pulse supply to the microcontroller. The reset output is low active and configured in an open drain structure. For this reason the output must be set at a defined level with external Vcc resistance.

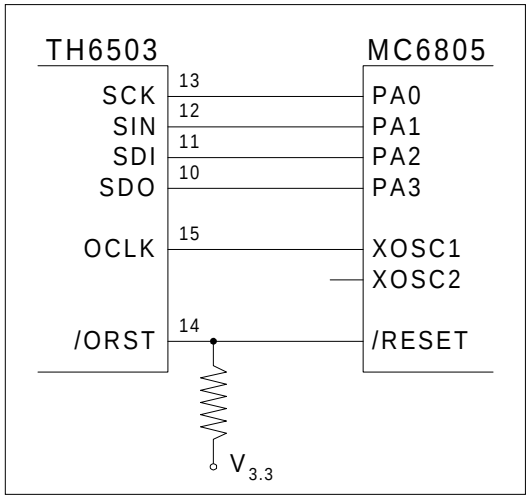


Figure 10. The Connection between the TH6503 and the MC6805 by Motorola

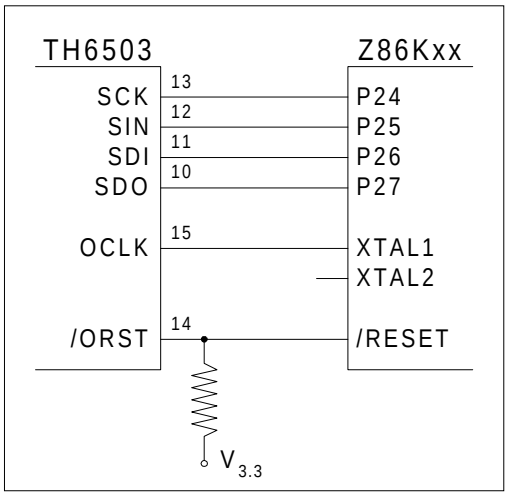


Figure 11. The Connection between the TH6503 and the Z86Kxx by Zilog

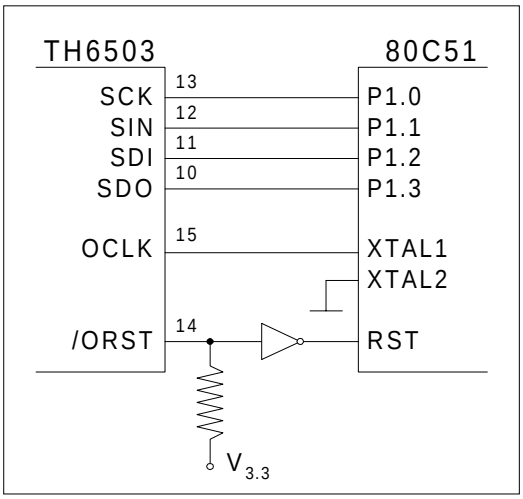


Figure 12. The Connection between the TH6503 and the 80C51 by Intel

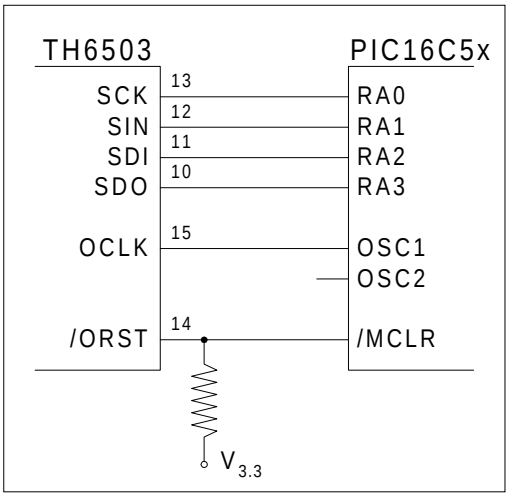


Figure 13. The Connection between the TH6503 and the PIC16C54 by Microchip

Application Wiring Diagram

Figure 14 shows a sample Application circuitry with the TH6503 and a MC68HC05.

To stabilize the internal power supply the V3.3 pin must always be connected with an 10µ capacitor.

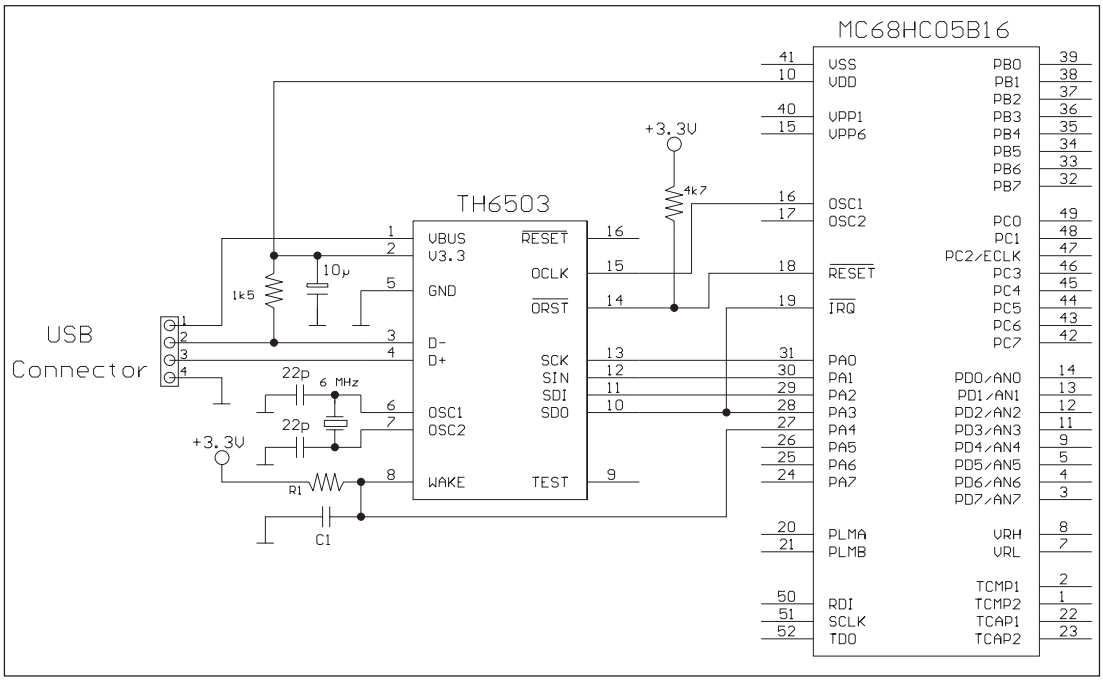


Figure 14. Sample Wiring diagram to connect the TH6503 with an MC68HC05

WAKE Function

The USB specification defines that a device has to go into suspend mode if no bus traffic was detected for ca. 3 ms. After the device is set to suspend mode, the WAKE pin can be used to Wake up the device with an external event.

If the WAKE pin is connected with an RC-Element, the TH6503 wakes up after the time defined by the RC-Element. This feature can be used to check for data in periodical time frames.

RESET Output

The reset output (/ORST) of the TH6503 can be connected with the reset input of the microcontroller. It's a low active signal.

This signal has a minimum length of 31 clock cycles with a frequency of 1.5 MHz (see Pin Description for details).

Register Description

The internal Registers of the TH6503 can only be written by the microcontroller. The StatusRegister and the OUT FIFO can only be read by the microcontroller.

StatusRegister (read only)

always the first byte of a data out transfer

is loaded in the out shift register with the falling edge of an pulse on SDI with SIN=0

Bit Number	Bit Mnemonic	Reset Status	Function
7	HWR	0	**Hardware Reset** ♦ is set if the reset source is POR, RESET pin or low voltage reset ♦ is reset automatically on reading the StatusRegister and also by the following SW-Reset before reading the StatusRegister
6	RES	0	**USB Reset** ♦ is set so long as a reset is received on the USB (SW reset) ♦ is reset automatically on reading the StatusRegister and also by the following HW-Reset before reading the StatusRegister ♦ the reset of this bit enables EP0 Out and EP0 In (EO0 and EI0 bits in the SerialFlag Register are set)
5	ACT	0	**USB Active** ♦ is set when the USB is active (all exept IDLE) ♦ is reset automatically on reading the StatusRegister ♦ can be used by the microcontroller to calculate the suspend time ♦ if set the SO and SMC bits in the BridgeConfigRegister are reset
4	RDT	0	**USB Resume Detect** ♦ is set automatically if a resume status has been decoded ♦ is reset automatically if the resume status has been terminated ♦ if set the SO and SMC bits in the BridgeConfigRegister are reset
3	ID12	1	**EP1/2 IN Done** ♦ is set if the data requested by an IN token have been completely transmitted to the USB host and an ACK has been received ♦ is reset with the falling SIN edge (end of IN transfer)
2	ID0	1	**EP0 IN Done** ♦ is set if data requested by an IN token have been completely transmitted to the USB host and an ACK has been received ♦ is reset with the falling SIN edge (end of IN transfer)
1	OD	0	**OUT Done** ♦ is set automatically if the data are complete in the FIFO after a valid SETUP or OUT token has been received and an ACK has been sent to the USB host ♦ is reset with the rising SIN edge (end of OUT transfer)
0	WA	0	**WAKE Activity** ♦ is set and reset automatically depending on the voltage level at the WAKE pin ♦ is an inverted copy of the WAKE pin and can be used as low active interrupt output

Register Description (continued)

CntOutRegister (read only)

second byte of each out transfer following an OUT packet sync

Bit Number	Bit Mnemonic	Reset Status	Function
7-6	RC		**Revision Control** 00 TH6503.1 and TH6503.2 01 TH6503.3 10 reserved 11 reserved
5	TO	0	**Toggle OUT** ♦ is set if the data packet PID was DATA1 and reset if the data packet PID was DATA0 ♦ is latched with a valid EP0 SETUP or a OUT Token
4	SET	0	**Setup** ♦ is set if a SETUP token is received ♦ is reset after OUT transfer to microcontroller ♦ a STALL or NAK is sent while a SETUP token is not permitted on the EP0 ♦ the SO0 and SI0 (STALL EP0) flags in the USBFlagRegister are reset on rising edge of Setup ♦ a SETUP token flash all IN FIFOs
3-0	OC3-0	0	**EP0 OUT Byte Count** amount of OUT data received in the EP0 FIFO in bytes ♦ applicable values from 0 to 8 ♦ a zero data transfer is identified 0

Adr/CntInRegister (write only)

first byte of each data in transfer following the packet sync

Bit Number	Bit Mnemonic	Reset Status	Function
7	TI	0	**Toggle IN** ♦ is set if the data packet PID is DATA1 and reset if the data packet PID is DATA0
6-4	RA2-0	0	**Internal Address** destination address for a write operation to a TH6503 register
3-0	IC3-0	0	**IN Byte Count** number of data bytes to be transmitted without Adr/CntInRegister from the microcontroller to the TH6503 if the destination address was an IN FIFO ♦ applicable values from 0 to 8 ♦ 0 indicates a zero data transfer to the InFIFO

Register Description (continued)

EP0/1/2 FIFO (write only)

Internal Address: b000, b001 or b010
Size: 8 bytes

The device user data is stored temporarily at this location for transfer to the USB host.

- the address b000 indicates a data transfer from EP0
- the address b001 indicates a data transfer from EP1
- the address b010 indicates a data transfer from EP2
- only one of the three addresses may be used at any one time; FIFO is used alternately, depending on the device function
- will be flushed with a new SETUP token for as long as CntOutRegister.SETUP is set

SerialFlagRegister (write only)

Internal address: b100
Size: 8 bits

All endpoints must remain deactivated until USB reset has been decoded (Statusregister <6>).

Bit Number	Bit Mnemonic	Reset Status	Function
7-6	X	X	reserved - must be set to 0
5	EO2	0	**Enable EP2 OUT** activate endpoint 2 OUT ♦ Only for future implementation of USB Specification ♦ Must be set to 0 to be conform with USB Specification 1.0 ♦ If set the CntOutRegister bit <7-6> show the source of the last OUT transfer binary coded
4	EO1	0	**Enable EP1 OUT** activate endpoint 1 OUT ♦ Only for future implementation of USB Specification ♦ Must be set to 0 to be conform with USB Specification 1.0 ♦ If set the CntOutRegister bit <7-6> show the source of the last OUT transfer binary coded
3	EI2	0	**Enable EP2 IN** activate endpoint 2 IN ♦ Microcontroller can set the bit after detecting a USB reset in order to enable data transfers to the USB host via EP2
2	EI1	0	**Enable EP1 IN** activate endpoint 1 IN ♦ Microcontroller can set the bit after detecting a USB reset in order to enable data transfers to the USB host via EP1
1	EI0	0	**Enable EP0 IN** activate endpoint 0 (IN transfer) ♦ is set automatically after detecting a USB reset to enable IN control transfers to the USB host
0	EO0	0	**Enable EP0 OUT** activate endpoint 0 (OUT transfer) ♦ is set automatically after detecting a USB reset to enable OUT control transfers to the USB host

Register Description (continued)

USBFlagRegister (write only)

Internal address: b101

Size: 8 bits

Bit Number	Bit Mnemonic	Reset Status	Function
7	FI2	1	**Flush EP2 IN** clears EP2 FIFO ♦ is set and reset automatically depending on the actual FIFO Status ♦ must be set before EP2 of the EP1/2 FIFO can be overwritten by the microcontroller
6	FI1	1	**Flush EP1 IN** clears EP1 FIFO ♦ is set and reset automatically depending on the actual FIFO Status ♦ must be set before EP1 of the EP1/2 FIFO can be overwritten by the microcontroller
5	FI0	1	**Flush EP0 IN** clears EP0 FIFO ♦ is set and reset automatically depending on the actual FIFO Status ♦ must be set before the EP0 FIFO can be overwritten by the microcontroller
4	BO0	0	**Busy OUT** blocks the EP0 OUT FIFO for the USB host ♦ is set and reset automatically depending on the actual FIFO Status ♦ TH6503 responds with no handshake for a USB host SETUP token or with a NAK signal for an OUT token (NAK state) ♦ to leave the NAK state, the microcontroller does an OutFIFO read (the microcontroller rereads the last data)
3	SI2	0	**STALL EP2** sets EP2 to STALL ♦ TH6503 responds with a STALL for a USB host IN or OUT token if the address and EP2 have been decoded ♦ only operative if EP2 is active
2	SI1	0	**STALL EP1** sets EP1 to STALL ♦ TH6503 responds with a STALL for a USB host IN or OUT token if the address and EP1 have been decoded ♦ only operative if EP1 is active
1	SI0	0	**STALL EP0 IN** sets EP0 In to STALL ♦ TH6503 responds with a STALL for a USB host IN token if the address and EP0 have been decoded
0	SO0	0	**STALL EP0 OUT** sets EP0 OUT to STALL ♦ TH6503 responds with a STALL for a USB host OUT token, if the address and EP0 have been decoded ♦ STALL is inoperative for a SETUP token from the USB host

USBAddressRegister (write only)

Internal address: b110

Size: 8 bits

Bit Number	Bit Mnemonic	Reset Status	Function
7	X	0	reserved
6-0	AD6-0	0	**USB device address** USB address entered by microcontroller ♦ zero after reset ♦ microcontroller must decode the address from descriptor data after a SETUP (SET_ADDRESS) token and write it in this register

Register Description (continued)

BridgeConfigRegister (write only)

Bits only take effect after the linear transfer has been completed.

Internal address: b111

Size : 8 bits

Bit Number	Bit Mnemonic	Reset Status	Function
7	X	0	reserved
6	OS	0	**OCLK Static** ♦ is set and reset by microcontroller ♦ if set the OCLK pin drives a static level on the OCLK pin, this level depends on the SMC bit in the BridgeConfigRegister OS SMC OCLK Output 0 0 Clock, programmed by OCR<1-0> bits 0 1 0 1 0 0 1 1 1 ♦ can be used as signal for an external microcontroller with own clock for ending stop state ♦ works like a low active interrupt
5	FR	0	**Force Resume** terminates suspend mode ♦ is set by microcontroller if data is sent from connected device ♦ the TH6503 signals a Resume to the USB host ♦ the timing (10-15 ms) of the Resume State must be done by microcontroller
4	SUS	0	**Suspend** sets the TH6503 in suspend mode ♦ should be set by the microcontroller if no bus traffic is detected for longer than 3 ms ♦ can be set and reset by microcontroller only
3	SO	0	**Stop Oscillator** stops the microcontroller and the USB bridge (the SMC bit is set automatically) ♦ is set by the microcontroller ♦ is reset by an external wake up signal, USB activity or reset
2	SMC	0	**Stop Microcontroller Clock** stops the microcontroller ♦ is set by the microcontroller ♦ is reset by an external wake up signal, USB activity or reset ♦ only affects the OCLK pin
1-0	OCR1-0	0 0	**Out Clock Rate** output frequency on the OCLK pin 0 0 1.5 MHz (default) 0 1 2.0 MHz 1 0 3.0 MHz 1 1 6.0 MHz, without guarantee of symmetry, it depends on the quality of the oscillation element

Flowchart for Programming the TH6503

Main Program

Figure 15 shows the main order of events of the USB specific part of firmware for the microcontroller. The bits located in the StatusRegister mark the event. Depending on these bits the firmware must branch.

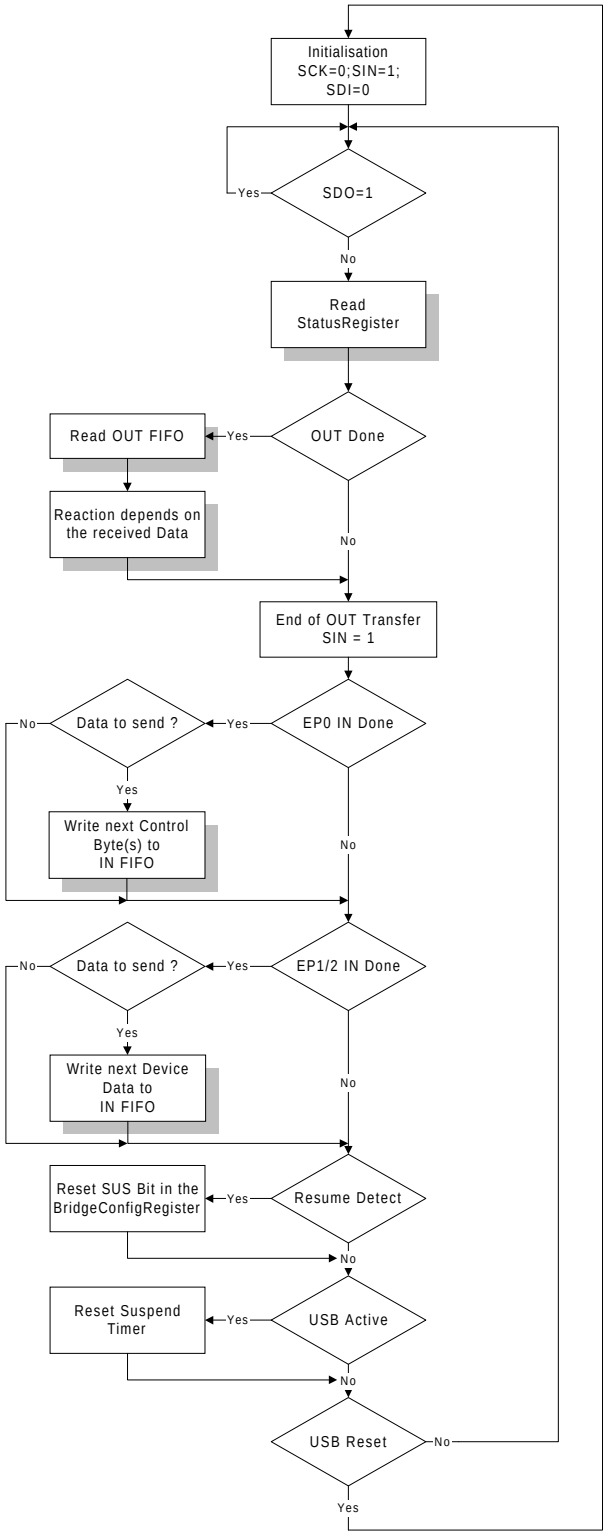


Figure 15. Flowchart for Main Program

Flowchart for Programming the TH6503 (continued)

Reading the StatusRegister

The Reading of the Status Register is the first action of the microcontroller. The TH6503 stores the information on what's happened on the USB in this Register

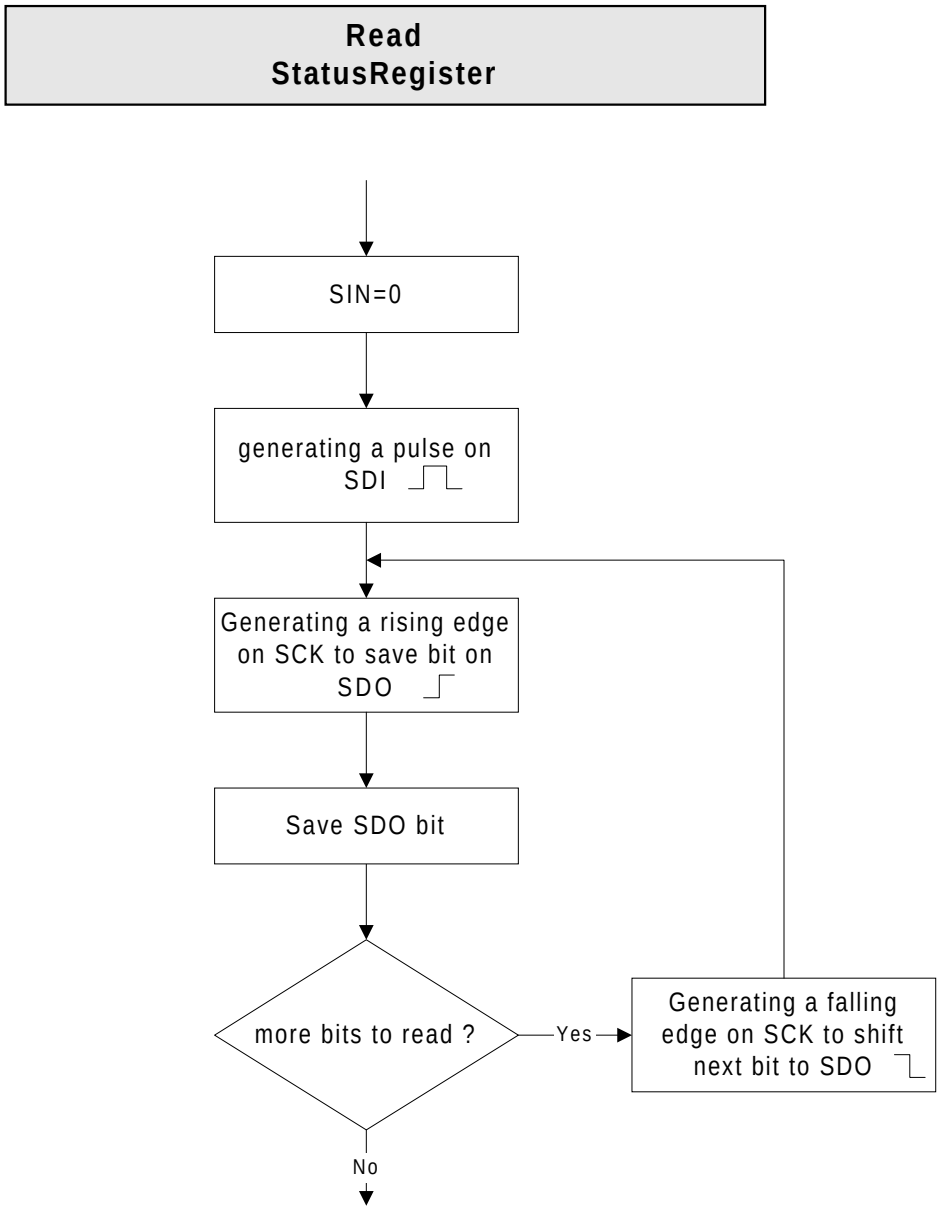


Figure 16. Reading the StatusRegister

Flowchart for Programming the TH6503
(continued)

Reading the OUT FIFO

If the EP0 Done bit in the StatusRegister is set, the microcontroller must receive the data collected from the OUT FIFO.

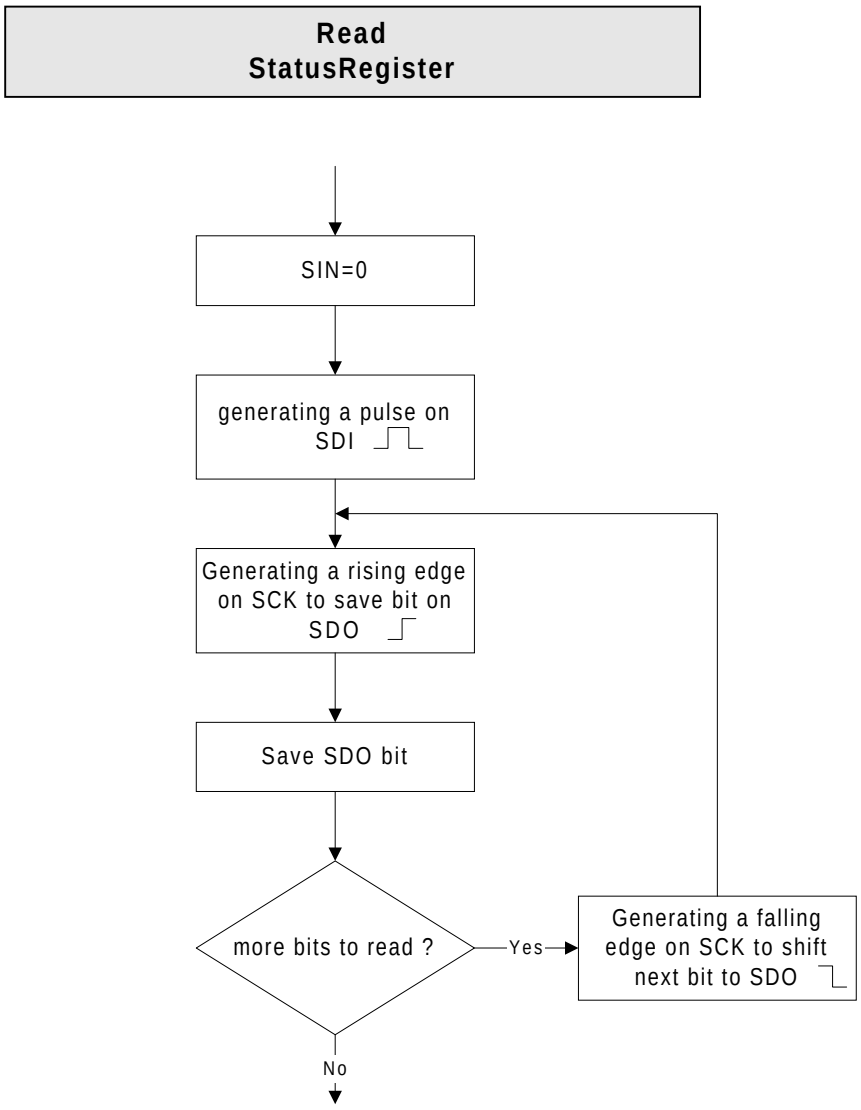


Figure 17. Reading the OUT FIFO

Flowchart for Programming the TH6503
(continued)

Reaction on the FIFO data

After the microcontroller has collected the FIFO data, the microcontroller must decode the FIFO data and reacts appropriately.

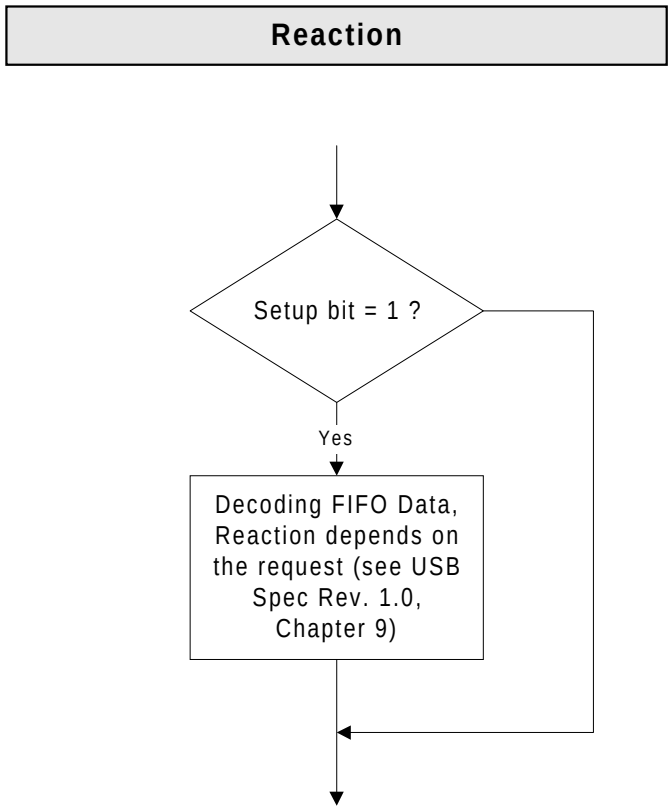


Figure 18. Reaction on the received Data

Flowchart for Programming the TH6503
(continued)

Write to IN FIFO

If data has to be sent to the USB host the microcontroller must wait until the corresponding IN DONE bit is set (IN FIFO is empty). Then the microcontroller can store the data in the IN FIFO.

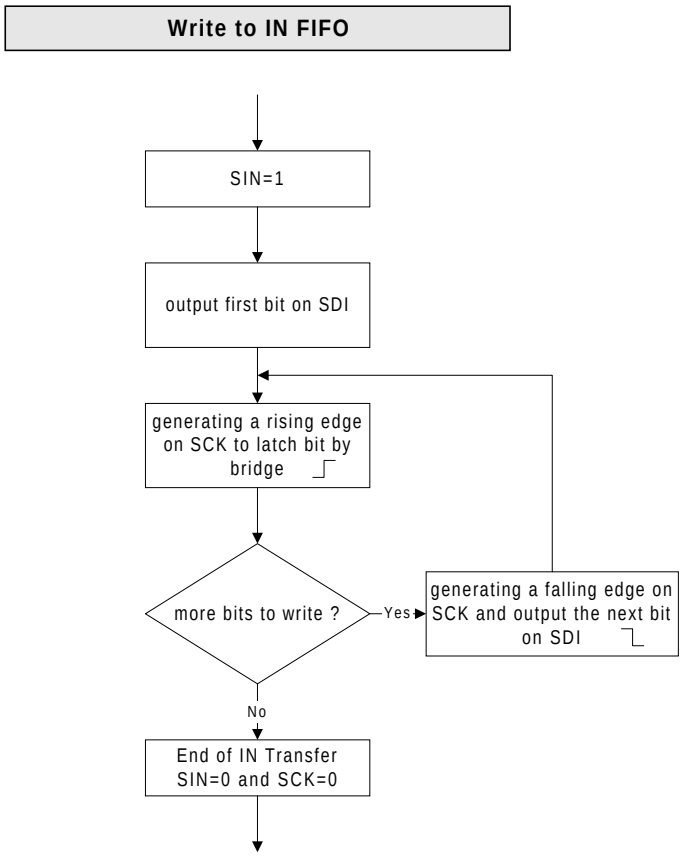


Figure 19. Writing to IN FIFO

Electrical Characteristics

All voltage values are referenced to GND (GND = 0 V). All values are based on the USB specification V1.0. If any value is unspecified, the value from the USB specification V1.0 is valid.

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
DC supply voltage	VDD	- 0.3	7.0	V
Input voltage	VIN	- 0.3	V3.3 + 0.3	V
Output Voltage	VOUT	- 0.3	V3.3 + 0.3	V
Input Current	I IN	- 10	10	mA
Storage temperature range (ceramic)	TSTGC	- 65	150	°C
Storage temperature range (plastic)	TSTGP	- 40	125	°C
Power Dissipation (SOP16)	PD		600	mW

Recommended Operational Conditions

Parameter	Symbol	Min	Typ	Max	Unit
DC supply voltage	VDD	4.40	5.00	5.25	V
Operating temperature range	TA	0		70	°C
Junction temperature	TJ			< 150	°C
Operating Frequency	FOP	6.00			MHz

Electrical Characteristics

Static Characteristics

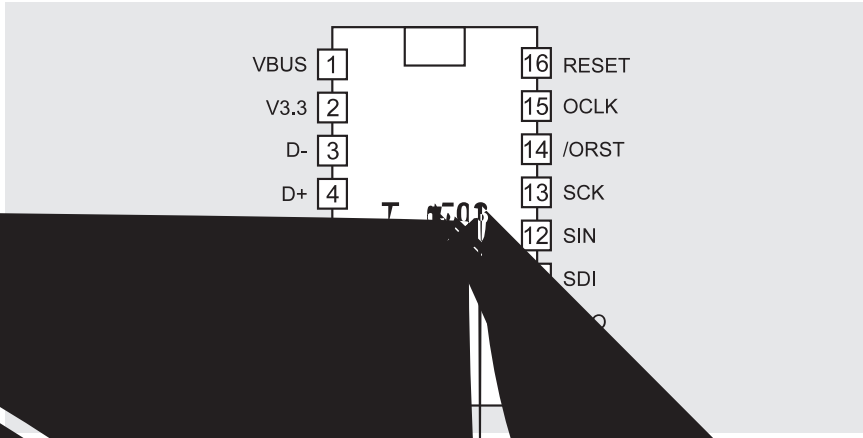
Parameter	Symbol	Condition[4]	Min	Typ	Max	Unit
Power supply voltage	V3.3		3.00	3.30	3.60	V
Power supply current	I3.3				60	mA
Stand-by Current [5]	ISTB			80	150,00	µA
Voltage input LOW	VILCMOS				0.3V3.3	V
Voltage input HIGH	VIHCMOS		0.7 V3.3			V
Schmitt trigger, positive going threshold	VT+CMOS				2.4	V
Schmitt trigger, negative going threshold	VT-CMOS		0.8			V
Hysteresis, Schmitt trigger (VT+ – VT-)	VHYSCMOS	VIL to VIH,VIH to VIL	0.5			V
Differential Input Sensitivity	VDI	|(D+)-(D-)|	0.2			V
Differential Common Mode Range	VCM	Includes VDI	0.8		2.5	V
Single Ended Receiver Threshold	VSE		0.8		2.0	V
Single Ended Receiver Hysteresis	VHYSE		0.1			V
Input low current	IIL	VIN = GND	-10		10	µA
Input with pullup	IILU	VIN = GND	-50	-21.0	-7	µA
Input high current	IIH	VIN = V3.3	-10		10	µA
Input with pulldown	IIHD	VIN = V3.3	7	22.9	65	µA
Voltage output LOW	VOL	IOL = 1 mA			0.4	V
Voltage output HIGH	VOH	IOH = 1 mA	2.4			V
Differential output LOW	VOLD	RL of 15 Kohms to GND	2.8		3.6	V
Differential output HIGH	VOHD	RL of 1.5 Kohms to 3.6 V			0.3	V
Hi-Z Output Leakage Current	IOZ	VIN = GND or V3.3	-10		10	µA

Notes:
4 Specified at VDD = VBUS = 4.40V to 5.25V and tested at room temperature only
5 Differential Transceiver fs in Suspend Mode, tested without pull-down and pullup Resistors on the D- and D+ data line

Pin Description

Pin Description			
USB Interface			
1	VBus	I	adjacent 5V bus voltage
5	GND	I	Ground
4	D+	I/O	USB data
3	D-	I/O	USB data ♦ must be connected via 1.5 kOhm resistor to 3.3 V for low speed devices
Microcontroller Interface			
13	SCK	I	Serial Clock (generated by microcontroller) ♦ OUT transfer: SDO is accepted by the microcontroller in high status or with falling SCK edge. The USB bridge shifts the next bit to SDO in low status or with rising edge. ♦ IN Transfer: SDI is accepted by the USB bridge in high status or with falling SCK edge. ♦ The microcontroller shifts the next bit to SDI in low status or with rising edge. ♦ internal pulldown
12	SIN	I	Serial Input Direction (generated by the microcontroller) ♦ specifies the direction of the data transfer and marks the end of a FIFO transfer ♦ SIN = 0: data is sent from the USB bridge to the microcontroller via SDO. An OUT packet sync for the StatusRegister or CntOutRegister can be triggered via SDI. A rising edge terminates a status or OUT transfer and the USB OUT Done status bit is cleared. ♦ SIN = 1: Data is sent from the microcontroller to the USB bridge via SDI. SDO emits an /INT signal. A falling edge terminates an IN transfer and the EP0 IN Done or EP1/2 IN Done status bit is cleared if the destination address is a FIFO address. ♦ rising edge indicates the commencement of an IN transfer (IN packet sync). The IN is started once SCK is pulsed. The Adr/CntInRegister is transferred initially. ♦ internal pulldown
11	SDI	I	Serial Data IN (from the microcontroller to the USB bridge) ♦ generated by the microcontroller ♦ SIN = 0: the falling edge from a single SDI impulse loads the first bit (LSB first) of the StatusRegisters to SDO. The StatusRegister can be read. Two SDI impulses load the first bit of the CntOutRegister. ♦ SIN = 1: SDI transfers the serial data. ♦ internal pulldown
10	SDO	O	Serial Data Out (from the USB bridge to the microcontroller) ♦ generated by the USB bridge ♦ SIN = 0: SDO show the Status of bit 0 of the StatusRegister (WA) and after a SDI pulse SDO transfers the serial data. ♦ SIN = 1: SDO is used to generate the /INT signal which can be used to control the microcontroller interrupt ♦ /INT: - Low active signal to SDO at SIN 1 - is a NOR connection of the RESUME signal, USB reset and an interrupt latch - Interrupt latch is set for all increases in OUTDone, EP0 IN Done and EP1/2 IN Done edge. - Interrupt latch is reset, if the StatusRegister is read (SDI impulse at SIN= 0).
15	OCLK	O	Clock out for microcontroller (programmable frequency)
14	/ORST	open drain	Reset Out (HW- or SW reset) ♦ ORST=0 reset state ♦ ORST=1 normal operation ♦ must be connected with an external pullup resistor (to V3.3) ♦ all resets are indicated on this pin ♦ this type of reset can be determined by evaluating the bits POR or BUSR in the StatusRegister <7> or <6> ♦ Reset conditions: - internal POR - RESET pin - min. 20µs (31 OCLK cycles at 1.5 MHz) or as long as the RESET pin is active - Low voltage reset if VBUS<3.3V ± 10% with a minimum of 20 µs (31 OCLK cycles at 1.5 MHz) or as long as VBUS < 3.3V - USB-Reset - reduced to 20 µs (31 OCLK cycles at 1.5 MHz), the end of a USB reset is indicated by a rising edge of /INT and by cleared RES bit in the StatusRegister
Miscellaneous			
6	OSC1	I	Oscillator In for a quartz, ceramic resonator or external clock input, 6 MHz ± 1.5%
7	OSC2	O	Oscillator Out
8	WAKE	I	♦ if a specific trigger level is reached (Schmitt Trigger Characteristic) the USB bridge oscillator is restarted and the SO and SMC bit in the BridgeConfigRegister is cleared. ♦ it may be connected to an RC element to achieve restart cycles from 50 to 100 ms ♦ the input signal is compatible with large slew rate ♦ if the SO or SMC bit in the BridgeConfigRegister is set a rising edge on the WAKE pin generates an interrupt signal on SDO
16	/RESET	I	RESET input with Schmitt-Trigger characteristic (internal pullup)
2	V3.3	O	3.3 V output must be connected with an external capacitor (approx. 10µ)
9	TEST	I	♦ Test pin, internal pulled up (do not connect to external circuitry)

Pinout Information (Top View)



Package Information (SOP 16 WB)

Small Ou… SOP 16…						
Pa…					α	…ge Code
S…			…13 0.020	0.012 0.050	10 °	…16
			…nch			
	…62	0.05 0.36	1.27	0.33 0.51	0.30 1.27	10 °	DF16
…1 mm, original dimension: inch						

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…SB Low-Speed Interface is available in a 16 pin SOP WB package.

…er number is

Quality data is available on request. Contact: **Quality Data**

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