DATA SHEET

TDA9965

12-bit, 5.0 V, 30 Msps analog-to-digital interface for CCD cameras

Preliminary specification
Supersedes data of 2001 May 31
File under Integrated Circuits, IC02

2002 Feb 07

Philips
Semiconductors

PHILIPS

FEATURES

- Clamp and Track/Hold (CTH) circuit with adjustable bandwidth, Programmable Gain Amplifier (PGA), 12-bit Analog-to-Digital Converter (ADC) and reference regulator
- Fully programmable via a 3-wire serial interface
- Sampling frequency up to 30 MHz
- PGA gain from 0 to 36 dB (in 0.05 dB steps)
- CTH programmable bandwidth from 35 to 284 MHz typical
- Standby mode (20 mW typical)
- Low power consumption of only 425 mW typical
- 5 V operation and 2.5 to 5.25 V operation for the digital outputs
- TTL compatible inputs; TTL and CMOS compatible outputs.

APPLICATIONS

- CCD camera systems.

GENERAL DESCRIPTION

The TDA9965 is a 12-bit analog-to-digital interface for CCD cameras. The device includes a CTH circuit, PGA and a low-power 12-bit ADC, together with its reference voltage regulator.

The CTH has a bandwidth circuit controlled by on-chip DACs via a serial interface.

A 10-bit digital clamp controls the ADC input clamp level.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9965HL	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.75	5	5.25	V
V_{CCD}	digital supply voltage		4.75	5	5.25	V
V_{CCO}	digital output supply voltage		2.5	3	5.25	V
I_{CCA}	analog supply current	with internal regulator	–	65	–	mA
I_{CCD}	digital supply current	with internal regulator	–	19	–	mA
I_{CCO}	digital output supply current	f_{pix} = 30 MHz; C_L = 10 pF on all data outputs; ramp input	–	1	–	mA
ADC_{res}	ADC resolution		–	12	–	bits
$V_{i(IN)(p-p)}$	CTH input voltage (peak-to-peak value)		–	2	–	V
G_{CTH}	CTH output amplifier gain		–	0	–	dB
PGA_{dyn}	PGA dynamic range		–	36	–	dB
$f_{pix(max)}$	maximum pixel frequency	code $f_{co(CTH)}$ = 0000	30	–	–	MHz
$N_{tot(rms)}$	total noise from CTH input to ADC output (RMS value)	G_{PGA} = 0 dB; code $f_{co(CTH)}$ = 0000	–	0.75	–	LSB
$V_{n(i)(eq)(rms)}$	equivalent input noise (RMS value)	G_{PGA} = 36 dB; code $f_{co(CTH)}$ = 0000	–	75	–	μV
P_{tot}	total power consumption		–	425	–	mW

BLOCK DIAGRAM

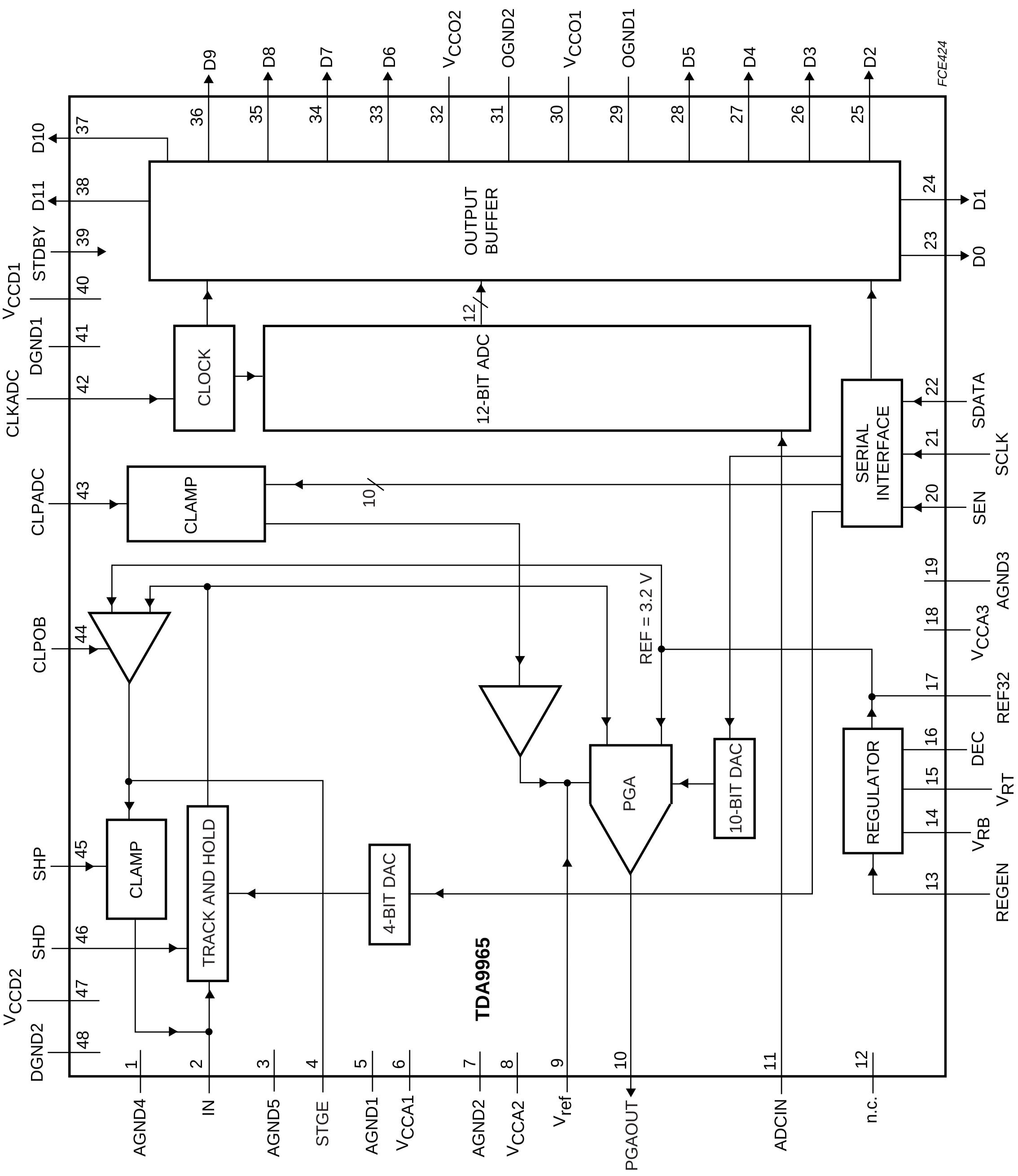


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
AGND4	1	analog ground 4
IN	2	data input signal from CCD
AGND5	3	analog ground 5
STGE	4	clamp storage capacitor pin
AGND1	5	analog ground 1
V_{CCA1}	6	analog supply voltage 1
AGND2	7	analog ground 2
V_{CCA2}	8	analog supply voltage 2
V_{ref}	9	ADC clamp reference voltage input; short-circuited to ground via a capacitor
PGAOUT	10	PGA amplifier signal output
ADCIN	11	ADC analog signal input; externally connected to pin PGAOUT
n.c.	12	not connected
REGEN	13	regulator enable input (active HIGH)
V_{RB}	14	regulator reference voltage bottom
V_{RT}	15	regulator reference voltage top
DEC	16	regulator decoupling; decoupled to ground via a capacitor
REF32	17	internal reference voltage; decoupled to ground via a capacitor
V_{CCA3}	18	analog supply voltage 3
AGND3	19	analog ground 3
SEN	20	enable input for the serial interface shift register (active LOW)
SCLK	21	serial clock input for the serial interface
SDATA	22	serial data input: 10-bit PGA gain, 4-bit DAC for the frequency cut-off, 10 low significant bits for the digital ADC clamp and edge pulse control
D0	23	ADC digital output 0 (LSB)
D1	24	ADC digital output 1
D2	25	ADC digital output 2
D3	26	ADC digital output 3
D4	27	ADC digital output 4
D5	28	ADC digital output 5
OGND1	29	digital output ground 1
V_{CCO1}	30	digital output supply voltage 1
OGND2	31	digital output ground 2
V_{CCO2}	32	digital output supply voltage 2
D6	33	ADC digital output 6
D7	34	ADC digital output 7
D8	35	ADC digital output 8
D9	36	ADC digital output 9
D10	37	ADC digital output 10
D11	38	ADC digital output 11 (MSB)
STDBY	39	standby control input (active HIGH); all output bits are logic 0 when standby is enabled

SYMBOL	PIN	DESCRIPTION
V_{CCD1}	40	digital supply voltage 1
DGND1	41	digital ground 1
CLKADC	42	ADC clock input
CLPADC	43	clamp control pulse input for ADC analog input signal
CLPOB	44	clamp control pulse input at optical black
SHP	45	preset sample hold pulse input
SHD	46	data sample and hold pulse input
V_{CCD2}	47	digital supply voltage 2
DGND2	48	digital ground 2

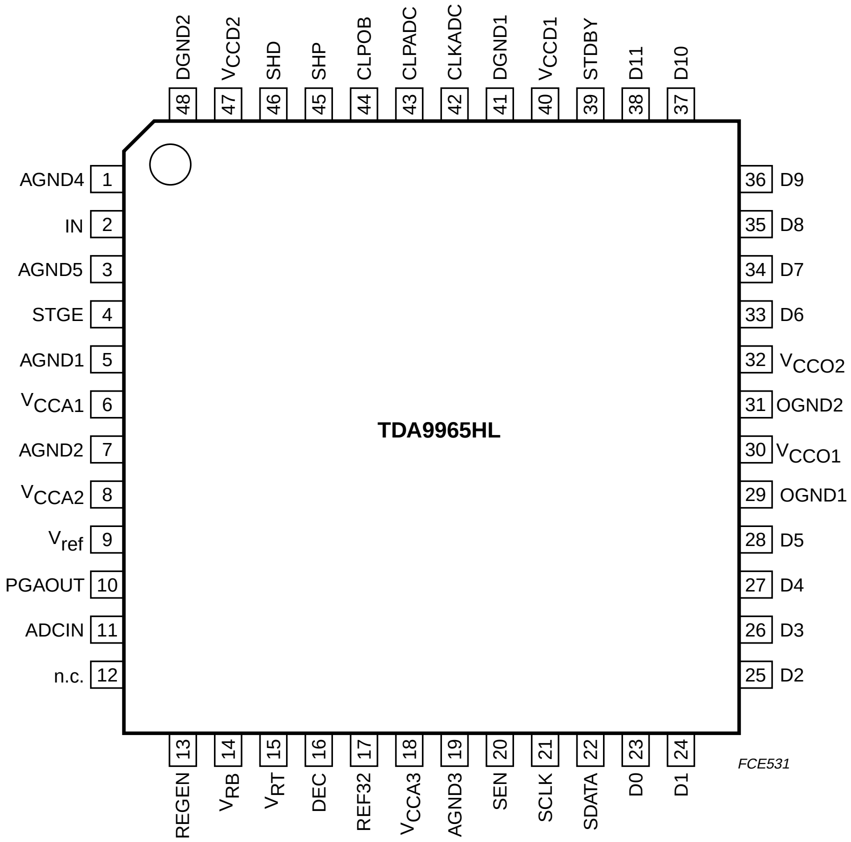


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage	note 1	–0.3	+7.0	V
V_{CCD}	digital supply voltage	note 1	–0.3	+7.0	V
V_{CCO}	digital output supply voltage	note 1	–0.3	+7.0	V
ΔV_{CC}	supply voltage difference				
	between V_{CCA} and V_{CCD}		–1.0	+1.0	V
	between V_{CCD} and V_{CCO}		–1.0	+4.0	V
V_i	input voltage	referenced to AGND	–0.3	+7.0	V
I_o	output current		–10	+10	mA
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		–20	+75	°C
T_j	junction temperature		–	150	°C

Note

1. All supplies are connected together.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j\text{-}a)}$	thermal resistance from junction to ambient	in free air	76	K/W

CHARACTERISTICS

$V_{CCA} = V_{CCD} = 5$ V; $V_{CCO} = 3$ V; $f_{pix} = 30$ MHz; $T_{amb} = -20$ to +75 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CCA}	analog supply voltage		4.75	5	5.25	V
V_{CCD}	digital supply voltage		4.75	5	5.25	V
V_{CCO}	digital output supply voltage		2.5	3	5.25	V
I_{CCA}	analog supply current	with internal regulator	–	65	–	mA
I_{CCD}	digital supply current	with internal regulator	–	19	–	mA
I_{CCO}	digital output supply current	$f_{pix} = 30$ MHz; $C_L = 10$ pF on all data outputs; ramp input	–	1	–	mA
Digital inputs						
CLOCK INPUT: PIN CLKADC (REFERENCED TO DGND)						
V_{IL}	LOW-level input voltage		0	–	0.8	V
V_{IH}	HIGH-level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW-level input current	$V_{CLKADC} = 0.8$ V	–1	–	+1	µA
I_{IH}	HIGH-level input current	$V_{CLKADC} = 2.0$ V	–	–	20	µA
Z_i	input impedance		–	63	–	kΩ
C_i	input capacitance		–	1	–	pF
CONTROL INPUTS: PINS SEN, SCLK, SDATA, STDBY, CLPOB, CLPADC AND REGEN						
V_{IL}	LOW-level input voltage		0	–	0.8	V
V_{IH}	HIGH-level input voltage		2.0	–	V_{CCD}	V
I_i	input current		–2	–	+2	µA
SAMPLE AND HOLD INPUTS: PINS SHP AND SHD						
V_{IL}	LOW-level input voltage		0	–	0.8	V
V_{IH}	HIGH-level input voltage		2.0	–	V_{CCD}	V
I_i	input current		–10	–	+10	µA
Clamp and Track/Hold (CTH) circuit: pins IN, SHD and SHP						
$V_{i(IN)(p-p)}$	CTH input voltage (peak-to-peak value)		–	2	–	V
$I_{i(IN)}$	input current		–3	–	+3	µA
$t_{W(SHP)}$	SHP pulse width	$V_{i(IN)} = 1000$ mV; transition (99%) in 1 pixel; code $f_{co(CTH)} = 0000$; see Fig.5	9	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{W(SHD)}$	SHD pulse width	$V_{i(IN)}$ = 1000 mV; transition (99%) in 1 pixel; code $f_{co(CTH)}$ = 0000; see Fig.5	9	–	–	ns
		code $f_{co(CTH)}$				
		0000	–	8	–	ns
		0001	–	13	–	ns
		0010	–	17	–	ns
		0100	–	23	–	ns
		1000	–	33	–	ns
		1111	–	51	–	ns
$t_{h(IN\text{-}SHP)}$	CTH input hold time compared to control pulse SHP	see Fig.5	–	3	–	ns
$t_{h(IN\text{-}SHD)}$	CTH input hold time compared to control pulse SHD	see Fig.5	–	3	–	ns
Programmable Gain Amplifier (PGA) output: pin PGAOUT						
$V_{PGAOUT(p\text{-}p)}$	PGA output amplifier dynamic voltage level (peak-to-peak value)		–	2000	–	mV
$V_{PGAOUT(b)}$	PGA output amplifier black level voltage	code $C_{(CLP)}$ = 0	–	1.475	–	V
Z_{PGAOUT}	PGA output amplifier output impedance	$f_{(pix)}$ at 10 kHz for minimum and maximum values	–	5	–	Ω
I_{PGAOUT}	PGA output current drive	static	–	–	1	mA
$G_{PGA(min)}$	minimum gain of PGA circuit	code G_{PGA} = 0	–	0	–	dB
$G_{PGA(max)}$	maximum gain of PGA circuit	code G_{PGA} ≥767	–	36	–	dB
Analog-to-Digital Converter (ADC)						
$f_{pix(max)}$	maximum pixel frequency		30	–	–	MHz
$t_{W(CLKADC)H}$	CLKADC pulse width HIGH	$V_{i(IN)}$ = 1000 mV; transition (99.5%) in 1 pixel; code $f_{co(CTH)}$ = 0000; code G_{PGA} = 128; see Fig.5	12	–	–	ns
$t_{W(CLKADC)L}$	CLKADC pulse width LOW	$V_{i(IN)}$ = 1000 mV; transition (99.5%) in 1 pixel; code $f_{co(CTH)}$ = 0000; code G_{PGA} = 128	12	–	–	ns
SR_{CLKADC}	CLKADC input slew rate	rising and falling edges; 10% to 90%	0.5	–	–	V/ns
$V_{i(ADCIN)(p\text{-}p)}$	ADC input voltage (peak-to-peak value)	with internal regulator	–	2	–	V
$I_{i(ADCIN)}$	ADC input current		–2	–	+120	µA
V_{RB}	ADC reference voltage bottom		–	1.30	–	V
V_{RT}	ADC reference voltage top		–	3.65	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DNL	differential non linearity	ramp input	–	±0.5	±0.9	LSB
$t_{d(s)}$	sampling delay	see Fig.5	–	–	5	ns
Total chain characteristics (CTH + PGA + ADC)						
$t_{d(SHD\text{-}CLKADC)}$	time delay between SHD and CLKADC	$V_{i(IN)}$ = 1000 mV; transition (99%) in 1 pixel; code $f_{co(CTH)}$ = 0000; code G_{PGA} = 128; see Fig.5	–	16	–	ns
$t_{h(SHD\text{-}CLKADC)}$	SHD hold time compared to CLKADC	$V_{i(IN)}$ = 32 mV; transition (99%) in 1 pixel; code $f_{co(CTH)}$ = 0000; code G_{PGA} = 767; see Fig.5	–	0	–	ns
$N_{tot(rms)}$	total noise from CTH input to ADC output (RMS value)	G_{PGA} = 0 dB; code $f_{co(CTH)}$ = 0000	–	0.75	–	LSB
		G_{PGA} = 36 dB; code $f_{co(CTH)}$ = 0000	–	10	–	LSB
$O_{CCD(max)}$	maximum offset voltage between CCD floating level and CCD dark pixel level	see Fig.11	–200	–	+200	mV
$V_{n(i)(eq)(rms)}$	equivalent input noise (RMS value)	G_{PGA} = 36 dB; code $f_{co(CTH)}$ = 0000	–	75	–	μV
Digital outputs (f_{pix} = 30 MHz; C_L = 10 pF)						
V_{OH}	HIGH-level output voltage	I_{OH} = –1 mA	V_{CCO} – 0.5	–	V_{CCO}	V
V_{OL}	LOW-level output voltage	I_{OL} = 1 mA	0	–	0.5	V
$t_{h(o)}$	output hold time	see Fig.5	8	–	–	ns
$t_{d(o)}$	output delay	V_{CCO} = 5.25 V	–	15	19	ns
		V_{CCO} = 3 V	–	16	20	ns
		V_{CCO} = 2.5 V	–	18	22	ns
Serial interface						
$f_{SCLK(max)}$	maximum clock frequency of serial interface		5	–	–	MHz

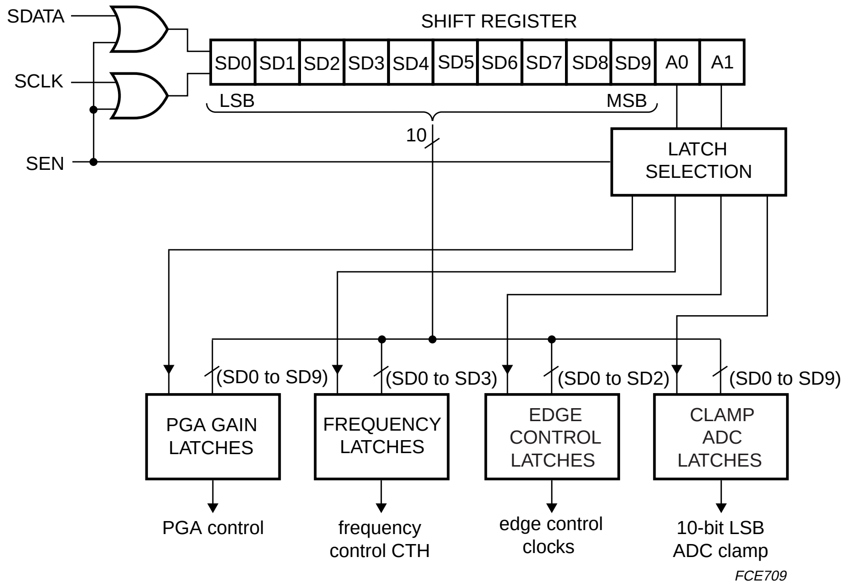
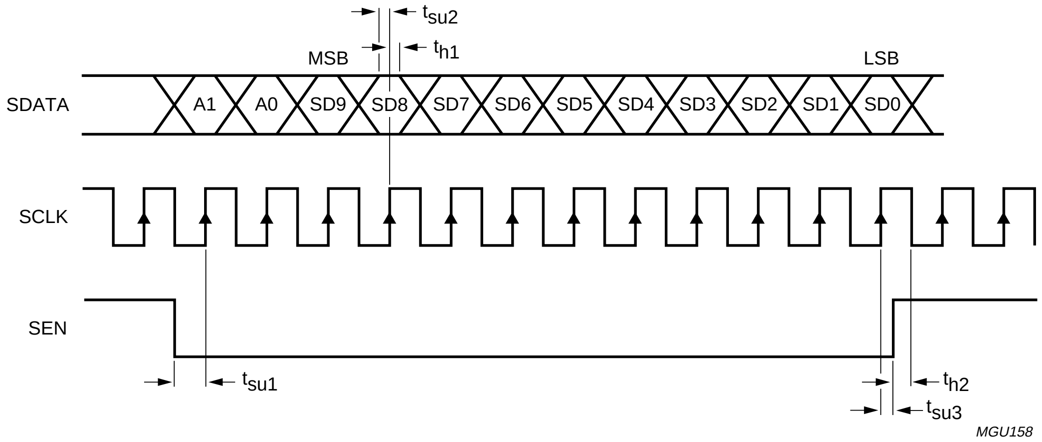


Fig.3 Serial interface block diagram.



$t_{su1} = t_{su2} = t_{su3}$ = 4 ns (minimum);
$t_{h1} = t_{h2}$ = 4 ns (minimum).

Fig.4 Loading sequence of control DACs input data via the serial interface.

Table 1 Serial interface programming

ADDRESS BITS		SDATA BITS SD0 to SD9
A1	A0	
0	0	clamp reference of ADC (SD0 to SD9) (note 1)
0	1	cut-off frequency of CTH (SD0 to SD3)
1	0	PGA gain control (SD0 to SD9)
1	1	edge control for pulses SHP, SHD, CLPOB, CLPADC and CLKADC (note 2): SD0 = 1, SHP and SHD sample on LOW level SD1 = 1, CLPADC and CLPOB activated on HIGH level SD2 = 1, CLKADC activated with rising edge

Notes

1. PGA gain register must always be refreshed after clamp code register content has been changed.
2. When pin CLPADC = HIGH (SD1 = 1; serial interface), the ADC input is clamped to the voltage level of V_{ref}. Pin V_{ref} is connected to ground via a capacitor.

When the power supplies increase from zero to V_{CC}, the init-on-power block initializes the circuit as follows:

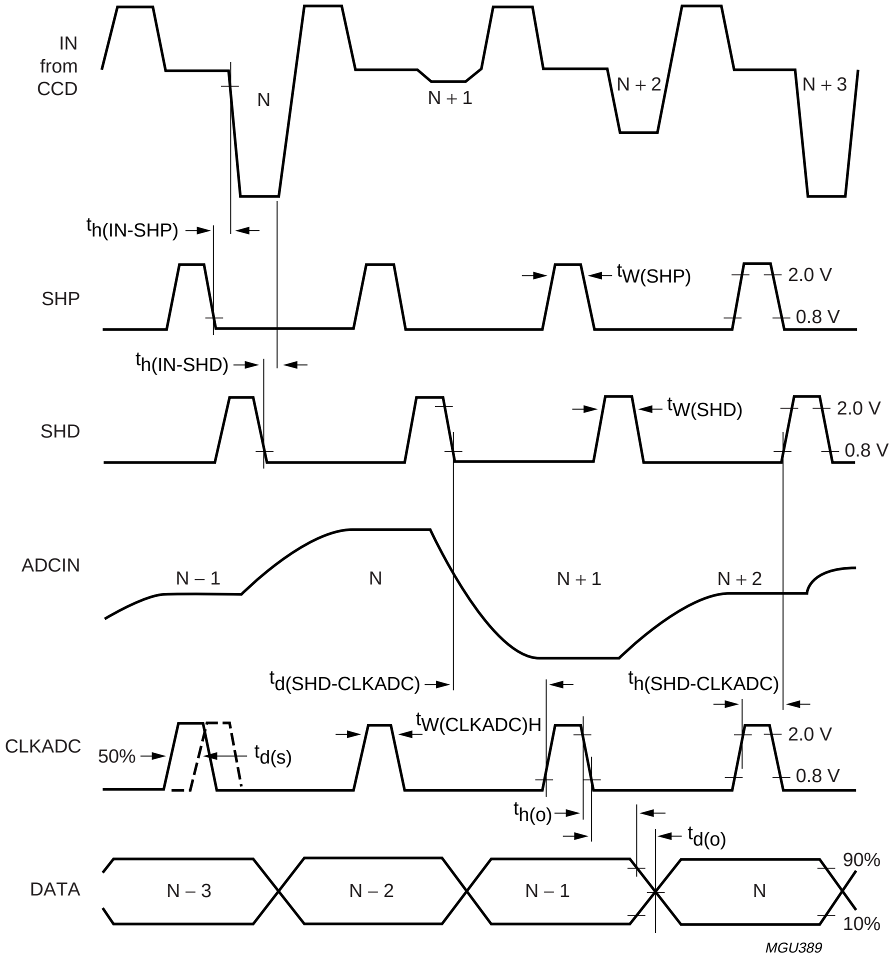
- Cut-off frequency of the CTH circuit is set to: code $f_{co(CTH)} = 0$
- PGA gain control is set to: code $G_{PGA} = 0$
- Clamp code of the ADC is set to: code $ADC_{CLP} = 0$
- SHP and SHD sample on HIGH level; CLKADC activated with rising edge.

Table 2 Standby selection

PIN STDBY	DATA BITS SD9 to SD0	$I_{CCA} + I_{CCD}$
HIGH	logic 0	4 mA (typical); note 1
LOW	active	84 mA (typical)

Note

1. In case an external regulator is used, it has to be switched off in standby mode in order to avoid an extra consumption of the TDA9965.



The polarities used in this case are:

- SHP and SHD sample on HIGH level
- CLKADC activated with rising edge.

Fig.5 Pixel frequency timing diagram.

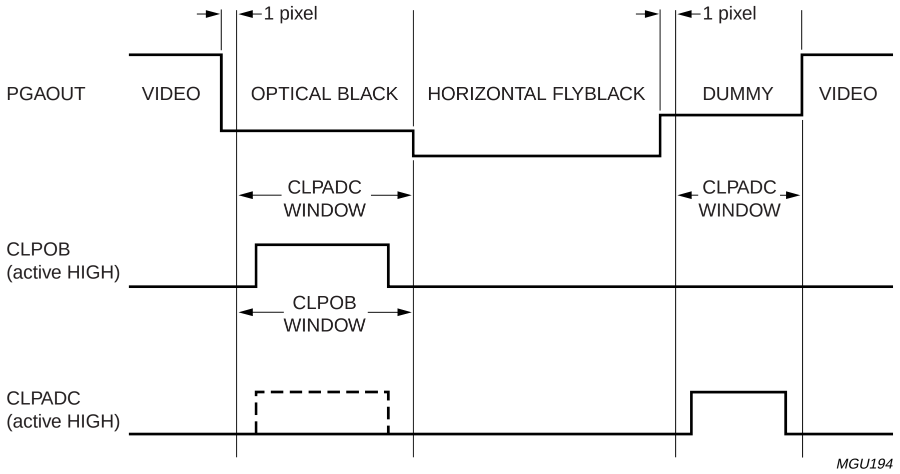


Fig.6 Line frequency timing diagram.

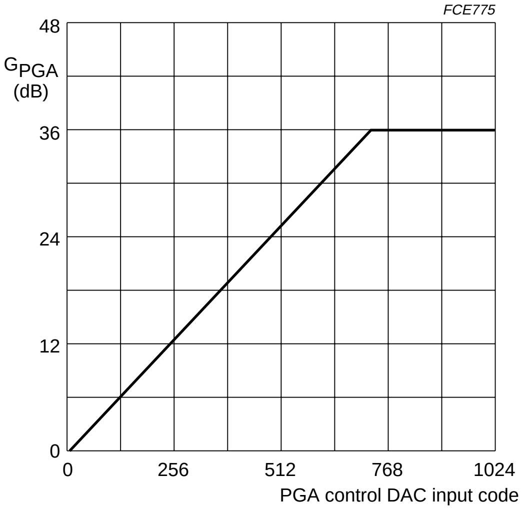


Fig.7 PGA gain as a function of PGA control DAC input code.

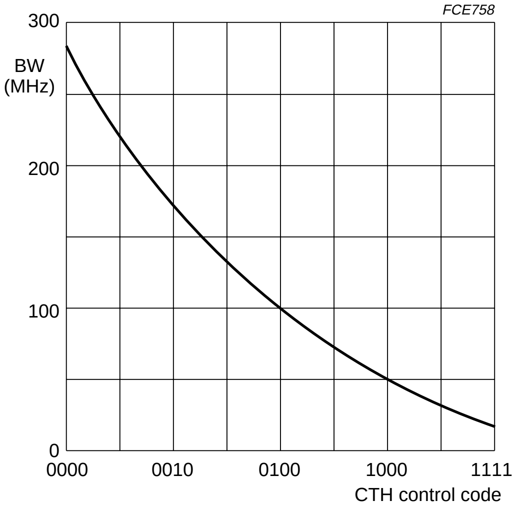


Fig.8 CTH bandwidth as a function of CTH control code.

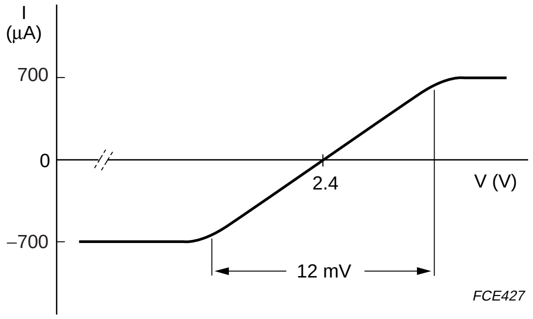
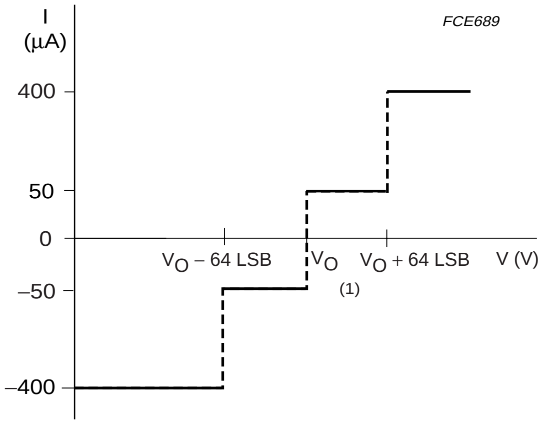


Fig.9 Typical clamp current as a function of voltage on pin STGE.



(1) V_O depends on the clamp code.

Fig.10 Typical clamp current as a function of voltage on pin V_{ref}.

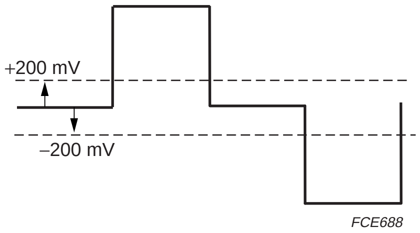
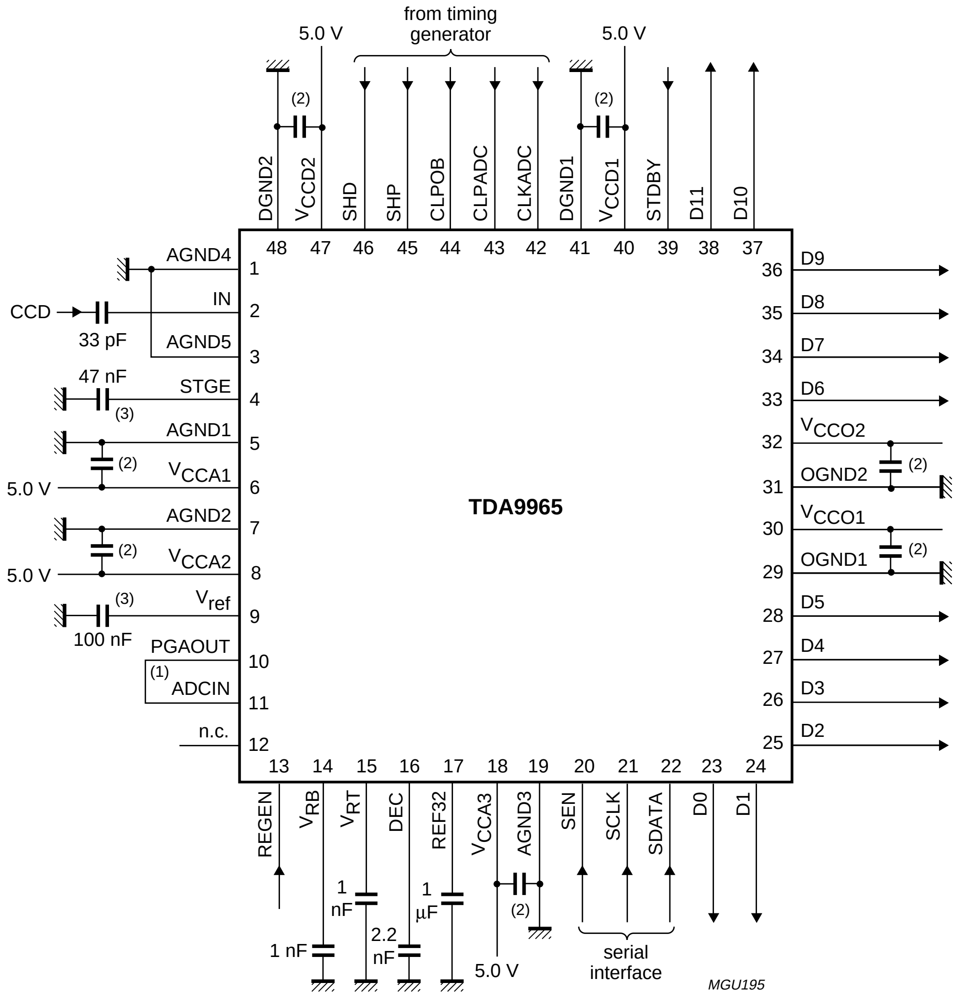


Fig.11 Maximum offset voltage between CCD floating and dark pixel level.

APPLICATION DIAGRAM



(1) The clamp level of the signal input at pin ADCIN can be tuned from code 0 to code 1023 in one LSB step of the ADC via the serial interface (clamp ADC activated).

(2) All supply pins must be decoupled with 100 nF capacitors as closely as possible to the device.

(3) The capacitors on pins STGE and V_{ref} have typical values, performing a typical device start-up time of 300 μs from standby to active (supplies on).

Fig.12 Application diagram.

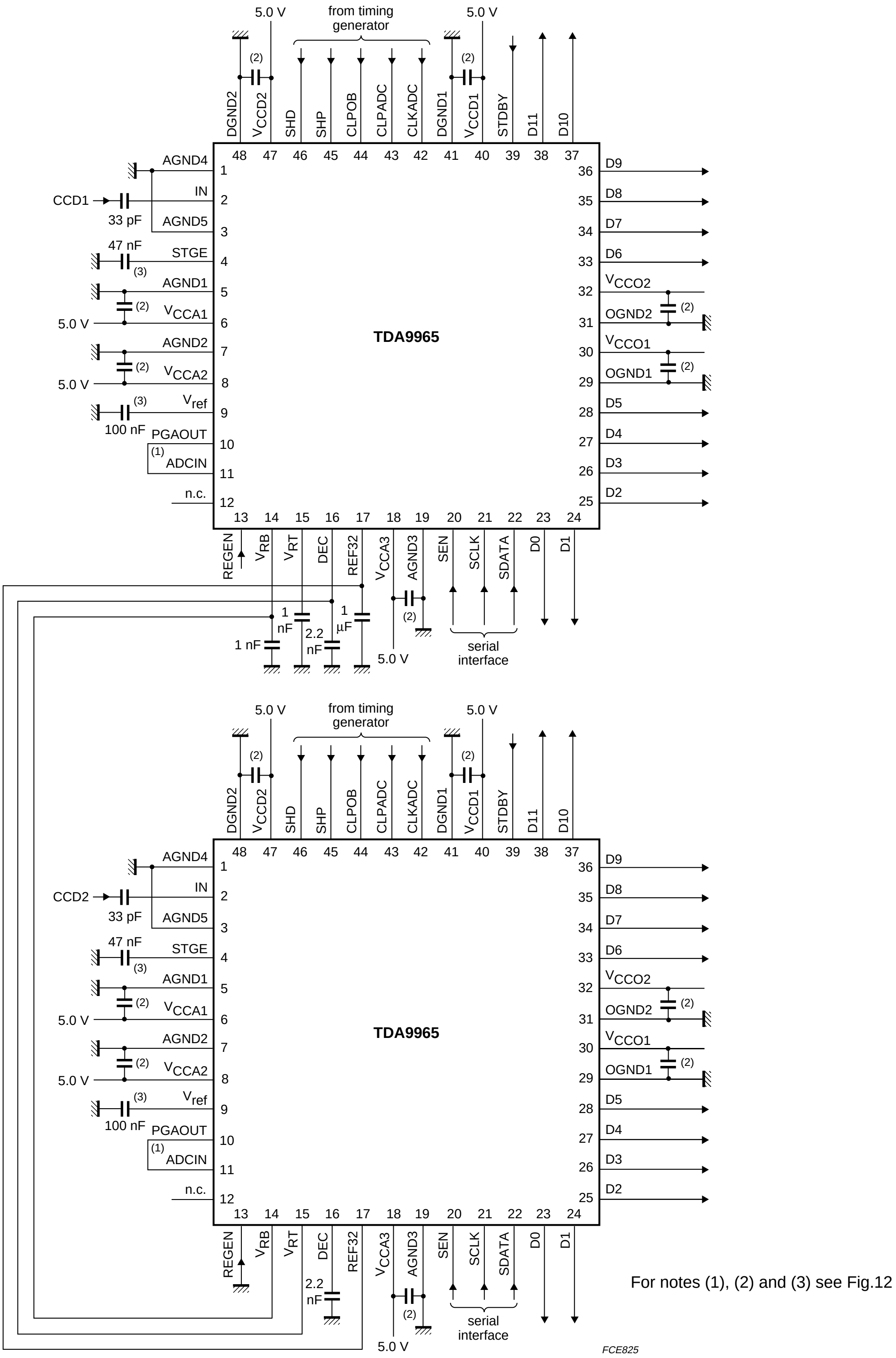


Fig.13 Application diagram with 2 CCDs.

Power and grounding recommendations

Care should be taken to minimize the noise when designing a printed-circuit board for applications such as PC cameras, surveillance cameras, camcorders, and digital still cameras.

For the front end integrated circuit, the basic rules of printed-circuit board design and implementation of analog components (such as classical operational amplifiers) must be taken into account, particularly with respect to power and ground connections.

The following additional recommendation is given for the CTH input (pin IN) which is internally connected to the programmable gain amplifier.

The connections between CCD interface and CTH input should be as short as possible and a ground ring protection around these connections can be beneficial.

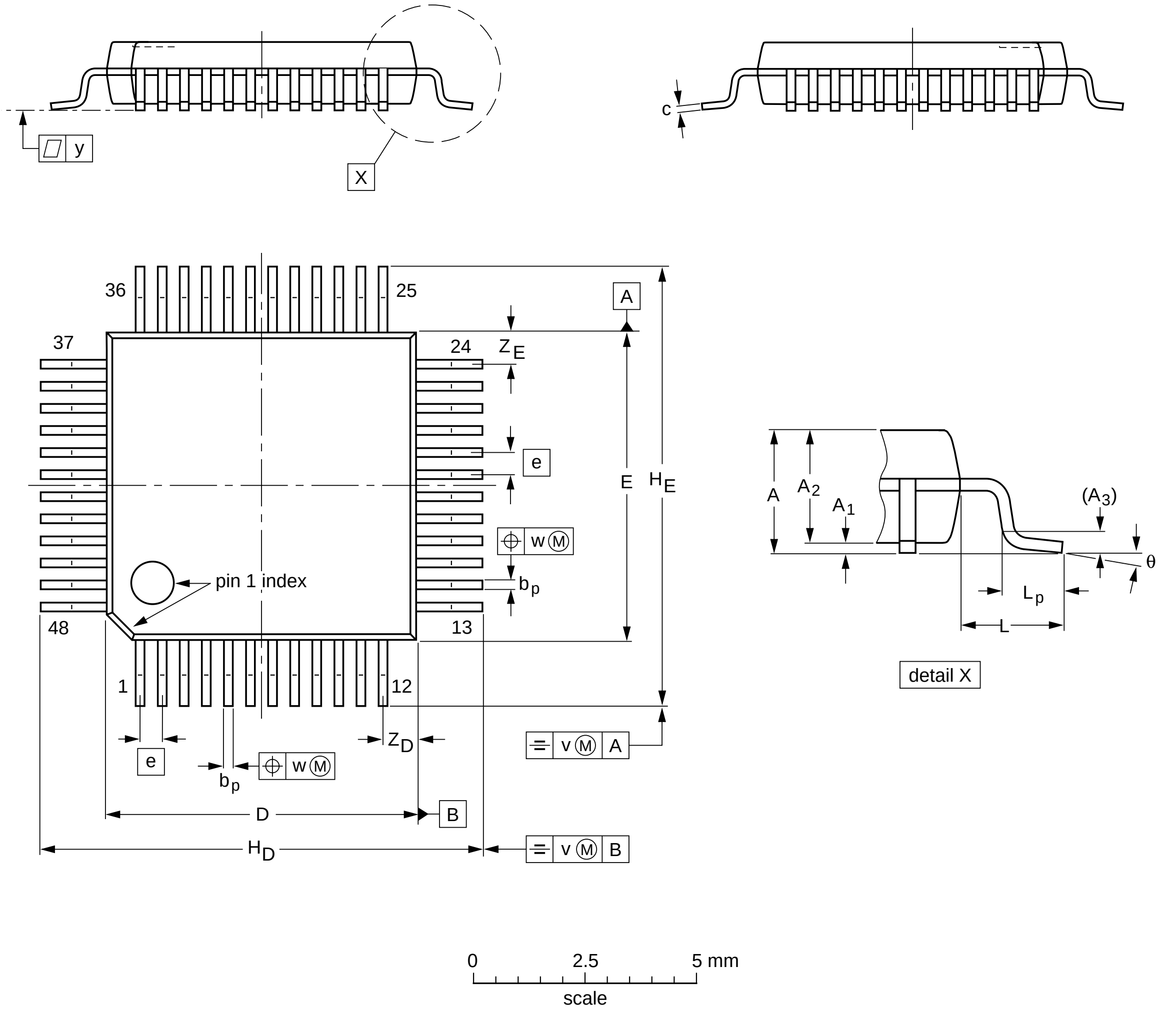
Separate analog and digital supplies provide the best solution. If it is not possible to do this on the board then the analog supply pins must be decoupled effectively from the digital supply pins. If the same power supply and ground are used for all the pins, then the decoupling capacitors must be placed as closely as possible to the IC package.

In a two-ground system, in order to minimize the noise through the package and die parasitics, the following recommendation must be implemented:

- All the analog and digital supply pins must be decoupled to the analog ground plane. Only the ground pin associated with the digital outputs must be connected to the digital ground plane. All the other ground pins should be connected to the analog ground plane. The analog and digital ground planes must be connected together at one point as closely as possible to the ground pin associated with the digital outputs.
- The digital output pins and their associated lines should be shielded by the digital ground plane which can then be used as a return path for the digital signals.

PACKAGE OUTLINE

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT313-2	136E05	MS-026				~~99-12-27~~ 00-01-19

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, HBGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *“Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”*.
2. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

DATA SHEET STATUS[1]	PRODUCT STATUS[2]	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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SCA74

Printed in The Netherlands 753504/03/pp24 Date of release: 2002 Feb 07 Document order number: 9397 750 08893

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