DATA SHEET

TDA8566TH

2 × 40 W/2 Ω stereo BTL car radio power amplifier with differential inputs and diagnostic outputs

Product specification
Supersedes data of 2001 Apr 24

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Philips
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2 × 40 W/2 Ω stereo BTL car radio power amplifier with differential inputs and diagnostic outputs

TDA8566TH

FEATURES

- Differential inputs
- Very high Common Mode Rejection Ratio (CMRR)
- High common mode input signal handling
- Requires very few external components
- High output power
- 4 and 2 Ω load driving capability
- Low offset voltage at output
- Fixed gain
- Diagnostic facility (distortion, short-circuit and temperature pre-warning)
- Good ripple rejection
- Mode select switch (operating, mute and standby)
- Load dump protection
- Short-circuit proof to ground, to V_P and across the load
- Low power dissipation in any short-circuit condition
- Thermally protected
- Reverse polarity safe
- Protected against electrostatic discharge
- No switch-on/switch-off plops
- Low thermal resistance.

GENERAL DESCRIPTION

The TDA8566TH is an integrated class-B output amplifier contained in a 20-lead small outline plastic package. The device contains 2 amplifiers in a Bridge-Tied Load (BTL) configuration. The output power is 2 × 25 W in a 4 Ω load or 2 × 40 W in a 2 Ω load. It has a differential input stage and 2 diagnostic outputs. The device is primarily developed for car radio applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	operating supply voltage		6	14.4	18	V
I_{ORM}	repetitive peak output current		–	–	7.5	A
$I_{q(tot)}$	total quiescent current		–	115	–	mA
I_{stb}	standby current		–	0.1	10	μA
I_{sw}	switch-on current		–	–	40	μA
Z_i	input impedance		100	120	–	kΩ
P_{out}	output power	R_L = 4 Ω; THD = 10%	–	25	–	W
		R_L = 2 Ω; THD = 10%	–	40	–	W
SVRR	supply voltage ripple rejection	R_S = 0 Ω	–	60	–	dB
α_{cs}	channel separation	R_S = 10 kΩ	–	50	–	dB
CMRR	common mode rejection ratio		–	75	–	dB
G_v	closed loop voltage gain		25	26	27	dB
$V_{n(o)}$	noise output voltage	R_S = 0 Ω	–	–	120	μV

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8566TH	HSOP20	plastic thermal enhanced small outline package; 20 leads; low stand-off height; heatsink	SOT418-3

BLOCK DIAGRAM

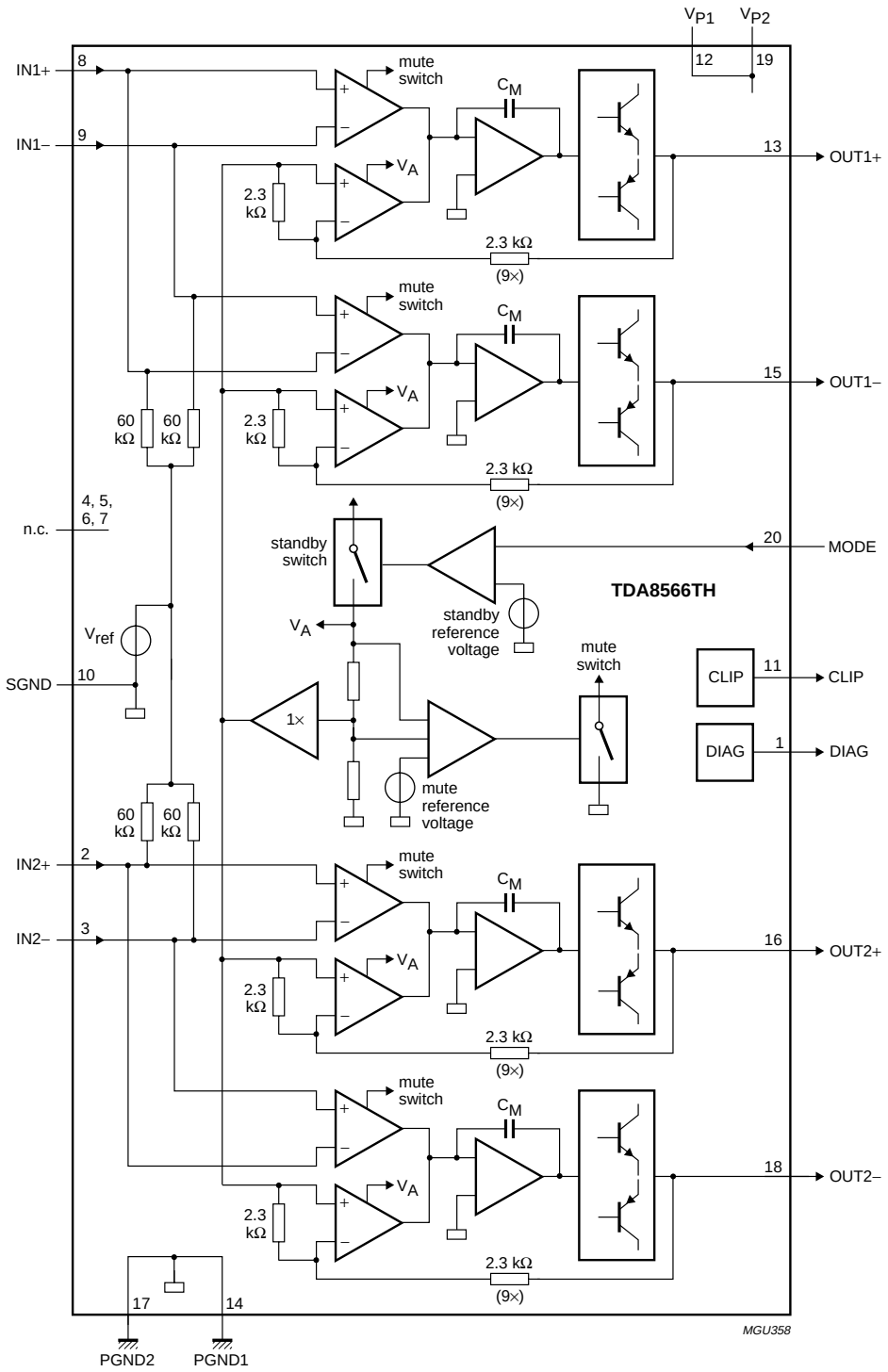


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
DIAG	1	short-circuit and temperature pre-warning diagnostic output
IN2+	2	channel 2 input positive
IN2–	3	channel 2 input negative
n.c.	4	not connected
n.c.	5	not connected
n.c.	6	not connected
n.c.	7	not connected
IN1+	8	channel 1 input positive
IN1–	9	channel 1 input negative
SGND	10	signal ground
CLIP	11	clip detection output
V_{P1}	12	supply voltage 1
OUT1+	13	channel 1 output positive
PGND1	14	power ground 1
OUT1–	15	channel 1 output negative
OUT2+	16	channel 2 output positive
PGND2	17	power ground 2
OUT2–	18	channel 2 output negative
V_{P2}	19	supply voltage 2
MODE	20	mode select switch input (standby/mute/operating)

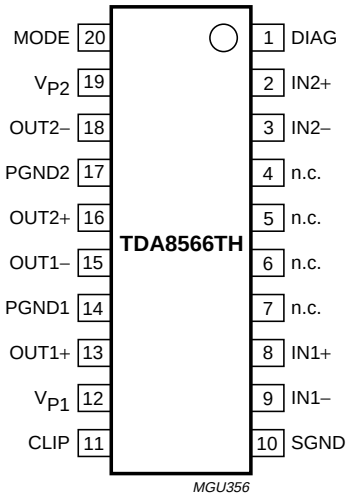


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA8566TH contains 2 identical amplifiers and can be used for BTL applications. The gain of each amplifier is fixed at 26 dB. Special features of this device are:

1. Mode select switch
2. Clip detection
3. Short-circuit diagnostic
4. Temperature pre-warning
5. Open-collector diagnostic outputs
6. Differential inputs.

Mode select switch (pin MODE)

- Standby: low supply current
- Mute: input signal suppressed
- Operating: normal on condition.

Since this pin has a very low input current (<40 μA), a low cost supply switch can be applied. To avoid switch-on plops, it is advisable to keep the amplifier in the mute mode for a period of ≥150 ms (charging the input capacitors at pins IN1+, IN1–, IN2+ and IN2–). This can be realized by using a microcontroller or by using an external timing circuit as illustrated in Fig.7.

Clip detection (pin CLIP)

When clipping occurs at one or more output stages, the dynamic distortion detector becomes active and pin CLIP goes LOW. This information can be used to drive a sound processor or a DC volume control to attenuate the input signal and so limit the level of distortion. The output level of pin CLIP is independent of the number of channels that are being clipped. The clip detection circuit is disabled in a short-circuit condition, so if a fault condition occurs at the outputs, pin CLIP will remain at a HIGH level. The clip detection waveforms are illustrated in Fig.3.

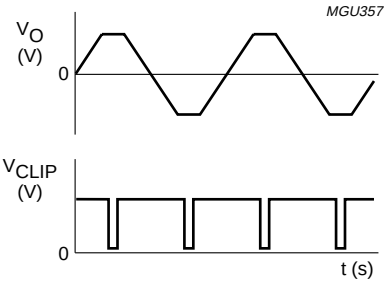


Fig.3 Clip detection waveforms.

Short-circuit diagnostic (pin DIAG)

When a short-circuit occurs at one or more outputs to ground or to the supply voltage, the output stages are switched off until the short-circuit is removed and the device is switched on again (with a delay of approximately 20 ms after the removal of the short-circuit). During this short-circuit condition, pin DIAG is continuously LOW.

When a short-circuit occurs across the load of one or both channels, the output stages are switched off for approximately 20 ms. After that time the load condition is checked during approximately 50 μs to see whether the short-circuit is still present. Due to this duty cycle of 50 μs/20 ms the average current consumption during the short-circuit condition is very low (approximately 40 mA). During this condition, pin DIAG is LOW for 20 ms and HIGH for 50 μs; see Fig.4. The power dissipation in any short-circuit condition is very low.

Temperature pre-warning (pin DIAG)

When the junction temperature (T_{vj}) reaches 145 °C, pin DIAG will become continuously LOW.

Open-collector diagnostic outputs

Pins DIAG and CLIP are open-collector outputs, therefore more devices can be tied together. Pins DIAG and CLIP can also be tied together. An external pull-up resistor is required.

Differential inputs

The input stage is a high-impedance fully differential balanced input stage that is also capable of operating in a single-ended mode with one of the inputs capacitively coupled to an audio ground. It should be noted that if a source resistance is added (input voltage dividers) the CMRR degrades to lower values.

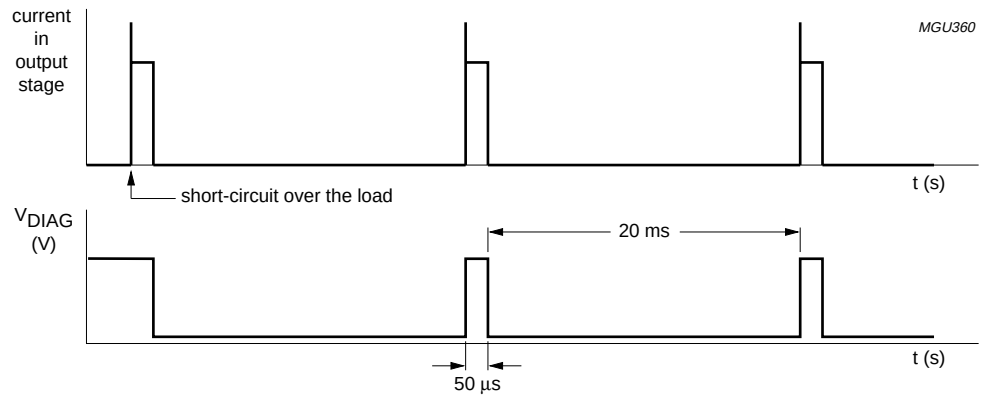


Fig.4 Short-circuit diagnostic timing diagram.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage	operating	–	18	V
		non-operating	–	30	V
		load dump protection; during 50 ms; $t_r \geq 2.5$ ms	–	45	V
I_{OSM}	non-repetitive peak output current		–	10	A
I_{ORM}	repetitive peak output current		–	7.5	A
T_{stg}	storage temperature		–55	+150	°C
T_{vj}	virtual junction temperature		–	150	°C
T_{amb}	ambient temperature		–40	+85	°C
V_{psc}	short-circuit safe voltage		–	18	V
V_{rp}	reverse polarity voltage		–	6.0	V
P_{tot}	total power dissipation		–	60	W

QUALITY SPECIFICATION

Quality specification in accordance with *"SNW-FQ-611D"*, if this type is used as an audio amplifier.

THERMAL CHARACTERISTICS

Thermal characteristics in accordance with IEC 60747-1.

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-c)}$	thermal resistance from junction to case	see Fig.5	1.9	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	40	K/W

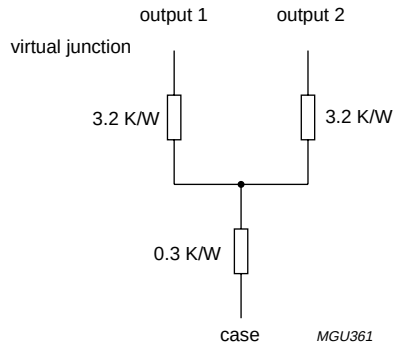


Fig.5 Equivalent thermal resistance network.

DC CHARACTERISTICS

V_P = 14.4 V; T_{amb} = 25 °C; measured in test circuit of Fig.6; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage	note 1	6	14.4	18	V
I_q	quiescent current	$R_L = \infty$	–	115	180	mA
Operating condition						
V_{MODE}	mode select switch level		8.5	–	V_P	V
I_{MODE}	mode select switch current	V_{MODE} = 14.4 V	–	15	40	μA
V_O	output voltage	note 2	–	7.0	–	V
V_{OO}	output offset voltage		–	–	100	mV
Mute condition						
V_{MODE}	mode select switch level		3.3	–	6.4	V
V_O	output voltage	note 2	–	7.0	–	V
V_{OO}	output offset voltage		–	–	60	mV
ΔV_{OO}	output offset voltage difference	with respect to operating condition	–	–	60	mV
Standby condition						
V_{MODE}	mode select switch level		0	–	2	V
I_{stb}	standby current		–	0.1	10	μA
Diagnostic						
V_{DIAG}	diagnostic output voltage	during any fault condition	–	–	0.6	V

Notes

1. The circuit is DC adjusted at V_P = 6 to 18 V and AC operating at V_P = 8.5 to 18 V.
2. At V_P = 18 to 30 V the DC output voltage is $\leq 0.5V_P$.

AC CHARACTERISTICS

V_P = 14.4 V; T_{amb} = 25 °C; R_L = 2 Ω; f_i = 1 kHz; measured in test circuit of Fig.6; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_o	output power	THD = 0.5%	25	30	–	W
		THD = 10%	33	40	–	W
		THD = 30%	45	55	–	W
		V_P = 13.5 V; THD = 0.5%	–	25	–	W
		V_P = 13.5 V; THD = 10%	–	35	–	W
		THD = 0.5%; R_L = 4 Ω	16	19	–	W
		THD = 10%; R_L = 4 Ω	21	25	–	W
		THD = 30%; R_L = 4 Ω	28	35	–	W
		V_P = 13.5 V; THD = 0.5%; R_L = 4 Ω	–	14	–	W
		V_P = 13.5 V; THD = 10%; R_L = 4 Ω	–	22	–	W
THD	total harmonic distortion	P_o = 1 W	–	0.1	–	%
		V_{CLIP} = 0.6 V; note 1	–	8	–	%
		P_o = 1 W; R_L = 4 Ω	–	0.05	–	%
B	power bandwidth	THD = 0.5%; P_o = –1 dB with respect to 25 W	–	20 to 20000	–	Hz
$f_{ro(l)}$	low frequency roll off	–1 dB; note 2	–	25	–	Hz
$f_{ro(h)}$	high frequency roll off	–1 dB	20	–	–	kHz
G_v	closed loop voltage gain		25	26	27	dB
SVRR	supply voltage ripple rejection	operating; note 3	50	–	–	dB
		mute; note 3	50	–	–	dB
		standby; note 3	80	–	–	dB
Z_i	input impedance	differential	100	120	150	kΩ
		single-ended	50	60	75	kΩ
$\lvert\Delta Z_i\rvert$	input impedance mismatch		–	2	–	%
$V_{n(o)}$	noise output voltage	operating; R_S = 0 Ω; note 4	–	85	120	μV
		operating; R_S = 10 kΩ; note 4	–	100	–	μV
		mute; independent of R_S; note 4	–	60	–	μV
α_{cs}	channel separation	P_o = 25 W; R_S = 10 kΩ	45	–	–	dB
$\lvert\Delta G_v\rvert$	channel unbalance		–	–	1	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{o(mute)}$	output signal voltage in mute	$V_{in} = V_{in(max)}$ = 1 V (RMS)	–	–	2	mV
CMRR	common mode rejection ratio	R_s = 0 Ω; note 5	60	75	–	dB
		R_s = 45 kΩ; note 6	40	–	–	dB

Notes

1. Dynamic distortion detector active; pin CLIP is LOW.
2. Frequency response externally fixed.
3. $V_{ripple} = V_{ripple(max)}$ = 2 V (p-p); R_s = 0 Ω.
4. Noise measured in a bandwidth of 20 Hz to 20 kHz.
5. Common mode rejection ratio measured at the output (over R_L) with both inputs tied together; $V_{common} \leq$ 3.5 V (RMS); f_i = 100 Hz to 10 kHz; R_s = 0 Ω.
6. Common mode rejection ratio measured at the output (over R_L) with both inputs tied together; $V_{common} \leq$ 3.5 V (RMS); f_i = 1 kHz; R_s = 45 kΩ. The mismatch of the input coupling capacitors is excluded.

TEST AND APPLICATION INFORMATION

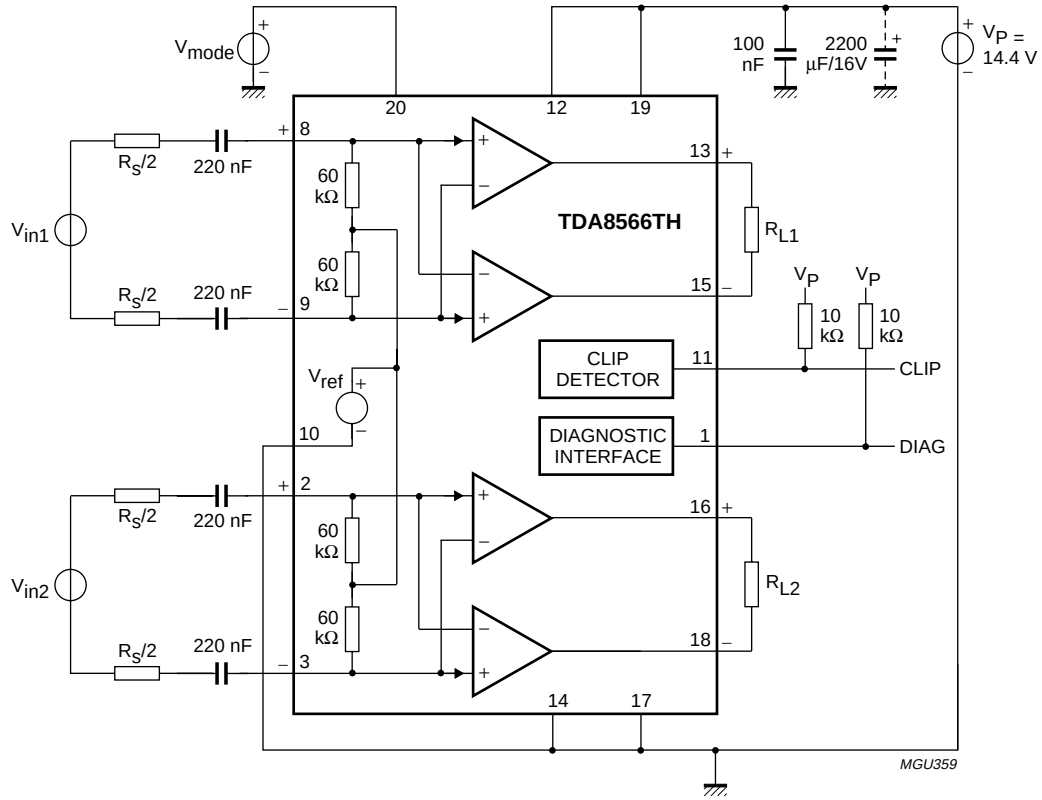


Fig.6 Stereo BTL test diagram.

Application information

DIAGNOSTIC OUTPUT

Special care must be taken in the PCB layout to separate pin CLIP from pins IN1+, IN1−, IN2+ and IN2− to minimize the crosstalk between the CLIP output and the inputs.

MODE SELECT SWITCH

To avoid switch-on plops, it is advisable to keep the amplifier in the mute mode during ≥150 ms (charging of the input capacitors at pins IN1+, IN1−, IN2+ and IN2−). The circuit in Fig.7 slowly ramps-up the voltage at the mode select switch pin when switching on and results in fast muting when switching off.

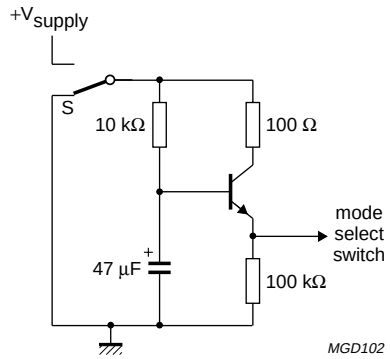
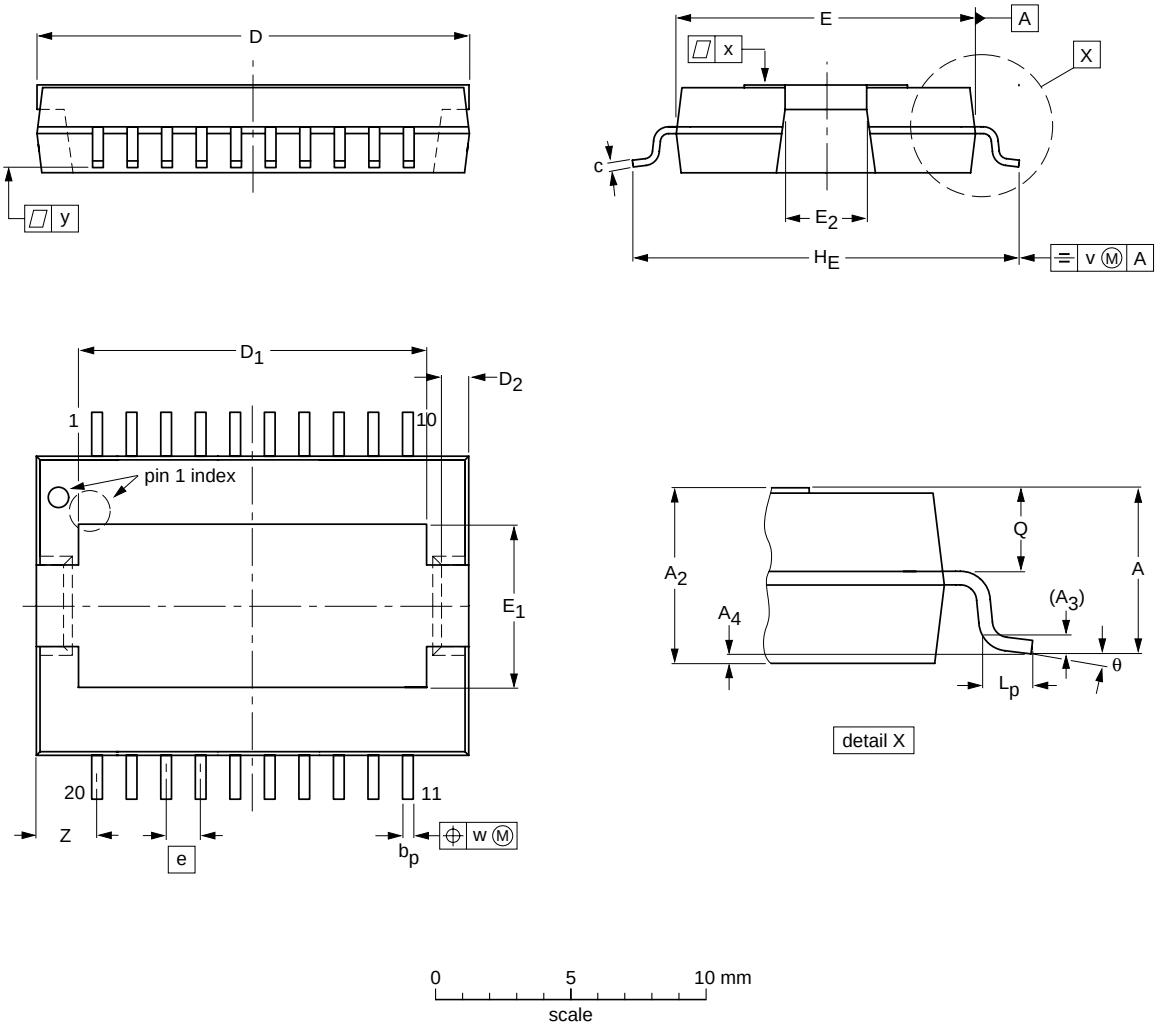


Fig.7 Mode select switch circuit.

PACKAGE OUTLINE

HSOP20: plastic thermal enhanced small outline package; 20 leads; low stand-off height; heatsink SOT418-3



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_2	A_3	A_4(1)	b_p	c	D(2)	D_1	D_2	E(2)	E_1	E_2	e	H_E	L_p	Q	v	w	x	y	Z	θ
mm	3.5	3.5 3.2	0.35	+0.08 –0.04	0.53 0.40	0.32 0.23	16.0 15.8	13.0 12.6	1.1 0.9	11.1 10.9	6.2 5.8	2.9 2.5	1.27	14.5 13.9	1.1 0.8	1.7 1.5	0.25	0.25	0.03	0.07	2.5 2.0	8° 0°

Notes

1. Limits per individual lead.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT418-3						02-02-12

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 220 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA and SSOP-T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 235 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE[1]	SOLDERING METHOD	
	WAVE	REFLOW[2]
BGA, LBGA, LFBGA, SQFP, SSOP-T[3], TFBGA, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[4]	suitable
PLCC[5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[5][6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[7]	suitable

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note*" (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.
4. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
5. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
6. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
7. Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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