DATA SHEET

TDA8060ATS
Satellite ZERO-IF QPSK down-converter

Product specification
File under Integrated Circuits, IC02

2000 Nov 10

Philips
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FEATURES

- Direct conversion Quadrature Phase Shift Keying (QPSK) demodulation (Zero IF)
- 920 to 2200 MHz range
- On-chip loop-controlled 0 or 90° phase shifter
- Variable gain on RF input
- 60 MHz, at –3 dB, bandwidth for baseband I and Q amplifiers
- Local oscillator output to PLL satellite or terrestrial
- 5 V supply voltage.

APPLICATIONS

- Direct Broadcasting Satellite (DBS) QPSK demodulation
- Digital Video Broadcasting (DVB) QPSK demodulation.

GENERAL DESCRIPTION

The direct conversion QPSK demodulator is the front-end receiver dedicated to digital TV broadcasting, satisfying both DVB and DBS TV standards.

The 920 to 2200 MHz wide range oscillator covers American, European and Asian satellite bands as well as the SMA-TV US standard.

Accurate QPSK demodulation is ensured by the on-chip loop-controlled phase shifter. The Zero-IF concept discards traditional IF filtering and intermediate conversion techniques. It also simplifies the signal path.

The baseband I and Q signal bandwidth only depends, to a certain extent, on the external filter used in the application.

Optimum signal level is guaranteed by a gain-controlled amplifier at the RF input. The pin AGC sets the gain for both I and Q channels, providing a 37 dB range.

The chip also offers a selectable internal LO prescaler (divide-by-2) and buffer that has been designed to be compatible with the input of a terrestrial or satellite frequency synthesizer.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	4.75	5.00	5.25	V
$\Delta\Phi$	quadrature error	–	–	3	deg
f_{osc}	oscillator frequency	920	–	2200	MHz
$V_{o(p-p)}$	output voltage (peak-to-peak value)	–	1	–	V
T_{amb}	ambient temperature	–20	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8060ATS	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1

BLOCK DIAGRAM

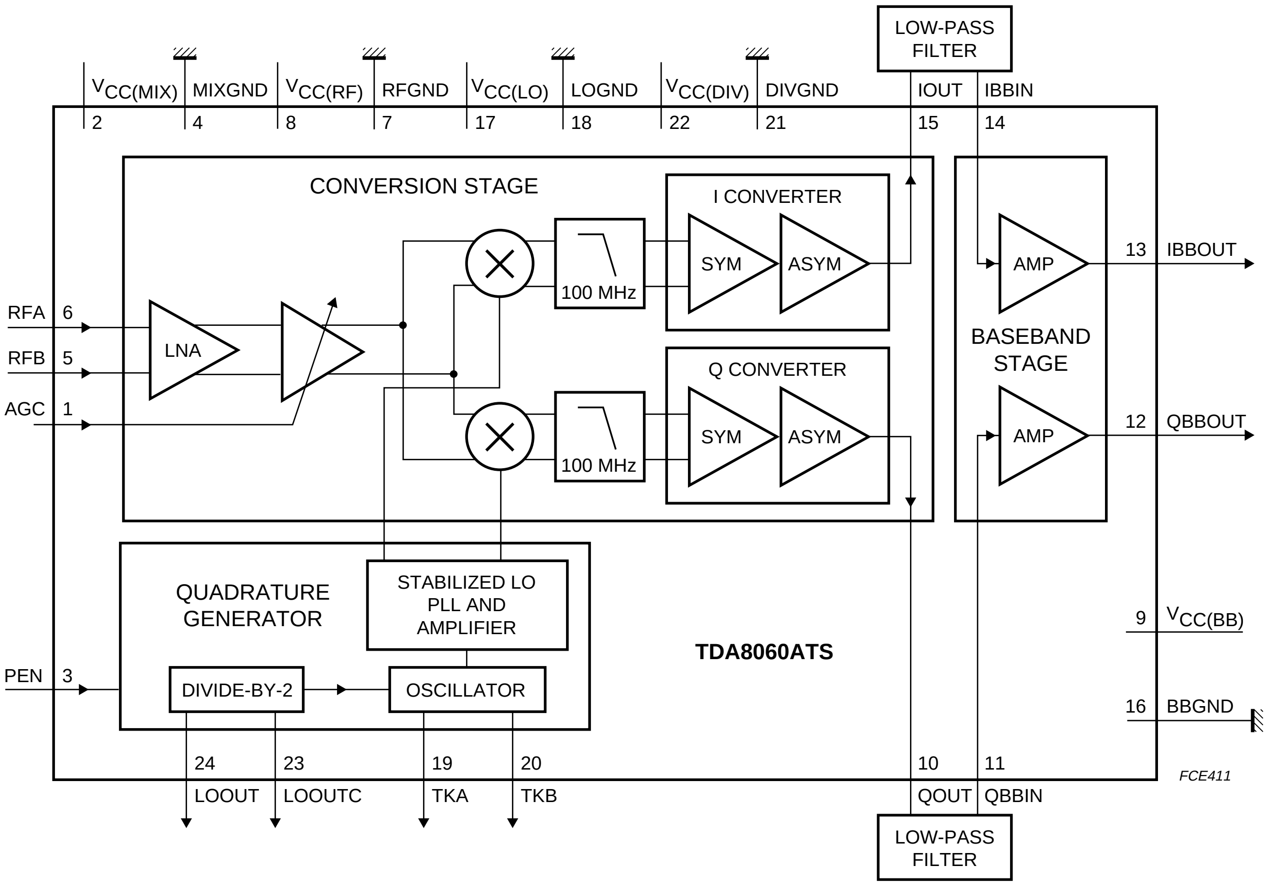


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
AGC	1	RF amplifier gain control input
$V_{CC(MIX)}$	2	supply voltage for mixer circuit (5 V)
PEN	3	prescaler enable
MIXGND	4	ground for mixer circuit
RFB	5	RF signal input B
RFA	6	RF signal input A
RFGND	7	ground for RF circuit
$V_{CC(RF)}$	8	supply voltage for RF circuit (5 V)
$V_{CC(BB)}$	9	supply voltage for baseband circuit (5 V)
QOUT	10	‘Q’ output from demodulator
QBBIN	11	‘Q’ baseband amplifier input
QBBOUT	12	‘Q’ baseband amplifier output
IBBOUT	13	‘I’ baseband amplifier output
IBBIN	14	‘I’ baseband amplifier input
IOUT	15	‘I’ output from demodulator
BBGND	16	ground for baseband circuit
$V_{CC(LO)}$	17	supply voltage for local oscillator circuit (5 V)
LOGND	18	ground for local oscillator circuit
TKA	19	tank circuit input A
TKB	20	tank circuit input B
DIVGND	21	ground for divider circuit
$V_{CC(DIV)}$	22	supply voltage for divider circuit (5 V)
LOOUTC	23	local oscillator output to synthesizer divided or not according to PEN voltage
LOOUT	24	

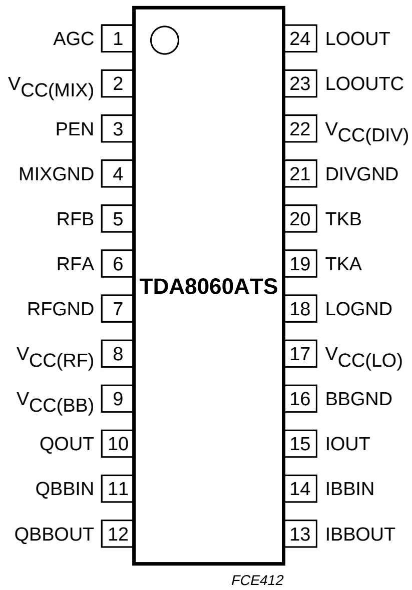


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–0.3	+6.0	V
$V_{i(max)}$	maximum input voltage on all pins	–0.3	V_{CC}	V
$t_{sc(max)}$	maximum short-circuit time	–	10	s
T_{amb}	ambient temperature	–20	+85	°C
T_{stg}	storage temperature	–55	+150	°C
T_j	junction temperature	–	150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	120	K/W

DC CHARACTERISTICS

V_{CC} = 4.75 to 5.25 V; T_{amb} = –20 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		4.75	5.00	5.25	V
I_{CC}	supply current	PEN = 5 V	73	83	93	mA
		PEN = 0 V	70	80	90	mA
Conversion stage						
$V_{I(RFA)}$	DC input voltage on pin RFA		–	0.9	–	V
$V_{I(RFB)}$	DC input voltage on pin RFB		–	0.9	–	V
$V_{O(IOUT)}$	DC output voltage on pin IOUT		–	1.85	–	V
$V_{O(QOUT)}$	DC output voltage on pin QOUT		–	1.85	–	V
Quadrature generator						
$V_{O(LOOUT)}$	DC output voltage on pin LOOUT		–	4.0	–	V
$V_{O(LOOUTC)}$	DC output voltage on pin LOOUTC		–	4.0	–	V
Baseband stage						
$V_{I(IBBIN)}$	DC input voltage on pin IBBIN		–	2.5	–	V
$V_{I(QBBIN)}$	DC input voltage on pin QBBIN		–	2.5	–	V
$V_{O(IBBOUT)}$	DC output voltage on pin IBBOUT		–	2.5	–	V
$V_{O(QBBOUT)}$	DC output voltage on pin QBBOUT		–	2.5	–	V

AC CHARACTERISTICS

T_{amb} = 25 °C; V_{CC} = 5 V; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Quadrature generator						
f_{osc}	oscillator frequency	note 1	920	–	2200	MHz
ΦN_{osc}	oscillator phase noise	at 10 kHz offset; note 2	–	–80	–75	dBc/Hz
$\lvert\Delta\Phi\rvert$	absolute quadrature error	note 4	–	0	3	deg
f_{LOOUT}	output frequency	V_{PEN} = 0 V	–	f_{osc}	–	
		V_{PEN} = V_{CC}	–	$\frac{1}{2}f_{osc}$	–	
$V_{o(diff)(LOOUT)}$	differential output voltage at pin LOOUT	R_L = 100 Ω differential	–30	–22	–	dBm
R_{2H}	second harmonic rejection	note 3	–	30	–	dBc
$\lvert Z_{o(diff)(LOOUT)}\rvert$	differential output impedance at pin LOOUT		–	60	–	Ω
Conversion stage						
$R_{i(diff)}$	series real part of differential input impedance at pins RFA and RFB	note 5	–	34	–	Ω
$L_{i(diff)}$	series inductance of differential input impedance at pins RFA and RFB	note 5	–	5	–	nH
$P_{i(max)}$	maximum input power per channel		–	–25	–	dBm
$P_{i(min)}$	minimum input power per channel		–	–62	–60	dBm
$\Delta G_v/\Delta V_{(slope)}$	AGC slope	at $G_{v(RF-IOUT)(min)}$	–	30	43	dB/V
$\Delta G_{v(I-Q)}$	voltage gain mismatch between I and Q		–	–	1	dB
$\Delta t_{d(g)(RF-IOUT)}$	group delay variation per channel (40 MHz) from RF input to pin IOUT		–	0.5	2	ns
$\Delta t_{d(g)(RF-QOUT)}$	group delay variation per channel (40 MHz) from RF input to pin QOUT		–	0.5	2	ns
$t_{d(g)(I-Q)(40)}$	group delay mismatch per channel (40 MHz) between I and Q		–	0	0.5	ns
$B_{(-1dB)(RF-IOUT)}$	channel –1 dB bandwidth from RF input to pin IOUT		–	40	–	MHz
$B_{(-1dB)(RF-QOUT)}$	channel –1 dB bandwidth from RF input to pin QOUT		–	40	–	MHz
$B_{(-3dB)(RF-IOUT)}$	channel –3 dB bandwidth from RF input to pin IOUT		–	70	–	MHz
$B_{(-3dB)(RF-QOUT)}$	channel –3 dB bandwidth from RF input to pin QOUT		–	70	–	MHz
$Z_{o(IOUT)}$	output impedance at pin IOUT		–	65	–	Ω
$Z_{o(QOUT)}$	output impedance at pin QOUT		–	65	–	Ω
$V_{o(IOUT)}$	nominal output voltage level at pin IOUT	per channel	–	28	–	dBmV
$V_{o(QOUT)}$	nominal output voltage level at pin QOUT	per channel	–	28	–	dBmV
$R_{L(IOUT)}$	resistive load at pin IOUT		400	–	–	Ω
$R_{L(QOUT)}$	resistive load at pin QOUT		400	–	–	Ω

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SYMMETRICAL RF INPUT (Fig.4)						
$G_{v(RF\text{-}IOUT)(min)}$	minimum voltage gain from RF input to pin IOUT	$V_{AGC} = 0.1V_{CC}$; note 6	–	–	6	dB
$G_{v(RF\text{-}IOUT)(max)}$	maximum voltage gain from RF input to pin IOUT	$V_{AGC} = 0.9V_{CC}$; note 6	41	43	–	dB
$G_{v(RF\text{-}QOUT)(min)}$	minimum voltage gain from RF input to pin QOUT	$V_{AGC} = 0.1V_{CC}$; note 6	–	–	6	dB
$G_{v(RF\text{-}QOUT)(max)}$	maximum voltage gain from RF input to pin QOUT	$V_{AGC} = 0.9V_{CC}$; note 6	41	43	–	dB
$IP_{3i(I)}$	I 3rd-order interception point at RF input		1	4	–	dBm
$IP_{2i(I)}$	I 2nd-order interception point at RF input		12	15	–	dBm
$IP_{3i(Q)}$	Q 3rd-order interception point at RF input		1	4	–	dBm
$IP_{2i(Q)}$	Q 2nd-order interception point at RF input		12	15	–	dBm
F_i	noise figure at maximum gain	$V_{AGC} = 0.9V_{CC}$; $Z_{source} = 50\ \Omega$	–	12	15	dB
ASYMMETRICAL RF INPUT (Fig.5)						
$G_{v(RF\text{-}IOUT)(min)}$	minimum voltage gain from RF input to pin IOUT	$V_{AGC} = 0.1V_{CC}$; note 7	–	–	6	dB
$G_{v(RF\text{-}IOUT)(max)}$	maximum voltage gain from RF input to pin IOUT	$V_{AGC} = 0.9V_{CC}$; note 7	–	43	–	dB
$G_{v(RF\text{-}QOUT)(min)}$	minimum voltage gain from RF input to pin QOUT	$V_{AGC} = 0.1V_{CC}$; note 7	–	–	6	dB
$G_{v(RF\text{-}QOUT)(max)}$	maximum voltage gain from RF input to pin QOUT	$V_{AGC} = 0.9V_{CC}$; note 7	–	43	–	dB
$IP_{3i(I)}$	I 3rd-order interception point at RF input		–	3	–	dBm
$IP_{2i(I)}$	I 2nd-order interception point at RF input		–	15	–	dBm
$IP_{3i(Q)}$	Q 3rd-order interception point at RF input		–	3	–	dBm
$IP_{2i(Q)}$	Q 2nd-order interception point at RF input		–	15	–	dBm
F_i	noise figure at maximum gain	$V_{AGC} = 0.9V_{CC}$; $Z_{source} = 50\ \Omega$	–	13	–	dB
Baseband stages						
Z_i	input impedance		–	6	–	kΩ
V_i	nominal input voltage level	per channel	–	28	–	dBmV
$G_{v(IBBIN\text{-}IBBOUT)}$	voltage gain from pin IBBIN to pin IBBOUT		19	20	22	dB
$G_{v(QBBIN\text{-}QBBOUT)}$	voltage gain from pin QBBIN to pin QBBOUT		19	20	22	dB
$G_{v(I\text{-}Q)}$	voltage gain mismatch between I and Q		–	0	1	dB
IP_{3i}	3rd-order interception point at IQBBIN input		–	63	–	dBmV
IP_{2i}	2nd-order interception point at IQBBIN input		–	79	–	dBmV
$\Delta t_{d(g)(40)}$	group delay variation in 40 MHz bandwidth		–	0.5	2	ns
$t_{d(g)(I\text{-}Q)(40)}$	group delay mismatch in 40 MHz band between I and Q		–	0.5	2	ns
$B_{(-1dB)}$	channel –1 dB bandwidth		–	40	–	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$B_{(-3dB)}$	channel –3 dB bandwidth		–	80	–	MHz
Z_o	output impedance		–	50	–	Ω
$V_{o(p-p)}$	output voltage level (peak-to-peak value)	note 8	–	1	–	V
$R_{o(L)}$	resistive load at output		400	–	–	Ω
Overall with a 100 nF capacitor instead of LP1 and LP2						
$t_{d(g)(I-Q)(40)}$	group delay mismatch in 40 MHz band between I and Q		–	0.5	2	ns
$t_{d(g)(I-Q)(R40)}$	group delay ripple in 40 MHz band for I or Q		–	0.5	1	ns
$G_{v(I-Q)(40)}$	voltage gain mismatch in 40 MHz band between I and Q		–	–	1	dB
$G_{R(I-Q)(40)}$	voltage gain ripple in 40 MHz band for I or Q		–	–	1	dB
SYMMETRICAL RF INPUT						
$G_{v(RF-IBBOUT)(min)}$	minimum voltage gain from RF input to pin IBBOUT	$V_{AGC} = 0.1V_{CC}$	–	26	–	dB
$G_{v(RF-IBBOUT)(max)}$	maximum voltage gain from RF input to pin IBBOUT	$V_{AGC} = 0.9V_{CC}$	–	63	–	dB
$G_{v(RF-QBBOUT)(min)}$	minimum voltage gain from RF input to pin QBBOUT	$V_{AGC} = 0.1V_{CC}$	–	26	–	dB
$G_{v(RF-QBBOUT)(max)}$	maximum voltage gain from RF input to pin QBBOUT	$V_{AGC} = 0.9V_{CC}$	–	63	–	dB
F_i	noise figure at maximum gain	$V_{AGC} = 0.9V_{CC}$; $Z_{source} = 50\ \Omega$	–	13	16	dB
ASYMMETRICAL RF INPUT						
$G_{v(RF-IBBOUT)(min)}$	minimum voltage gain from RF input to pin IBBOUT	$V_{AGC} = 0.1V_{CC}$	–	26	–	dB
$G_{v(RF-IBBOUT)(max)}$	maximum voltage gain from RF input to pin IBBOUT	$V_{AGC} = 0.9V_{CC}$	–	63	–	dB
$G_{v(RF-QBBOUT)(min)}$	minimum voltage gain from RF input to pin QBBOUT	$V_{AGC} = 0.1V_{CC}$	–	26	–	dB
$G_{v(RF-QBBOUT)(max)}$	maximum voltage gain from RF input to pin QBBOUT	$V_{AGC} = 0.9V_{CC}$	–	63	–	dB
F_i	noise figure at maximum gain	$V_{AGC} = 0.9V_{CC}$; $Z_{source} = 50\ \Omega$	–	14	–	dB

Notes

1. This parameter is very dependent on the application; the range represents the capacity of the oscillator.
2. Measured in baseband (at pin IOUT or pin QOUT) on a carrier at 2 MHz and 25 dBmV.
3. f_{LO} = 1000 MHz; RF wanted = 1005 MHz; RF unwanted = 2002 MHz (see Fig.3). Done on the demo board OM5732.
4. Quadrature error with respect to 90°.
5. The differential input impedance of the IC is 34 Ω in series with the IC pins which give an inductance of 5 nH. For optimum performance, this inductance should be cancelled by a matching network. Coupling capacitors of 1 pF give an acceptable result.
6. Gain = $V_{o(dB)} - V_{i(dB)}$ (see Fig.4). Gain for symmetrical RF input.

7. Gain = $V_{o(dB)} - V_{i(dB)}$ (see Fig.5). Gain for asymmetrical RF input.
8. 2 non-coherent channels (1 desired + 1 adjacent), at 700 mV each, give a total level of 1 V.

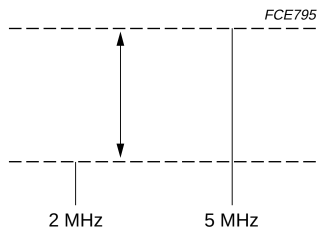


Fig.3 $V_{o(diff)(LOOUT)}$ conditions.

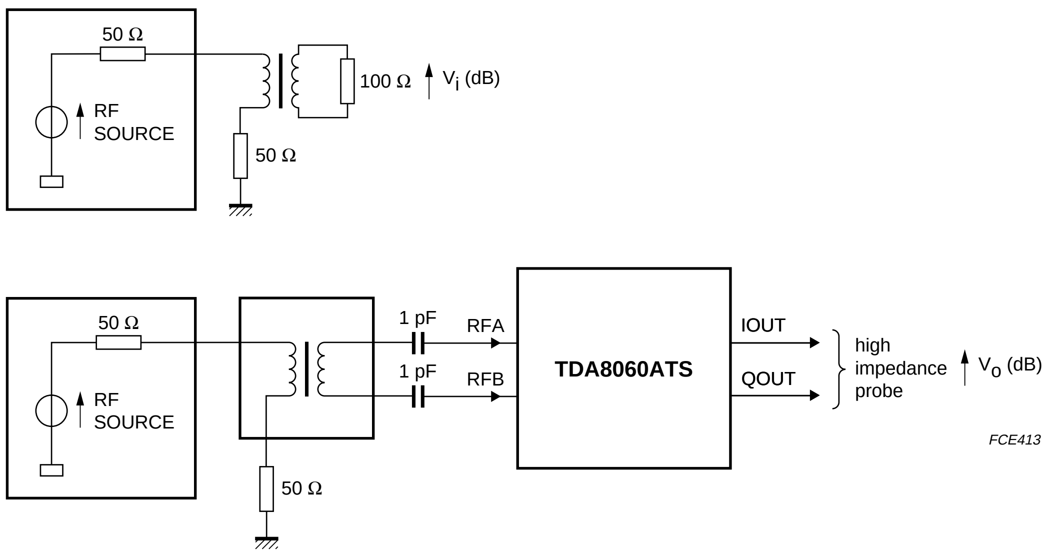


Fig.4 Gain control diagram for symmetrical RF input.

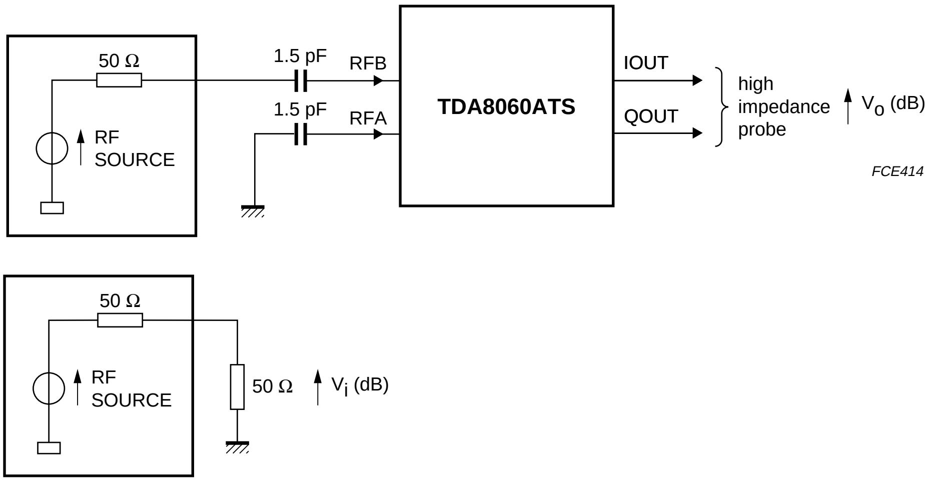


Fig.5 Gain control diagram for asymmetrical RF input.

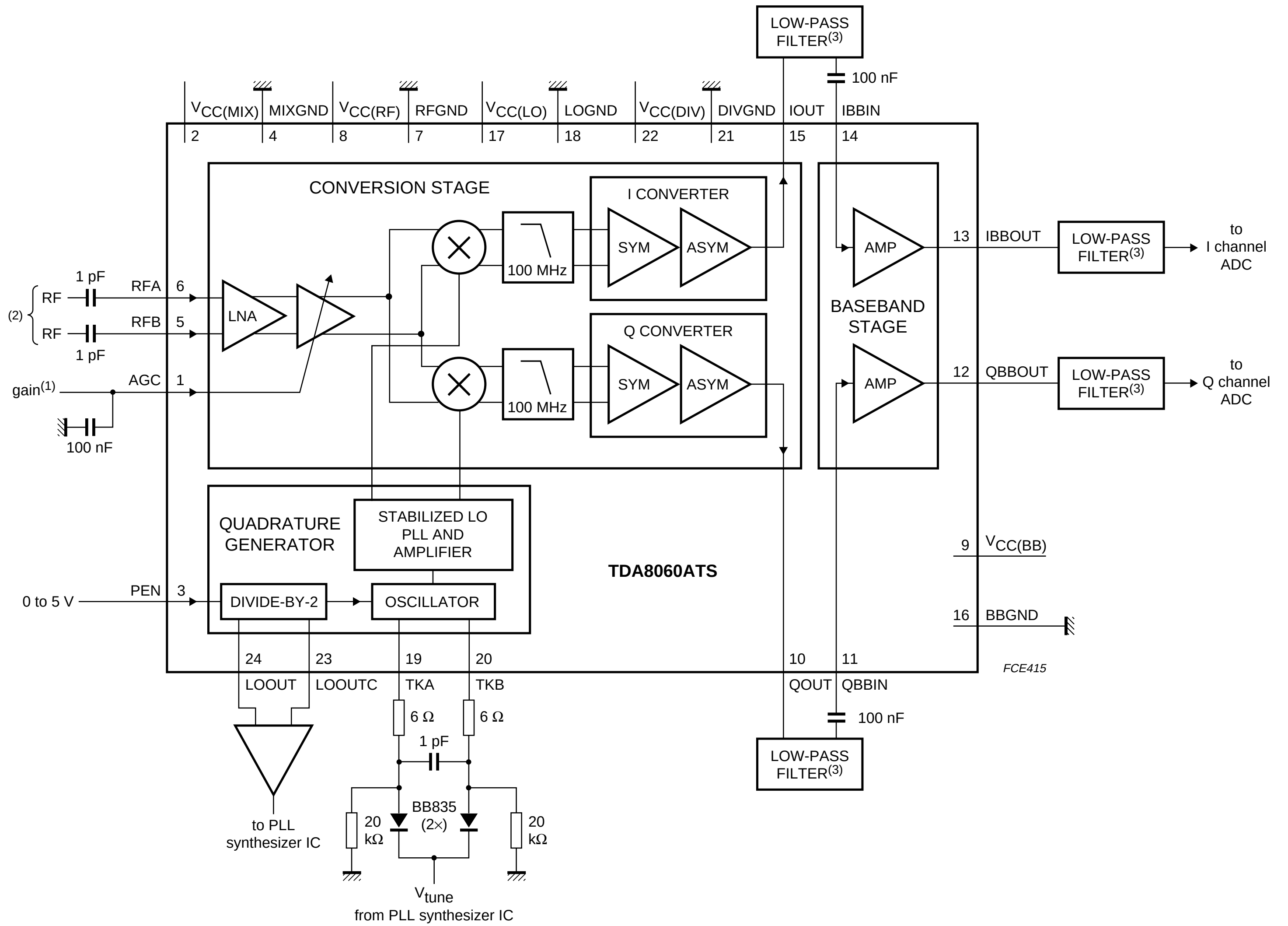
APPLICATION INFORMATION

Close attention should be paid to the design of the external tank circuit of the VCO so that it covers the 920 to 2200 MHz frequency range. Both series 6 Ω resistors kill all parasitic oscillations that could alter this frequency range. The BB835 Siemens varicap diodes are mentioned because they provide the highest C_{max}/C_{min} ratio as well as the least parasitic elements in our frequency range. The U-shaped inductance can be printed with a total length of approximately 20 mm.

Filters LP1 and LP2 are not detailed in this data sheet because their design only depends on the global system. As the TDA8060ATS has been designed to be compatible with DVB, DSS and Asian DVB, the cut-off frequencies and the tolerance in group delay, the orders of the filters cannot be globally established.

Nevertheless, the TDA8060ATS internally filters the baseband at 100 MHz and the nominal levels at inputs and outputs mentioned in the characteristics table should be respected. The input impedance of LP1 and LP2 must exceed 400 Ω to avoid signal distortion.

The converter outputs (pin IOUT and pin QOUT) must be AC-coupled via the low-pass filter to the baseband amplifiers inputs (pin IBBIN and pin QBBIN). Because of the high impedance at pin IQBBIN, a 100 nF capacitor gives a high-pass frequency of 160 Hz.



(1) Gain control voltage; minimum gain at $0.1V_{CC}$, maximum gain at $0.9V_{CC}$; 30 dB range.

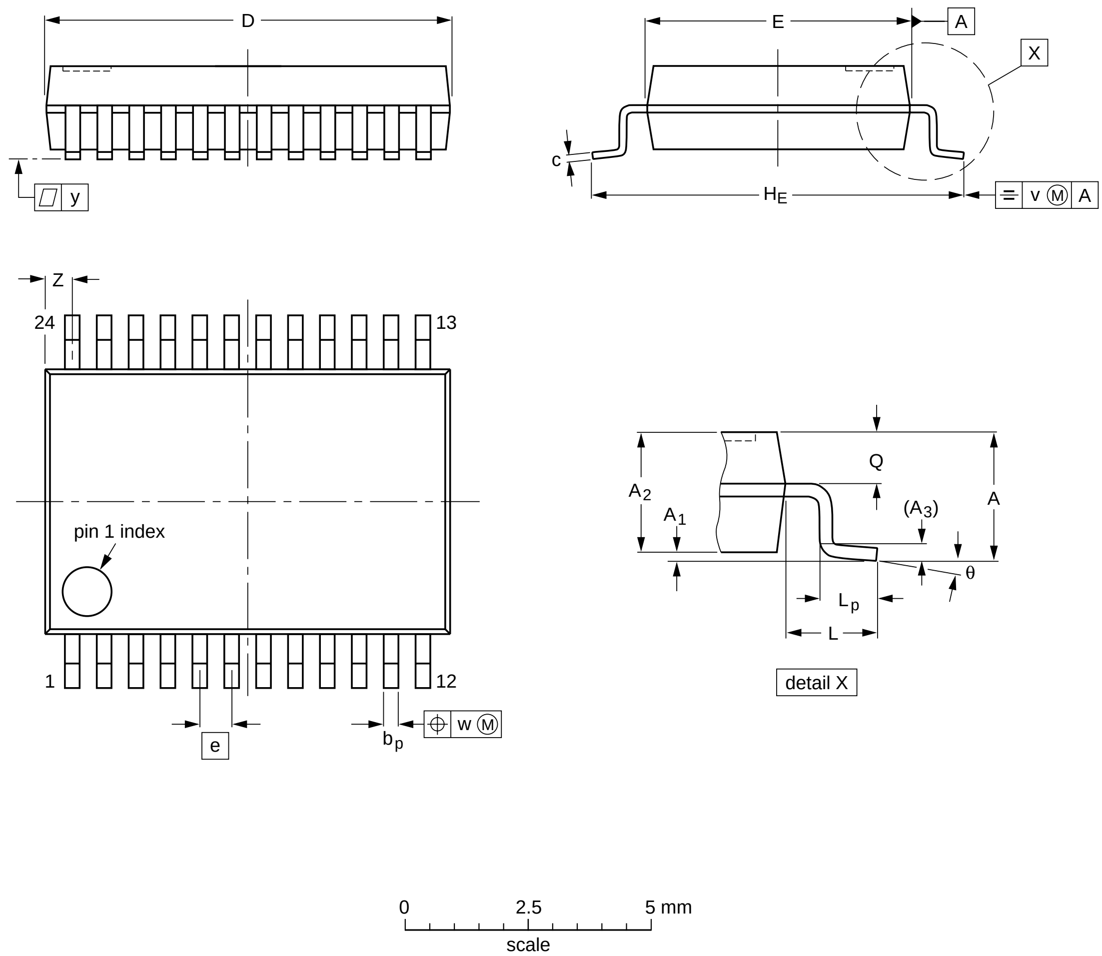
(2) Differential RF input 950 to 2200 MHz; level = –22 to –52 dBm per channel.

(3) The filter input impedance is 400 Ω minimum.

Fig.6 Application diagram.

PACKAGE OUTLINE

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8^o 0^o

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT340-1		MO-150				~~95-02-04~~ 99-12-27

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *“Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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Printed in The Netherlands   753504/01/pp16   Date of release: 2000 Nov 10   Document order number: 9397 750 07382