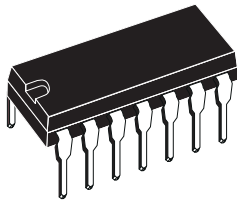
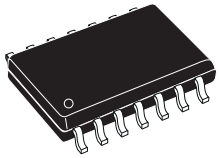
TDA7332

RDS FILTER

- HIGH PERFORMANCE, STABLE 57KHz FILTER
- HIGH SELECTIVITY
- FLAT GROUP DELAY
- HIGH PERFORMANCE LIMITER
- VERY FEW EXTERNAL COMPONENTS
- 4.332MHz CLOCK OSCILLATOR (8.664MHz OPTIONAL)





DIP14 **SO14**

ORDERING NUMBERS:

TDA7332 TDA7332D

TDA7332DIE1 (Chip on wafer)

DESCRIPTION

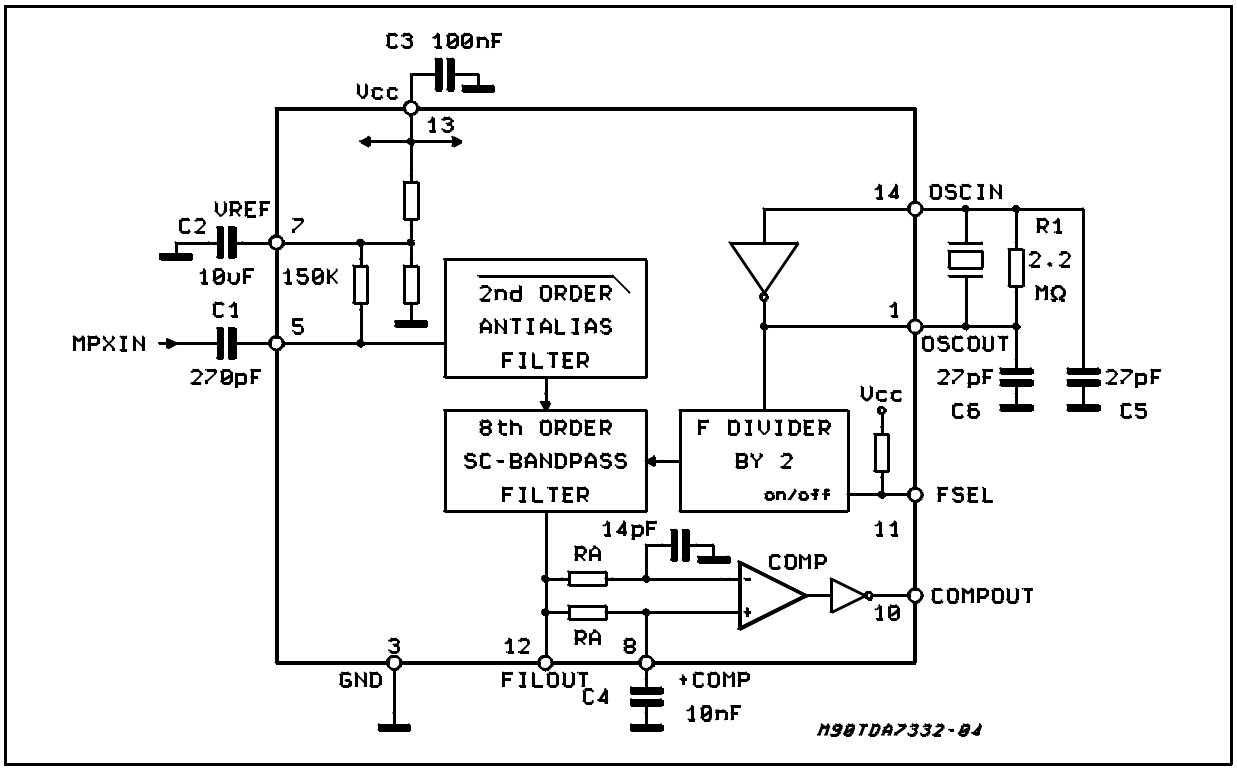
The TDA7332 is an RDS filter, realized in switched capacitor technique.

The 4 biquad stage architecture is working with 4.332MHz clock.

Optionally a 8.664MHz xtal can be used.

The filter has a center frequency of 57KHz and a bandwidth of 3KHz. Input 2nd order antialiasing filter and output smoothing filter are provided.

TEST CIRCUIT



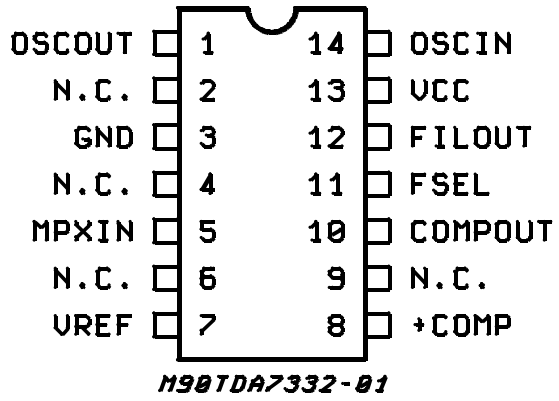
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	7	V
T_{op}	Operating Temperature Range	-40 to 85	°C
T_{stg}	Storage Temperature	-40 to 150	°C

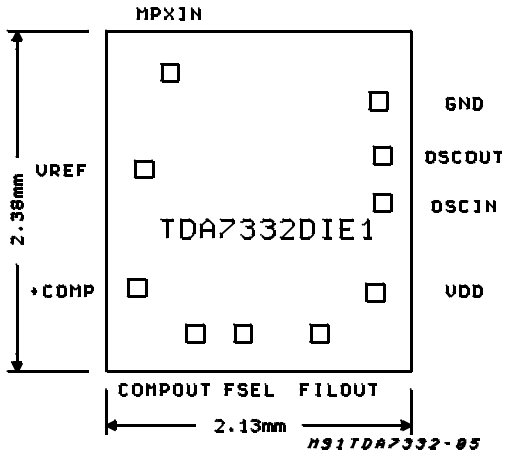
THERMAL DATA

Symbol	Description		DIP14	SO14	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Typ.	100	200	°C/W

PIN CONNECTION (Top view)



BONDING PAD LOCATIONS (Top view)



ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, Tamb = 25°C; fosc = 4.332MHz; V_{IN} = 20mVrms unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SUPPLY SECTION						
V_{CC}	Supply Voltage		4.5	5	5.5	V
I_S	Supply Current		6	9	14	mA
FILTER						
F_C	Center Frequency		56.5	57	57.5	KHz
BW	3dB Bandwidth		2.5	3	3.5	KHz
G	Gain	f = 57KHz	18	20	22	dB
A	Attenuation	$\Delta f = \pm 4$KHz f = 38KHz; V_i = 500mVrms f = 67KHz; V_i = 250mVrms	18 50 35	22 80 50		dB dB dB
ΔPh	Phase non linearity	A (see note1) B (see note1) C (see note1)		0.5 1 2	5 7.5 10	DEG DEG DEG
R_i	Input Impedance		100	160	200	KΩ
S/N	Signal to Noise Ratio	V_i = 3mVrms	30	40		dB
V_i	Input Signal	f = 19KHz; T3 ≤ –40dB (see note2) f = 57KHz (RDS + ARI)			1 50	Vrms mVrms
R_L	Load Impedance	Pin 12	100			KΩ
LIMITER						
RA	Resistance pin 8-12		15	21	28	KΩ
V_{OL}	Comp. Output LOW	I_O = +0.5mA			1	V
V_{OH}	Comp. Output HIGH	IO = –0.5mA	4			V
	Duty Cycle	V_i = 1mVrms		50		%
OSCILLATOR						
F_{OSC}	Oscillator Frequency	F_{SEL} = Open F_{SEL} = Closed to Ground		4.332 8.664		MHz MHz
	Output Amplitude			5		V_{PP}
V_{CLL}	Clock Input Level LOW				1	V
V_{OLH}	Clock Input Level HIGH		4			V
CRYSTAL TYPE = EURO QUARTZ						

Note (1):
The phase non linearity is defined as: $\Delta Ph = | -2\,\phi f2 + \phi f1 + \phi f3 |$
where ϕfx is the input-output phase difference at the frequency fx (x = 1,2,3)

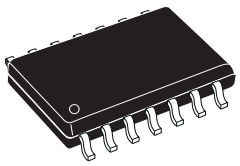
Measure	f1 (KHz)	f2 (KHz)	f3 (KHz)	ΔPh max
A	56.5	57	57.5	<5°
B	56	57	58	<7.5°
C	55.5	57	58.5	<10°

Note (2): The 3th harmonic (57KHz) at the output (pin12) must be less than -40dB in respect to the input signal plus gain.

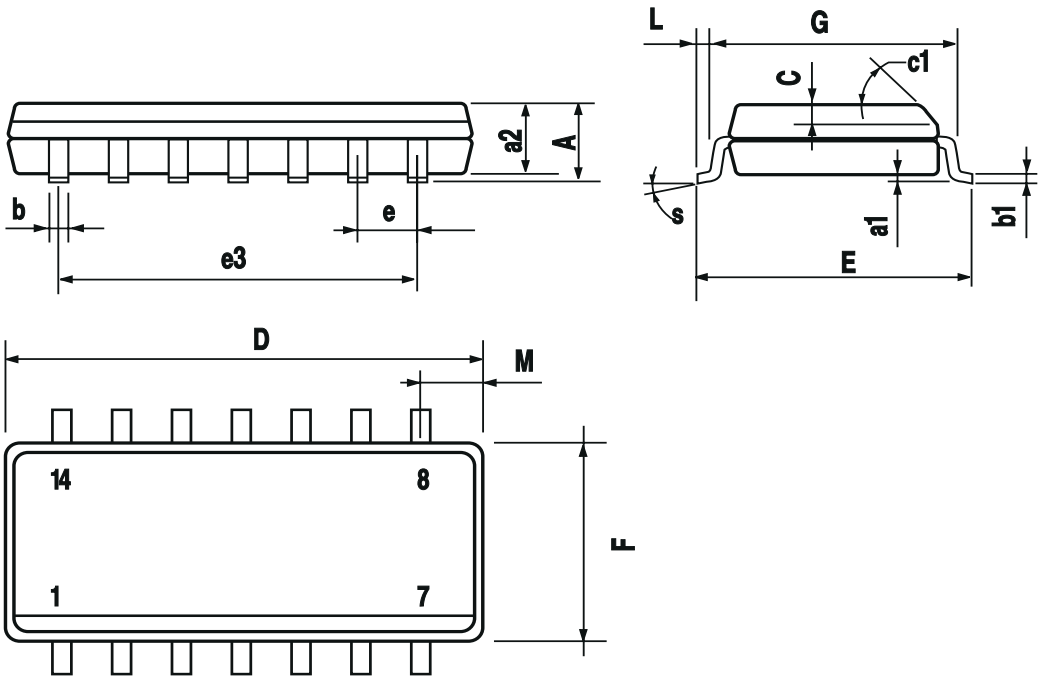
DIM.	mm			inch		
	MIN..	TYP.	MAX..	MIN..	TYP..	MAX..
A			1.75			0.069
a1	0.1		0.25	0.004		0.009
a2			1.6			0.063
b	0.35		0.46	0.014		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.020	
c1	45° (typ.)					
D (1)	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F (1)	3.8		4	0.150		0.157
G	4.6		5.3	0.181		0.209
L	0.4		1.27	0.016		0.050
M			0.68			0.027
S	8° (max)					

(1) D and F do not include mold flash or protrusions. Mold flash or potrusions shall not exceed 0.15mm (.006inch).

OUTLINE AND MECHANICAL DATA

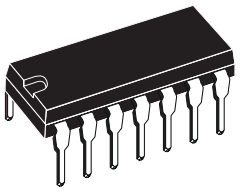


SO14



DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100

OUTLINE AND MECHANICAL DATA



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