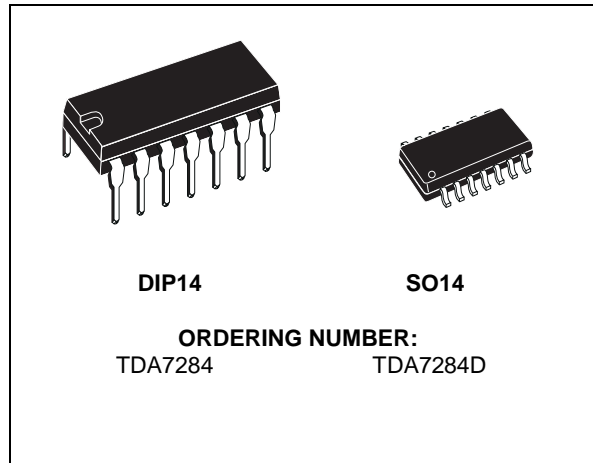


RECORD/PLAYBACK CIRCUIT WITH ALC

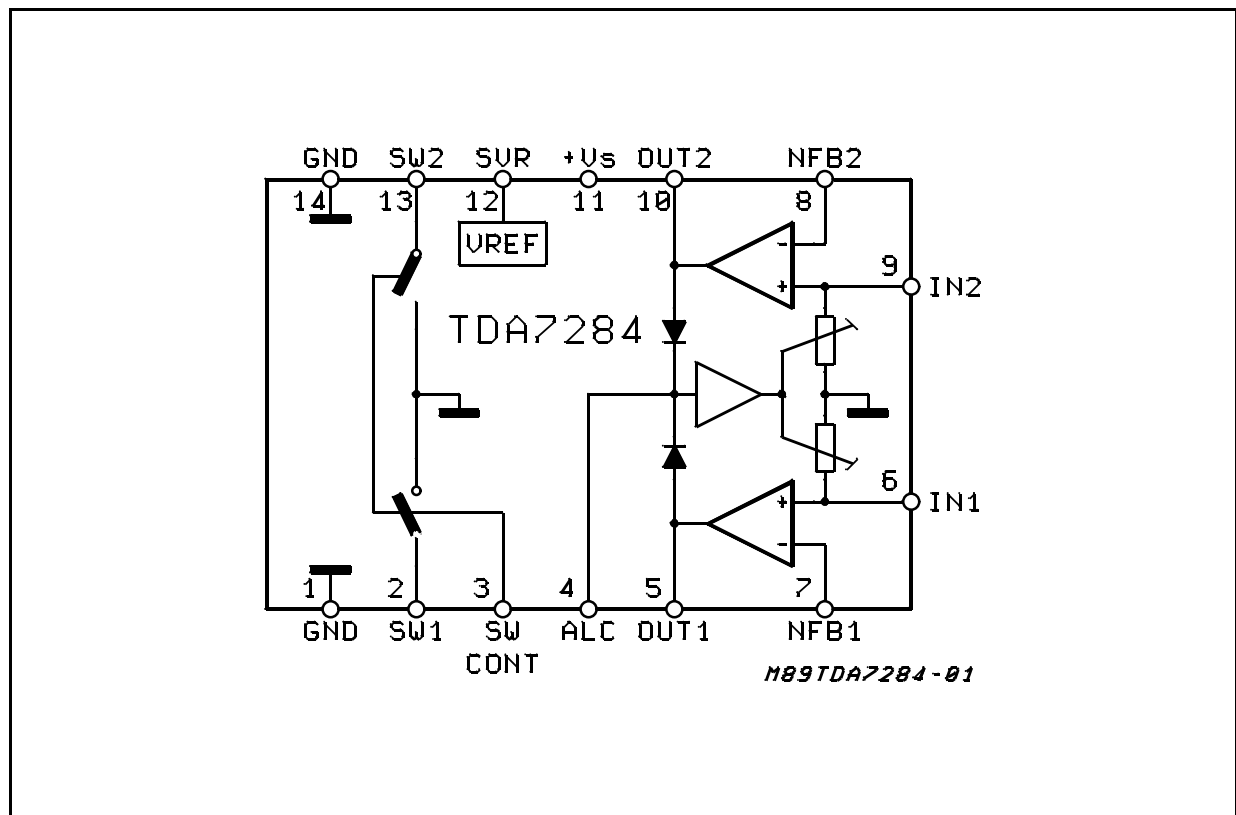
- WIDE OPERATING SUPPLY VOLTAGE (3V to 12V)
- VERY LOW INPUT NOISE ($V_i = 1.2\mu\text{V}$)
- INTERNAL COMPENSATION FOR HIGH GAIN APPLICATION (DOUBLE SPEED RECORDING)
- BUILT-IN ALC CIRCUITRY
- GOOD SVR
- DC CONTROLLED SWITCHES FOR MUTE OR EQUALIZATION SWITCHING FUNCTIONS

DESCRIPTION

The TDA7284 is a monolithic integrated circuit in a DIP/SO-14 designed for 6V, 9V and 12V AC/DC portable cassette equipment application.

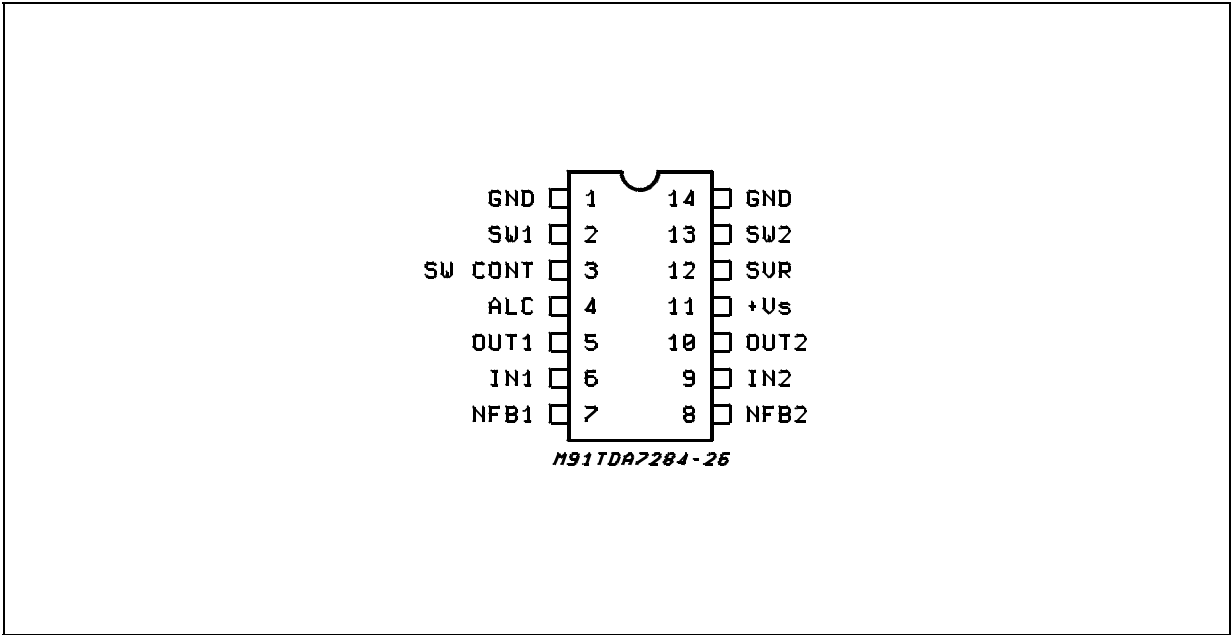


BLOCK DIAGRAM



TDA7284

PIN CONNECTION (Top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	14	V
T_{OP}	Operating Temperature Range	-20 to 70	°C
T_{stg}, T_J	Storage and Junction Temperature Range	-40 to 150	°C

THERMAL DATA

Symbol	Description		S014	DIP14	Unit
$R_{th\ j-amb}$	Thermal Resistance Junction-ambient	Max	200	120	°C/W

DC CHARACTERISTICS ($T_{amb} = 25^{\circ}$; $V_S = 6V$; $V_i = 0V$; $R_i = 10K\Omega$; ALC = OFF)

Terminal No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Terminal Voltage (V)	0	0	0	0	2.6	0	1.3	1.3	0	2.6	6	4.6	0	0

Figure 1: Test and Application Circuit

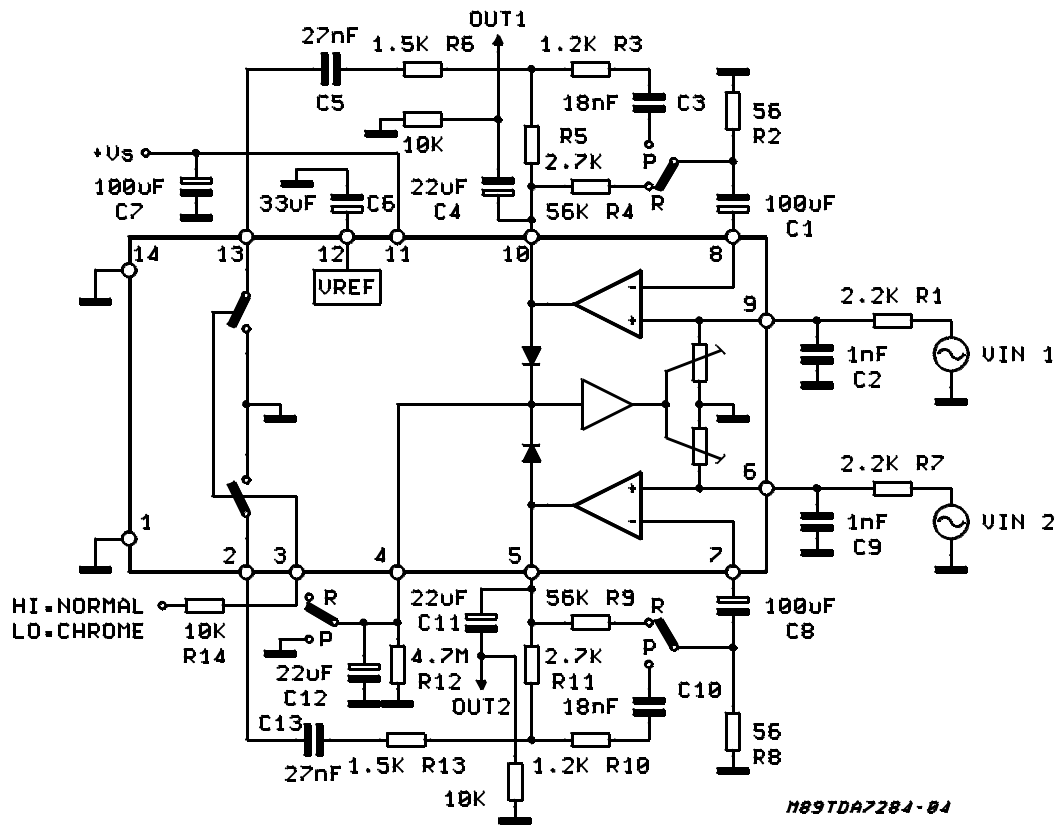
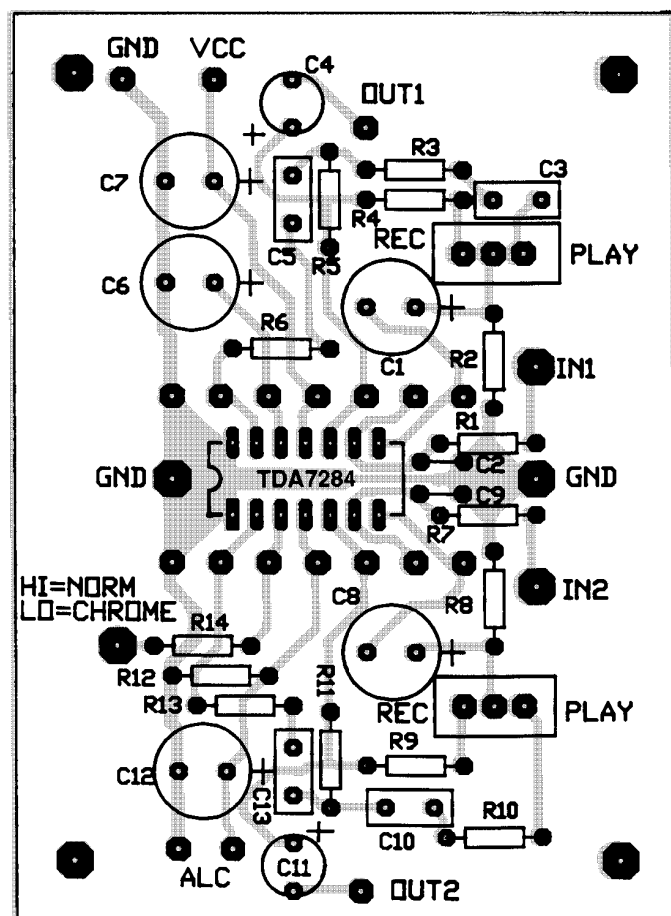


Figure 2: P.C. Board and Component Layout of the Circuit of Fig. 1 (1:1 scale).

ELECTRICAL CHARACTERISTICS ($V_S = 6V$, $T_{amb} = 25^\circ C$ unless otherwise specified refer to test circuit)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply Voltage		3		12	V
I_d	Quiescent Current			4.5	8	mA
E_n	Input Noise	$R_g = 2.2K\Omega$ $BW = 22Hz \text{ to } 22kHz$		1.2		μV
R_I	Input Resistance		30	50	70	$K\Omega$
G_O	Open Loop Gain		65	78		dB
V_O	Output Voltage	THD $\leq 1\%$ ALC OFF ALC ON	1.2 0.7	1.8 0.9	1.1	V_{rms} V_{rms}
THD	Total Harmonic Distortion	$V_O = 1V_{rms}$ ALC = ON $V_I = 100mV$		0.1 0.3	0.5 1	% %
	ALC Range	$\Delta V_O = 3dB$		47		dB
CB	Channel Balance	ALC ON		0	2	dB
SVR	Supply Voltage Rejection	$f = 120Hz$, $C_{SVR} = 33\mu F$ $V_R = 100mV$, $R_g = 10K\Omega$ ALC = Off		50		dB
CS	Cross-talk	ALC OFF		70		dB
Pin 3	Turn Off Threshold	$I_O = <1\mu A$	0.8	1.3		V
Pin 3	Turn On Threshold			1.7	2.25	V
Pin 3	Turn On Saturation	$R_L = 10K\Omega$		0.1	0.2	V

Figure 3: Drain Current vs. Supply Voltage

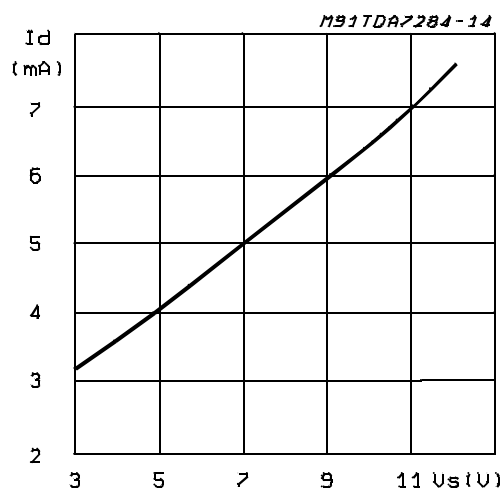


Figure 4: Recording Closed Loop Gain vs. Frequency

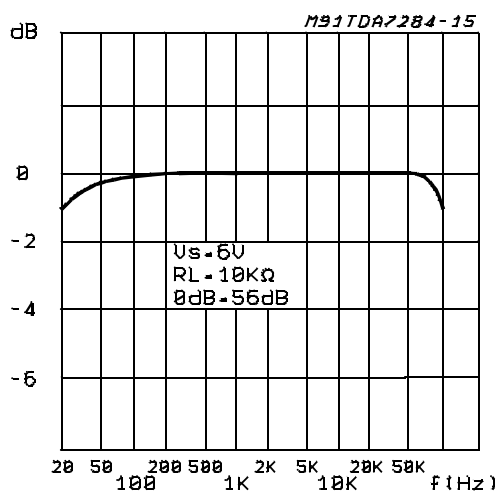


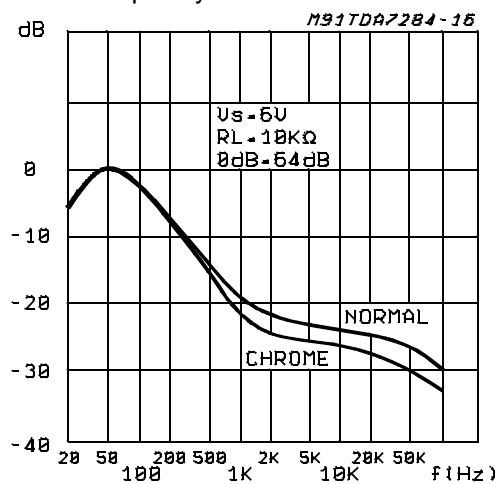
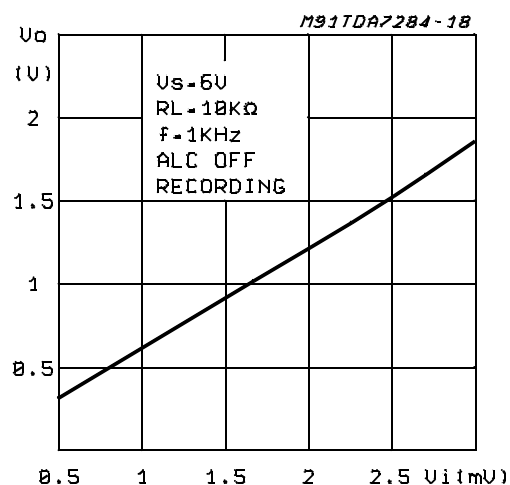
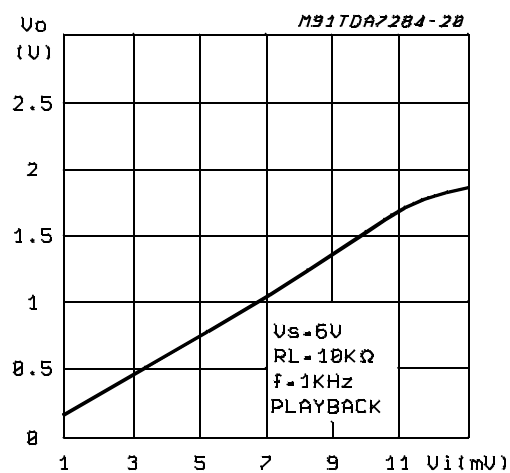
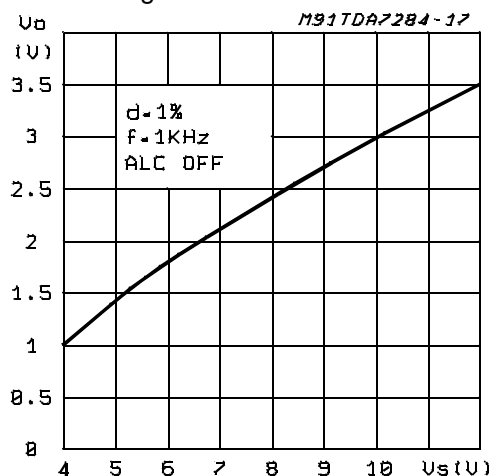
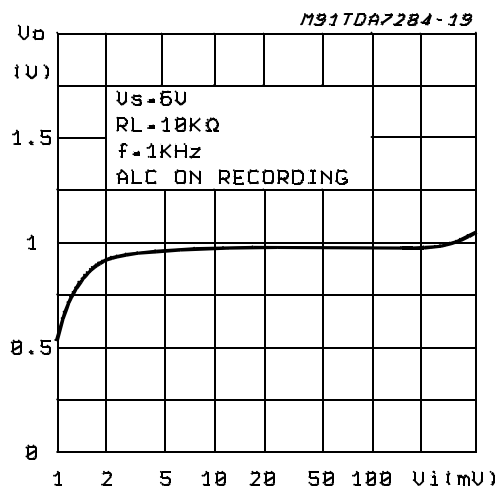
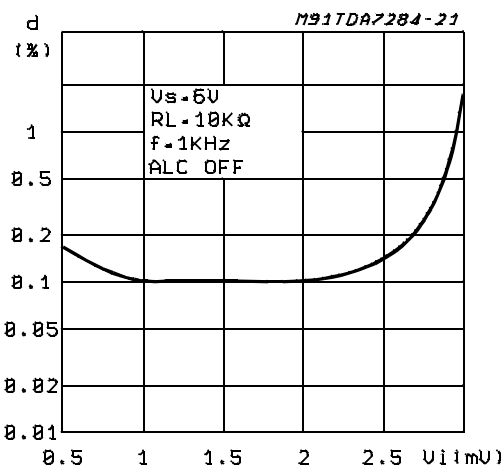
Figure 5: Playback Closed Loop Gain vs Frequency**Figure 7:** Output Voltage vs. Input Voltage**Figure 9:** Output Voltage vs. Input Voltage**Figure 6:** Normalized Output Voltage vs. Supply Voltage**Figure 8:** Output Voltage vs. Input Voltage**Figure 10:** Distortion vs. Input Voltage

Figure 11: Distortion vs. Input Voltage

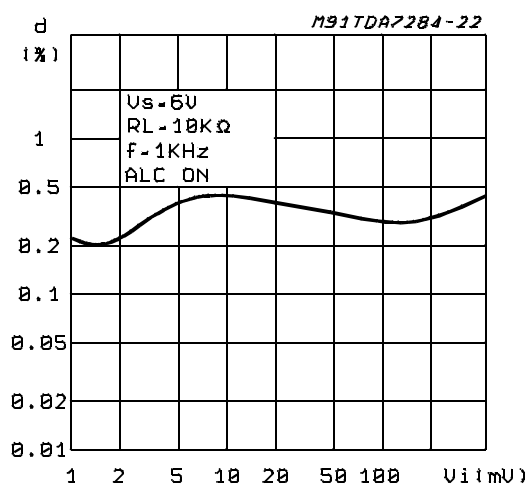


Figure 12: SVR vs. Frequency (ALC = Off)

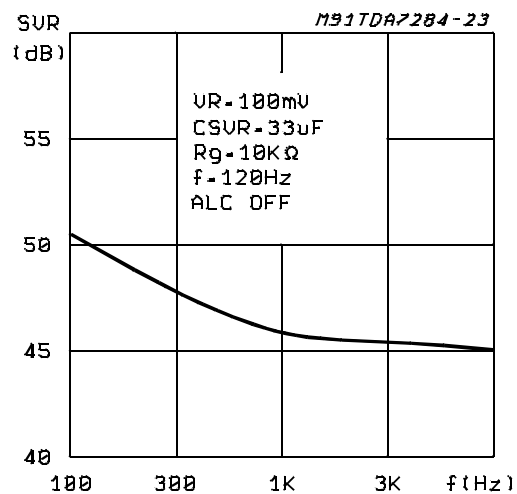


Figure 13: Crosstalk vs. Frequency (ALC = Off)

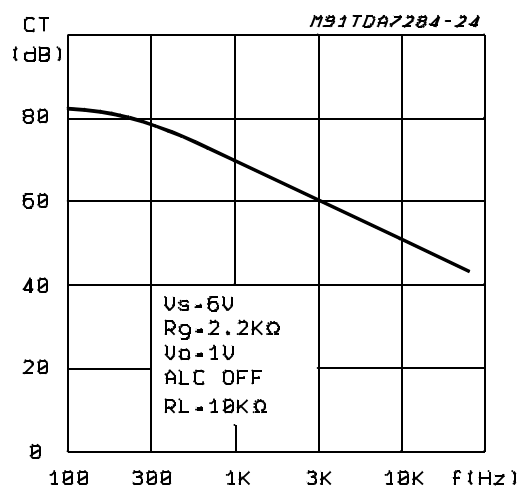
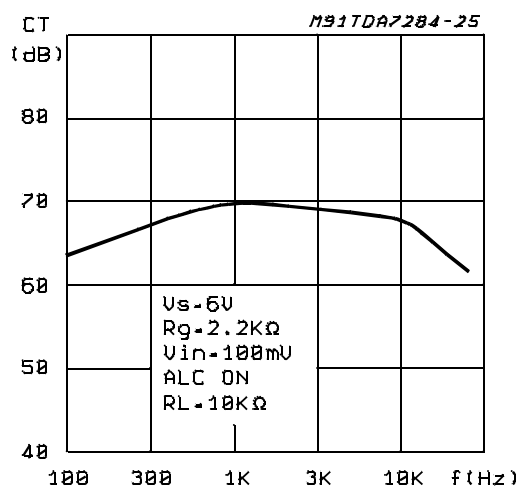


Figure 14: Crosstalk vs. Frequency (ALC = Off)



CIRCUIT DESCRIPTION

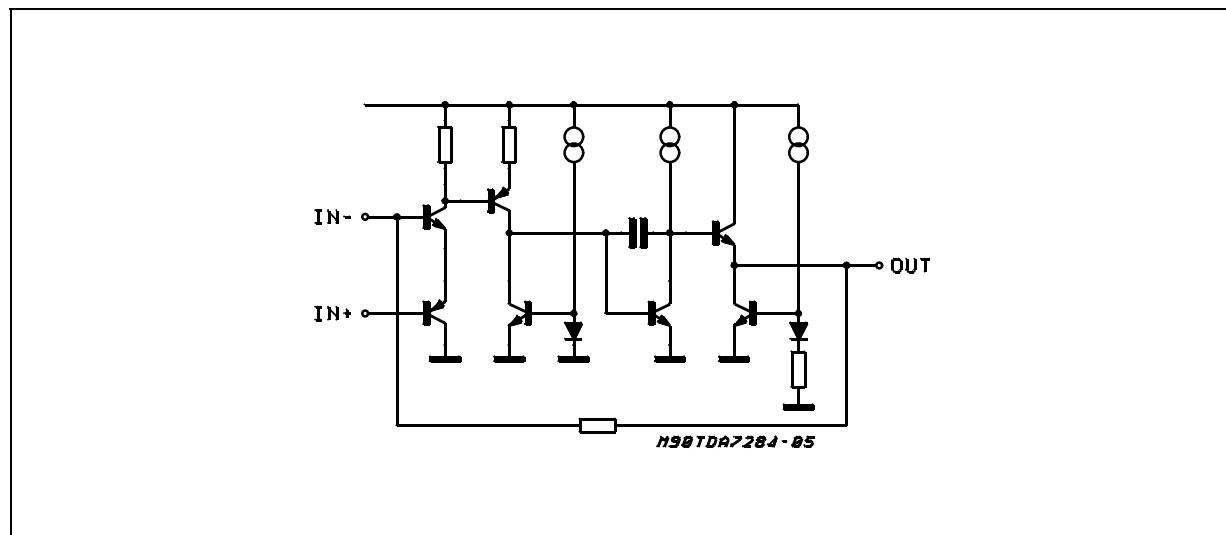
OPERATIONAL AMPLIFIER

The operational amplifier consists essentially of a very low noise input stage decoupled from the

single-ended output stage by means of an emitter follower (fig. 15).

The compensations provided in order to have high gain bandwidth product allowing the use for double speed recording application.

Figure 15

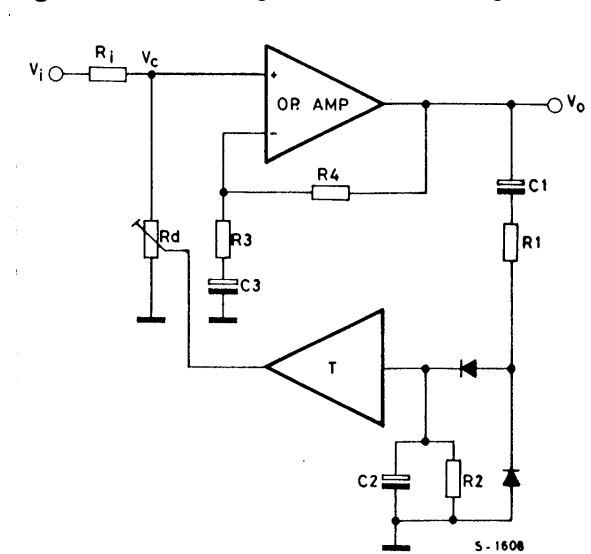


AUTOMATIC LEVEL CONTROL SYSTEM (ALC)

This system maintains the level of the signal to be recorded at a value which prevents saturation of the tape and which optimizes the signal to noise ratio even there are notable variations in the input signal.

Before presenting the ALC circuit of TDA7284 it is worth describing the operation of the automatic level control as a system. A diagram showing the basis of operation is given in fig.16.

Figure 16: Basic Diagram of the ALC stage



This consists of an amplifier (op-amp) having constant gain ($G_v = 1 + R_4/R_3$), which in feedback transforms output signal level information (usually by means of a peak-to-peak detector) into a continuous voltage which drives the networks indicated by T and Rd.

The element T transforms the continuous voltage level into a signal capable of modifying the circuit conditions symbolized by variable resistor Rd.

The value assumed by the resistor Rd is a function of the output signal level Vo and is such that the voltage Vc at the input of the op-amp is constant, even variations of Vi are present. Obviously if Vo is less than a certain value the system is not controlled.

In this case :

$$V_i = V_c = V_o / G_v$$

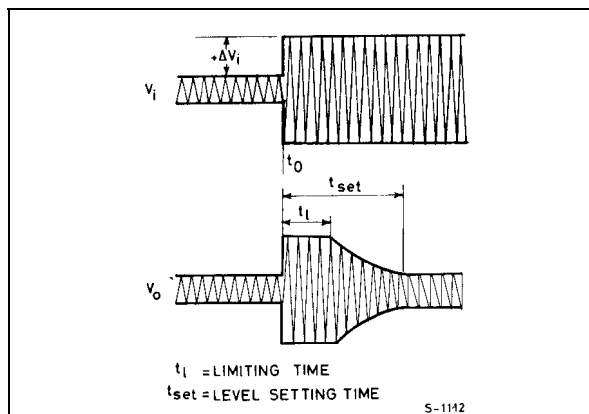
(Gv is the gain of the op-amp)

For the TDA7284 the value of Vo below which the system is not controlled is around 1 Vrms.

Let us now consider the speed of response of the system (when controlled) to positive and negative changes of the input signal i.e. the limiting time, the time for return to nominal level (1 Vrms) and the recovery time.

Limiting time, and time for return to nominal level.

Let us suppose that at certain moment To, the input signal increases by $+\Delta V_i$ as shown in fig. 17.

Figure 17: Limiting and Level Setting Time

Usually such an increase drives the op-amp into saturation and the time for which it remains in this condition is called the limiting time (T_L).

T_L depends on the relationship between the external capacitances, the time constant $T = R_1 \cdot C_1$, the supply voltage and the signal variation.

The criteria for choosing the length of T_L are the result of several compromises. In particular if T_L is too long, there will be audible distortion during playback (during T_L the output is a square wave), and if it is too short, the sensation of increased level will be lost while dynamic compression phenomena and instability may occur.

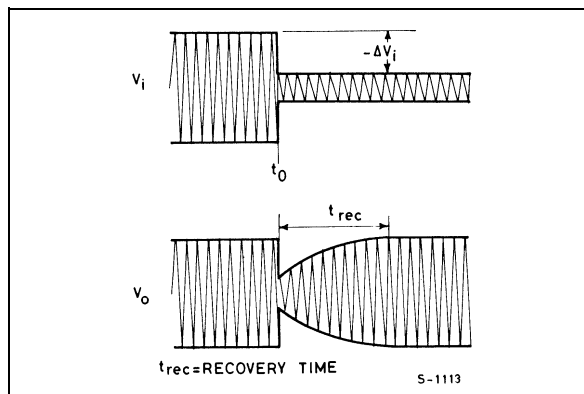
The time for return to nominal level is defined as the total time between the instant T_0 and the instant in which the output reassumes the nominal value. This time (T_s) is roughly equal to $5 \cdot T_L$.

On the basis of tests carried out it has been found that a musical signal with high dynamic range

($\Delta V_i = +40 \text{ dB}$) is to be recorded, the best value of T_s is between 200 and 300ms.

Recovery time.

let us now suppose that at the instant T_0 the input signal decreases of ΔV_i (fig. 18).

Figure 18: Recovery Time

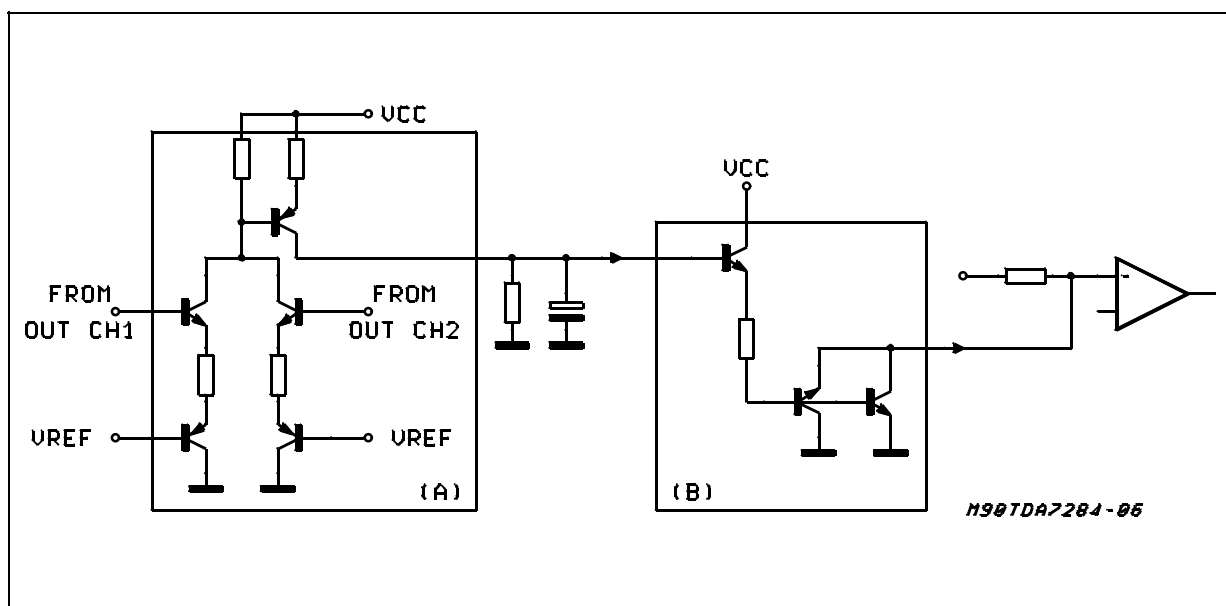
The recovery time (T_{rec}) is defined as the time between the instant T_0 and the instant in which the output signal returns to the nominal level.

This time depends essentially on the discharge time constant of $R_2 \cdot C_2$ (see fig. 16) and on the size of the step $-\Delta V_i$. In this case too, if this time is too long the signal to noise ratio on the tape deteriorates.

If it is too short the sensation of the low signal level is lost during playback.

The ALC system of the TDA7284

Fig. 16 becomes the following (fig. 19) where the

Figure 19

peak-to-peak detector of fig. 16 is now inside the broken line 1 while the system which allows a dynamic resistance varying with the DC voltage level (i.e. inversely proportional to the op-amp output signal), is inside the broken line 2.

It should be noted that the generator resistance R_i has no influence on the controlled voltage value V_c , although its value should be between 1 and 47 Kohm.

The lower limit is determined by the minimum dynamic resistance of 10 ohm and therefore to have a control range of 40 dB for the input signal, R_i must be greater than 1.5 Kohm.

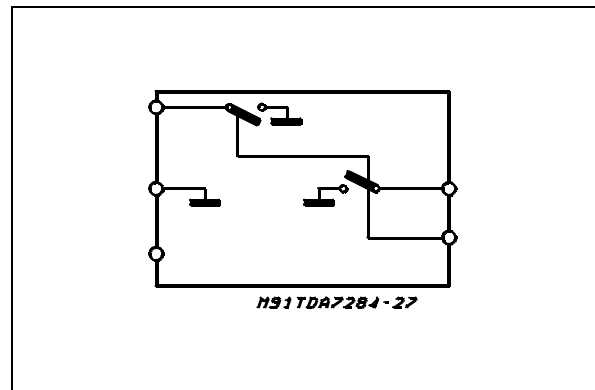
The upper limit results from the necessity to limit the attenuation of the signal by the input impedance of the op-amp.

Switches

Two DC-controlled switches are also included in the chip (fig. 20)

Fig. 19 shows the typical application circuit of the TDA7284 utilizing the equalization switch for normal or chrome tape playback equalization. The advantage is the components can be placed near

Figure 20



to the IC, while the tape selector switch can be at a remote location, hence reduce the chances of noise and oscillation due to components layout. Another advantage is that only one pole is needed for the tape selector switch as compared to the two poles needed by conventional circuits (one separate pole for each channel).

Fig. 22 shows the use of the switches to obtain the mute function.

Figure 21: Application Circuit with DC Switching of Normal/Chrome Tape Equalization

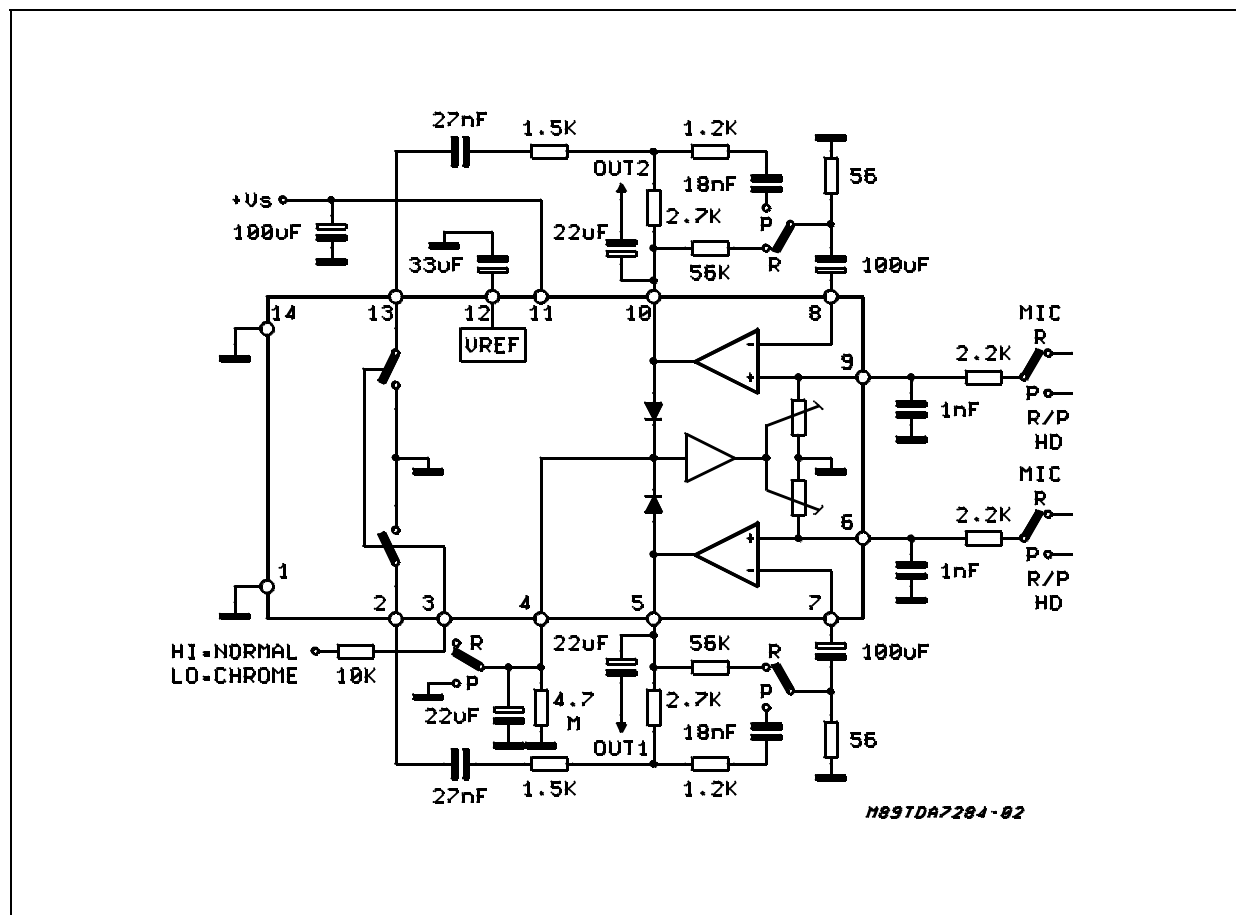
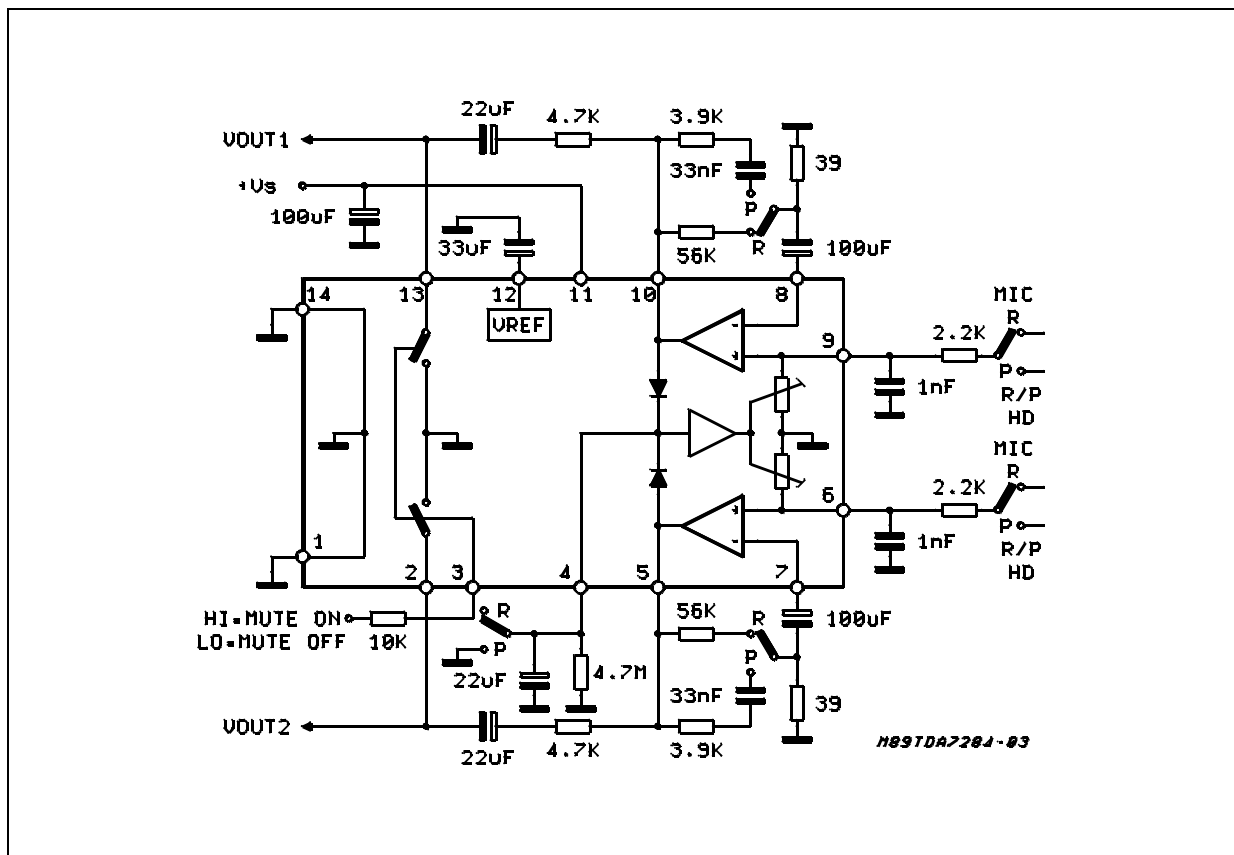


Figure 22: Application Circuit with Output Muting**SVR**

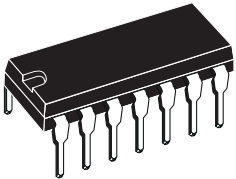
A reference circuit is enclosed to provide a stable voltage and to supply a stable current to all cur-

rent mirrors.

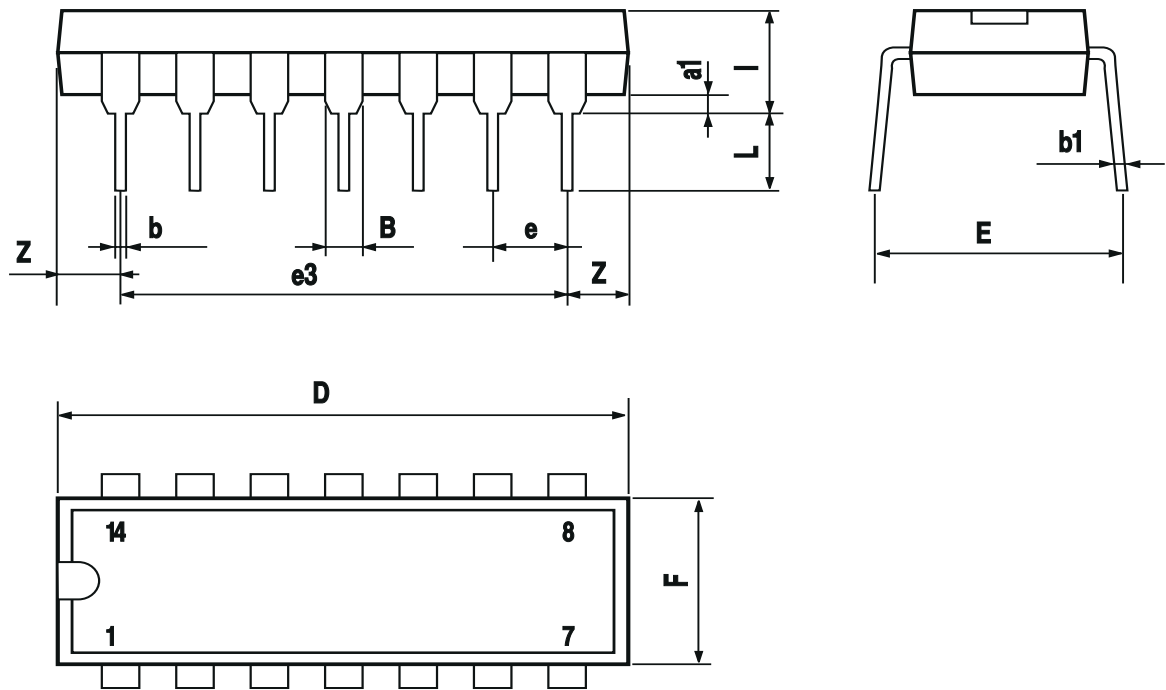
SVR capacitor is also connected to this block for good ripple rejection.

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100

**OUTLINE AND
MECHANICAL DATA**

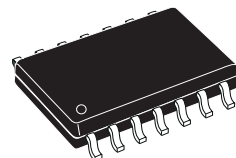


DIP14



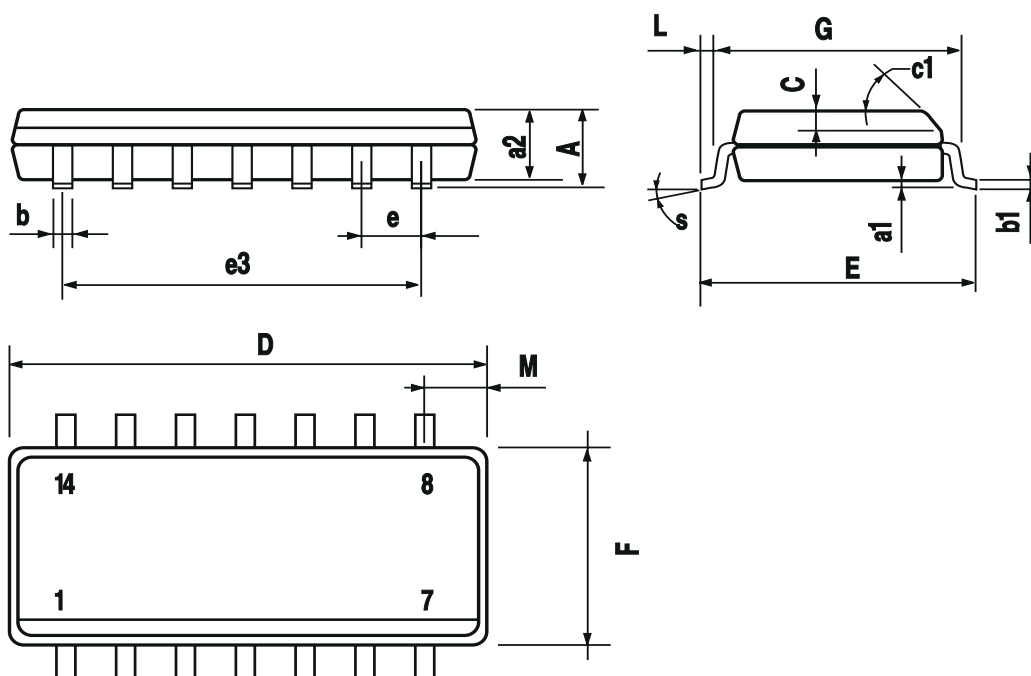
DIM.	mm			inch		
	MIN..	TYP.	MAX..	MIN..	TYP..	MAX..
A			1.75			0.069
a1	0.1		0.25	0.004		0.009
a2			1.6			0.063
b	0.35		0.46	0.014		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.020	
c1	45° (typ.)					
D (1)	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F (1)	3.8		4	0.150		0.157
G	4.6		5.3	0.181		0.209
L	0.4		1.27	0.016		0.050
M			0.68			0.027
S	8° (max)					

OUTLINE AND MECHANICAL DATA



SO14

(1) D and F do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (.006inch).



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