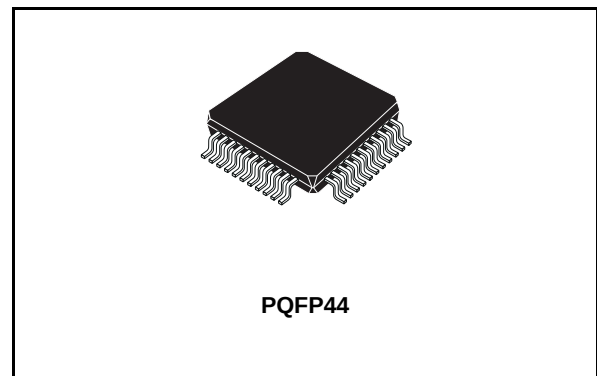


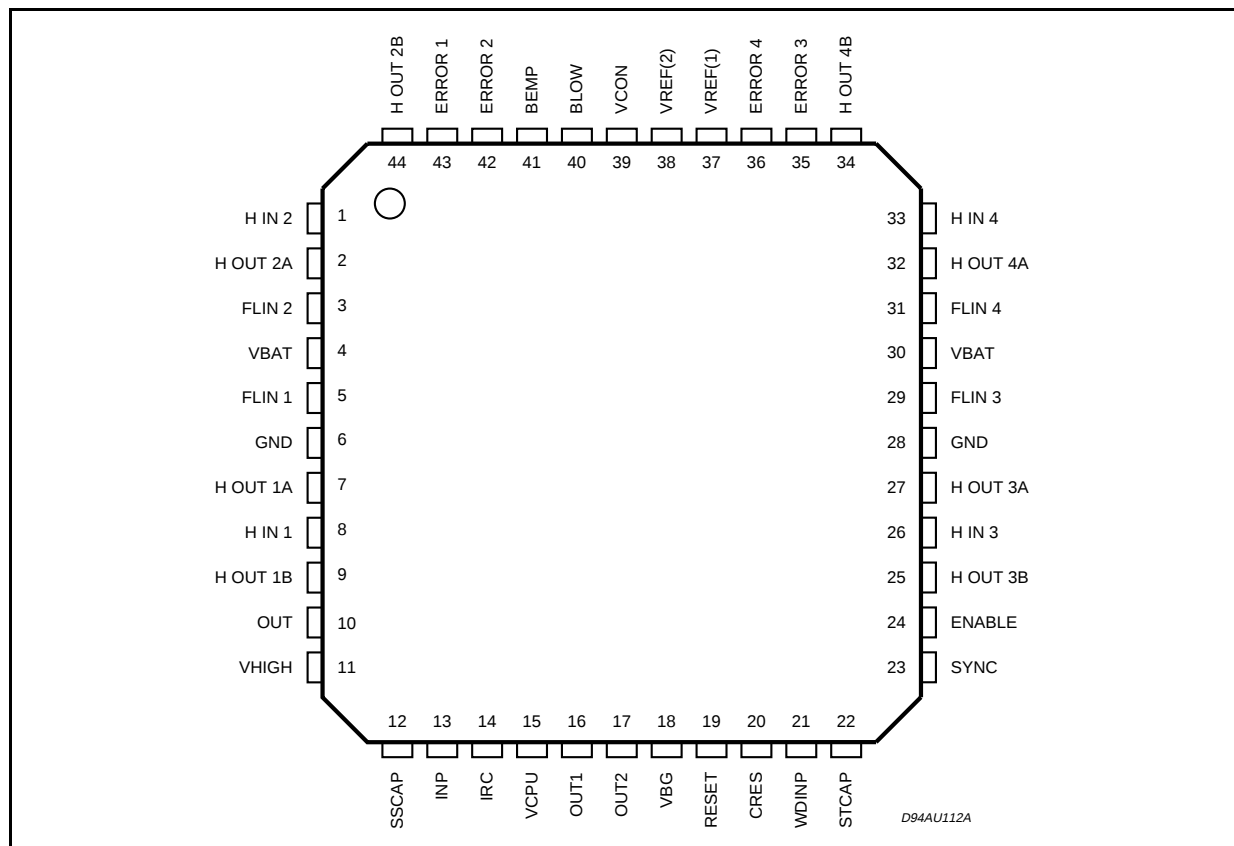
HIGH-EFFICIENCY CD ACTUATOR DRIVER

- WIDE OPERATIVE SUPPLY RANGE (1.6 to 5V) LOW VOLTAGE OPERATION CAPABILITY
- 4 LOAD DRIVING VOLTAGES PWM REGULATED (STEP DOWN FROM BATTERY)
- LOW ON RESISTANCE H BRIDGES (2 x 1.6Ω MAX + 2 x 2.5Ω MAX) FOR:
 - FOCUS AND TRACKING ACTUATORS
 - SLEDGE AND SPINDLE MOTORS
- SYNCHRONIZABLE SAWTOOTH OSCILLATOR
- CONFIGURABLE DC/DC CONVERTER FOR ADJUSTABLE MAIN POWER SUPPLY, WITH LOW ON RESISTANCE (0.4Ω MAX) SWITCH
- GENERAL ENABLE INPUT
- ADJUSTABLE WATCH DOG AND DELAYED POWER ON RESET FUNCTIONS



- ADJUSTABLE COMPARATORS FOR BATTERY LOW AND BATTERY EMPTY DETECTION

PIN CONNECTION



ABSOLUTE MAXIMUM RATINGS (25°C)

Pin Name	Min	Max	Unit
HIN 1, HIN 2, HIN 3, HIN 4	-0.4	8	V
HOUT 1A, HOUT 2A, HOUT 3A, HOUT 4A, HOUT 1B, HOUT 2B, HOUT 3B, HOUT 4B	-0.4	8	V
FLIN 1, FLIN 2, FLIN 3, FLIN 4	-0.4	10	V
ERROR 1, ERROR 2, ERROR 3, ERROR 4,	-0.4	7	V
V _{BAT}	-0.4	8	V
V _{REF 1} , V _{REF 2}	-0.4	7	V
BLOW, BEMP, V _{CON}	-0.4	7	V
OUT, VHIGH	-0.4	16	V
OUT 2	-0.4	8	V
OUT 1	-0.4	16	V
SSCAP, IRC, INP	-0.4	7	V
V _{CPU}	-0.4	7	V
VBG, RESET, CRES, WDINP, STCAP, SYNC	-0.4	7	V
EN	-0.4	8	V

* Pin 1, 8, 12, 14, 20, 26 and 33 are ESD sensitive (max. voltage $\pm 1\text{KV}$)

THERMAL DATA

Symbol	Parameter	Value	Unit
T _{op}	Operating Temperature range	-25 to 70	°C
T _j	Max. Junction Temperature	100	°C
T _{j-amb}	Thermal Resistance Junction to Ambient	70	°C/W

PIN FUNCTIONS

N°	Name	Function	
21	WDINP	Watch dog input - AC coupled to WD μ controller output (Disabled when connected to GND)	Watch dog & reset circuit
20	CRES	Start up reset control for μ C & watch dog time constant	
19	RESET	Reset output command to μ C (open collector)	
41	BEMP	Battery empty comparator input	Battery control circuit
40	BLOW	Battery low comparator input	
39	VCON	Battery level control output VCON = Z VBEMP > VBCON > VBG VCON = 1 VBEMP > VBG > VBLOW VCON = 0 VBG > VBEMP > VBLOW	
24	ENABLE	General Enable Input (active Low)	Band Gap Reference
18	VBG	Reference voltage capacitor	
12	SSCAP	Soft start capacitor	VCPU DC-DC converter
16	OUT 1	Switching transistor terminal high	
17	OUT 2	Switching transistor terminal low	
15	VCPU	Regulated voltage	
14	IRC	Error amplifier output	
13	INP	Error amplifier inverting input	
11	VHIGH	Regulated Voltage	Vhigh Boost DC-DC Converter
10	OUT	Switching transistor output	
22	STCAP	Sawtooth toth	Oscillator
23	SYNC	Oscillator synchronizing input	
4, 30	V _{BAT}	Power supply voltage	
6, 28	GND	Power ground	
38	VREF 2	Buffered reference output voltage	
37	VREF 1	Reference input voltage	
5	FLIN 1	Switching Output	Focus actuator step down converter & H bridge
7	HOUT 1A	H bridge positive output	
8	HIN 1	Regulated voltage H bridge supply	
9	HOUT 1B	H bridge negative output	
43	ERROR 1	Error input	
29	FLIN 3	Switching Output	Tracking actuator step down converter & H bridge
27	HOUT 3A	H bridge positive output	
26	HIN 3	Regulated voltage H bridge supply	
25	HOUT 3B	H bridge negative output	
35	ERROR 3	Error input	
3	FLIN 2	Switching output	Spindle motor step down converter & H bridge
2	HOUT2A	H bridge positive output	
1	HIN 2	Regulated voltage H bridge supply	
44	HOUT 2B	H bridge negative output	
42	ERROR 2	Error input	

ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}\text{C}$, $V_{BAT} = 1.6\text{V}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{BAT}	Power Supply ($T_{amb} = 25$ to 70°C)	Config. in fig. 3a: $V_{CPU} < 4\text{V}$	1.6		V_{CPU}	V
		Config. in fig. 3a: $V_{CPU} > 4\text{V}$	1.6		4	V
		Config. in fig. 3b	$V_{CPU} + 0.3$		4	V
		Config. in fig. 3c	1.6		4	V
	Stand-by condition					
	Config. in fig 3a				4	V
	Power Supply ($T_{amb} = 25$ to 60°C)	Config. in fig. 3a	1.6		V_{CPU}	V
		Config. in fig. 3b	$V_{CPU} + 0.3$		5	V
		Config. in fig. 3c	1.6		5	V
		Stand-by condition				
	Config. in fig 3a				5.5	V
	Current Consumption from V_{CPU} (1)	$V_{CPU} = 5\text{V}$		5		mA
	Current Consumption from V_{BAT} (3)			1.5		mA
	Leakage Current in stand-by condition	$V_{BAT} = 5\text{V}$			20	μA
V_{HIGH} $V_{CPU}(\text{adj})$	Output Voltages		$V_{BAT} + 4$ 2.4	$V_{BAT} + 7$	$V_{BAT} + 12$ 5	V V
	R_{ON} of DC/DC Converter Switch	$I = 1\text{A}$		0.25	0.4	Ω
	Max Output Current from V_{CPU}	$V_{CPU} < 4.5\text{V}$ Config. fig 3a	150			mA
	Voltage Ripple on V_{CPU}					
	Oscillator - free freq. - sync. freq. - Δ free freq.	STCAP = 470pF . $V_{BAT} = 1.6$ to 5V	80	200	180 20	KHz KHz KHz
	H_bridge - Ron, actuators (CH 1,3) - Ron, motors (CH 2,4)	$I = 100\text{mA}$		1.0 1.6	1.6 2.5	Ω Ω
	PWM Circuit - Ron, actuators - Ron, motors	$I = 100\text{mA}$		0.5 0.8	0.8 1.25	Ω Ω
V_{BG}	Reference Voltage		1.22	1.28	1.34	V
	Load Regulation	$I_{LOAD} = -10$ to $+10\mu\text{A}$	-30		30	mV
	Line Regulation	$V_{BAT} = 1.6$ to 5V			30	mV
AV	Bridge gain	From Error to H_{IN}	2.8	3.6	4.5	
K	Reset Time Coefficient	note 2	7.4	11	17.2	msec/ μF
Z_{IN}	Error Impedance Inputs		26	40		k Ω
	V_{REF2} Load Regulation	$I_{LOAD} = -1$ to $+1\text{mA}$	-30		30	mV
	V_{REF1} Impedance			750		k Ω
	WINDIP Impedance			30		k Ω
	BEMP & BLOW intervention threshold		0.55	0.65	0.75	V
	RESET Voltage Saturation	$I_{LOAD} = -100\mu\text{A}$			200	mV
	VCON Voltage Saturation	$I_{LOAD} = -100\mu\text{A}$ $I_{LOAD} = 100\mu\text{A}$	$V_{CPU}-200$		200	mV mV

(1): all the 4 PWM outputs switched off.

(2) $T_{RESET} = \text{width of the Reset pulse on pin 19} = K \cdot C$, where C is the capacitance on pin 20 (C_{RES}).
To avoid reset, the frequency of watch dog pulses must be greater than $(3 \cdot T_{RESET})^{-1}$

(3) All the 4 PWM output switched OFF, auxiliary and main DC/DC converters polarized but not switching

Figure 1: Block Diagram.

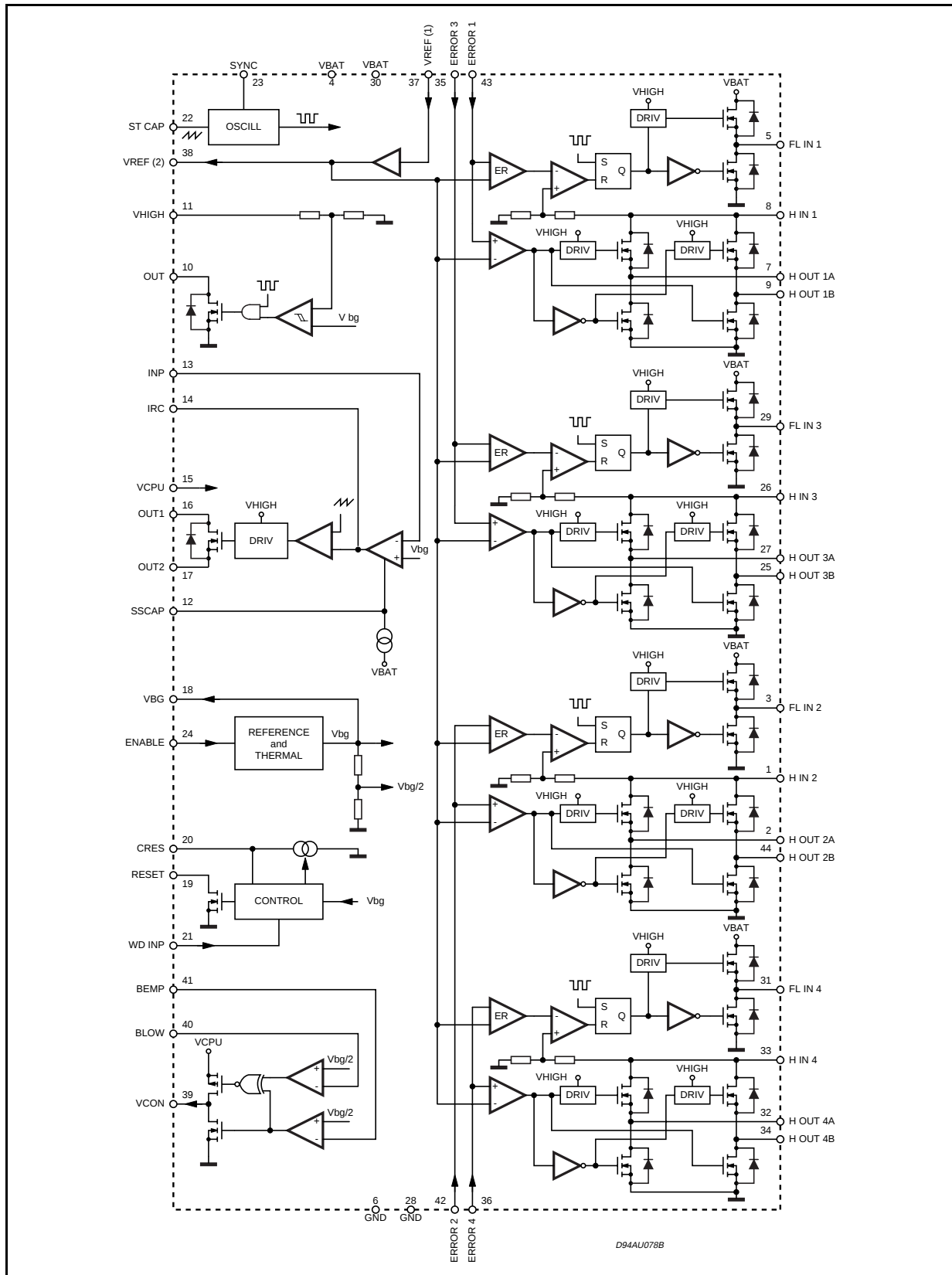


Figure 2: Test Circuit

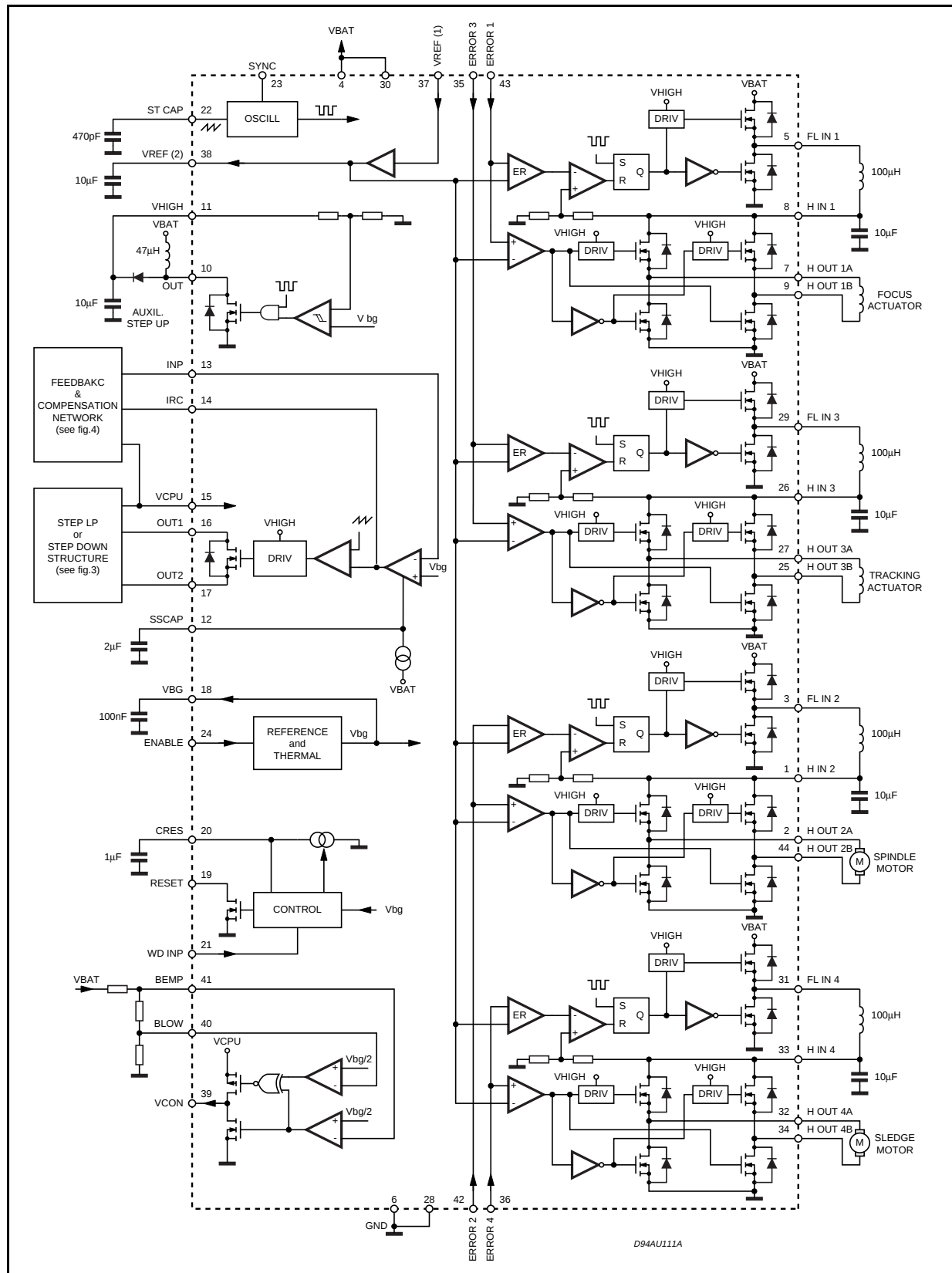
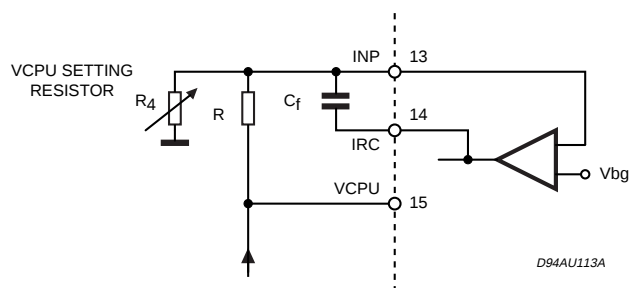
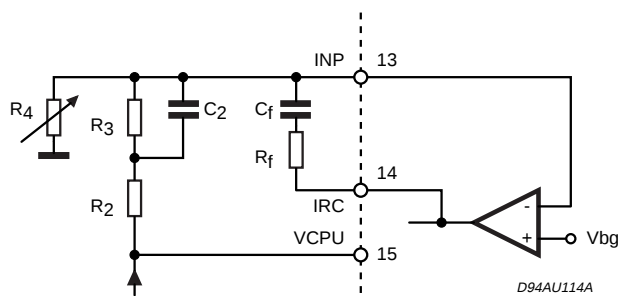
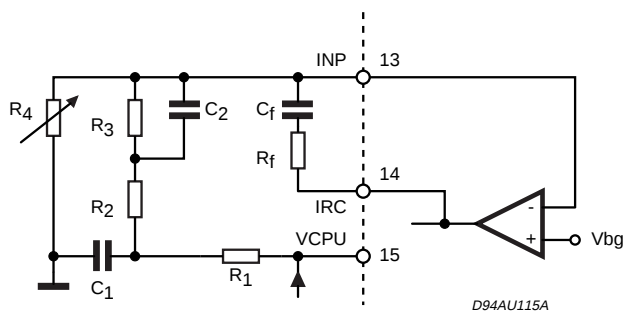


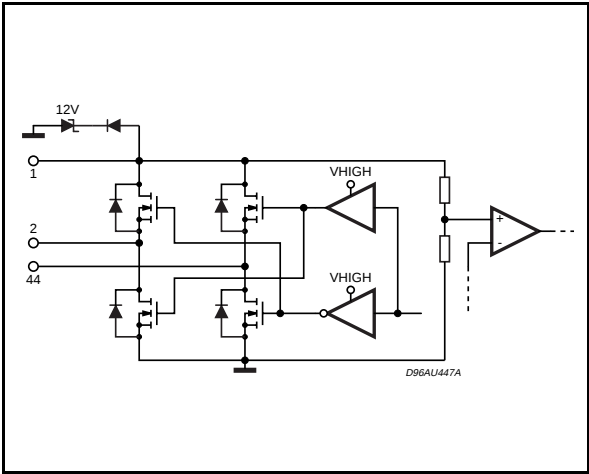


Figure 4: DC – DC Converter: Feedback and Compensation Networks.**a) Dominant Pole Compensation****b) Extended Bandwidth 2 zero, 2 pole compensation****c) Extended Bandwidth 2 zero, 3 pole compensation**

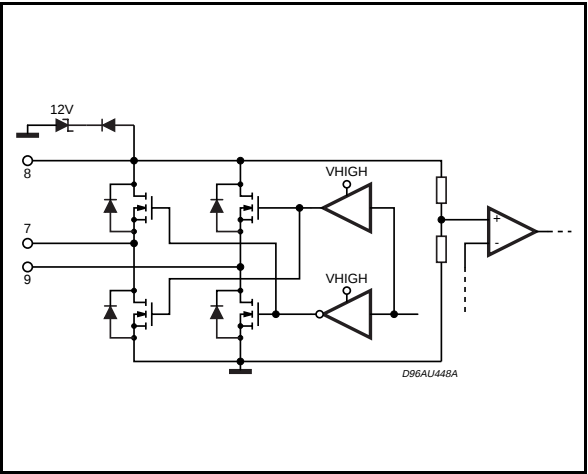
SUGGESTED VALUES FOR OUTPUT FILTER AND COMPENSATION NETWORK

DC- DC COVERTER CONFIGURATIONS	OUTPUT FILTER (see fig. 3)	COMPENSATION (see fig. 4)
STEP-DOWN	L = 47μH C = 47μF	a) DOMINANT POLE R = 50KΩ Cf = 47nF R4 = 35KΩ
		b) 2 ZERO, 2 POLE R2 = 11.18KΩ R3 = 100 KΩ C2 = 936pF Rf = 16.65KΩ Cf = 5.6nF R4 = 70KΩ
STEP-UP AND TRANSFORMER	L = 47μH C = 47μF	a) DOMINANT POLE R = 100KΩ Cf = 220nF R4 = 70KΩ
		c) 2 ZERO, 3 POLE R1 = 500Ω C1 = 18nF R2 = 20.8KΩ R3 = 250KΩ C2 = 636pF Rf = 21.4KΩ Cf = 7.44nF R4 = 200KΩ
	L = 11μH C = 47μF	c) 2 ZERO, 3 POLE R1 = 500Ω C1 = 18nF R2 = 10.4KΩ R3 = 250KΩ C2 = 318pF Rf = 21.4KΩ Cf = 3.7nF R4 = 200KΩ

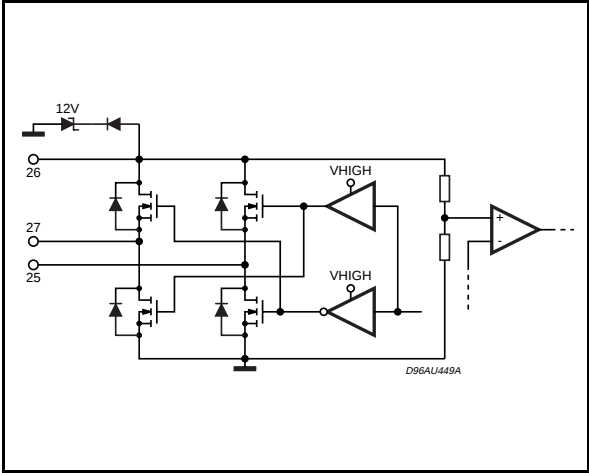
PINS: 1, 2, 44



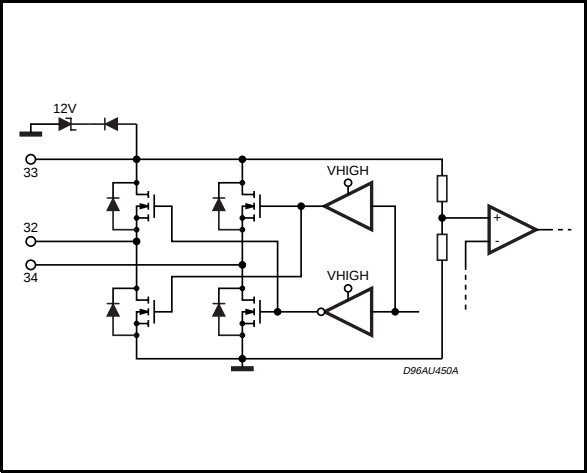
PINS: 8, 7, 9



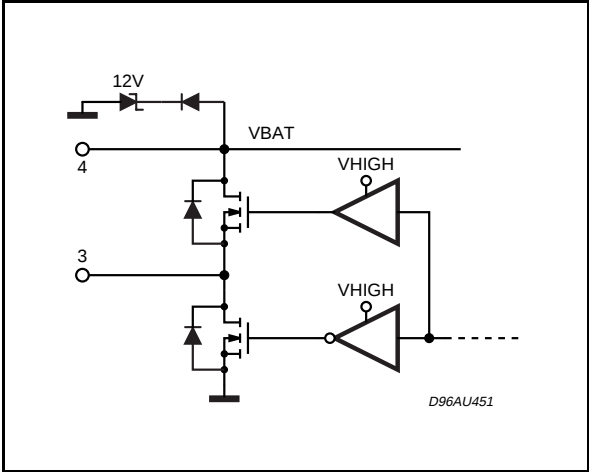
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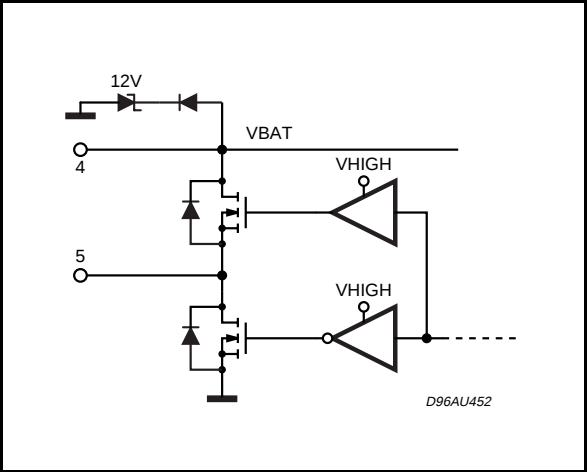
PINS: 32, 33, 34



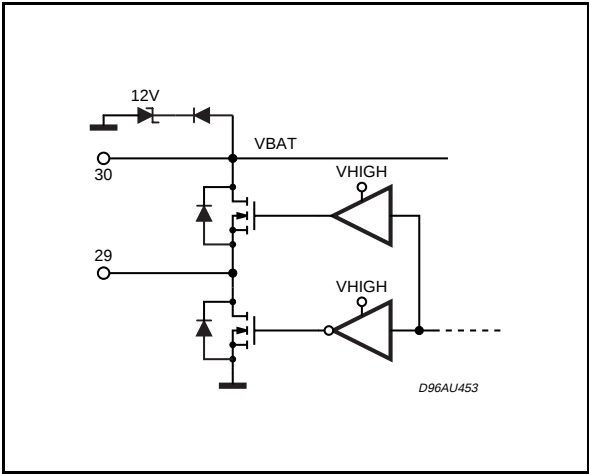
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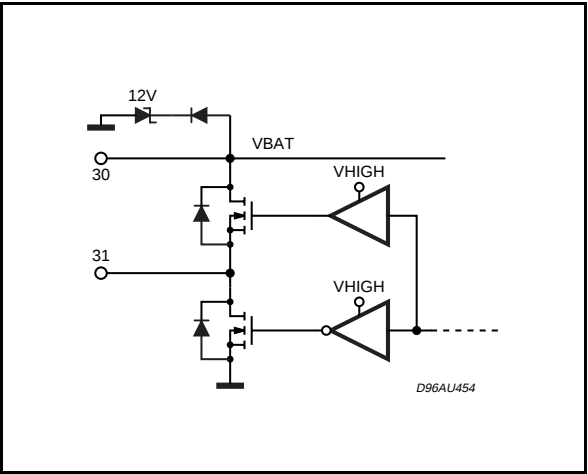
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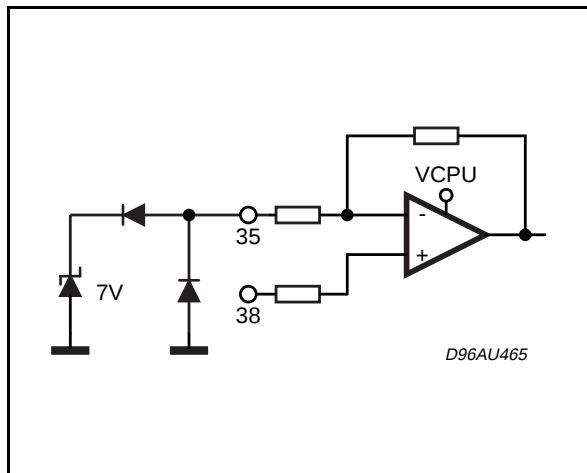
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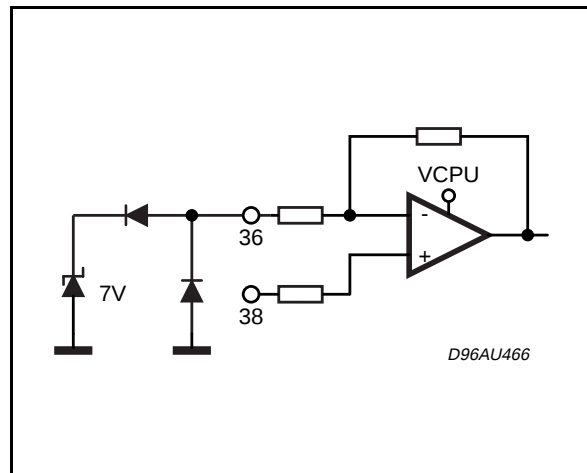
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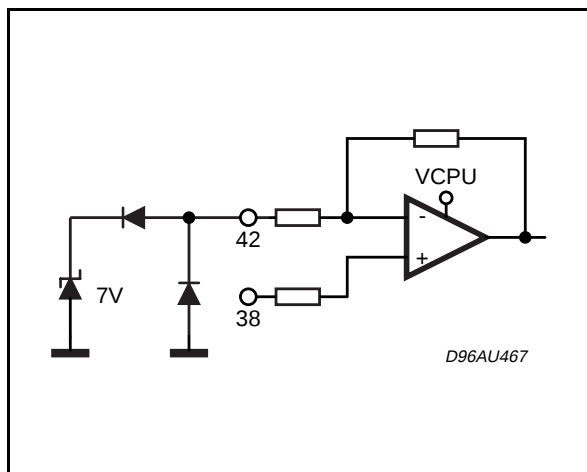
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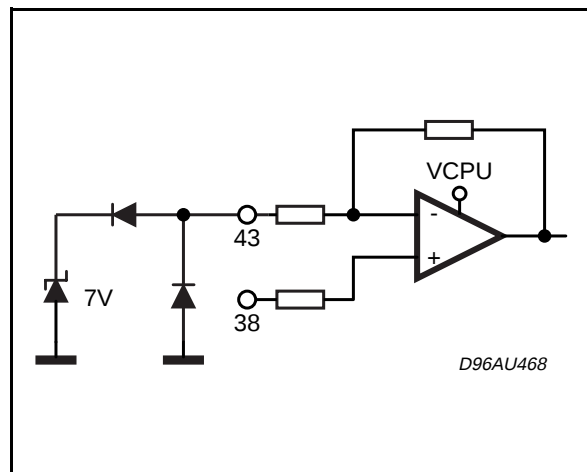
PIN: 36



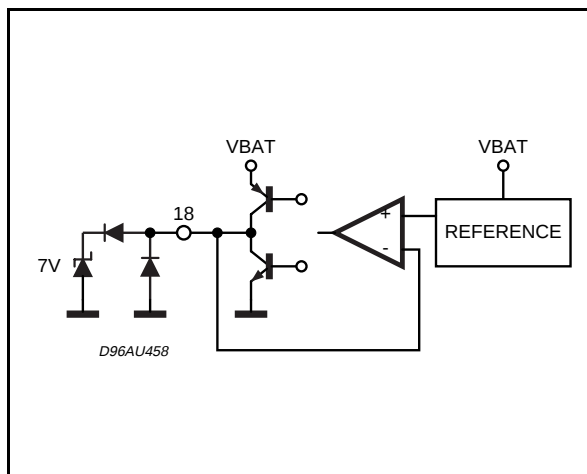
PIN: 42



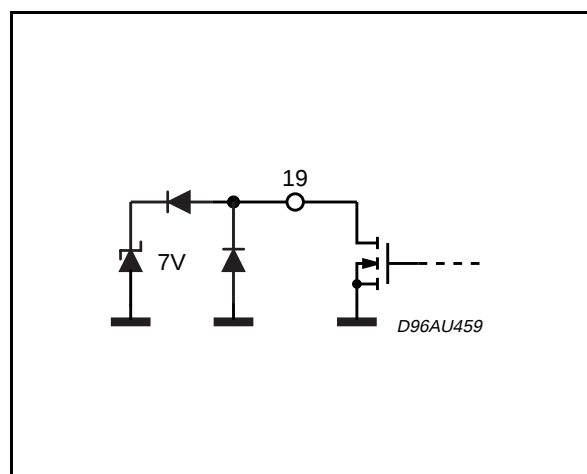
PIN: 43



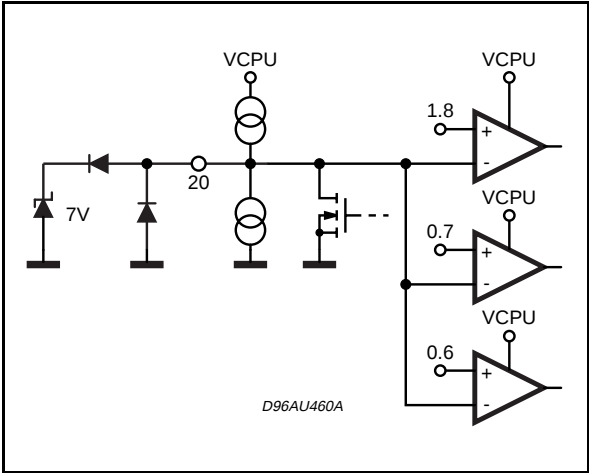
PIN: 18



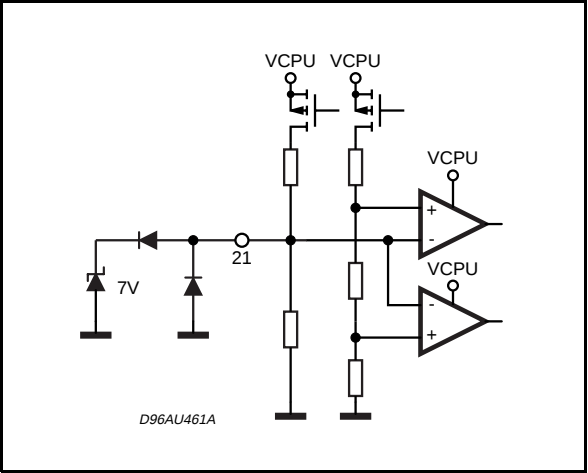
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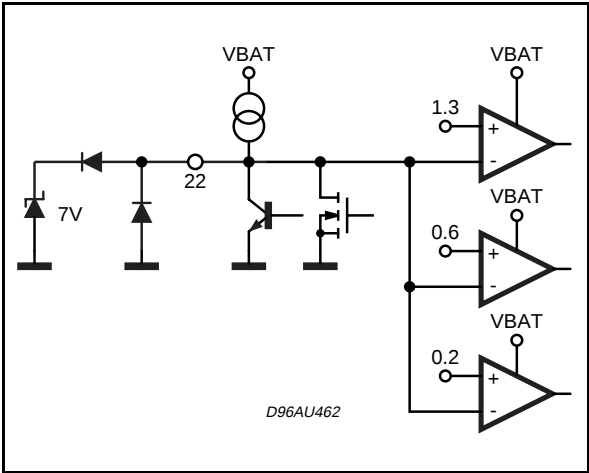
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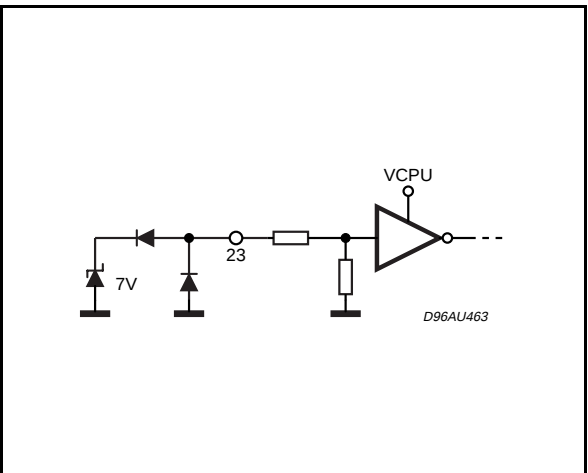
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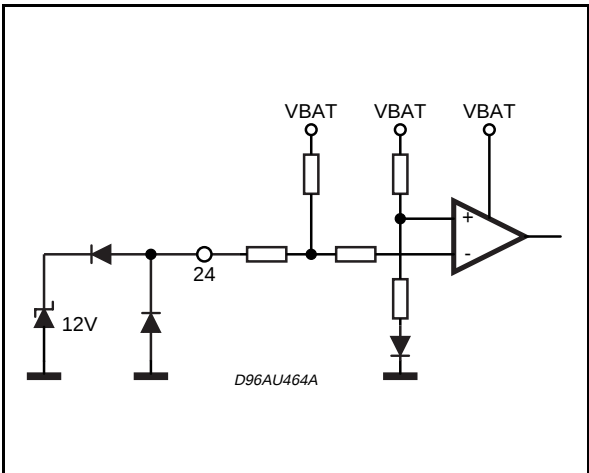
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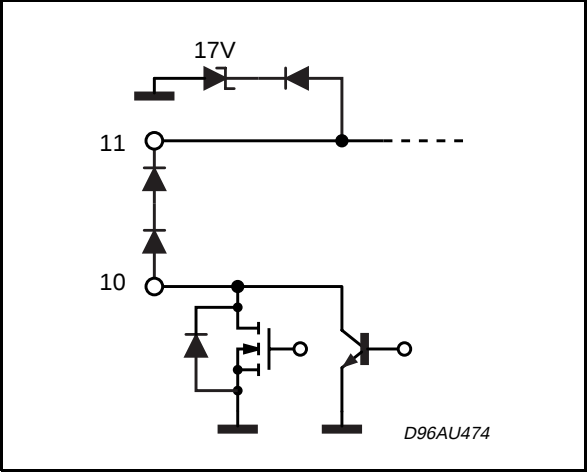
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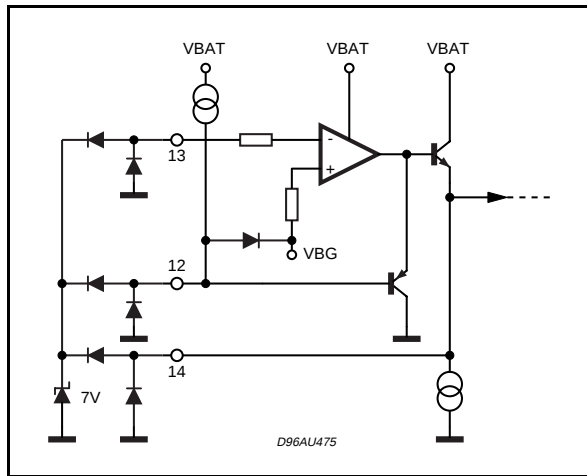
PIN: 24



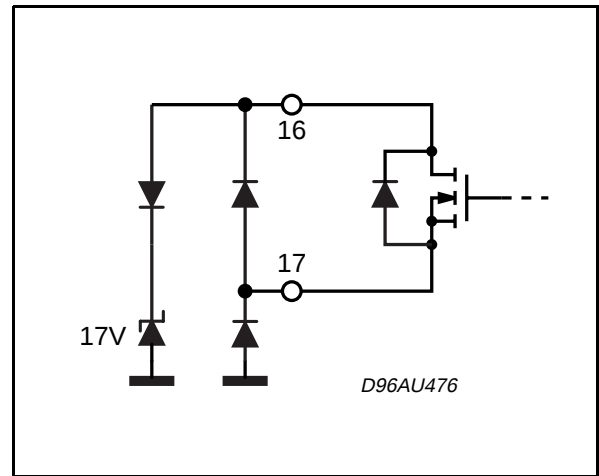
PINS: 10, 11



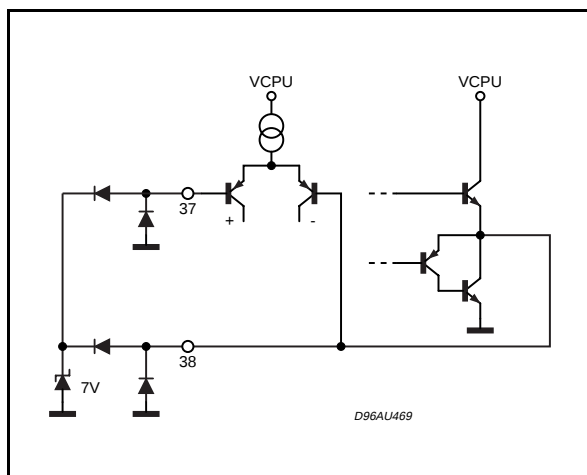
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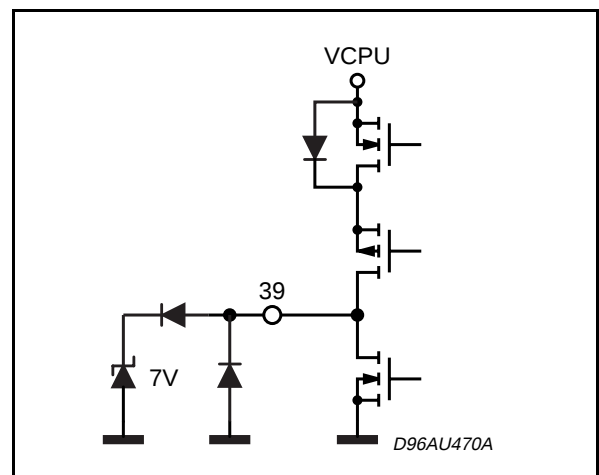
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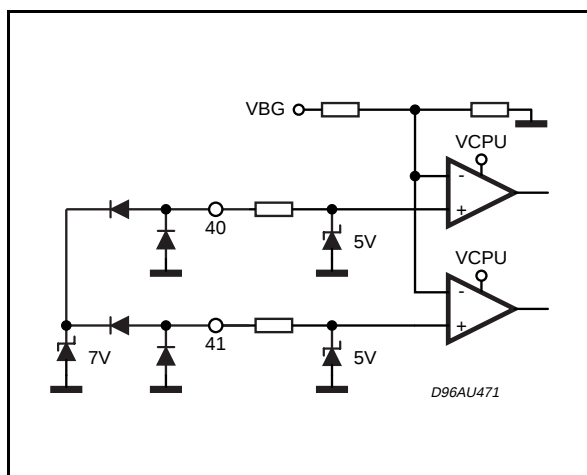
PINS: 37, 38



PIN: 39

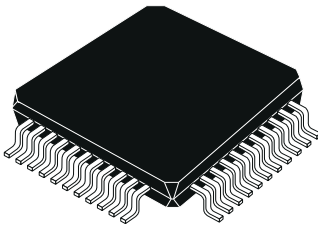


PINS: 40, 41

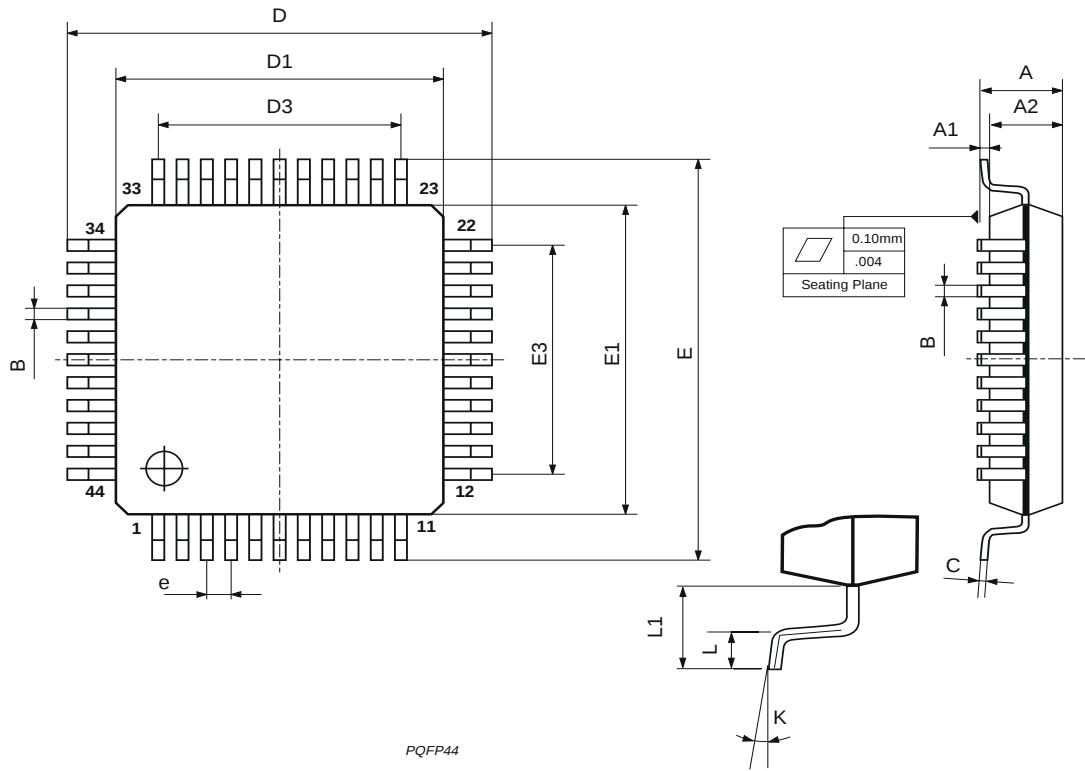


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.45			0.096
A1	0.25			0.010		
A2	1.95	2.00	2.10	0.077	0.079	0.083
B	0.30		0.45	0.012		0.018
c	0.13		0.23	0.005		0.009
D	12.95	13.20	13.45	0.51	0.52	0.53
D1	9.90	10.00	10.10	0.390	0.394	0.398
D3		8.00			0.315	
e		0.80			0.031	
E	12.95	13.20	13.45	0.510	0.520	0.530
E1	9.90	10.00	10.10	0.390	0.394	0.398
E3		8.00			0.315	
L	0.65	0.80	0.95	0.026	0.031	0.037
L1		1.60			0.063	
K	0°(min.), 7°(max.)					

OUTLINE AND
MECHANICAL DATA



PQFP44 (10 x 10)



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