DATA SHEET

TDA1519C
22 W BTL or 2 × 11 W stereo power amplifier

Product specification
File under Integrated Circuits, IC01

1998 Oct 16

Philips Semiconductors

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22 W BTL or 2 × 11 W stereo power amplifier

TDA1519C

FEATURES

- Requires very few external components for Bridge-Tied Load (BTL)
- Stereo or BTL application
- High output power
- Low offset voltage at output (important for BTL)
- Fixed gain
- Good ripple rejection
- Mute/standby switch
- Load dump protection
- AC and DC short-circuit-safe to ground and V_P
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs (V_P = 0 V)
- No switch-on/switch-off plop
- Protected against electrostatic discharge
- Low thermal resistance
- Identical inputs (inverting and non-inverting)
- Pin compatible with TDA1519B (TDA1519C and TDA1519CSP).

GENERAL DESCRIPTION

The TDA1519C is an integrated class-B dual output amplifier in a 9-lead plastic single in-line (SIL) power or 20-lead heatsink small outline package.

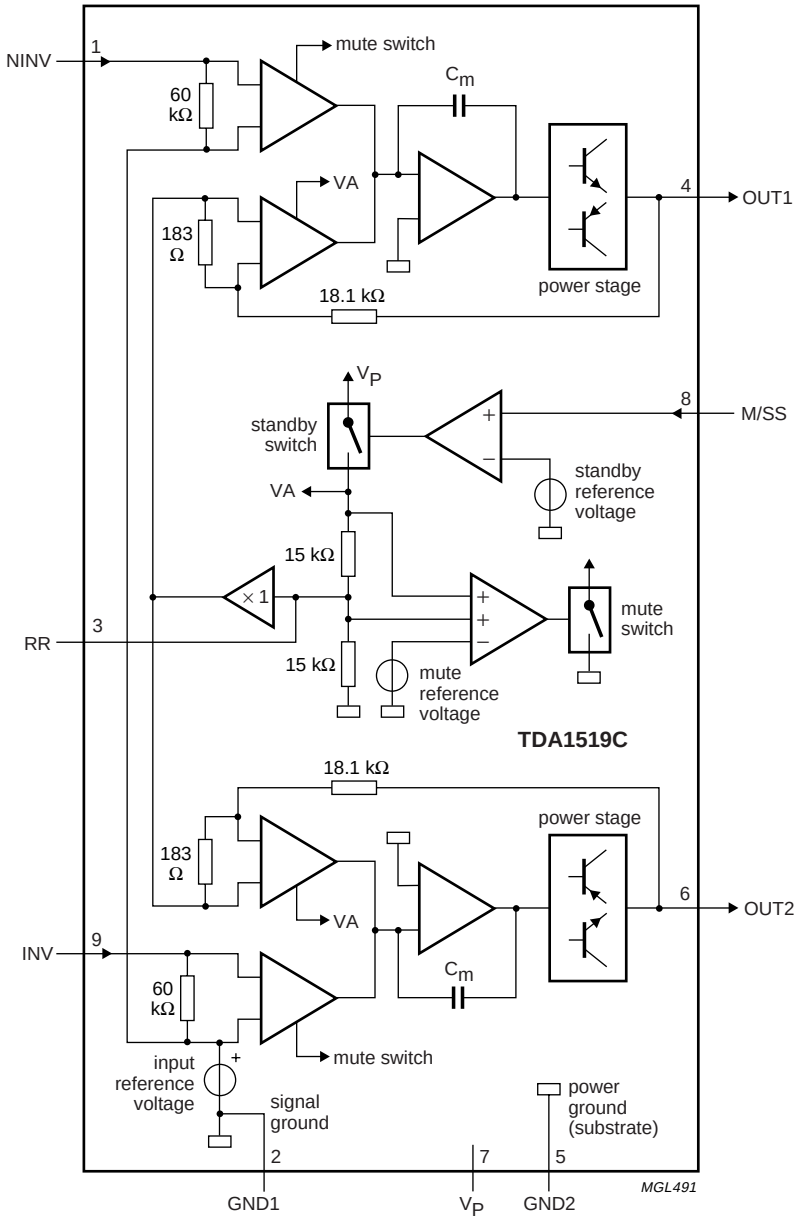
ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1519C	SIL9P	plastic single in-line power package; 9 leads	SOT131-2
TDA1519CSP	SMS9P	plastic surface mounted single in-line power package; 9 leads	SOT354-1
TDA1519CTH	HSOP20	heatsink small outline package; 20 leads; low stand-off	SOT418-2

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_P	supply voltage	operating	6.0	14.4	17.5	V
		non-operating	–	–	30	V
		load dump protected	–	–	45	V
I_{ORM}	repetitive peak output current		–	–	4	A
$I_{q(tot)}$	total quiescent current		–	40	80	mA
I_{stb}	standby current		–	0.1	100	μA
$I_{sw(on)}$	switch-on current		–	–	40	μA
Inputs						
$\lvert Z_i \rvert$	input impedance	BTL	25	–	–	kΩ
		stereo	50	–	–	kΩ
Stereo application						
P_o	output power	THD = 10%				
		R_L = 4 Ω	–	6	–	W
		R_L = 2 Ω	–	11	–	W
α_{cs}	channel separation		40	–	–	dB
$V_{n(o)(rms)}$	noise output voltage (RMS value)		–	150	–	μV
BTL application						
P_o	output power	THD = 10%; R_L = 4 Ω	–	22	–	W
SVRR	supply voltage ripple rejection	R_S = 0 Ω				
		f = 100 Hz	34	–	–	dB
		f = 1 to 10 kHz	48	–	–	dB
$\lvert \Delta V_{OO} \rvert$	DC output offset voltage		–	–	250	mV
T_j	junction temperature		–	–	150	°C

BLOCK DIAGRAM



The pin numbers refer to the TDA1519C and TDA1519CSP.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN		DESCRIPTION
	TDA1519C; TDA1519CSP	TDA1519CTH	
NINV	1	19	non-inverting input
GND1	2	20	ground 1 (signal)
RR	3	1	supply voltage ripple rejection
OUT1	4	3	output 1
GND2	5	5	ground 2 (substrate)
OUT2	6	8	output 2
V_P	7	10	positive supply voltage
M/SS	8	11	mute/standby switch input
INV	9	12	inverting input
n.c.	–	2, 4, 6, 7, 9 and 13 to 18	not connected

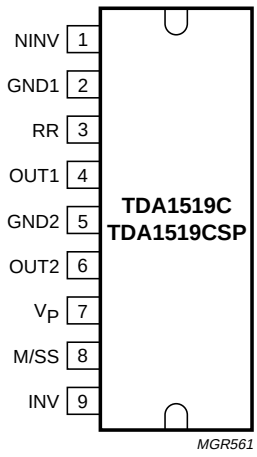


Fig.2 Pin configuration (SOT131-2 and SOT354-1).

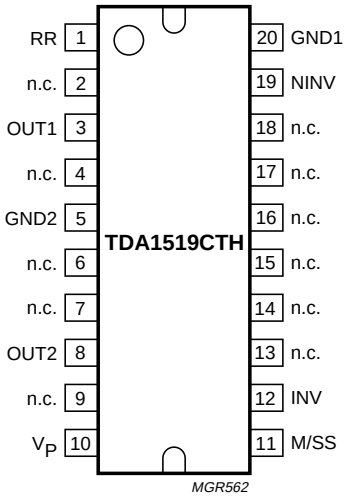


Fig.3 Pin configuration (SOT418-2).

FUNCTIONAL DESCRIPTION

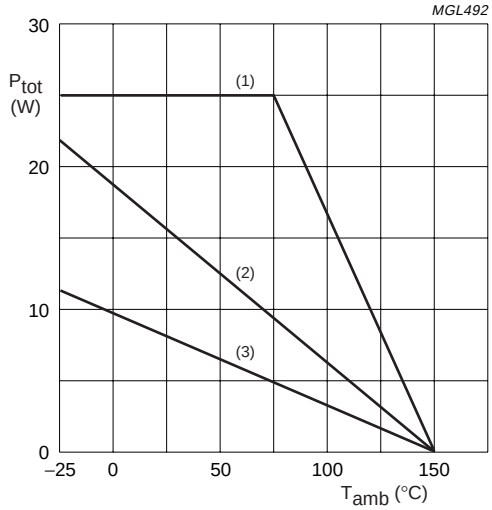
The TDA1519C contains two identical amplifiers with differential input stages. The gain of each amplifier is fixed at 40 dB. A special feature of this device is the mute/standby switch which has the following features:

- Low standby current (<100 μA)
- Low mute/standby switching current (low cost supply switch)
- Mute condition.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage	operating	–	17.5	V
		non-operating	–	30	V
		load dump protected; during 50 ms; $t_r \geq 2.5$ ms	–	45	V
V_{sc}	AC and DC short-circuit-safe voltage		–	17.5	V
V_{rp}	reverse polarity voltage		–	6	V
	energy handling capability at outputs	V_P = 0 V	–	200	mJ
I_{OSM}	non-repetitive peak output current		–	6	A
I_{ORM}	repetitive peak output current		–	4	A
P_{tot}	total power dissipation	see Fig.4	–	25	W
T_j	junction temperature		–	150	°C
T_{stg}	storage temperature		–55	+150	°C



(1) Infinite heatsink.
(2) $R_{th(c-a)}$ = 5 K/W.
(3) $R_{th(c-a)}$ = 13 K/W.

Fig.4 Power derating curve for SIL9P.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		
	TDA1519C		40	K/W
	TDA1519CTH		40	K/W
$R_{th(j-c)}$	thermal resistance from junction to case			
	TDA1519C		3	K/W
	TDA1519CTH		3	K/W

DC CHARACTERISTICS

V_P = 14.4 V; T_{amb} = 25 °C; measurements taken using Fig.5; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_P	supply voltage	note 1	6.0	14.4	17.5	V
$I_{q(tot)}$	total quiescent current		–	40	80	mA
V_O	DC output voltage	note 2	–	6.95	–	V
$\lvert\Delta V_{OO}\rvert$	DC output offset voltage		–	–	250	mV
Mute/standby switch						
$V_{sw(on)}$	Switch-on voltage level		8.5	–	–	V
Mute condition						
V_{mute}	mute voltage		3.3	–	6.4	V
V_O	output signal in mute position	V_I = 1 V (max.); f = 20 Hz to 15 kHz	–	–	20	mV
$\lvert\Delta V_{OO}\rvert$	DC output offset voltage		–	–	250	mV
Standby condition						
V_{stb}	standby voltage	standby mode	0	–	2	V
I_{stb}	standby current	standby mode	–	–	100	µA
$I_{sw(on)}$	switch-on current		–	12	40	µA

Notes

1. The circuit is DC adjusted at V_P = 6 to 17.5 V and AC operating at V_P = 8.5 to 17.5 V.
2. At V_P = 17.5 to 30 V, the DC output voltage $\leq 0.5V_P$.

AC CHARACTERISTICS

V_P = 14.4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Stereo application (see Fig.5)						
P_o	output power	note 1				
		THD = 0.5%	4	5	–	W
		THD = 10%	5.5	6.0	–	W
		R_L = 2 Ω; note 1				
		THD = 0.5%	7.5	8.5	–	W
		THD = 10%	10	11	–	W
THD	total harmonic distortion	P_o = 1 W	–	0.1	–	%
$f_{ro(l)}$	low frequency roll-off	–3 dB; note 2	–	45	–	Hz
$f_{ro(h)}$	high frequency roll-off	–1 dB	20	–	–	kHz
$G_{v(cl)}$	closed-loop voltage gain		39	40	41	dB
SVRR	supply voltage ripple rejection	on; notes 3 and 4	40	–	–	dB
		on; notes 3 and 5	45	–	–	dB
		mute; notes 3 and 6	45	–	–	dB
		standby; notes 3 and 6	80	–	–	dB
$\lvert Z_i \rvert$	input impedance		50	60	75	kΩ
$V_{n(o)(rms)}$	noise output voltage (RMS value)	note 7				
		on; R_S = 0 Ω	–	150	–	μV
		on; R_S = 10 kΩ	–	250	500	μV
		mute; note 8	–	120	–	μV
α_{cs}	channel separation	R_S = 10 kΩ	40	–	–	dB
$\lvert \Delta G_{v(ub)} \rvert$	channel unbalance		–	0.1	1	dB
BTL application (see Fig.6)						
P_o	output power	note 1				
		THD = 0.5%	15	17	–	W
		THD = 10%	20	22	–	W
	output power at V_P = 13.2 V	note 1				
		THD = 0.5%	–	13	–	W
		THD = 10%	–	17.5	-	W
THD	total harmonic distortion	P_o = 1 W	–	0.1	–	%
B_p	power bandwidth	THD = 0.5%; P_o = –1 dB; with respect to 15 W	–	35 to 15000	–	Hz
$f_{ro(l)}$	low frequency roll-off	–1 dB; note 2	–	45	–	Hz
$f_{ro(h)}$	high frequency roll-off	–1 dB	20	–	–	kHz
$G_{v(cl)}$	closed-loop voltage gain		45	46	47	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SVRR	supply voltage ripple rejection	on; notes 3 and 4	34	–	–	dB
		on; notes 3 and 5	48	–	–	dB
		mute; notes 3 and 6	48	–	–	dB
		standby; notes 3 and 6	80	–	–	dB
$\lvert Z_i \rvert$	input impedance		25	30	38	kΩ
$V_{n(o)(rms)}$	noise output voltage (RMS value)	note 7				
		on; R_S = 0 Ω	–	200	–	μV
		on; R_S = 10 kΩ	–	350	700	μV
		mute; note 8	–	180	–	μV

Notes

1. Output power is measured directly at the output pins of the IC.
2. Frequency response externally fixed.
3. Ripple rejection measured at the output with a source impedance of 0 Ω (maximum ripple amplitude of 2 V).
4. Frequency f = 100 Hz.
5. Frequency between 1 and 10 kHz.
6. Frequency between 100 Hz and 10 kHz.
7. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
8. Noise output voltage independent of R_S (V_i = 0 V).

APPLICATION INFORMATION

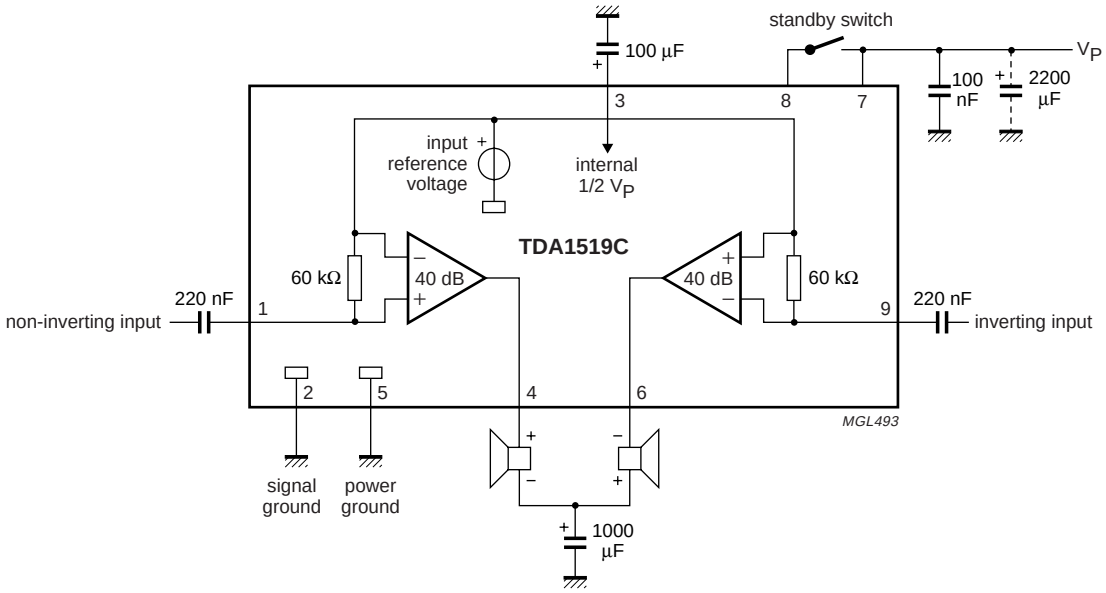


Fig.5 Stereo application diagram (SOT131-2 and SOT354-1).

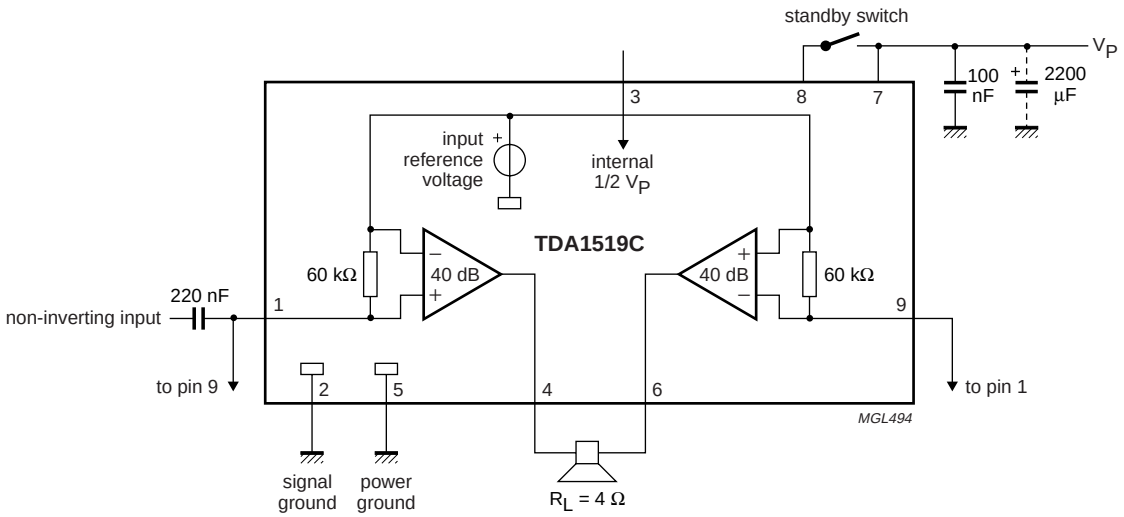


Fig.6 BTL application diagram (SOT131-2 and SOT354-1).

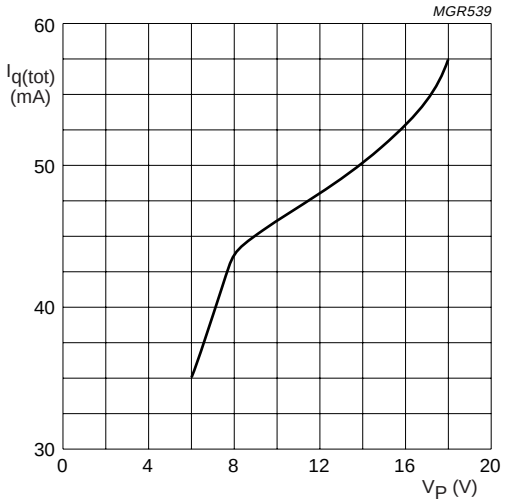


Fig.7 Total quiescent current ($I_{q(tot)}$) as a function of supply voltage (V_P).

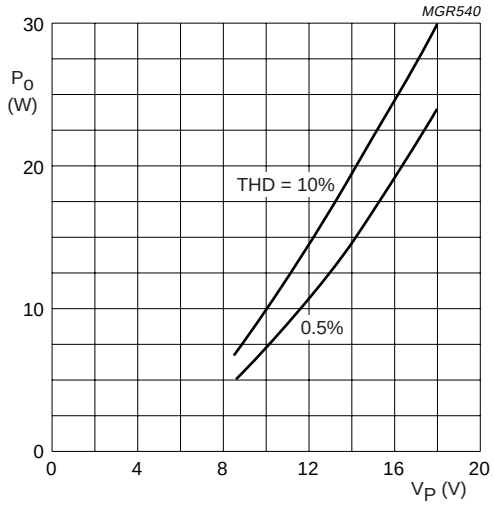


Fig.8 Output power (P_o) as a function of supply voltage (V_P) for BTL application at $R_L = 4\ \Omega$; f = 1 kHz.

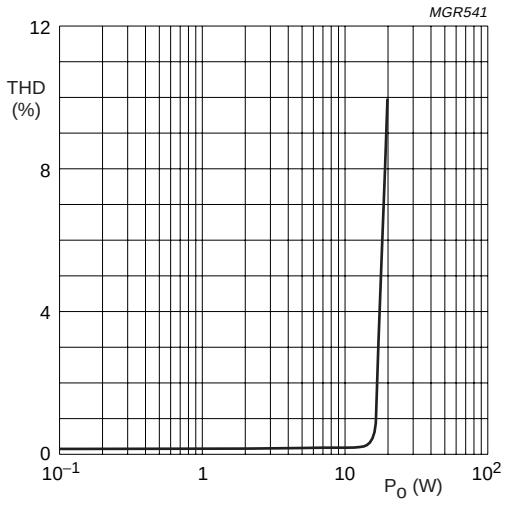


Fig.9 Total harmonic distortion (THD) as a function of output power (P_o) for BTL application at R_L = 4 Ω; f = 1 kHz.

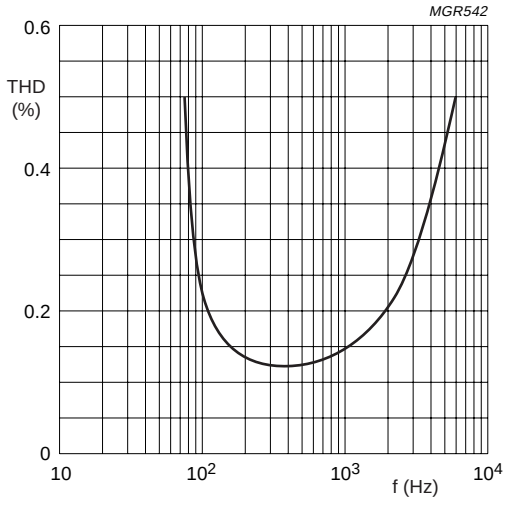
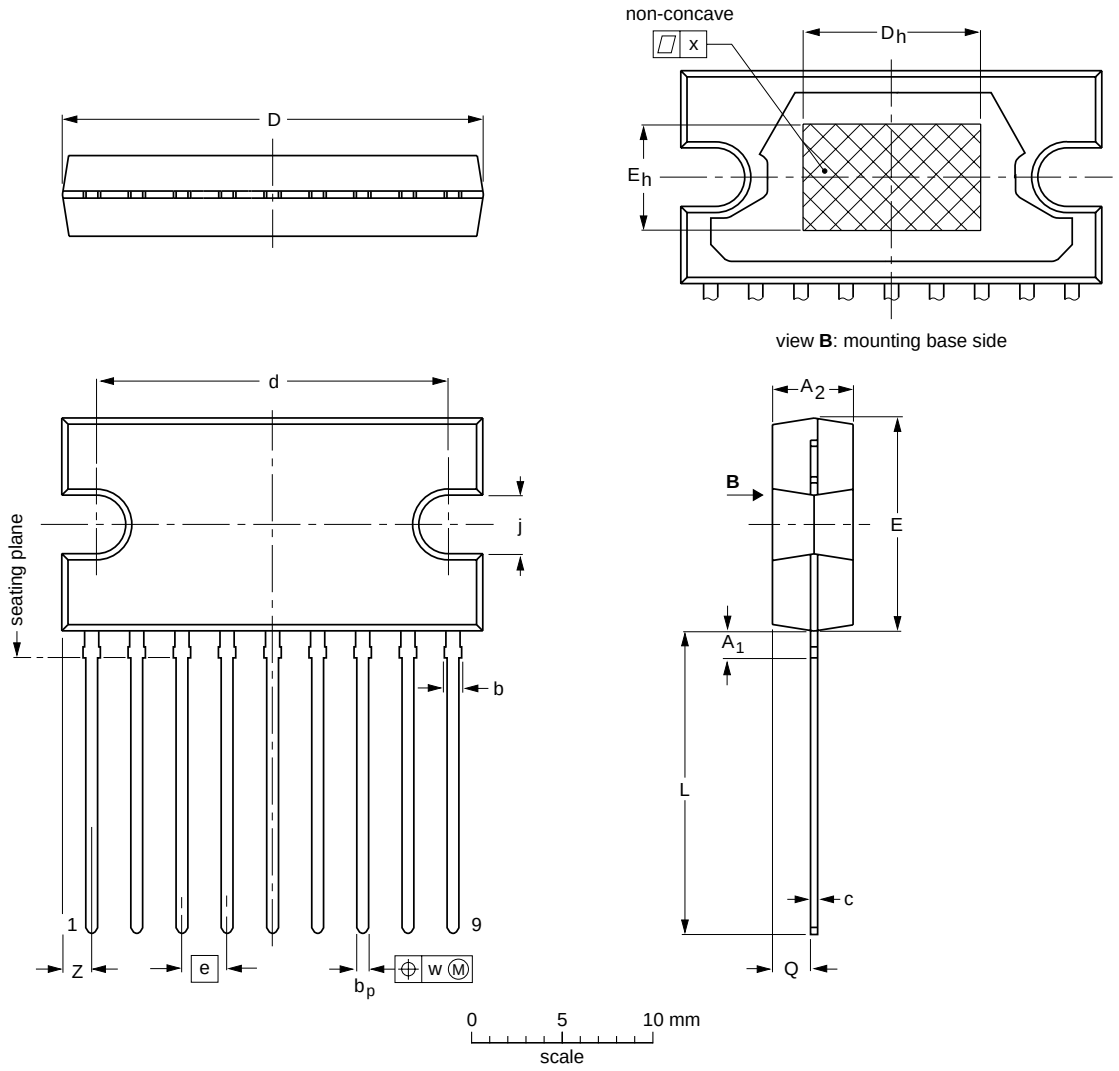


Fig.10 Total harmonic distortion (THD) as a function of operating frequency (f) for BTL application at R_L = 4 Ω; P_o = 1 W.

PACKAGE OUTLINES

SIL9P: plastic single in-line power package; 9 leads **SOT131-2**



DIMENSIONS (mm are the original dimensions)

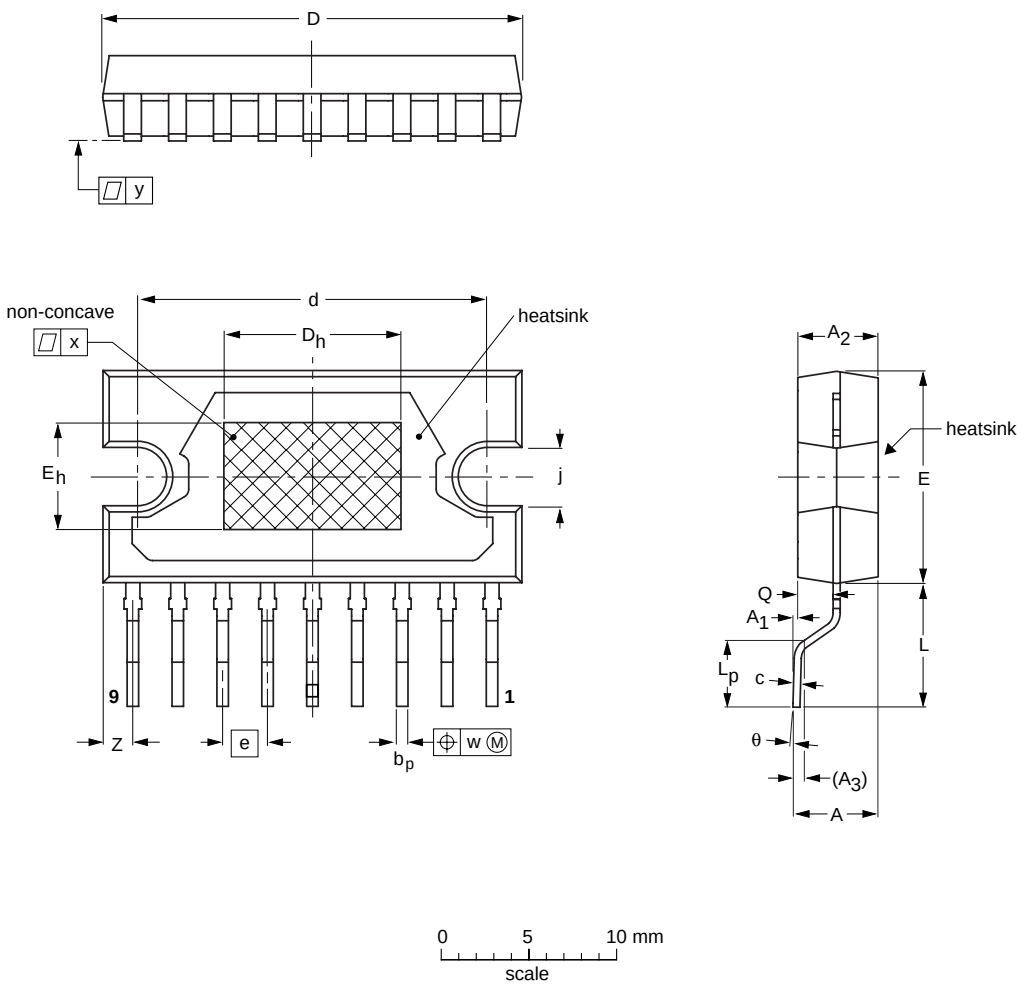
UNIT	A_1 max.	A_2	b max.	b_p	c	$D^{(1)}$	d	D_h	$E^{(1)}$	e	E_h	j	L	Q	w	x	$Z^{(1)}$
mm	2.0	4.6 4.2	1.1	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	2.54	6	3.4 3.1	17.2 16.5	2.1 1.8	0.25	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT131-2						~~92-11-17~~ 95-03-11

SMS9P: plastic surface mounted single in-line power package; 9 leads **SOT354-1**



DIMENSIONS (mm are the original dimensions)

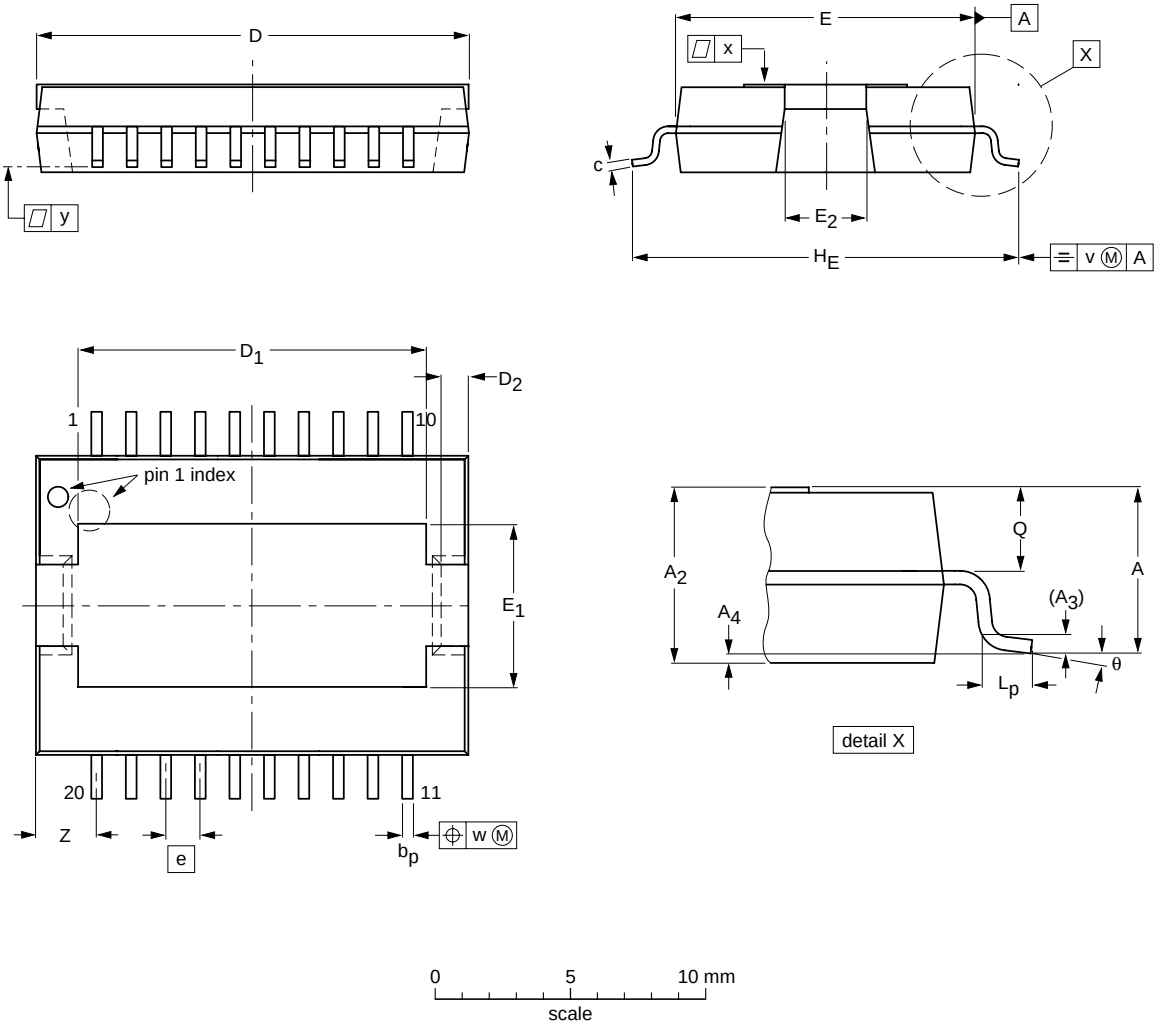
UNIT	A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	d	D_h	$E^{(1)}$	e	E_h	j	L	L_p	Q	w	x	y	$Z^{(1)}$	θ
mm	4.9 4.2	0.35 0.05	4.6 4.2	0.25	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	2.54	6	3.4 3.1	7.4 6.6	3.4 2.8	2.1 1.9	0.25	0.03	0.15	2.00 1.45	3° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT354-1						98-10-08

HSOP20: heatsink small outline package; 20 leads; low stand-off **SOT418-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_2	A_3	A_4(1)	b_p	c	D(2)	D_1	D_2	E(2)	E_1	E_2	e	H_E	L_p	Q	v	w	x	y	Z	θ
mm	3.5	3.5 3.2	0.35	+0.12 −0.02	0.53 0.40	0.32 0.23	16.0 15.8	13.0 12.6	1.1 0.9	11.1 10.9	6.2 5.8	2.9 2.5	1.27	14.5 13.9	1.1 0.8	1.7 1.5	0.25	0.25	0.03	0.07	2.5 2.0	8° 0°

Note

1. Limits per individual lead.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT418-2						~~97-10-29~~ 98-02-25

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (order code 9398 652 90011).

SIL

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

HSOP and SMS

Reflow soldering

Reflow soldering methods are suitable for HSOP and SMS packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 50 and 300 seconds depending on heating method. Typical reflow peak temperatures range from 215 to 250 °C.

Wave soldering

Wave soldering should **not** be applied to HSOP and SMS packages because no solder joint between printed-circuit board and heatsink (heatsink at bottom version) can be achieved, or to avoid solder sticking to the heatsink (heatsink on top version).

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

NOTES

NOTES

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213, Tel. +43 160 1010,
Fax. +43 160 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,
Tel. +45 32 88 2636, Fax. +45 31 57 0044

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615800, Fax. +358 9 61580920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex,
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: PT Philips Development Corporation, Semiconductors Division,
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,
TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Pakistan: see Singapore

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 319762,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,
Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Al. Vicente Pinzon, 173, 6th floor,
04547-130 SÃO PAULO, SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 93 301 6312, Fax. +34 93 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2741 Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2865, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 625 344, Fax.+381 11 635 777

For all other countries apply to: Philips Semiconductors,
International Marketing & Sales Communications, Building BE-p, P.O. Box 218,
5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

Internet: http://www.semiconductors.philips.com

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