IC INFORMATION

Function	Servo Control/DSP/DAC/LPF	TC9495F2	1/2	E
Type	CMOS	Model	DEH-P630/X1N/UC	

● **Pin Functions(TC9495F2)**

Pin No.	Pin Name	I/O	Function and Operation
1	TESTO	-	Test mode terminal
2	$\overline{\text{HSO}}$	O	Replay speed flag output terminal
3	$\overline{\text{UHSO}}$	O	Replay speed flag output terminal
4	EMPH	O	Emphasis flag output terminal for sub code Q data
5	LRCK	O	Channel clock (44.1 kHz) output terminal
6	VSS	-	Digital ground terminal
7	BCK	O	Bit clock output terminal
8	AOUT	O	Digital audio data output terminal
9	DOUT	O	Digital out output terminal
10	MBOV	O	Buffer memory over signal output terminal
11	IPF	O	Correction flag output terminal
12	SBOK	O	CRCC decision result output for sub code Q data
13	CLCK	I/O	Clock input/output terminal for sub code P-W data read
14	VDD	-	Digital + power supply terminal (5 V)
15	VSS	-	Digital ground terminal
16	DATA	O	Sub code P-W data output terminal
17	SFSY	O	Replay-system frame sync signal output terminal
18	SBSY	O	Sub code block sync output terminal
19	SPCK	O	Clock for processor status signal read
20	SPDA	O	Processor status signal output terminal
21	COFS	O	Correction-system frame clock (7.35 kHz) output terminal
22	MONIT	O	LSI internal signal output terminal
23	VDD	-	Digital + power supply terminal (5 V)
24	TESIO0	I	Test input/output terminal
25	P2VREF	-	PLL-system only 2VREF terminal
26	HSSW	O	The VREF voltage is reached for double or quad speed.
27	ZDET	O	One-bit DAC zero detection flag output terminal
28	PDO	O	Phase error signal issue between the EFM and PLCK signals
29	TMAXS	O	TMAX detection result output terminal
30	TAMX	O	TMAX detection result output terminal
31	LPFN	I	Reverse input terminal of amplifier for lowpass filter
32	LPFO	O	Output terminal of amplifier for lowpass filter
33	PVREF	-	PLL-system only VREF terminal
34	VCOREF	I	VCO center frequency reference level terminal
35	VCOF	O	Filter terminal for VCO
36	AVSS	-	Analog-system ground terminal
37	SLCO	O	Output terminal of DAC for data slice level generation
38	RFI	I	RF signal input terminal
39	AVDD	-	Analog-system power supply terminal (5 V)
40	RFCT	I	RFRP signal center level input terminal
41	RFZI	I	Input terminal for RFRP signal zero cross
42	RFRP	I	RF ripple signal input terminal
43	FEI	I	Focus error signal input terminal
44	SBAD	I	Sub beam addition signal input terminal
45	TSIN	I	Test input terminal
46	TEI	I	Tracking error input terminal
47	TEZI	I	Input terminal for tracking error or zero cross
48	FOO	O	Focus equalizer output terminal
49	TRO	O	Tracking equalizer output terminal
50	VREF	-	Analog reference power supply terminal
51	RFGC	O	RF amplitude adjustment control signal output terminal
52	TEBC	O	Tracking balance control signal output terminal
53	FMO	O	Feed equalizer output terminal
54	FVO	O	Speed error signal or feed search EQ output
55	DMO	O	Disc equalizer output terminal
56	2VREF	-	Analog reference power supply terminal
57	SEL	O	APC circuit ON/OFF signal output terminal

IC INFORMATION

Function	Servo Control/DSP/DAC/LPF	TC9495F2	2/2	E
Type	CMOS	Model	DEH-P630/X1N/UC	

Pin No.	Pin Name	I/O	Function and Operation
58-61	FLGA-D	O	External flag output terminal for internal signal monitor
62	VDD	-	Digital + power supply terminal (5 V)
63	VSS	-	Digital ground terminal
64	IO0	O	RF amplifier gain switching terminal
65	IO1	O	Not used
66	IO2	I	HOME detection switch input terminal
67	IO3	O	FocusDrv and signal output terminal
68	$\overline{\text{DMOUT}}$	I	Field equalizer PWM output terminal for IO0 and IO1 Disc equalizer PWM output terminal for IO2 and IO3
69	$\overline{\text{CKSE}}$	I	Usually open
70	$\overline{\text{DACT}}$	I	DAC test mode terminal
71	TESIN	I	Test input terminal
72	TESIO1	I	Test input/output terminal
73	VSS	-	Digital ground terminal
74	PXI	I	DPS-system clock oscillator circuit input terminal
75	PXO	O	DPS-system clock oscillator circuit output terminal
76	VDD	-	Digital + power supply terminal (5 V)
77	XVSS	-	Ground terminal for system clock oscillator circuit
78	XI	I	System clock oscillator circuit input terminal
79	XO	O	System clock oscillator circuit output terminal
80	XVDD	-	For system clock oscillator circuit + power supply terminal
81	DVSR	-	R channel D/A converting unit power supply terminal
82	RO	O	R channel data forward rotation output terminal
83	DVDD	-	D/A converting unit power supply terminal (5 V)
84	DVR	-	Reference voltage terminal
85	LO	O	L channel forward rotation output terminal
86	DVSL	-	L channel D/A converting unit power supply terminal
87-89	TEST1-3	I	Test mode terminal
90-93	BUS0-3	I/O	Data input/output terminal for microcomputer interface
94	VDD	-	Digital + power supply terminal (5 V)
95	VSS	-	Digital ground terminal
96	BUCK	I	Clock terminal for microcomputer interface
97	$\overline{\text{CEE}}$	I	Chip enable signal for microcomputer interface
98	TEST4	I	Test mode terminal
99	$\overline{\text{TSMOD}}$	I	Test mode terminal
100	$\overline{\text{RST}}$	I	Reset signal input terminal