TC7652

Low Noise, Chopper Stabilized Operational Amplifier

Features

- Low Offset Over Temperature Range: 10µV
- Ultra Low Long Term Drift: 150nV/Month
- Low Temperature Drift: 100nV/°C
- Low DC Input Bias Current: 15pA
- High Gain, CMRR and PSRR: 110dB Min
- Low Input Noise Voltage: $0.2\mu V_{p-p}$ (DC to 1Hz)
- Internally Compensated for Unity Gain Operation
- Clamp Circuit for Fast Overload Recovery

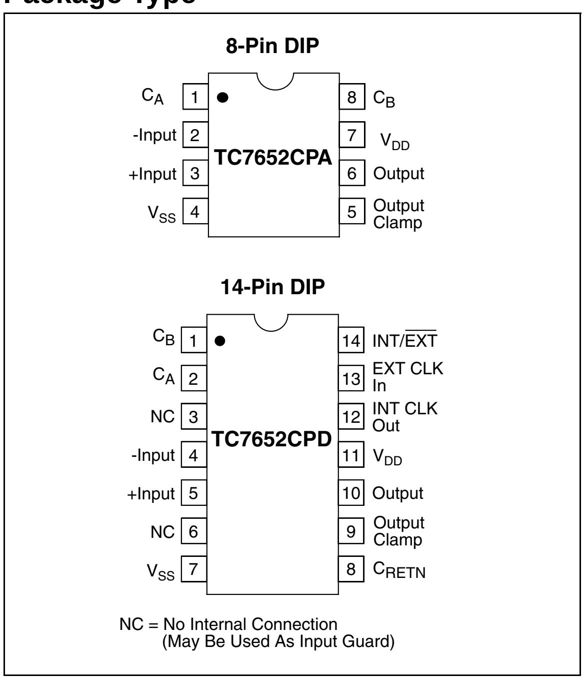
Applications

- Instrumentation
- Medical Instrumentation
- Embedded Control
- Temperature Sensor Amplifier
- Strain Gage Amplifier

Device Selection Table

Part Number	Package	Temperature Range
TC7652CPA	8-Pin Plastic DIP	0°C to +70°C
TC7652CPD	14-Pin Plastic DIP	0°C to +70°C

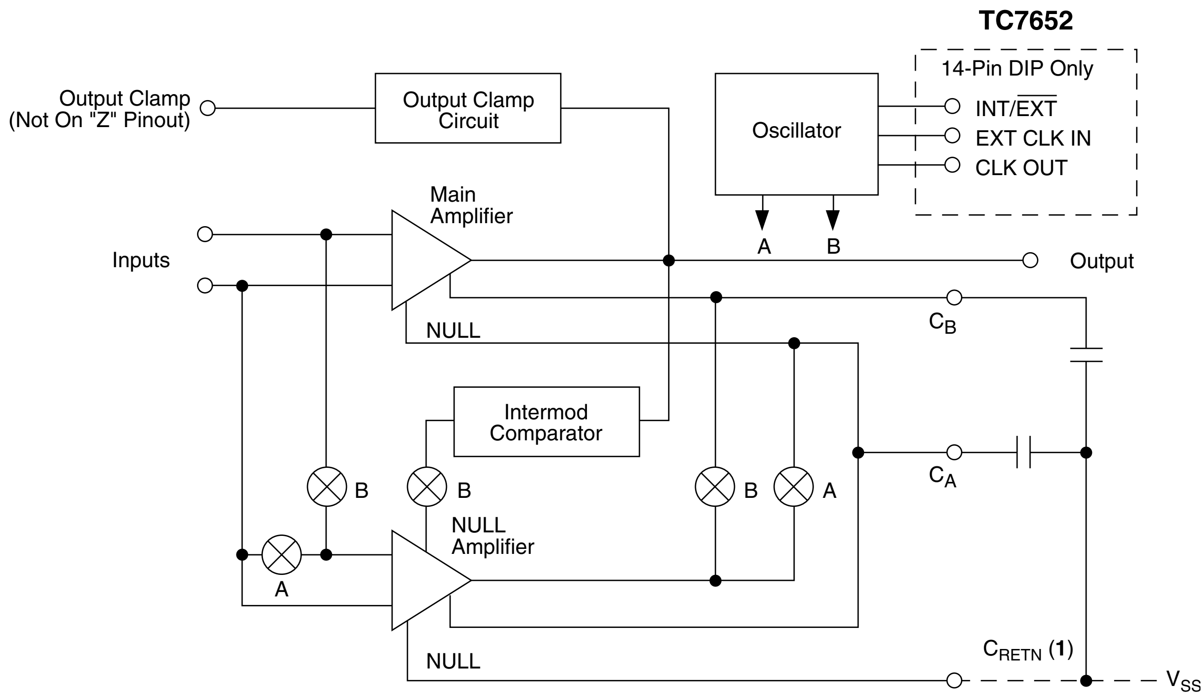
Package Type



General Description

The TC7652 is a lower noise version of the TC7650, sacrificing some input specifications (bias current and bandwidth) to achieve a 10x reduction in noise. All the other benefits of the chopper technique are present, (i.e, freedom from offset adjust, drift and reliability problems from external trim components). Like the TC7650, the TC7652 requires only two noncritical external caps for storing the chopped null potentials. There are no significant chopping spikes, internal effects or overrange lockup problems.

Functional Block Diagram



NOTE 1: For 8-pin DIP connect to V_{SS}, or to C_{RET} on "Z" pinout.

1.0 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Total Supply Voltage (V_{DD} to V_{SS}) .... +18V

Input Voltage .... (V_{DD} +0.3V) to (V_{SS} – 0.3V)

Voltage on Oscillator Control Pins.............. V_{DD} to V_{SS}

Duration of Output Short Circuit .... Indefinite

Current Into Any Pin 10mA

While Operating (**Note 1**) 100µA

Package Power Dissipation ($T_A \leq 70°C$)

8-Pin Plastic DIP 730mW

14-Pin Plastic DIP 800mW

Storage Temperature Range .... -65°C to +150°C

Operating Temperature Range

C Device .... 0°C to +70°C

I Device .... -25°C to +85°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods my affect device reliability.

TC7652 ELECTRICAL SPECIFICATIONS

Electrical Characteristics: V_{DD} = +5V, V_{SS} = -5V, T_A = +25°C, unless otherwise indicated.

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{OS}	Input Offset Voltage	—	±2	±5	µV	T_A = +25°C
TCV_{OS}	Average Temperature Co-efficient of Input Offset Voltage	—	0.01	0.05	µV/°C	0°C < T_A < +70°C
V_{OS}/DT	Offset Voltage vs Time	—	150	—	nV/mo	
I_{BIAS}	Input Bias Current (CLK On)	— — —	30 100 250	100 — 1000	pA	T_A = +25°C 0°C < T_A < +70°C -25°C < T_A < +85°C
I_{BIAS}	Input Bias Current (CLK Off)	— — —	15 35 100	30 — 1000	pA	T_A = +25°C 0°C < T_A < +70°C -25°C < T_A < +85°C
I_{OS}	Input Offset Current	—	25	150	pA	
R_{IN}	Input Resistance	—	10^{12}	—	Ω	
OL	Large Signal Voltage Gain	120	150	—	dB	R_L = 10kΩ, V_{OUT} = ±4V
V_{OUT}	Output Voltage Swing (**Note 2**)	±4.7 —	±4.85 ±4.95	— —	V	R_L = 10kΩ R_L = 100kΩ
CMVR	Common Mode Voltage Range	-4.3	—	+3.5	V	
MRR	Common Mode Rejection Ratio	120	140	—	dB	CMVR = -4.3V to +3.5V
PSRR	Power Supply	120	140	—	dB	±3V to ±8V
e_N	Input Noise Voltage	— —	0.2 0.7	1.5 5	$µV_{P-P}$ $µV_{P-P}$	R_S = 100Ω, DC to 1Hz DC to 10Hz
I_N	Input Noise Current	—	0.01	—	pA/ $\sqrt{Hz}$	f = 10Hz
GBW	Unity Gain Bandwidth	—	0.4	—	MHz	
SR	Slew Rate	—	1	—	V/µsec	C_L = 50pF, R_L = 10kΩ
	Overshoot	—	15	—	%	
V_{DD}, V_{SS}	Operating Supply Range	5	—	16	V	

Note 1: Limiting input current to 100µA is recommended to avoid latch-up problems. Typically 1mA is safe however, this is not guaranteed.

2: Output clamp not connected. See typical characteristics curves for output swing versus clamp current characteristics.

3: See "Output Clamp" under detailed description.

TC7652 ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: V_{DD} = +5V, V_{SS} = -5V, T_A = +25°C, unless otherwise indicated.						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Units**	**Test Conditions**
I_S	Supply Current	—	1	3	mA	No Load
f_{CH}	Internal Chopping Frequency	100	275	—	Hz	Pins 12 – 14 Open (DIP)
	Clamp ON Current (**Note 3**)	25	100	—	µA	R_L = 100kΩ
	Clamp OFF Current (**Note 3**)	—	1	—	pA	-4V ≤ V_{OUT} < +10V

Note 1: Limiting input current to 100µA is recommended to avoid latch-up problems. Typically 1mA is safe however, this is not guaranteed.

2: Output clamp not connected. See typical characteristics curves for output swing versus clamp current characteristics.

3: See “Output Clamp” under detailed description.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number		Symbol	Description
8-pin DIP	14-pin DIP		
1,8	2,1	C_A, C_B	Nulling capacitor pins
2	4	-INPUT	Inverting Input
3	5	+INPUT	Non-inverting Input
4	7	V_{SS}	Negative Power Supply
5	9	OUTPUT CLAMP	Output Voltage Clamp
6	10	OUTPUT	Output
7	11	V_{DD}	Positive Power Supply
—	3,6	NC	No internal connection
—	8	C_{RETN}	Capacitor current return pin
—	12	INT CLK OUT	Internal Clock Output
—	13	EXT CLK IN	External Clock Input
—	14	INT/$\overline{\text{EXT}}$	Select Internal or External Clock

3.0 DETAILED DESCRIPTION

3.1 Capacitor Connection

Connect the null storage capacitors to the C_A and C_B pins with a common connection to the C_{RET} pin (14-pin TC7652) or to V_{SS} (8-pin TC7652). When connecting to V_{SS}, avoid injecting load current IR drops into the capacitive circuitry by making this connection directly via a separate wire or PC trace.

3.2 Output Clamp

In chopper stabilized amplifiers, the output clamp pin reduces overload recovery time. When a connection is made to the inverting input pin (summing junction), a current path is created between that point and the output pin, just before the device output saturates. This prevents uncontrolled differential input voltages and charge build-up on correction storage capacitors. Output swing is reduced.

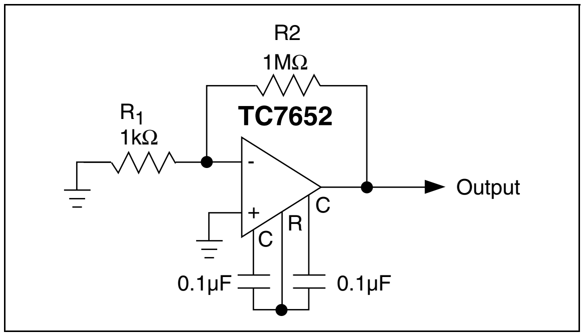
3.3 Clock

The TC7652 has a 550Hz internal oscillator, which is divided by two before clocking the input chopper switches. The 275Hz chopping frequency is available at INT CLK OUT (Pin 12) on 14-pin devices. In normal operation, INT/EXT (Pin 14), which has an internal pull-up, can be left open.

An external clock can also be used. To disable the internal clock and use an external one, the INT/EXT pin must be tied to V_{SS}. The external clock signal is then applied to the EXT CLK IN input (Pin 13). An internal divide-by-two provides a 50% switching duty cycle. The capacitors are only charged when EXT CLK IN is high, so a 50% to 80% positive duty cycle is recommended for higher clock frequencies. The external clock can swing between V_{DD} and V_{SS}, with the logic threshold about 2.5V below V_{DD}.

The output of the internal oscillator, before the divide-by-two circuit, is available at EXT CLK IN when INT/EXT is high or unconnected. This output can serve as the clock input for a second TC7652 (operating in a master/slave mode), so that both op amps will clock at the same frequency. This prevents clock intermodulation effects when two TC7652's are used in a differential amplifier configuration.

FIGURE 3-1: TEST CIRCUIT



If the TC7652's output saturates, error voltages on the external capacitors will slow overload recovery. This condition can be avoided if a strobe signal is available. The strobe signal is applied to EXT CLK IN and the overload signal is applied to the amplifier while the strobe is LOW. In this case, neither capacitor will be charged. The low leakage of the capacitor pins allow long measurements to be made within eligible errors (typical capacitor drift is 10µV/sec).

4.0 TYPICAL APPLICATIONS

4.1 Component Selection

C_A and C_B (external capacitors)should be in the 0.1µF to 1µF range. For minimum clock ripple noise, use a 1µF capacitor in broad bandwidth circuits. For limited bandwidth applications where clock ripple is filtered out, use a 0.1µF capacitor for slightly lower offset voltage. High quality, film type capacitors (polyester or polypropylene) are recommended, although a lower grade ceramic may work in some applications. For quickest settling after initial turn-on, use low dielectric absorption capacitors (e.g., polypropylene). With ceramic capacitors, settling to 1µV takes several seconds.

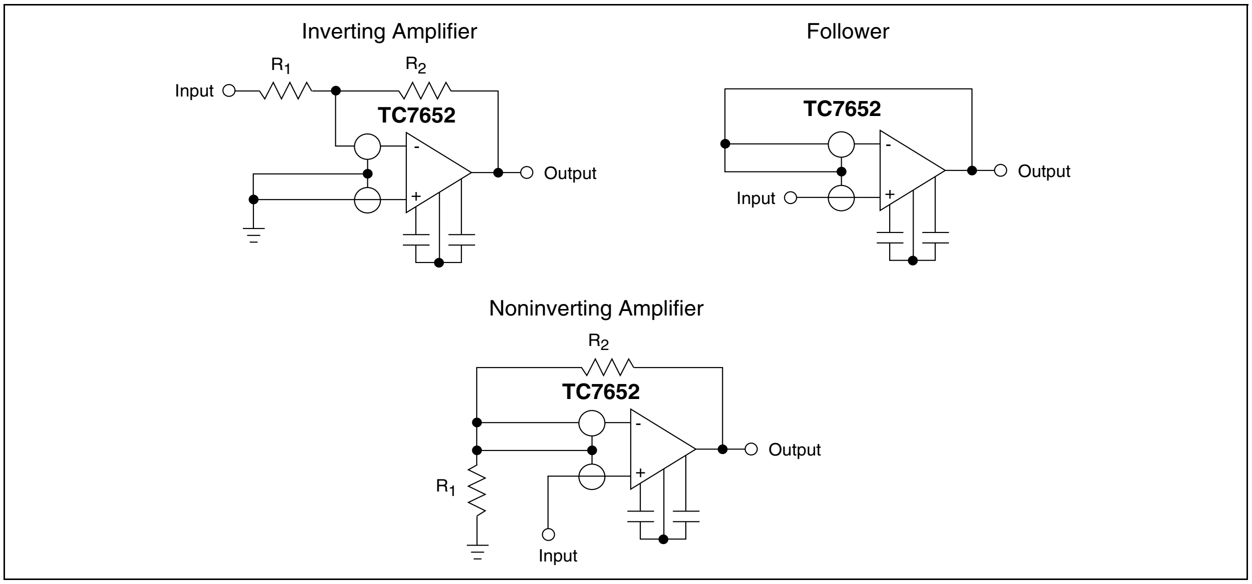
4.2 Static Protection

Although input diodes static protect all device pins, avoid strong electrostatic fields and discharges that can cause degraded diode junction characteristics and produce increased input-leakage currents.

4.3 Output Stage/Load Driving

The output circuit is high impedance (about 18kΩ). With lesser loads, the chopper amplifier behaves somewhat like a transconductance amplifier with an open-loop gain proportional to load resistance. (For example, the open-loop gain is 17dB lower with a 1kΩ. load than with a 10kΩ load.) If the amp is used only for DC, the DC gain is typically greater than 120dB (even with a 1kΩ load), and this lower gain is inconsequential. For wide band, the best frequency response occurs with a load resistor of at least 10kΩ. This produces a 6dB/octave response from 0.1Hz to 2MHz, with phase shifts of less than 2 degrees in the transition region, where the main amplifier takes over from the null amplifier.

FIGURE 4-1: CONNECTION OF INPUT GUARDS



4.4 Thermoelectric Effects

The thermoelectric (Seebeck) effects in thermocouple junctions of dissimilar metals, alloys, silicon, etc. limit ultra high precision DC amplifiers. Unless all junctions are at the same temperature, thermoelectric voltages around 0.1μV/°C (up to tens of μV/°C for some materials) are generated. To realize the low offset voltages of the chopper, avoid temperature gradients. Enclose components to eliminate air movement, especially from power dissipating elements in the system. Where possible, use low thermoelectric co-efficient connections. Keep power supply voltages and power dissipation to a minimum. Use high impedance loads and seek maximum separation from surrounding heat disipating elements.

4.5 Guarding

To benefit from TC7652 low input currents, take care assembling printed circuit boards. Clean boards with alcohol or TCE and blow dry with compressed air. To prevent contamination, coat boards with epoxy or silicone rubber.

Even if boards are cleaned and coated, leakage currents may occur because input pins are next to pins at supply potentials. To reduce this leakage, use guarding to lower the voltage difference between the inputs and adjacent metal runs. The guard (a conductive ring surrounding inputs) is connected to a low impedance point at about the same voltage as inputs. The guard absorbs leakage currents from high voltage pins.

The 14-pin dual-in-line arrangement simplifies guarding. Like the LM108 pin configuration (but unlike the 101A and 741), pins next to inputs are not used.

4.6 Pin Compatibility

Where possible, the 8-pin device pinout conforms to such industry standards as the LM101 and LM741. Null storing external capacitors connect to Pins 1 and 8, which are usually for offset null or compensation capacitors. Output clamp (Pin 5) is similarly used. For OP05 and OP07 devices, replacement of the offset null potentiometer (connected between Pins 1 and 8 and V_{DD} by two capacitors from those pins to V_{SS}) provides compatibility. Replacing the compensation capacitor between Pins 1 and 8 by two capacitors to V_{SS} is required. The same operation (with the removal of any connection to Pin 5) works for LM101, µA748 and similar parts.

Because NC pins provide guarding between input and other pins, the 14-pin device pinout conforms closely to the LM108. Because this device does not use any extra pins and does not provide offset nulling (but requires a compensation capacitor), some layout changes are necessary to convert to the TC7652.

4.7 Some Applications

Figures 4-2 and 4-3 show basic inverting and noninverting amplifier circuits using the output clamping circuit to enhance overload recovery performance. The only limitations on replacing other op amps with the TC7652 are supply voltage (±8V maximum) and output drive capability (10kΩ load for full swing). Overcome these limitations with a booster circuit (Figure 4-4) to combine output capabilities of the LM741 (or other standard device) with input capabilities of the TC7652. These two form a composite device, therefore, when adding the feedback network, the monitor loop gains stability.

FIGURE 4-2: NONINVERTING AMPLIFIER WITH OPTIONAL CLAMP

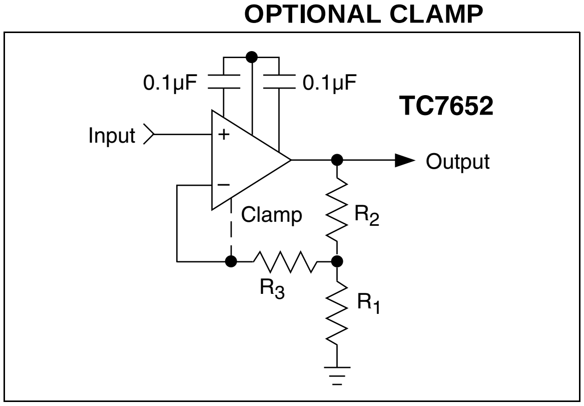


FIGURE 4-3: INVERTING AMPLIFIER WITH OPTIONAL CLAMP

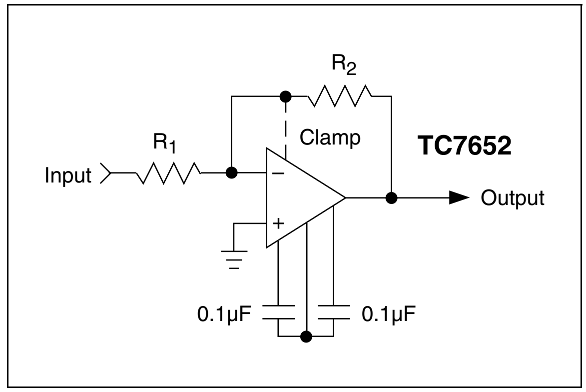


FIGURE 4-4: USING 741 TO BOOST OUTPUT DRIVE CAPABILITY

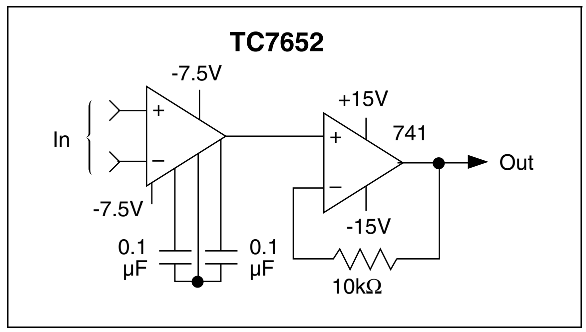


Figure 4-5 shows the clamp circuit of a zero offset comparator. Because the clamp circuit requires the inverting input to follow the input signal, problems with a chopper stabilized op amp are avoided. The threshold input must tolerate the output clamp current $\approx V_{IN}/R$ without disrupting other parts of the system.

Figure 4-6 shows how the TC7652 can offset null high slew rate and wideband amplifiers.

Mixing the TC7652 with circuits operating at ±15V requires a lower supply voltage divider with the TC7660 voltage converter circuit operated "backwards." Figure 4-7 shows an approximate connection.

FIGURE 4-5: LOW OFFSET COMPARATOR

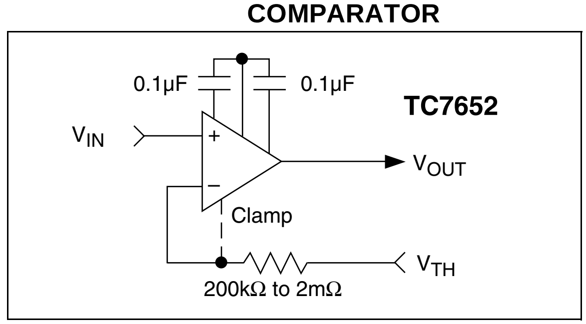


FIGURE 4-6: 1437 OFFSET NULLED BY TC7652

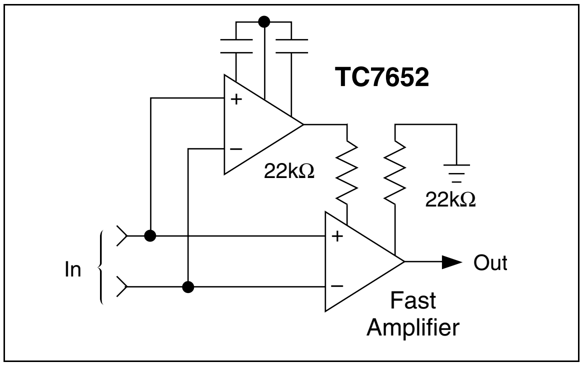
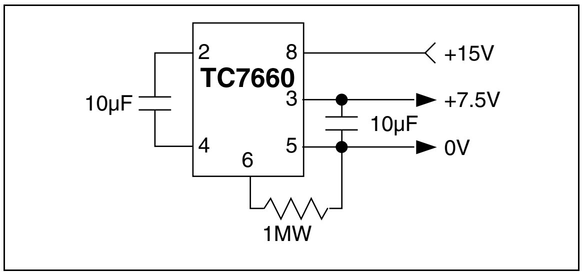


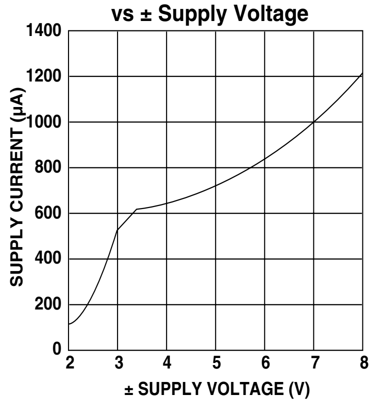
FIGURE 4-7: SPLITTING +15V WITH THE 7660 AT >95% EFFICIENCY



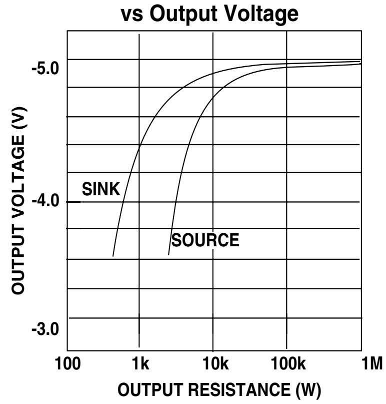
5.0 TYPICAL CHARACTERISTICS

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

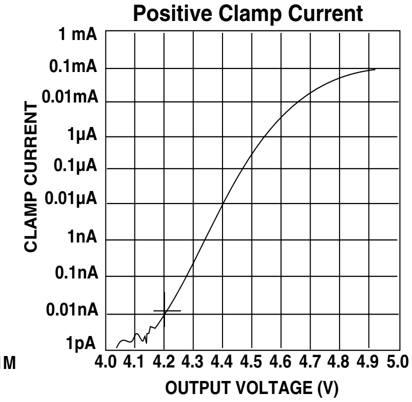
Supply Current vs ± Supply Voltage



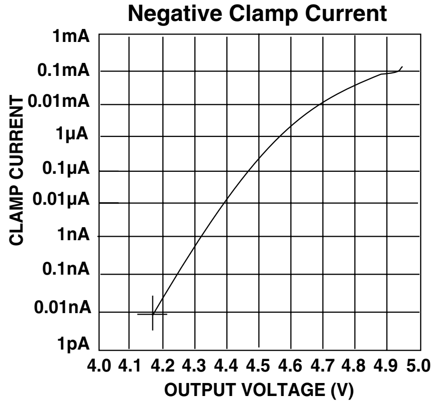
Output Resistance vs Output Voltage



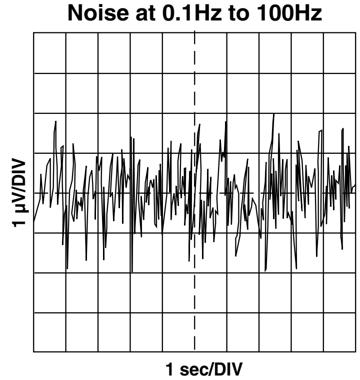
Positive Clamp Current



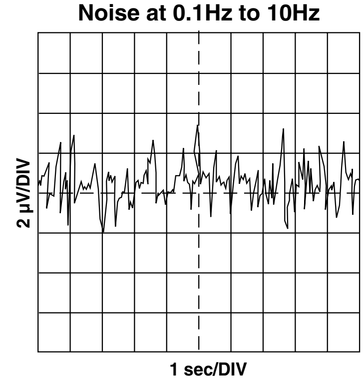
Negative Clamp Current



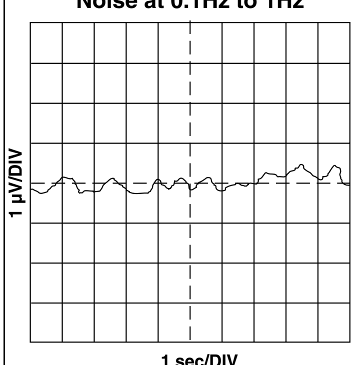
Noise at 0.1Hz to 100Hz



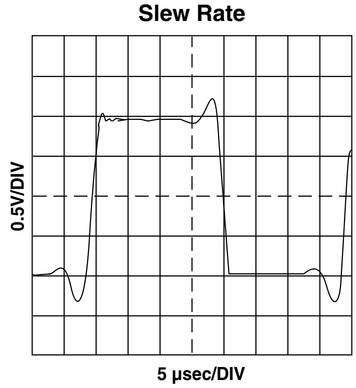
Noise at 0.1Hz to 10Hz



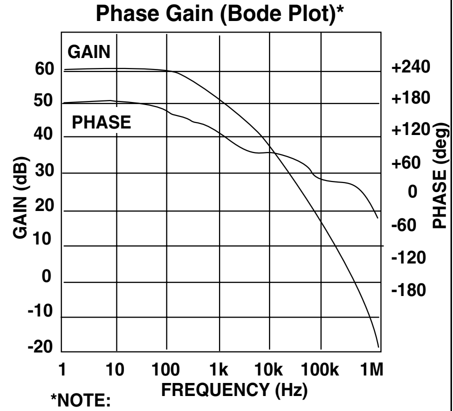
Noise at 0.1Hz to 1Hz



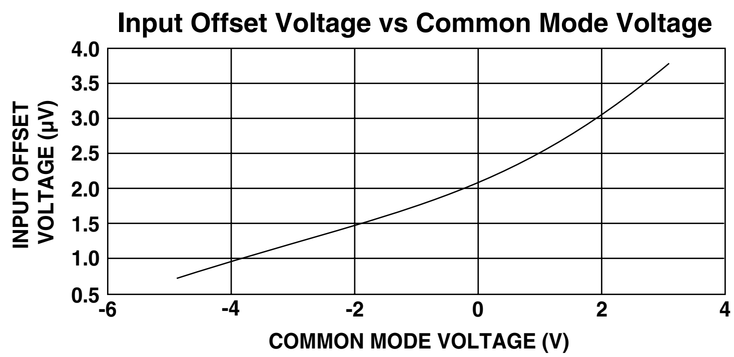
Slew Rate



Phase Gain (Bode Plot)*



*NOTE:
±5V, ±2.5V supplies; no load to 10k load.


Input Offset Voltage vs Common Mode Voltage
INPUT OFFSET VOLTAGE (µV)
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
-6
-4
-2
0
2
4
COMMON MODE VOLTAGE (V)

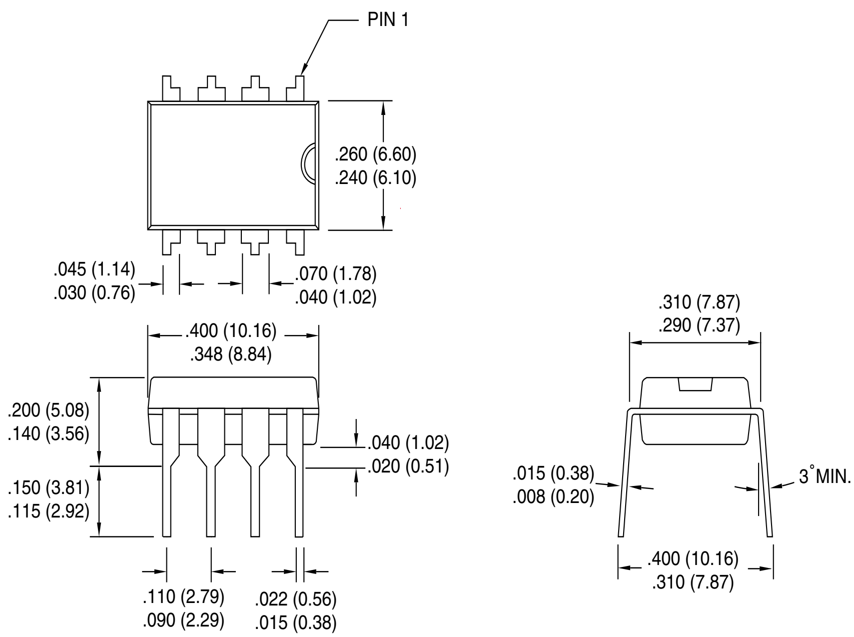
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

Package marking information not available at this time.

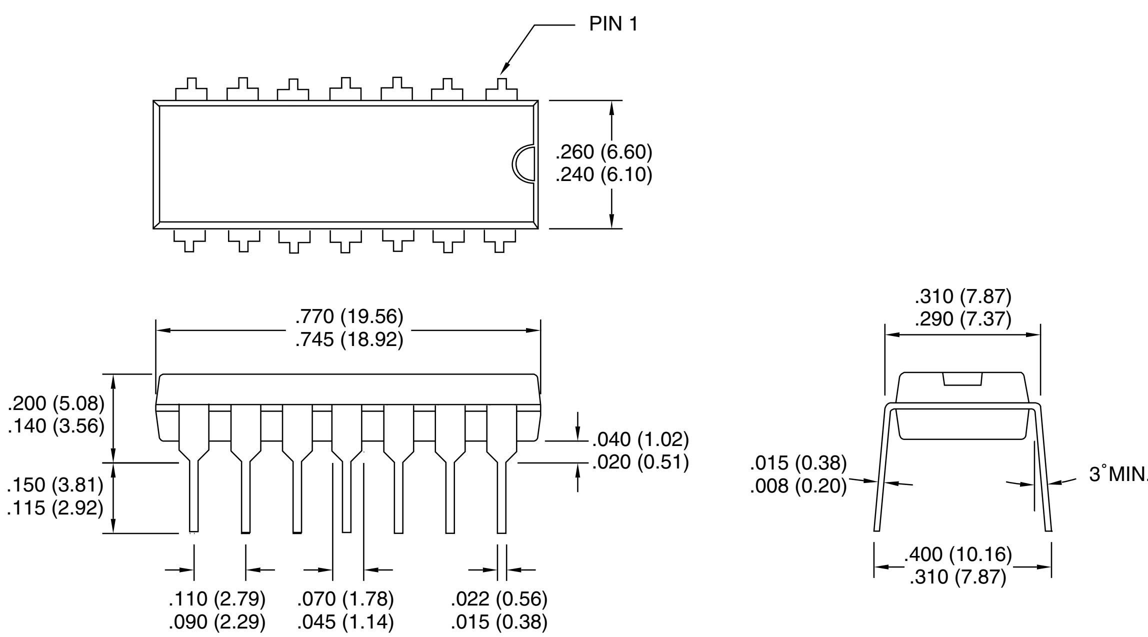
6.2 Package Dimensions

8-Pin Plastic DIP



Dimensions: inches (mm)

14-Pin PDIP (Narrow)



Dimensions: inches (mm)

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