TOSHIBA Bi-CMOS Digital Integrated Circuit Silicon Monolithic

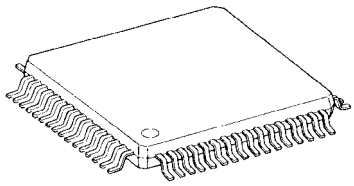
# TB6534F

Video Camera Cylinder Motor Controllers and Capstan Motor Controllers

The TB6534F is a single-chip IC for video camera cylinder motor controllers and capstan motor controllers.

The cylinder section is a soft-switching pre-driver based on a 3-phase full-wave sensorless driver and 180° trapezoidal wave commutation control.

The capstan section is a soft-switching pre-driver based on 3-phase full-wave drive and pseudo-sine wave commutation control.



LQFP64-P-1010-0.50A

Weight: 0.34 g (typ.)

## Features

- Operating voltage: $V_{CC\ (opr)}$ = 2.7 to 5.5 V

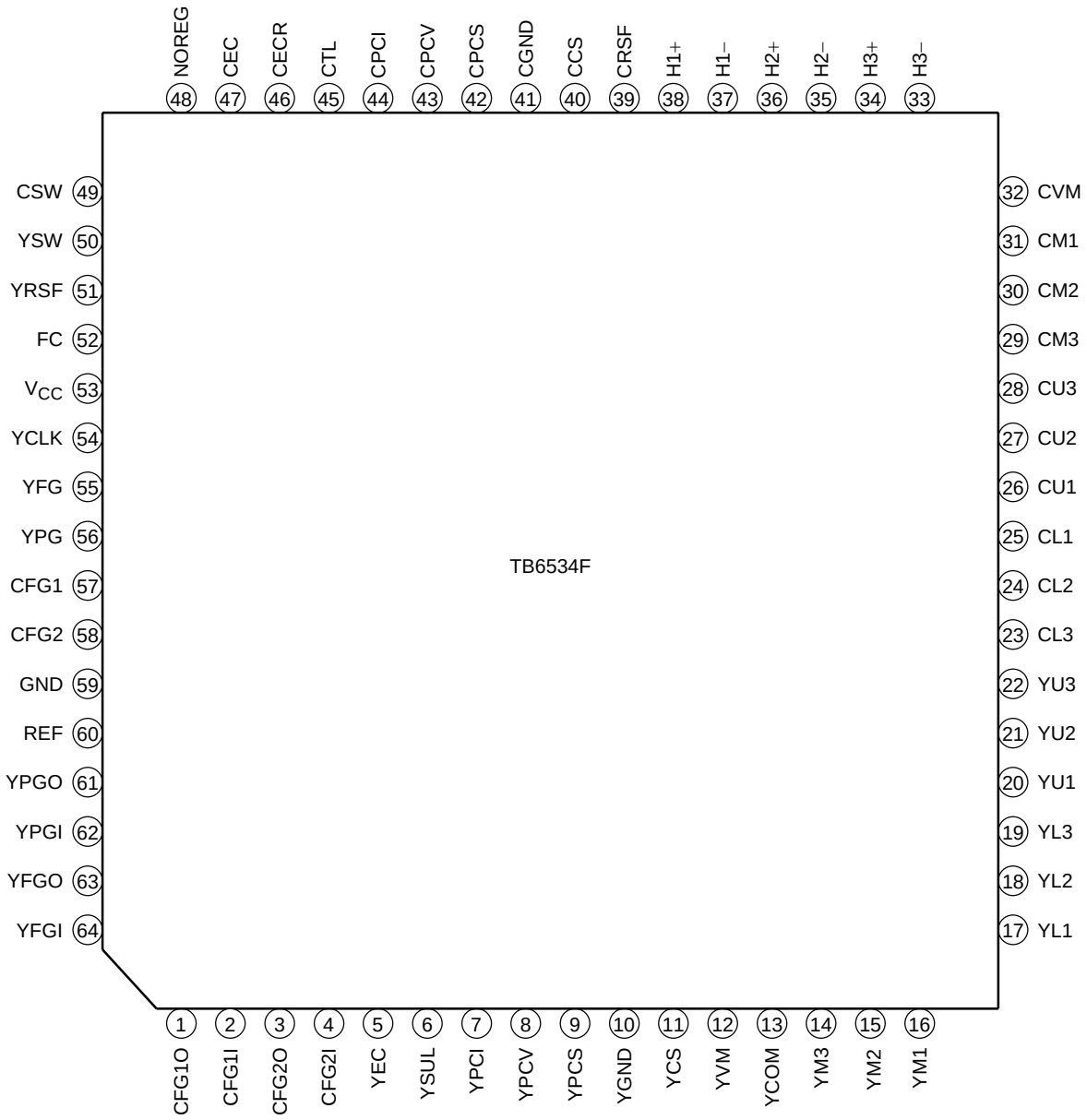
<Cylinder part>

- Built-in FG/PG amplifier
- CW, CCW, and stop modes are available
- Detect upper $V_{CE}$, and output PWM for external switch regulator
- Built-in current limiter
- Built-in $V_M$ short-protection

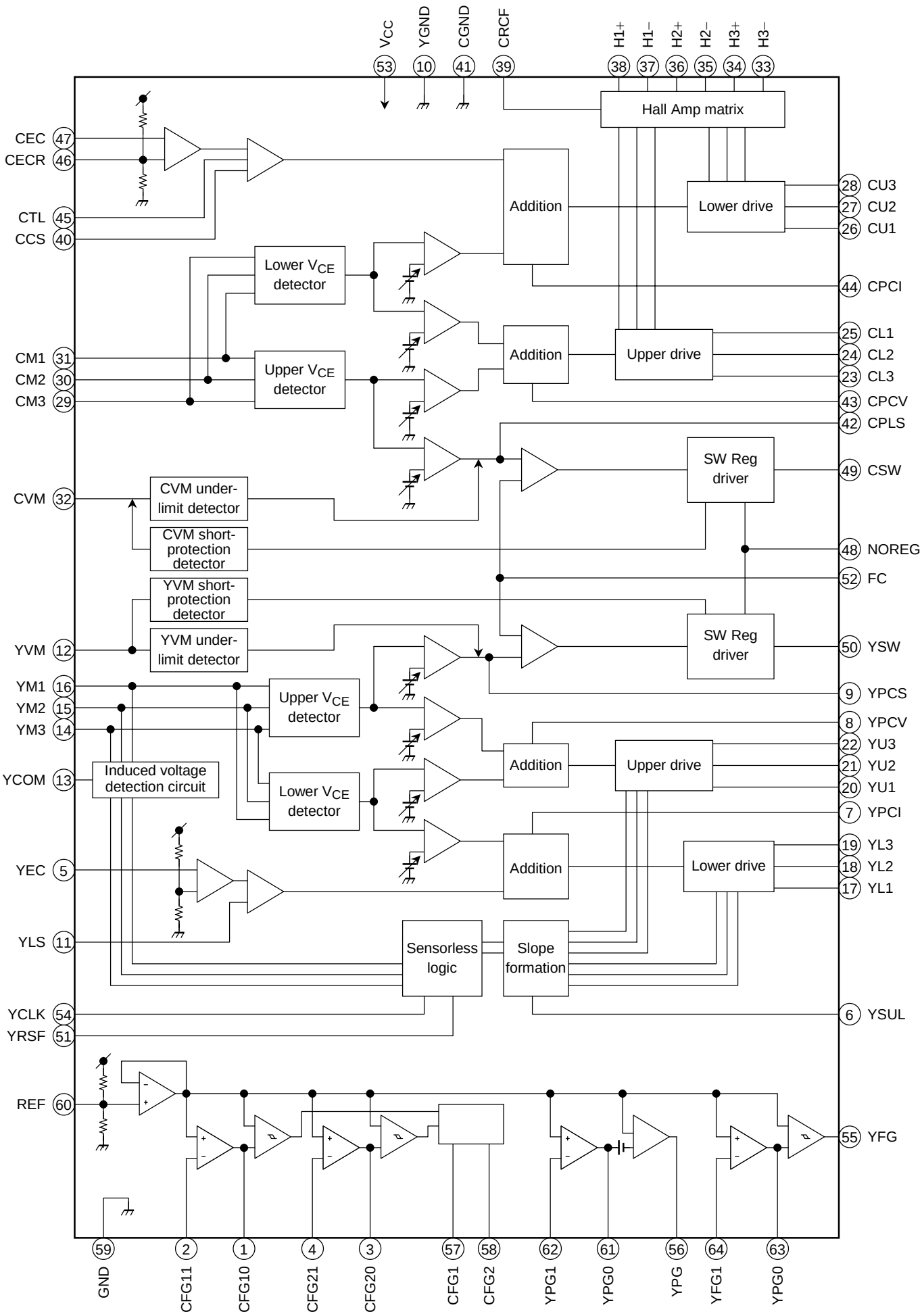
<Capstan part>

- 2-way FG amplifier
- CW, CCW, and stop modes are available
- Detect upper $V_{CE}$, and output PWM for external switch regulator
- Built-in current limiter
- Built-in $V_M$ short-protection

## Pin Connection



## Block Diagram



## Pin Function

| Pin No. | Symbol | Functional Description | Pin No. | Symbol | Functional Description |
|---|---|---|---|---|---|
| 1 | CFG1O | Capstan part FG amplifier output pin 1 | 33 | H3− | Capstan motor hall element input pin |
| 2 | CFG1I | Capstan part FG input pin 1 | 34 | H3+ | |
| 3 | CFG2O | Capstan part FG amplifier output pin 2 | 35 | H2− | |
| 4 | CFG2I | Capstan part FG input pin 2 | 36 | H2+ | |
| 5 | YEC | Cylinder part torque command input pin | 37 | H1− | |
| 6 | YSUL | Cylinder part slope voltage pin | 38 | H1+ | |
| 7 | YPCI | Cylinder part current feedback phase compensation | 39 | CRSF | Capstan part directional control input pin |
| 8 | YPCV | Cylinder part voltage feedback phase compensation | 40 | CCS | Capstan part current detection input pin |
| 9 | YPCS | Cylinder part switching voltage control output pin | 41 | CGND | Capstan part ground pin |
| 10 | YGND | Cylinder part ground pin | 42 | CPCS | Capstan part switching voltage control output |
| 11 | YCS | Cylinder part current detection input pin | 43 | CPCV | Capstan part voltage feedback phase compensation |
| 12 | YVM | Cylinder motor power voltage pin | 44 | CPCI | Capstan part current feedback phase compensation |
| 13 | YCOM | Cylinder motor coil neutral pin | 45 | CTL | Capstan part torque limit |
| 14 | YM3 | Cylinder motor coil pin | 46 | CECR | Capstan part torque command reference voltage |
| 15 | YM2 | | 47 | CEC | Capstan part torque command input pin |
| 16 | YM1 | | 48 | NOREG | SW Transistor charge removal pin |
| 17 | YL1 | Cylinder motor lower pre-driver output pin | 49 | CSW | Capstan part switching pre-driver output |
| 18 | YL2 | | 50 | YSW | Cylinder part switching pre-driver output |
| 19 | YL3 | | 51 | YRSF | Cylinder part standby switch input |
| 20 | YU1 | Cylinder motor upper pre-driver output pin | 52 | FC | Switching comparator's triangular-wave input pin |
| 21 | YU2 | | 53 | $V_{CC}$ | Power voltage supply pin for Logic |
| 22 | YU3 | | 54 | YCLK | Cylinder part clock input pin |
| 23 | CL3 | Capstan motor lower pre-driver output pin | 55 | YFG | Cylinder part FG pulse wave output |
| 24 | CL2 | | 56 | YPG | Cylinder part PG pulse wave output |
| 25 | CL1 | | 57 | CFG1 | Capstan part FG pulse wave output 1 |
| 26 | CU1 | Capstan motor upper pre-driver output pin | 58 | CFG2 | Capstan part PG pulse wave output 2 |
| 27 | CU2 | | 59 | GND | FG/PG part GND pin |
| 28 | CU3 | | 60 | REF | FG/PG part reference voltage pin |
| 29 | CM3 | Capstan motor coil pin | 61 | YPGO | Cylinder part PG amplifier output pin |
| 30 | CM2 | | 62 | YPGI | Cylinder part PG input |
| 31 | CM1 | | 63 | YFGO | Cylinder part FG amplifier output pin |
| 32 | CVM | Capstan motor power voltage pin | 64 | YFGI | Cylinder part FG input |

## Maximum Ratings (Ta = 25°C)

| Characteristics | Symbol | Rating | Unit | Note |
|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | 8 | V | $V_{CC}$ |
| Motor supply voltage | $V_M$ | 12 | V | YVM, CVM |
| Battery supply voltage | $V_B$ | 12 | V | NOREG (VB), YSW, CSW |
| Output pin voltage | $V_N$ | 12 | V | YM1, YM2, YM3, YU1, YU2, YU3, YL1, YL2, YL3, CM1, CM2, CM3, CU1, CU2, CU3, CL1, CL2, CL3 |
| Input pin voltage | $V_I$ | −0.3 to $V_{CC}$ + 0.3 | V | YSTB, YCLK, FC, YPGi, YFGi, CFG1i, CFG2i, CRSF, YCS, CCS, CTL, CECR, CEC, YEC |
| Power dissipation | $P_D$ | 0.95 | W | Before mounting on a PCB |
| Operating temperature | $T_{opr}$ | −20 to 85 | °C | |
| Storage temperature | $T_{stg}$ | −55 to 125 | °C | |

## Recommended Operating Condition

| Characteristics | Symbol | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | — | — | 2.7 | 3.0 | 3.3 | V |
| Clock input frequency | Vsl | — | — | 400 | 430 | 440 | kHz |

## Electrical Characteristics (unless otherwise specified, Ta = 25°C, $V_{CC}$ = 3.0 V, Vb = 7.2 V)

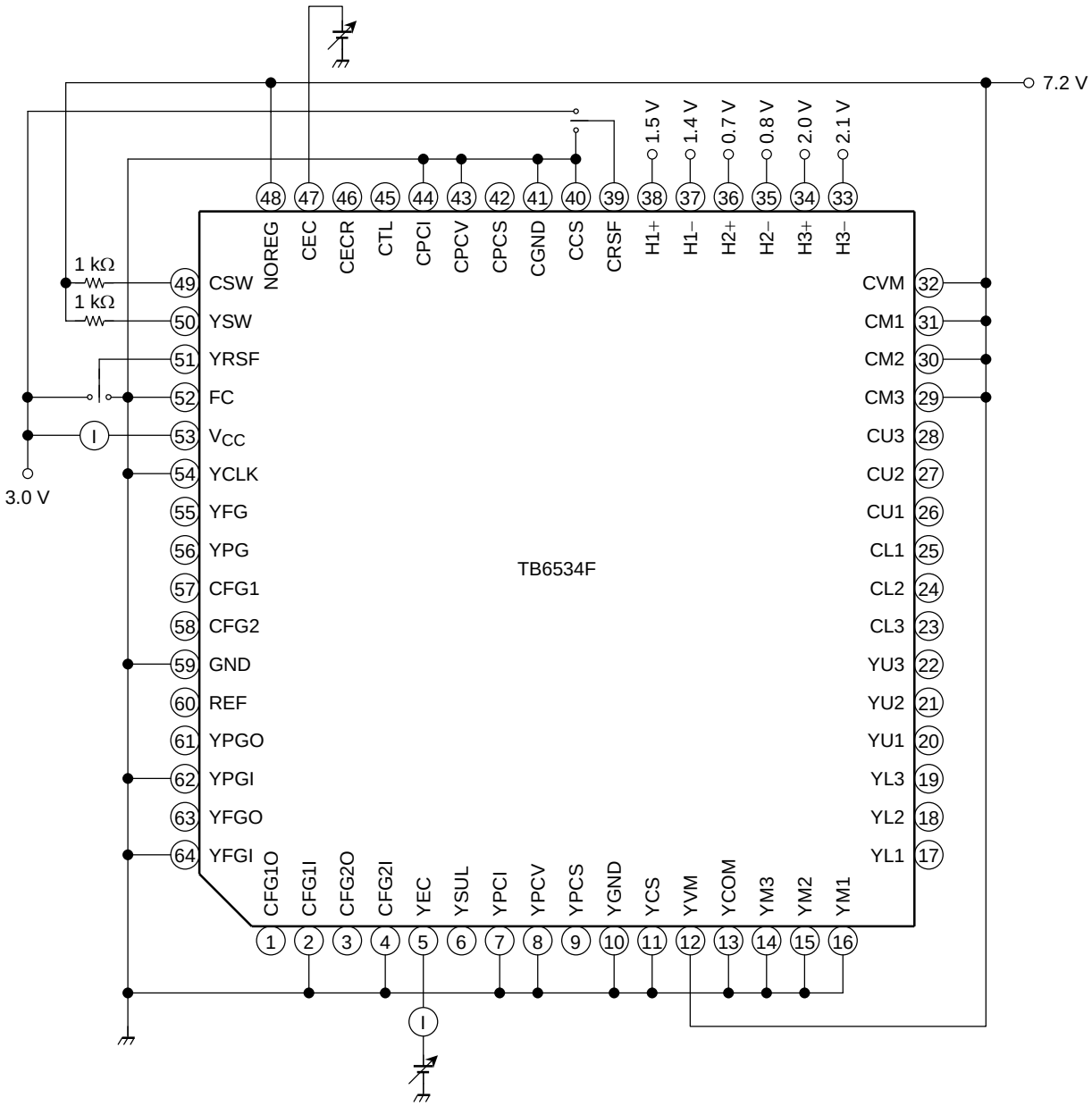
### Cylinder Part

| No. | Characteristics | Symbol | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| 1 | Supply current (1) | $I_{CC\ (1)}$ | 1 | Both cylinder and capstan parts are during operation. | — | 15 | 20 | mA |
| 2 | Supply current (2) | $I_{CC\ (2)}$ | 1 | Both cylinder and capstan parts are during standby state. | — | 6.1 | 12 | mA |
| 3 | ECR voltage | VECR | 2 | — | 1.5 | 1.7 | 1.9 | V |
| 4 | Torque control input current | YIEC | 1 | YEC = 0 V | −5 | −2 | — | μA |
| 5 | Input/output gain | YGio | 2 | — | 0.15 | 0.17 | 0.20 | |
| 6 | Maximum output voltage | YCSmax | 2 | RYCS = 0.22 Ω | 150 | 168 | 183 | mV |
| 7 | Lower side output voltage (1) | VL (1) | 3 | YCS = 54 mV | 0.15 | 0.2 | 0.3 | V |
| 8 | Lower side output voltage (2) | VL (2) | 3 | YECR = 1.5 V, YEC = 0 V | 0.35 | 0.5 | 0.65 | V |
| 9 | Upper side drive current | YIU | 4 | YIU = −10 mA | — | 0.65 | 1.2 | V |
| 10 | Lower side drive current | YIL | 4 | YIL = 10 mA | 1.1 | 1.6 | — | V |
| 11 | YFG amp gain | YGFG | 5 | $V_{p-p}$ = 1.5 mV, f = 1 kHz | 45 | — | — | |
| 12 | YFG high level | YFG (H) | 6 | IYFG = −100 μA | 2.5 | 2.8 | — | V |
| 13 | YFG low level | YFG (L) | 6 | IYFG = 100 μA | — | 0.1 | 0.5 | V |
| 14 | PG amp gain | YGPG | 5 | $V_{p-p}$ = 1.5 mV, f = 1 kHz | 45 | — | — | |
| 15 | PG amp offset voltage | ΔPGin | 6 | — | 0.4 | 0.45 | 0.52 | V |
| 16 | YPG high level | YPG (H) | 6 | IYPG = −100 μA | 2.5 | 2.8 | — | V |
| 17 | YPG low level | YPG (L) | 6 | IYPG = 100 μA | — | 0.1 | 0.5 | V |
| 18 | Forward rotation control voltage | YVf | 7 | — | — | — | 0.5 | V |
| 19 | STB control voltage | YVs | 7 | — | 1.2 | — | 1.9 | V |
| 20 | Reverse rotation control voltage | YVr | 7 | — | 2.4 | — | — | V |
| 21 | Amp reference voltage | $V_{REF}$ | 2 | — | 1.0 | 1.24 | 1.5 | V |
| 22 | Output idle voltage | YCSidle | 2 | RYCS = 0.22 Ω | — | 0 | 5 | mV |
| 23 | SW power voltage input offset | YSWofs | 8 | — | −30 | — | 30 | mV |
| 24 | SW power voltage control output gain | YGPCS | 9 | — | — | 80 | — | |
| 25 | SW power voltage control output voltage (1) | YVUD (1) | 9 | YEC = 1.5 V, YPCS = 1.7 V | 0.1 | 0.2 | 0.3 | V |
| 26 | SW power voltage control output voltage (2) | YVUD (2) | 9 | YEC = 0 V | 0.05 | 0.1 | 0.15 | V |
| 27 | SW power voltage output maximum current | YISWB | 9 | YEC = 0 V | 10 | — | — | mA |
| 28 | $V_M$ under limit | YVML | 10 | — | 1.2 | 1.5 | 1.7 | V |
| 29 | $V_M$ short protection | YVMS | 10 | — | 0.2 | 0.3 | 0.4 | V |
| 30 | SW output enforced ON EC voltage | YSWEC | 9 | — | 1.2 | 1.3 | 1.4 | V |

### Capstan Part

| No. | Characteristics | Symbol | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| 31 | Torque control input current | CIEC | 11 | CEC = CECR = 1.5 V | −3 | −1 | — | μA |
| 32 | Torque control reference voltage | CECR | 11 | — | 1.3 | 1.5 | 1.7 | V |
| 33 | Torque control input voltage | CEC | 12 | — | 0.2 | — | 2.8 | V |
| 34 | Output maximum voltage | CCSmax | 12 | RCCS = 0.27 Ω | 0.19 | 0.23 | — | V |
| 35 | Torque control I/O gain | CGio | 12 | — | 0.21 | 0.24 | 0.26 | V |
| 36 | Output idle voltage | CCSidle | 12 | — | — | 0 | 4 | mV |
| 37 | Torque control input offset | CECofs | 12 | — | −100 | 41 | 100 | mV |
| 38 | Torque control dead zone | CECdz | 12 | — | 50 | 88 | 130 | mV |
| 39 | Low side $V_{CE}$ voltage (1) | CVLL (1) | 13 | CCS = 60 mV | 0.17 | 0.23 | 0.35 | V |
| 40 | Low side $V_{CE}$ voltage (2) | CVLL (2) | 13 | CEC = 0 V, CTL = 1.0 V | 0.45 | 0.62 | 0.75 | V |
| 41 | Hall element permissible input voltage (1) | Hin (1) | 14 | — | 1.2 | — | 1.8 | V |
| 42 | Hall element permissible input voltage (2) | Hin (2) | 14 | — | 0.4 | — | 1.3 | V |
| 43 | Hall element permissible input voltage (3) | Hin (3) | 14 | — | 1.9 | — | 2.7 | V |
| 44 | Hall element input conversion offset | Hofs | 15 | — | −8 | −2 | 8 | mV |
| 45 | TL-CS offset | TLofs | 16 | CTL = 20 mV | 8 | 12 | 16 | mV |
| 46 | Forward rotation control voltage | CVf | 17 | — | — | — | 0.5 | V |
| 47 | Stop control voltage | CVs | 17 | — | 1.2 | — | 2.0 | V |
| 48 | Reverse rotation control voltage | CVr | 17 | — | 2.4 | — | — | V |
| 49 | Ripple cancel rate | R | 18 | CCS = 60 mV | 7 | 9 | 14 | % |
| 50 | Upper drive maximum voltage | CIU | 19 | CIU = −7 mA | — | 0.55 | 0.7 | V |
| 51 | Lower drive maximum voltage | CIL | 19 | CIL = 7 mA | 1.4 | 1.7 | — | V |
| 52 | SW power voltage input offset | CSWofs | 20 | — | −30 | — | 30 | mV |
| 53 | SW power voltage control output gain | CGPCS | 21 | — | — | 73 | — | |
| 54 | SW power voltage control output voltage (1) | CVUD (1) | 21 | CEC = CECR, CPCS = 1.7 V | 0.1 | 0.2 | 0.3 | V |
| 55 | SW power voltage control output voltage (2) | CVUD (2) | 21 | CEC = 0 V | — | 0 | 0.1 | V |
| 56 | SW power voltage output maximum current | CISWB | 21 | CEC = 0 V | 10 | — | — | mA |
| 57 | FG amplifier loop gain | CGFG | 22 | 1 kΩ, 220 kΩ, 3 $mV_{p-p}$, 1 kHz | 46 | — | — | |
| 58 | FG amplifier output voltage high level | CFGH | 22 | IFGH = −100 μA | 2.5 | — | — | V |
| 59 | FG amplifier output voltage low level | CFGL | 22 | IFGL = 100 μA | — | — | 0.5 | V |
| 60 | $V_M$ under limit | CVML | 23 | — | 0.7 | 0.82 | 1.1 | V |
| 61 | $V_M$ short protection | CVMS | 23 | — | 0.2 | 0.32 | 0.4 | V |
| 62 | SW output enforced ON EC voltage | CSWEC | 21 | — | — | — | 0.6 | V |
| 63 | NOREG pin current | IREG | 20 | — | — | 0 | 2.0 | μA |

## Test Circuit 1 $I_{CC\ (1)}$, $I_{CC\ (2)}$, YIEC




No.1 $I_{CC\ (1)}$

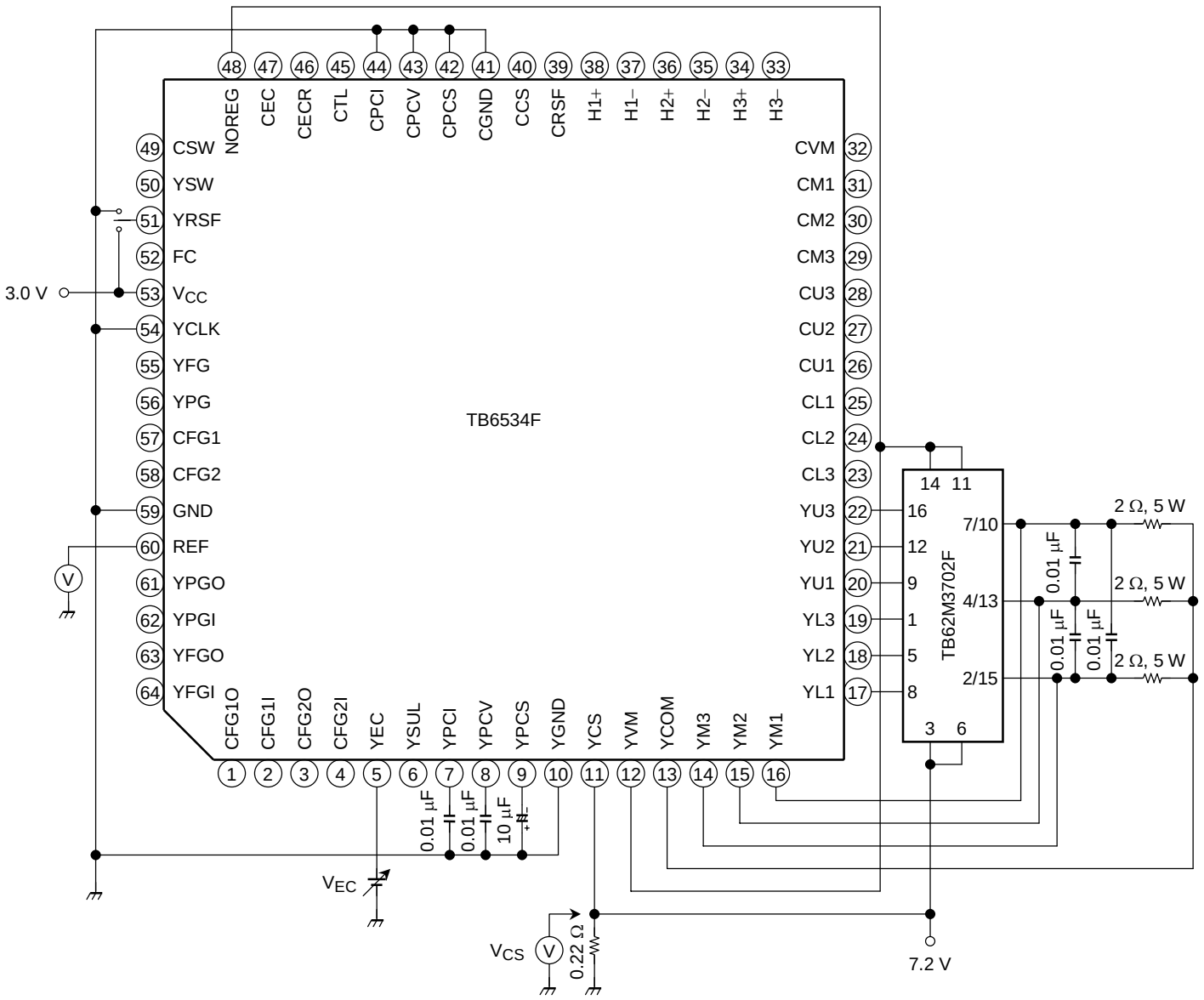
The input current to $V_{CC}$ pin when YRSF = 0 V, YEC = 0 V, CEC = 0 V, and CRSF = 0 V

No.2 $I_{CC\ (2)}$

Set YRSF = OPEN, YEC = 1.5 V, CEC = 1.5 V, and CRST = OPEN, then measure the current to $V_{CC}$ pin.

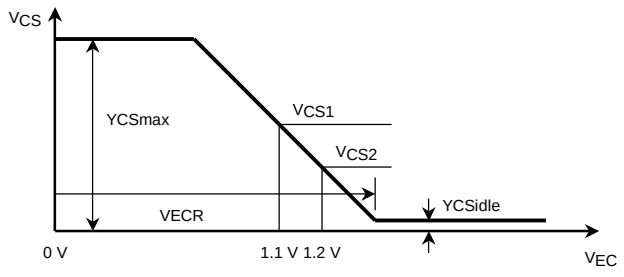
No.4 YIEC

### Test Circuit 2 VECR, YGio, YCSmax, YCSidle, $V_{REF}$



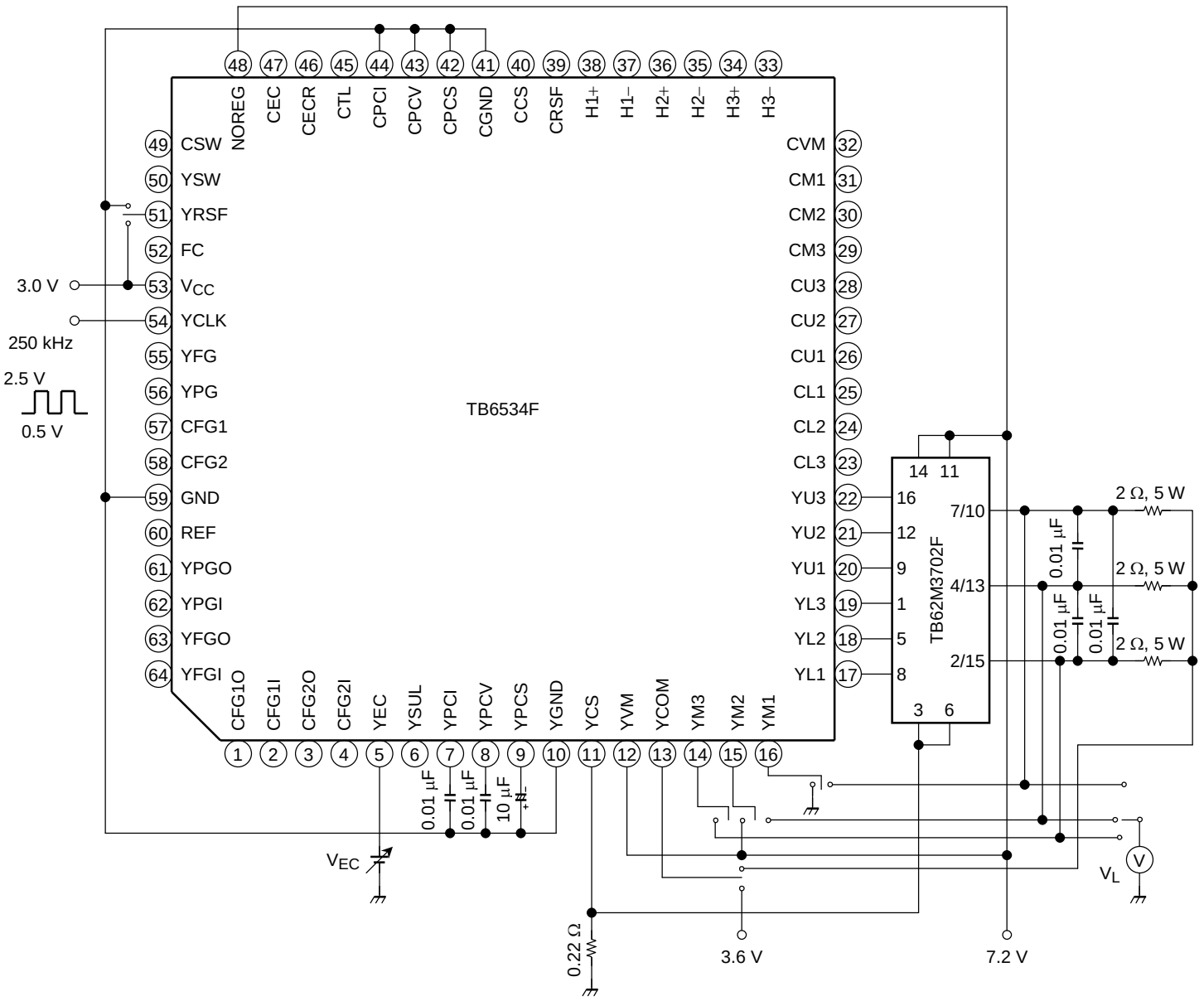

No.3 VECR, No.5 YGio, No.6 YCSmax, No.21 $V_{REF}$, No.22 YSCidle

Set YRSF = 0 V or 3 V, and change YEC from 0 V to 3 V, then measure the potential of YCS.




$$YGio = \frac{V_{CS1} - V_{CS2}}{0.1\,V}$$

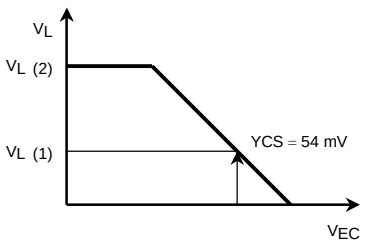
**Test Circuit 3 $V_{L\,(1)}$, $V_{L\,(2)}$**




No.7 $V_{L\,(1)}$, No.8 $V_{L\,(2)}$

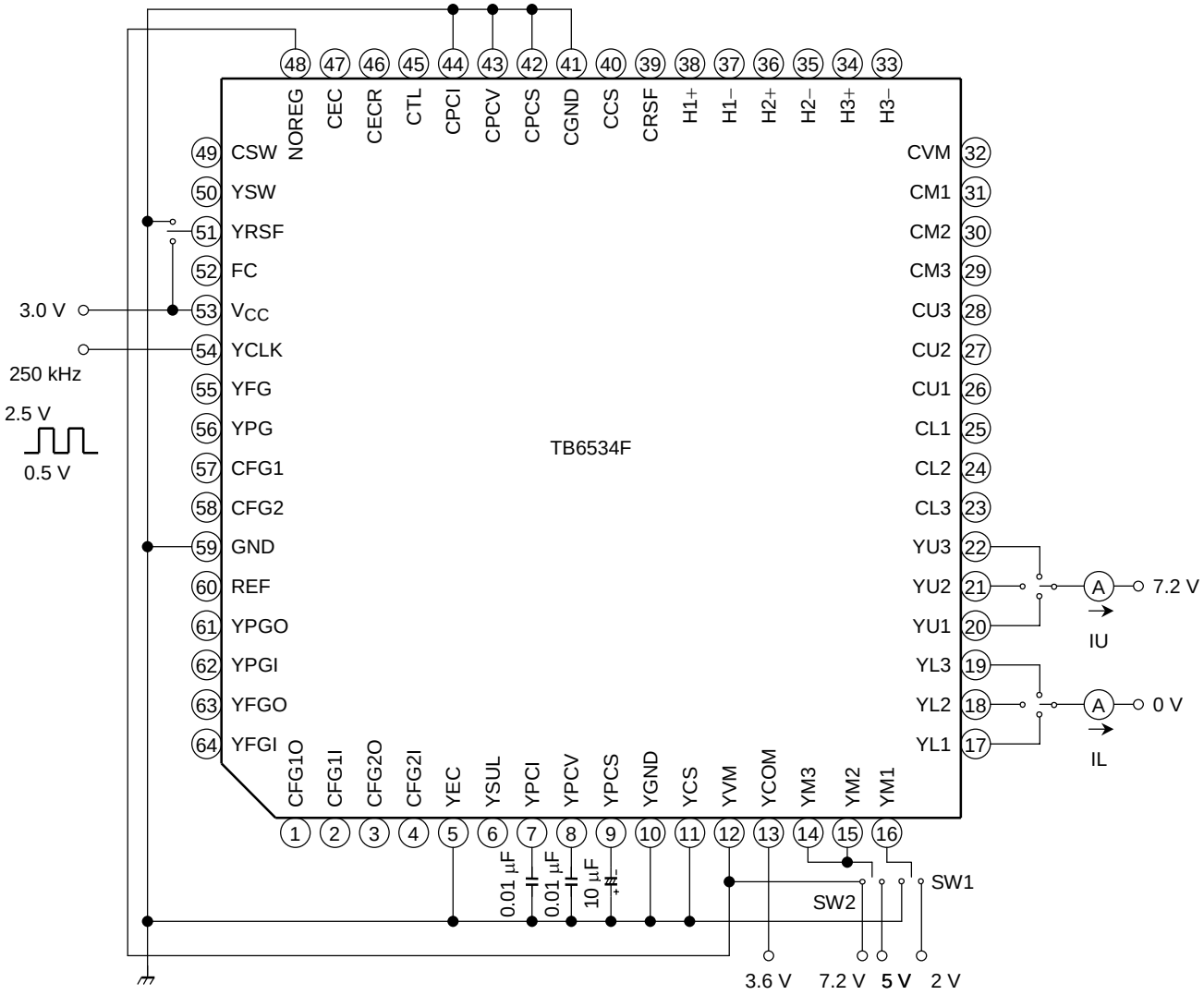
Change the pin YRSF from OPEN to L or H with YM1 = 0 V, YM2 = 6 V, YM3 = 6 V, and then enter the following clock counts into the pin YCLK in order to set the drive angle.

Connect the pins YM1, YM2, and YM3 to PWTR after setting the drive angle and then carry out the measurement.




| Clock | 160 | 300 | 540 |
|---|---|---|---|
| Test pin | YM3 | YM1 | YM2 |

## Test Circuit 4 YIU, YIL

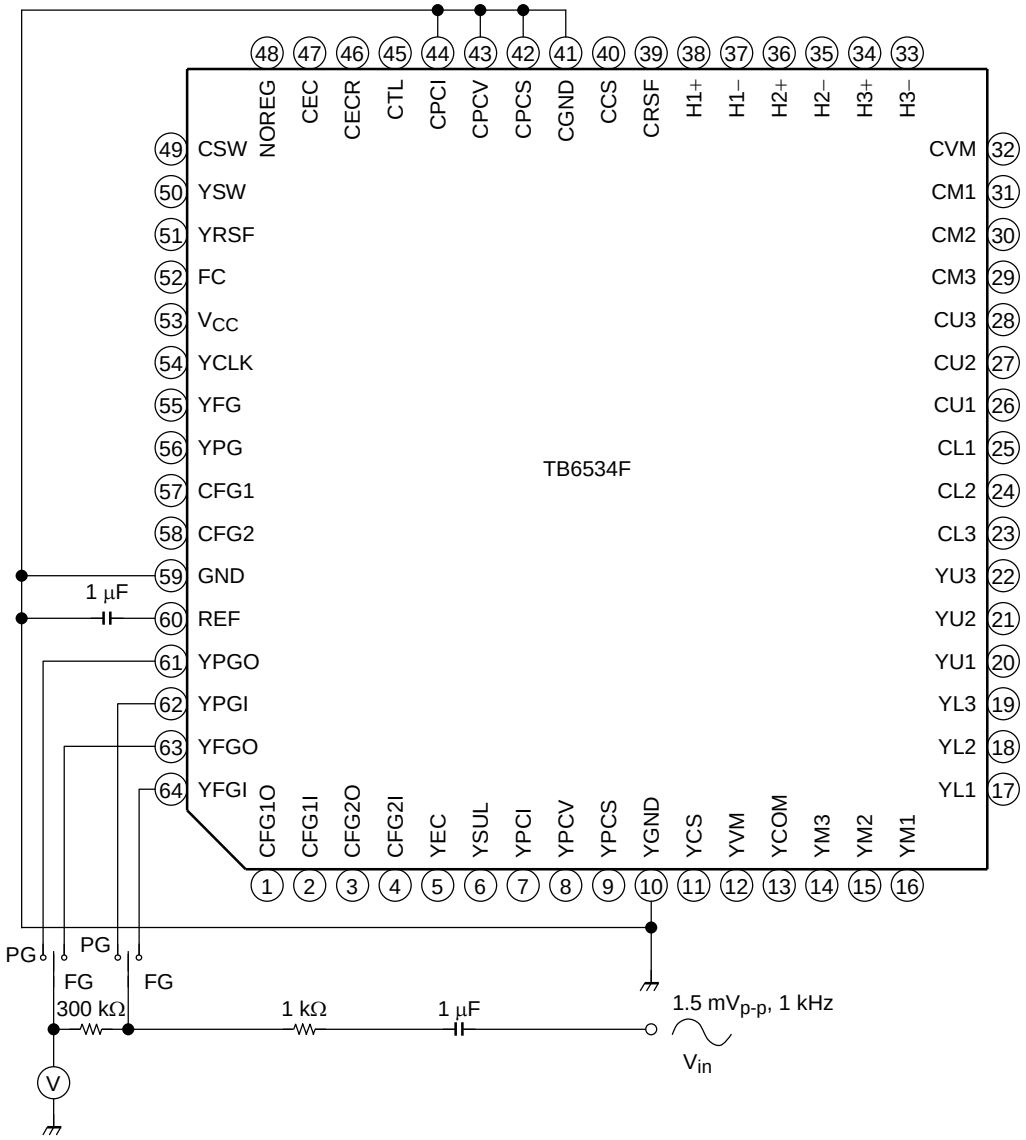



No.9 YIU, No.10 YIL

Change the pin YFRS from OPEN to L or H, and then enter the following clock counts into the pin YCLK in order to set the drive angle.

| Clock | 100 | | 210 | | 400 | |
|---|---|---|---|---|---|---|
| Test Pin | YU1 | YL3 | YU2 | YL1 | YU3 | YL2 |
| SW1 | 0 V | 2 V | 0 V | 2 V | 0 V | 2 V |
| SW2 | 5 V | 7.2 V | 5 V | 7.2 V | 5 V | 7.2 V |

## Test Circuit 5 YGFG, YGPG



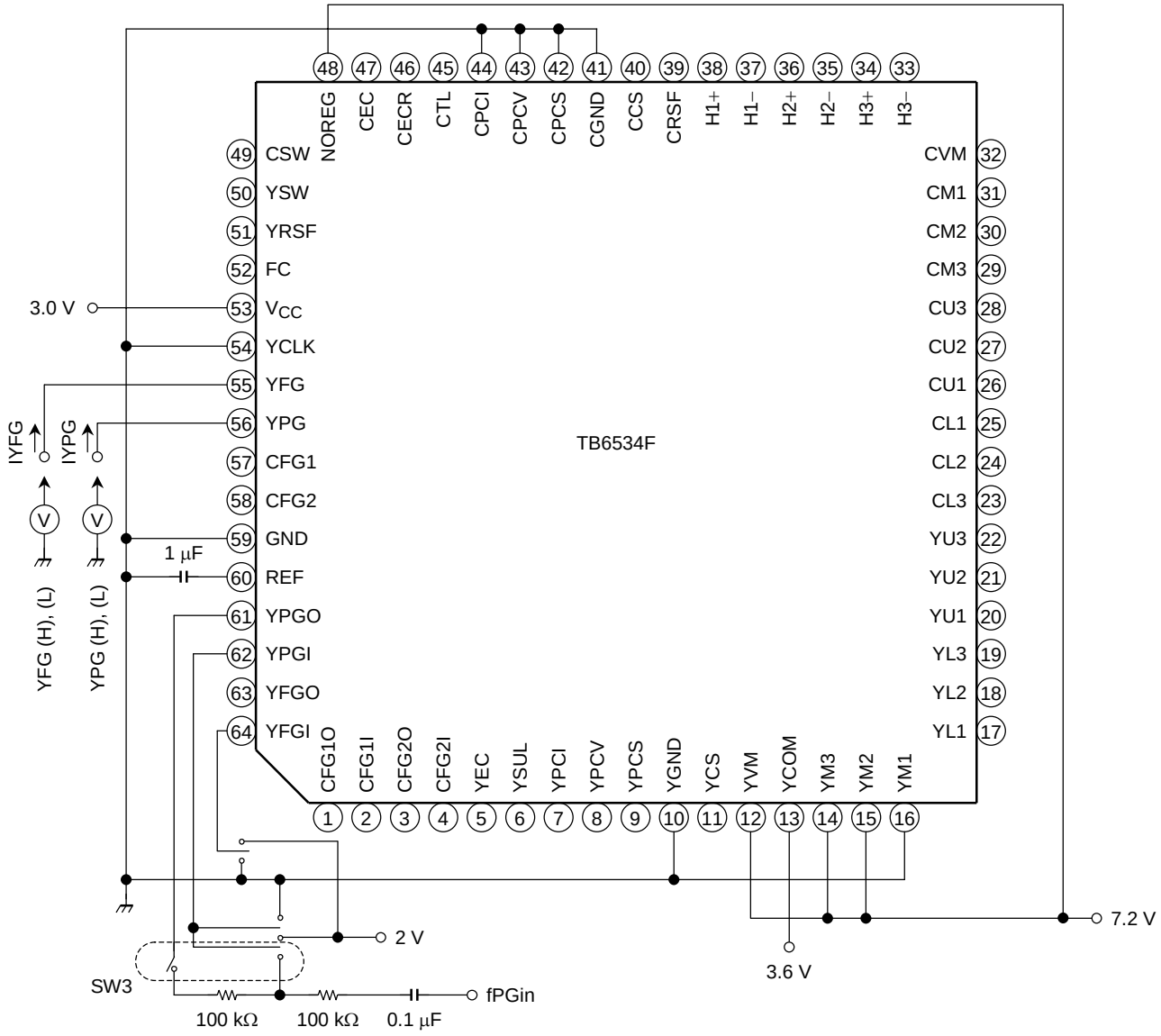

No.11 YGFG

Set the SW to FG, measure Vo when $V_{in}$ = 1.5 $mV_{p\text{-}p}$ at 1 kHz and acquire GFG = 20 ℓog ($Vo/V_{in}$)

No.15 YGPG

Set the SW to PG, measure Vo when $V_{in}$ = 1.5 $mV_{p\text{-}p}$ at 1 kHz and acquire GFG = 20 ℓog ($Vo/V_{in}$)

## Test Circuit 6 YFG (H), YFG (L), ΔPGin, YPG (H), YPG (L)




No.12 YFG (H)

Apply 2 V to YFGin and set YFG to High. Then measure the YFG potential when −100 μA is input to IYFG.

No.13 YFG (L)

Apply 0 V to YFGin and set YFG to Low. Then measure the YFG potential when 100 μA is input to IYFG.

No.15 ΔPGin

Turn SW3 on and input 10 kHz square wave from fPGin. Set fPGin to 1.2 $V_{p\text{-}p}$ (ΔPGin = 0.6 V) and check that the pin YPG is active.

Also, set $V_{p\text{-}p}$ to 0.8 V (ΔPGin = 0.4 V) and check that the pin YPG is not active.

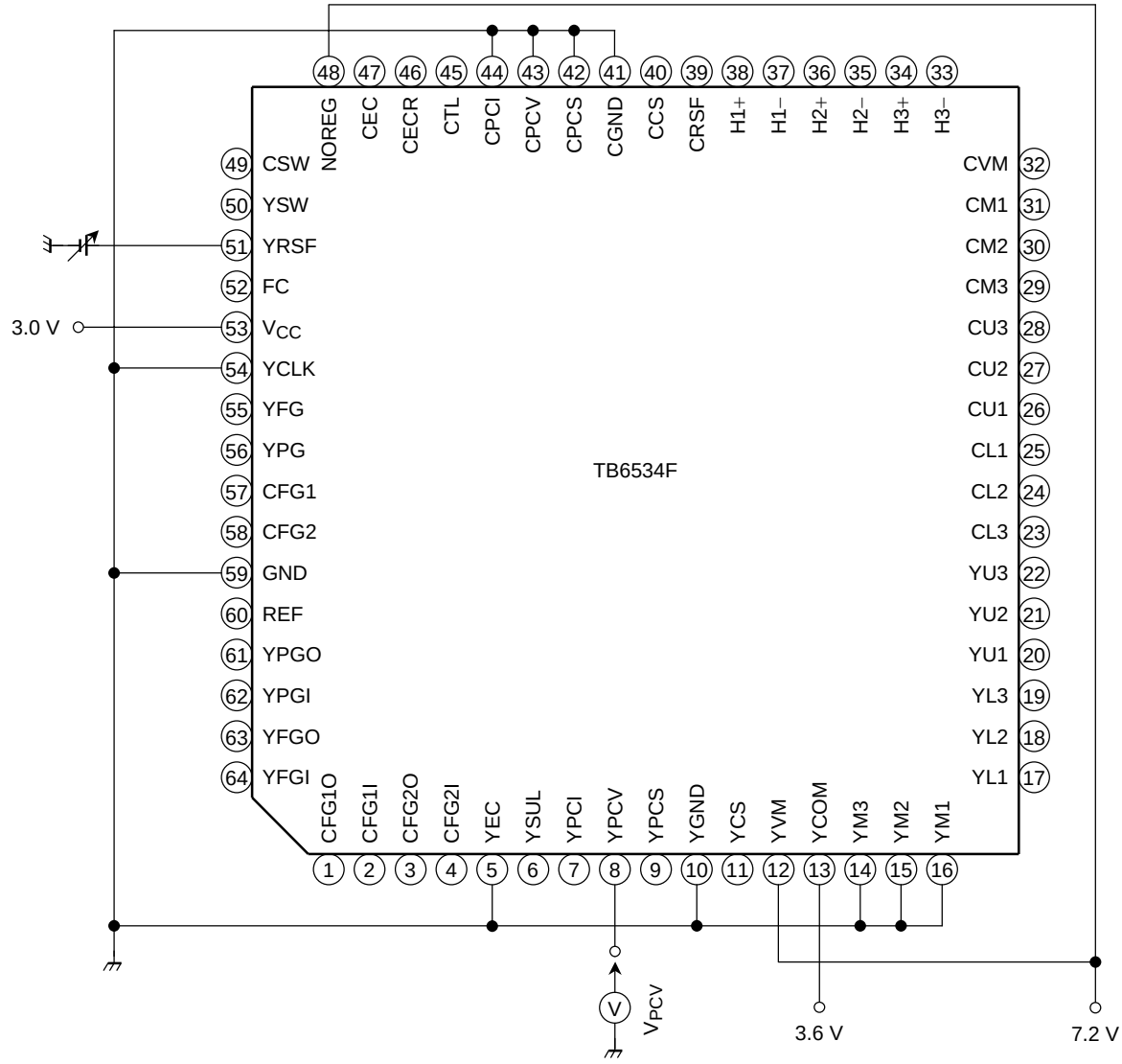
No.16 YPG (H)

Apply 2 V to YPGin and set YPG to High. Then measure the YFG potential when a current of IYPG = −100 μA is obtained.

No.17 YPG (L)

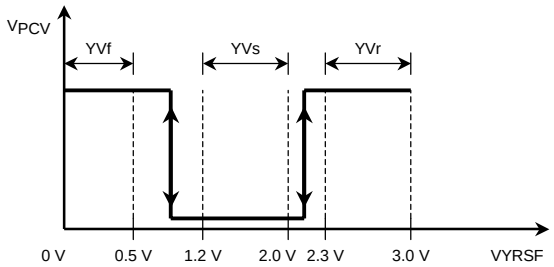
Apply 0 V to YPGin and set YPG to Low. Then measure the YFG potential when a current of IYPG = 100 μA is obtained.

## Test Circuit 7 YVf, YVs, YVr

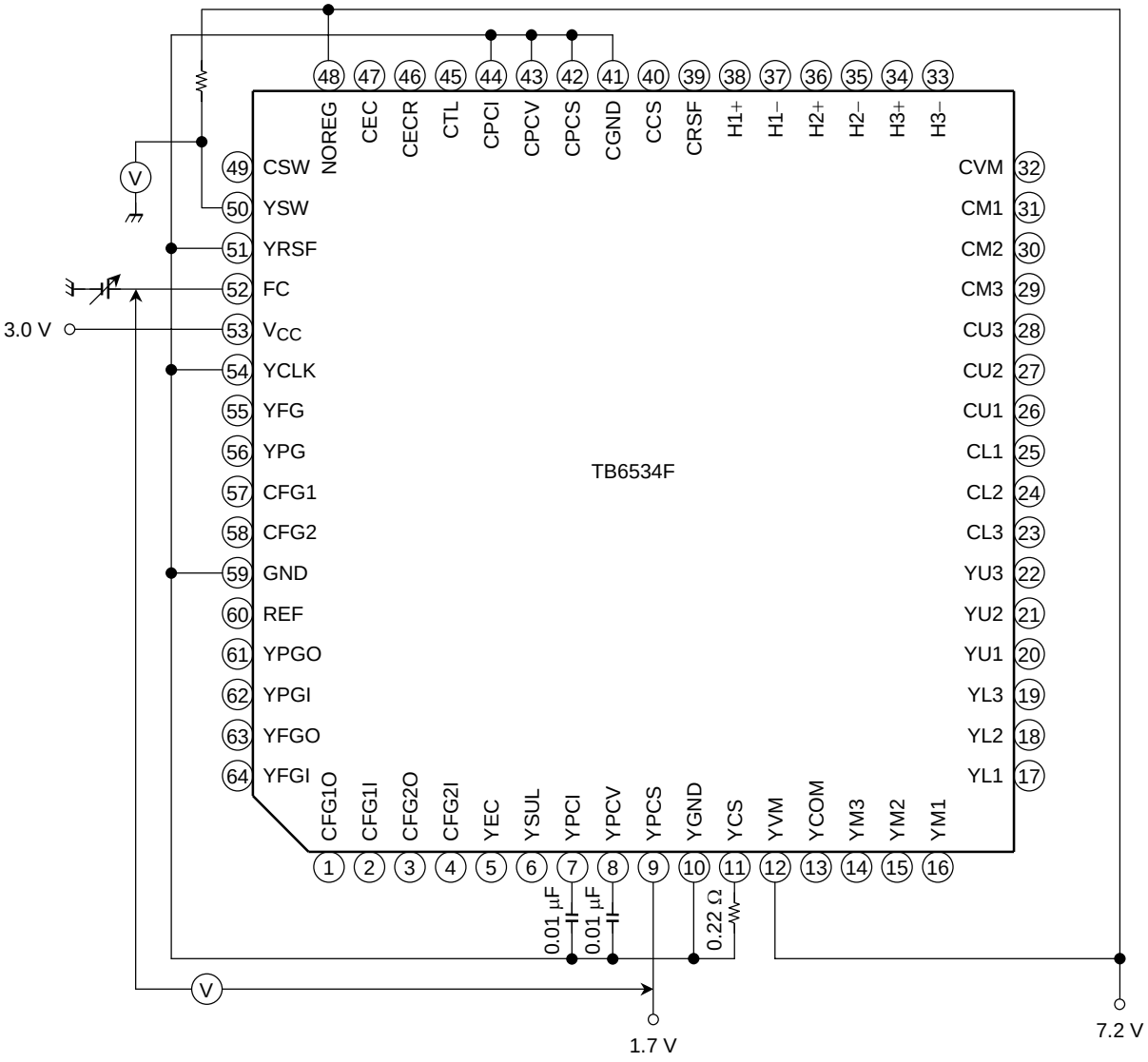



No.18 YVf, No.19 YVs, No.20 YVr

Change VRSF from 0 V to 3 V, and from 3 V to 0 V. Then measure $V_{PCV}$.

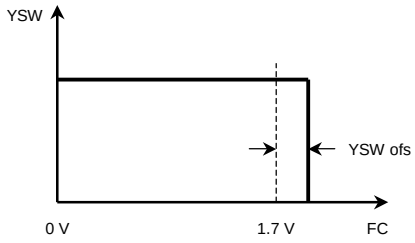


## Test Circuit 8 YSW ofs

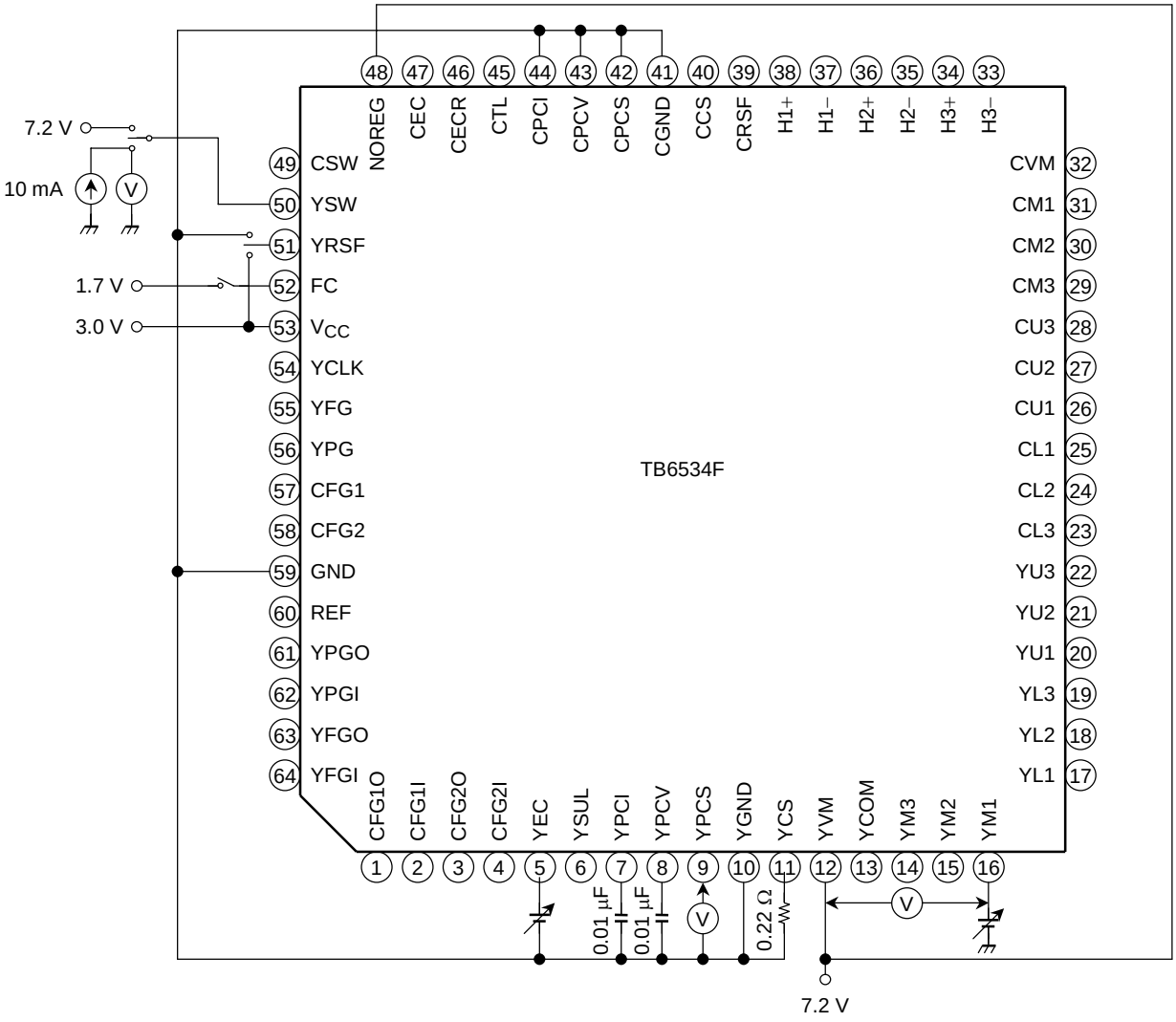



No.23 YSW ofs

Set YPCS = 1.7 V, and change FC from 0 V to 3.0 V. Then measure the potential difference between pins FC and YPCS (FC – YPCS) when YSW becomes Low from High.



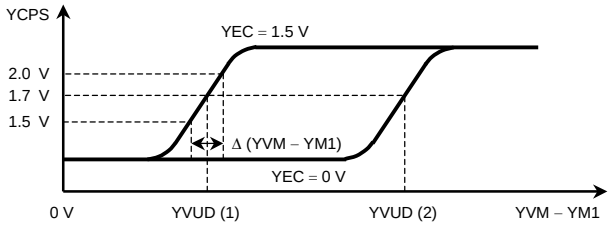
## Test Circuit 9 YGPCS, YVUD (1), YVUP (2), YISWB, YSWEC




No.24 YGPCS, No.25 YVUD (1), No.26 YVUD (2)

Set YEC = 0 V, and change CM1 from 7.2 V to 6.2 V. Then measure the potential difference between pins YVM and YM1 (YVM – YM1) when the potential of the pin YPCS becomes 1.7 V.

Set YEC = 1.5 V, and perform the same steps indicated above, and acquire the characteristics shown below.



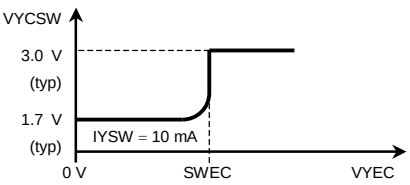

$$YGPCS = \frac{2.0\ V - 1.5\ V}{\Delta\,(YVM - YM1)}$$

No.27 YISWB

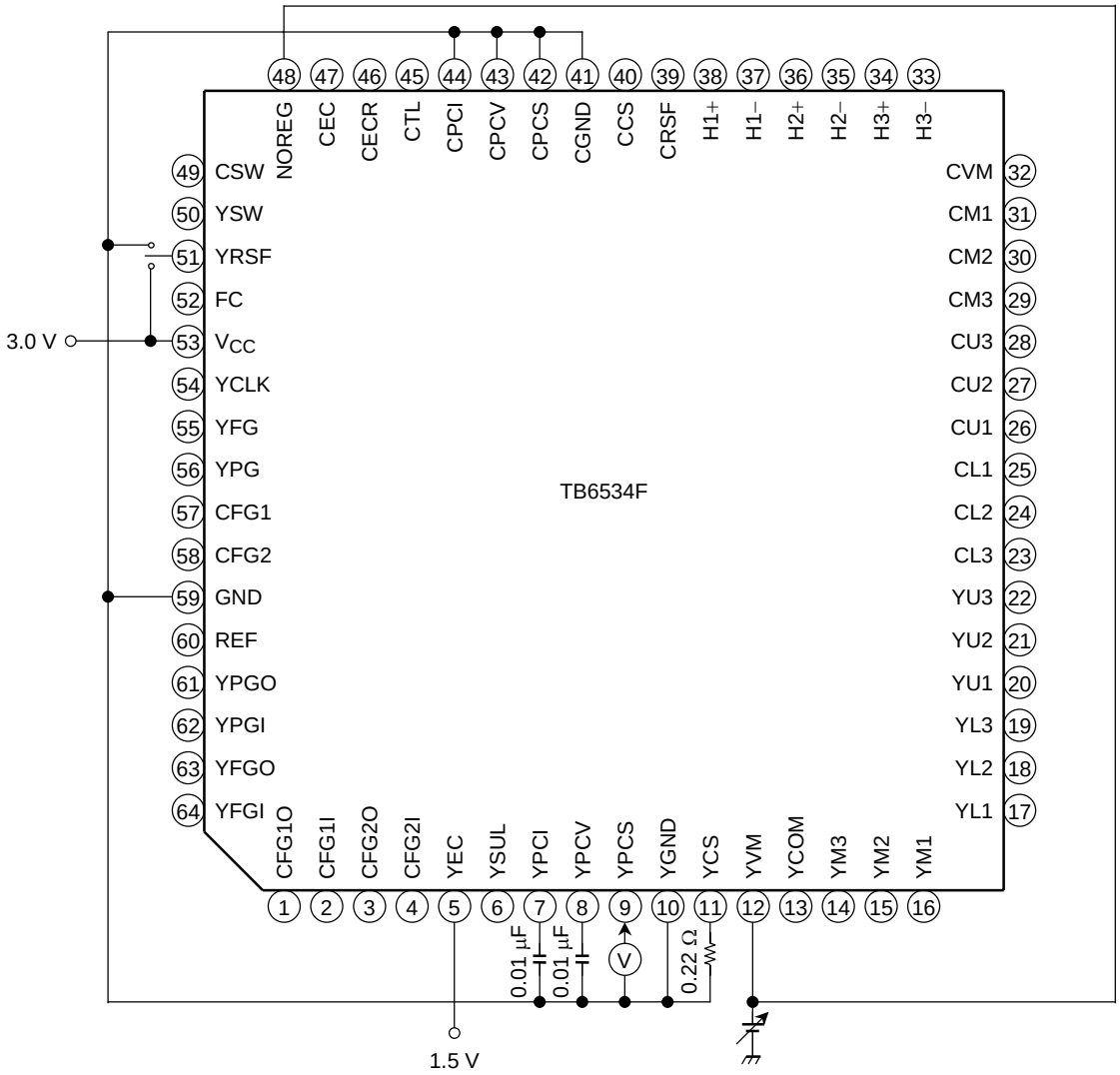
Set FC = 1.7 V, YEC = 0 V, and YM1 = 7.2 V, and measure the current that flows into the pin YSW.

No.30 YSWEC

Apply 10 mA to the pin YSW, and voltage to the pin YEC. Then acquire the characteristics shown on the right.

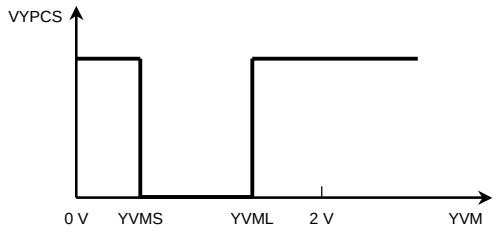


## Test Circuit 10 YVML, YVMS

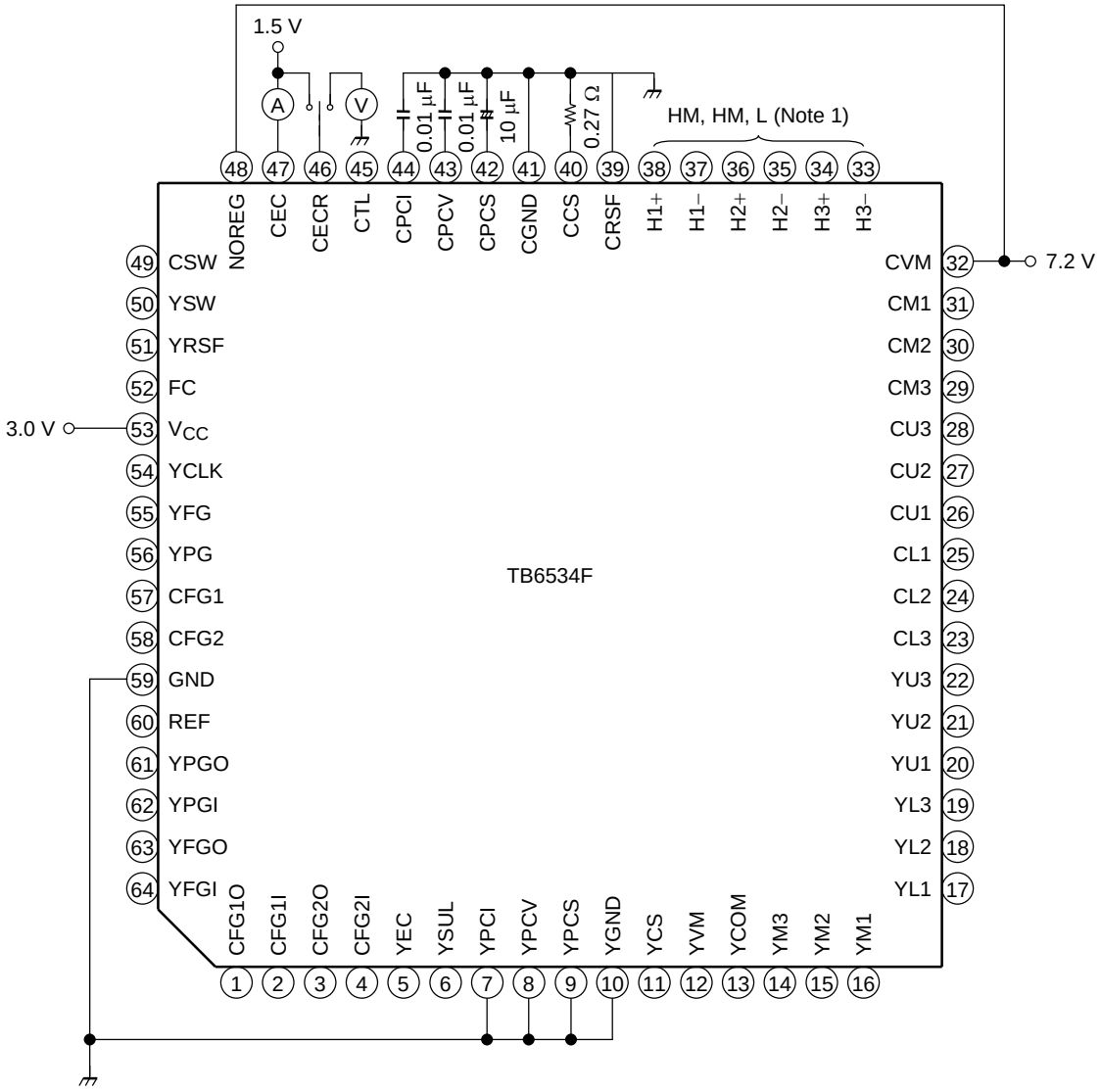



No.28 YVML, No.29 YVMS

Change YVM from 2 V to 0 V, and acquire the characteristics shown below.



## Test Circuit 11 CIEC, CECR




Note 1: Hall input setting

| | L | M | HM | H | Unit |
|---|---|---|---|---|---|
| H1+ | 1.45 | 1.5 | 1.525 | 1.55 | V |
| H1− | 1.5 | 1.5 | 1.5 | 1.5 | V |
| H2+ | 0.65 | 0.7 | 0.725 | 0.75 | V |
| H2− | 0.7 | 0.7 | 0.7 | 0.7 | V |
| H3+ | 1.95 | 2.0 | 2.025 | 2.05 | V |
| H3− | 2.0 | 2.0 | 2.0 | 2.0 | V |

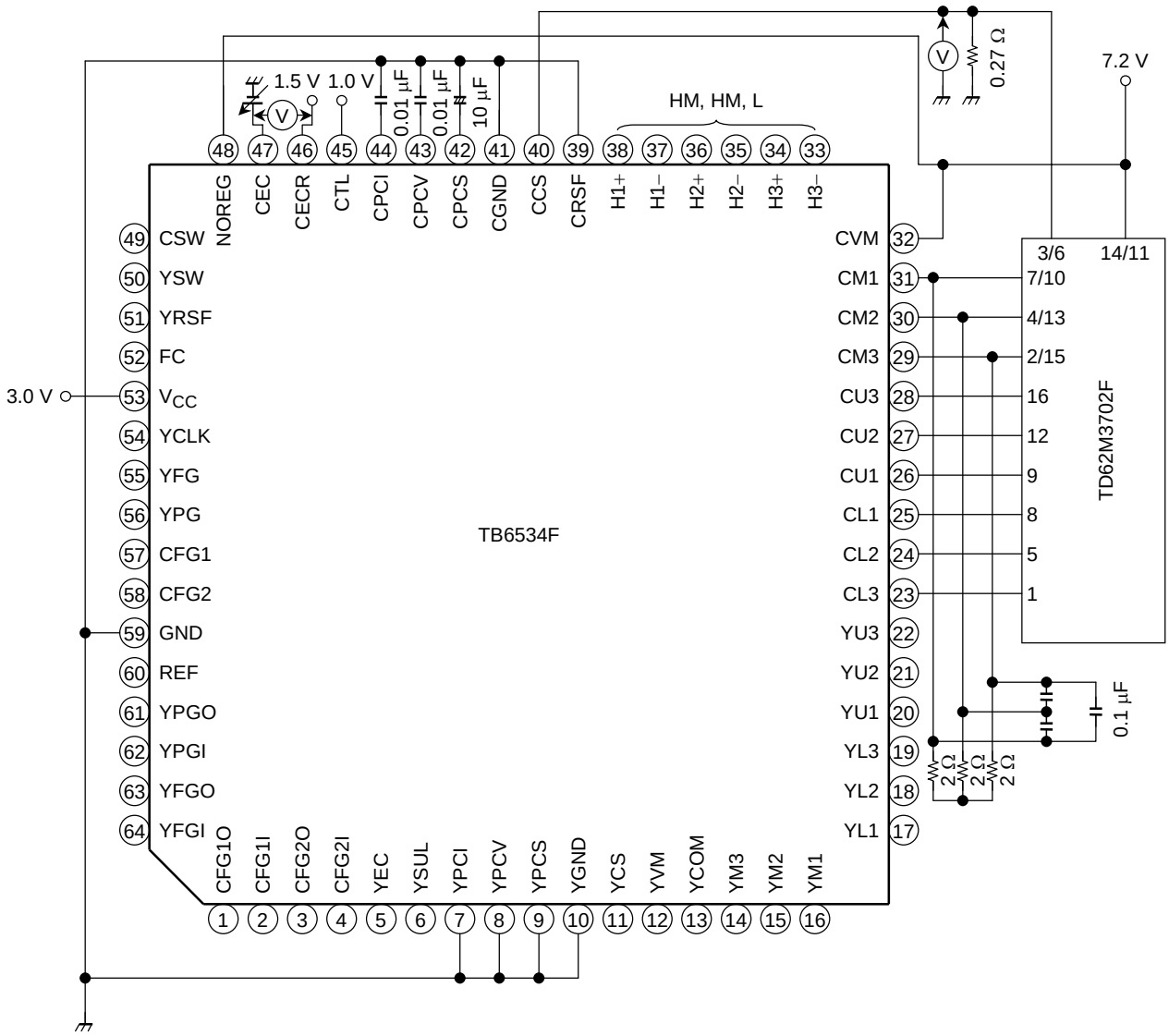
No.31 CIEC

Set CEC = CECR = 1.5 V, and measure the current that flows into the pin CEC.

No.32 CECR

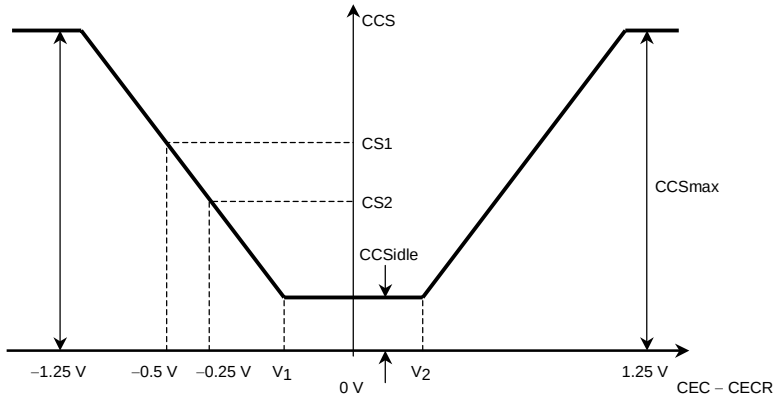
Measure the voltage of the pin CECR.

## Test Circuit 12 CEC, CCSmax, CGio, CCSidle, CECofs, CECdz




No.33 CEC, No.34 CCSmax, No.35 CGio, No.36 CCSidle
No.37 CECofs, No.38 CECdz

Set CTL = 1.0 V and CECR = 1.5 V, change CEC from 0 V to 3.0 V, and measure the potential of the pin CCS to confirm V characteristics.



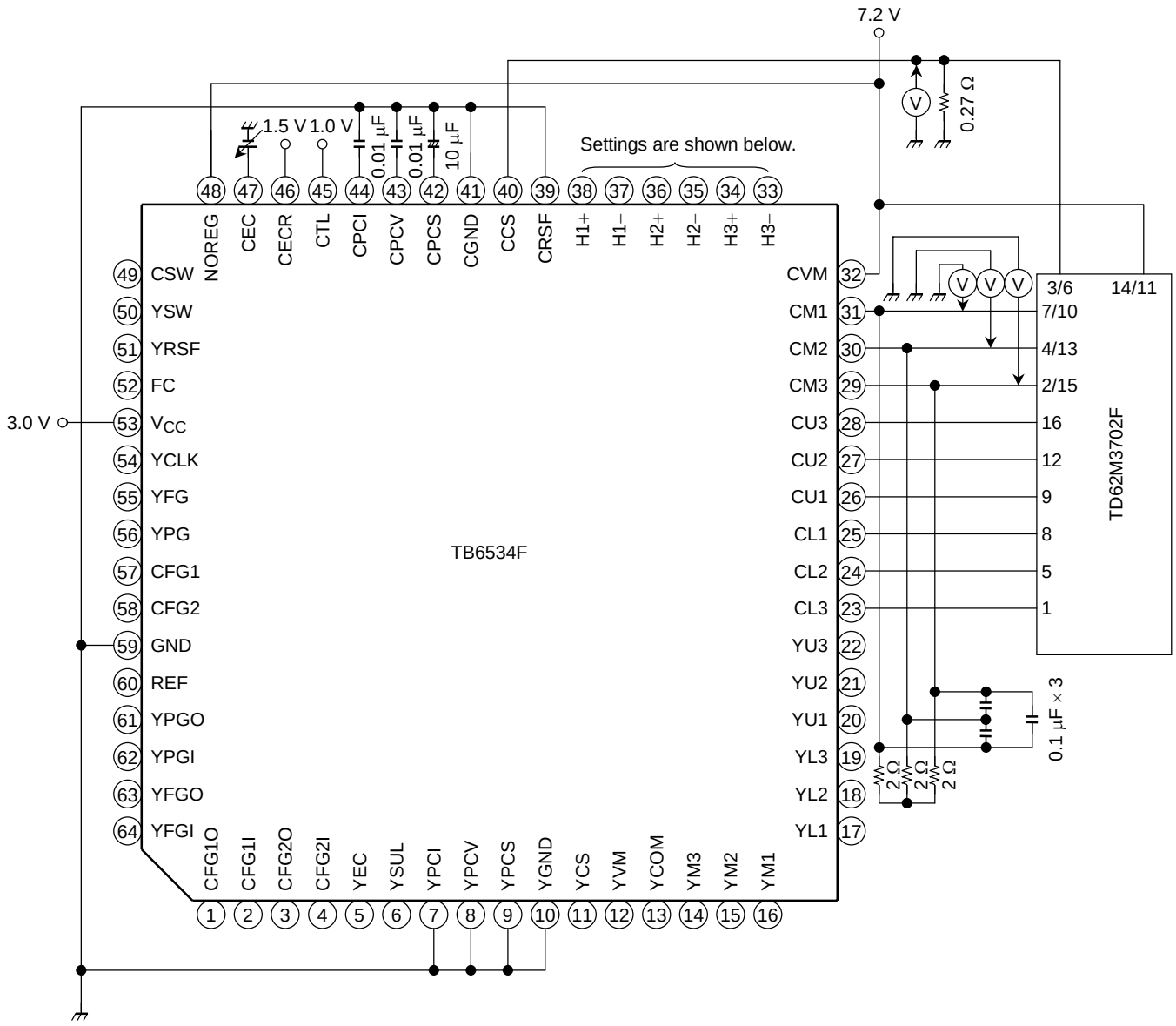

$$CGio = \frac{CS1 - CS2}{0.25\ V}$$

CCSidle : The CS potential within the dead zone.

$$CECofs = \frac{V_1 + V_2}{2}$$

$$CECdz = V_2 - V_1$$

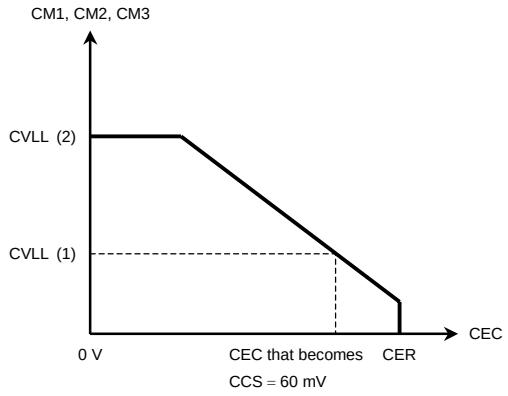
## Test Circuit 13 CVLL (1), CVLL (2)



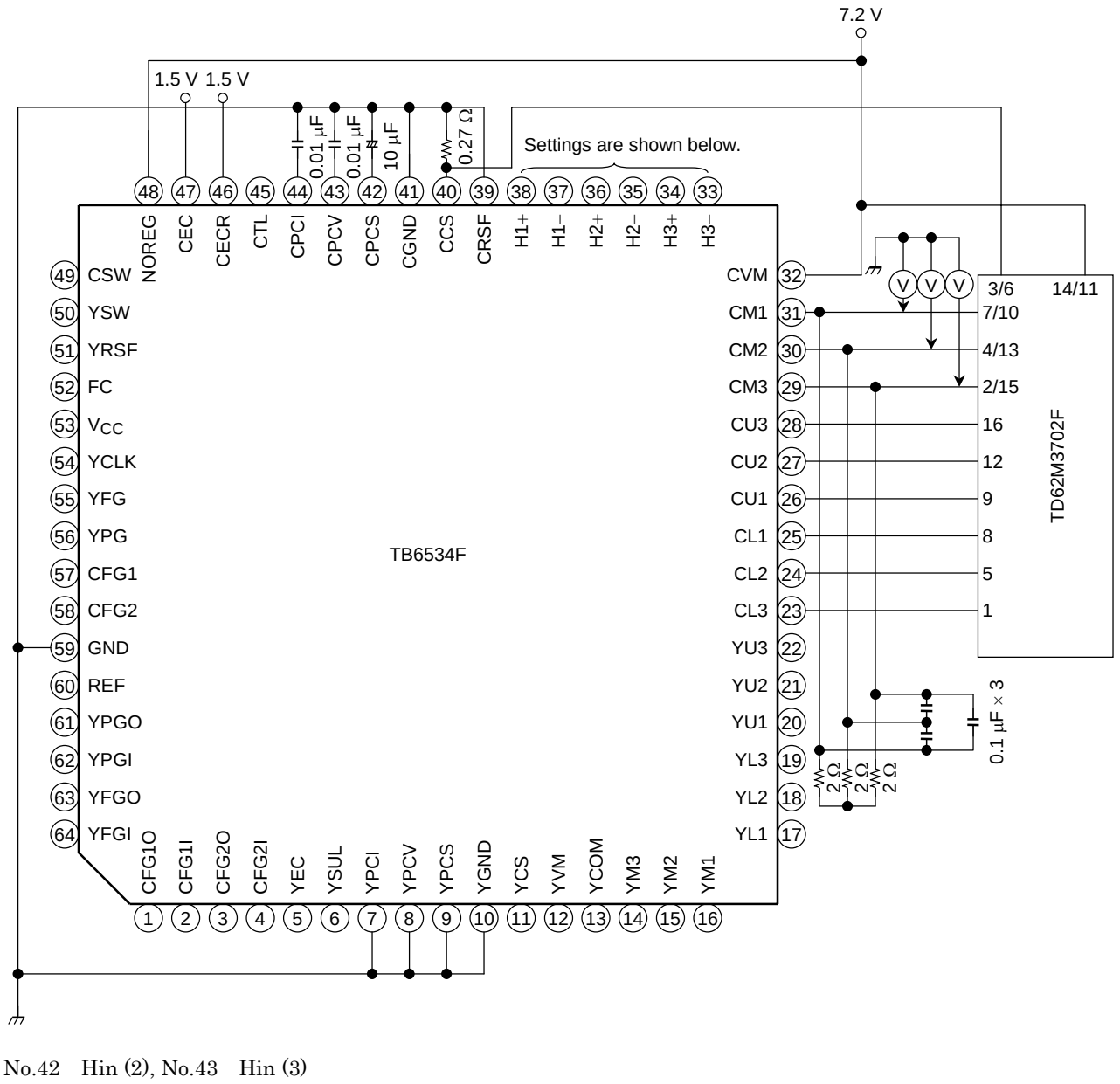

No.39 CVLL (1), No.40 CVLL (2)

CEC = 0 V when perform the setting as shown below, and adjust CEC voltage to CCS = 60 mV.

| | M1 | H2 | H3 | Test Pin |
|---|---|---|---|---|
| Setting 1 | H | L | M | CM1 |
| Setting 2 | M | H | L | CM2 |
| Setting 3 | L | M | H | CM3 |



## Test Circuit 14 Hin (1), Hin (2), Hin (3)

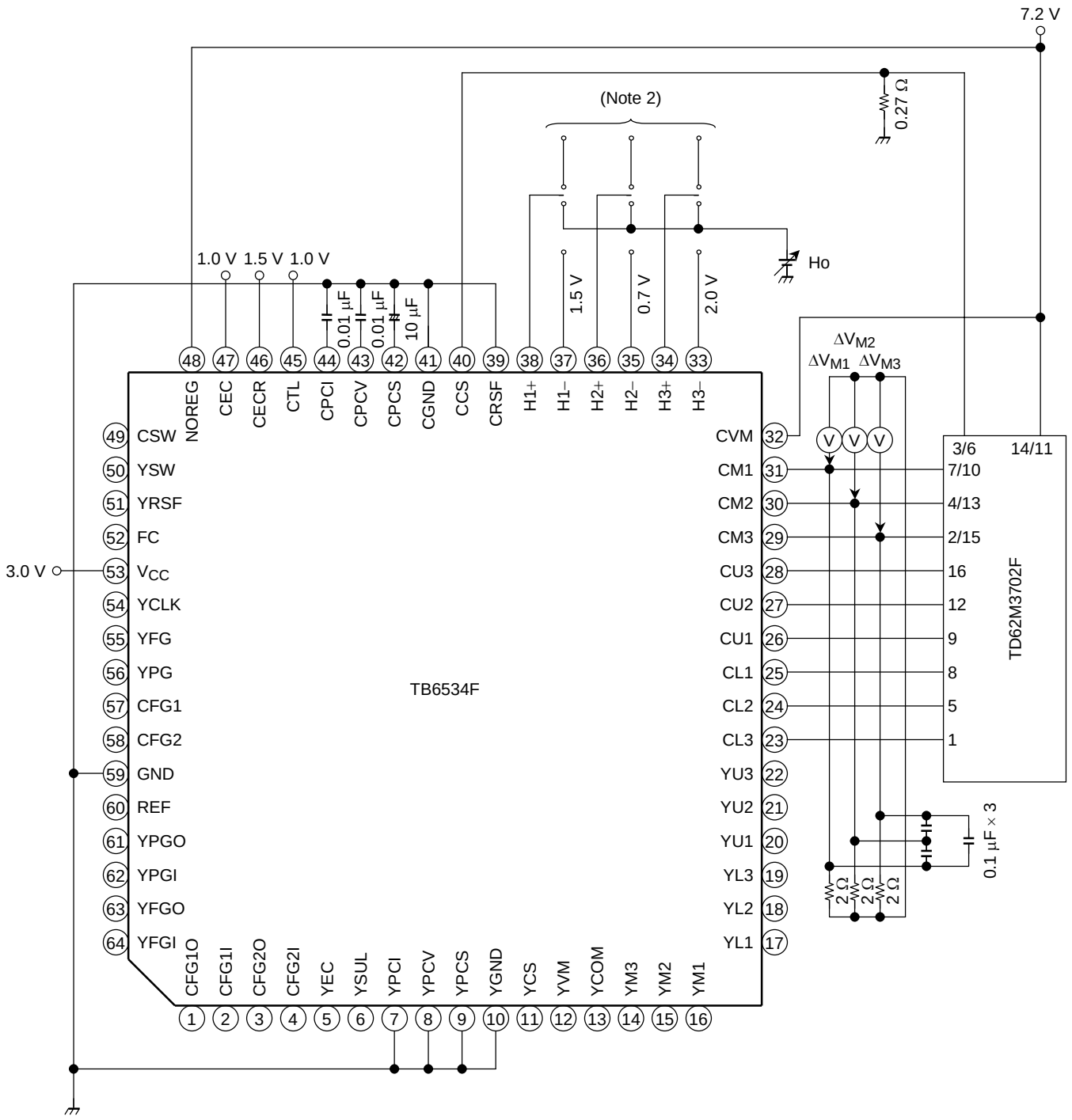



No.41 Hin (1), No.42 Hin (2), No.43 Hin (3)

Perform the setting as shown below, and measure the operating range of hall amp that does change in accordance with the changes in the Hin.

| | H1+ | H1– | H2+ | H2– | H3+ | H3– |
|---|---|---|---|---|---|---|
| Setting 1 | Hin | Hin | HM | M | L | M |
| Setting 2 | L | M | Hin | Hin | HM | M |
| Setting 3 | HM | M | L | M | Hin | Hin |

## Test Circuit 15 Hofs



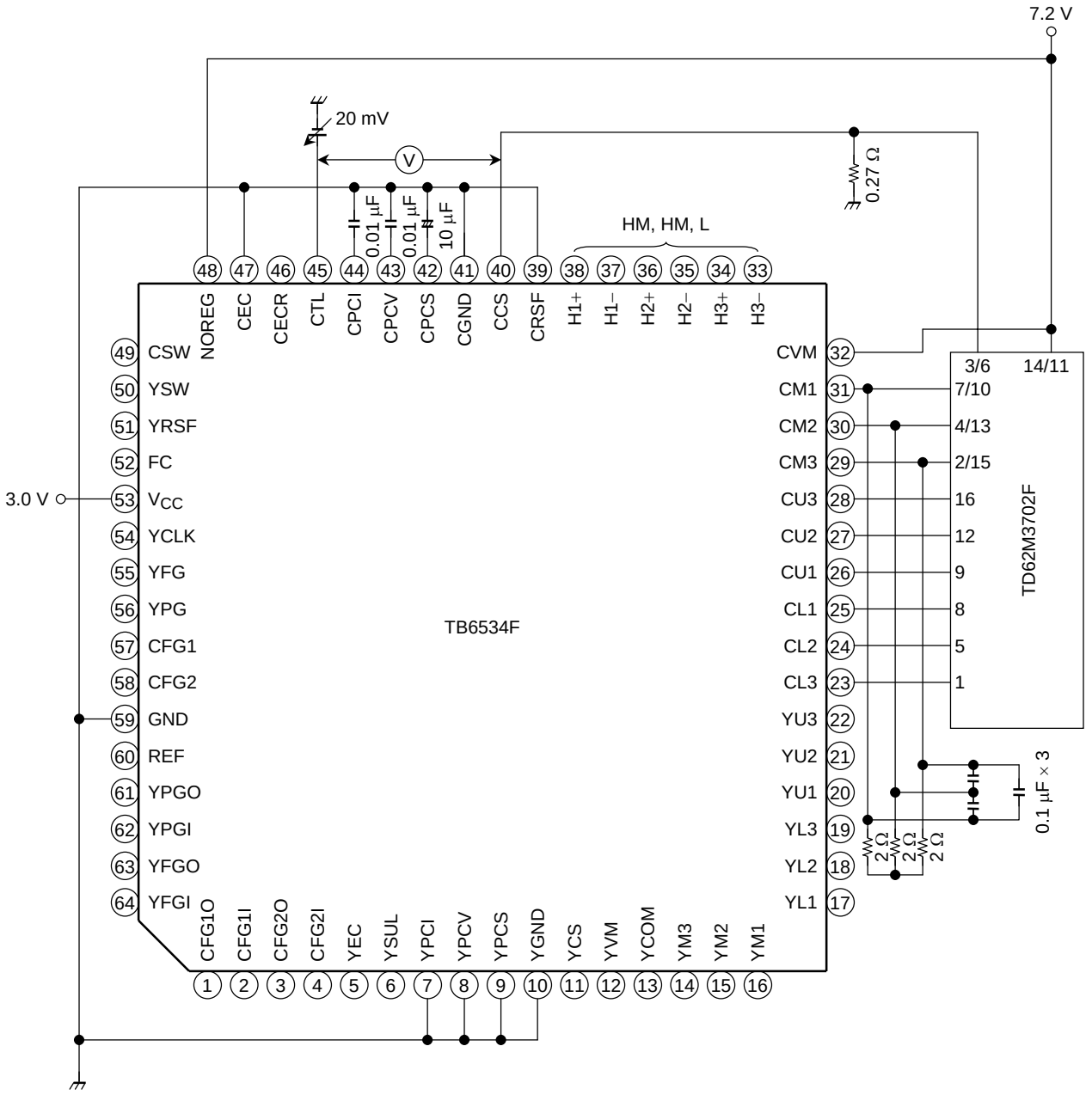

No.44 Hofs

Perform the setting as shown below, and measure the hall element input conversion offset.

| | H1+ | H2+ | H3+ | Offset Measurement |
|---|---|---|---|---|
| Setting 1 | Ho | HM | L | $V_{Ho}$ − 1.525 V when $\Delta V_{M1} = 0$ |
| Setting 2 | L | Ho | HM | $V_{Ho}$ − 0.725 V when $\Delta V_{M2} = 0$ |
| Setting 3 | HM | L | Ho | $V_{Ho}$ − 2.025 V when $\Delta V_{M3} = 0$ |

Note 2: H1− = 1.5 V, H2− = 0.7 V, H3− = 2.0 V fixed. (refer to the page of test circuit 11.)

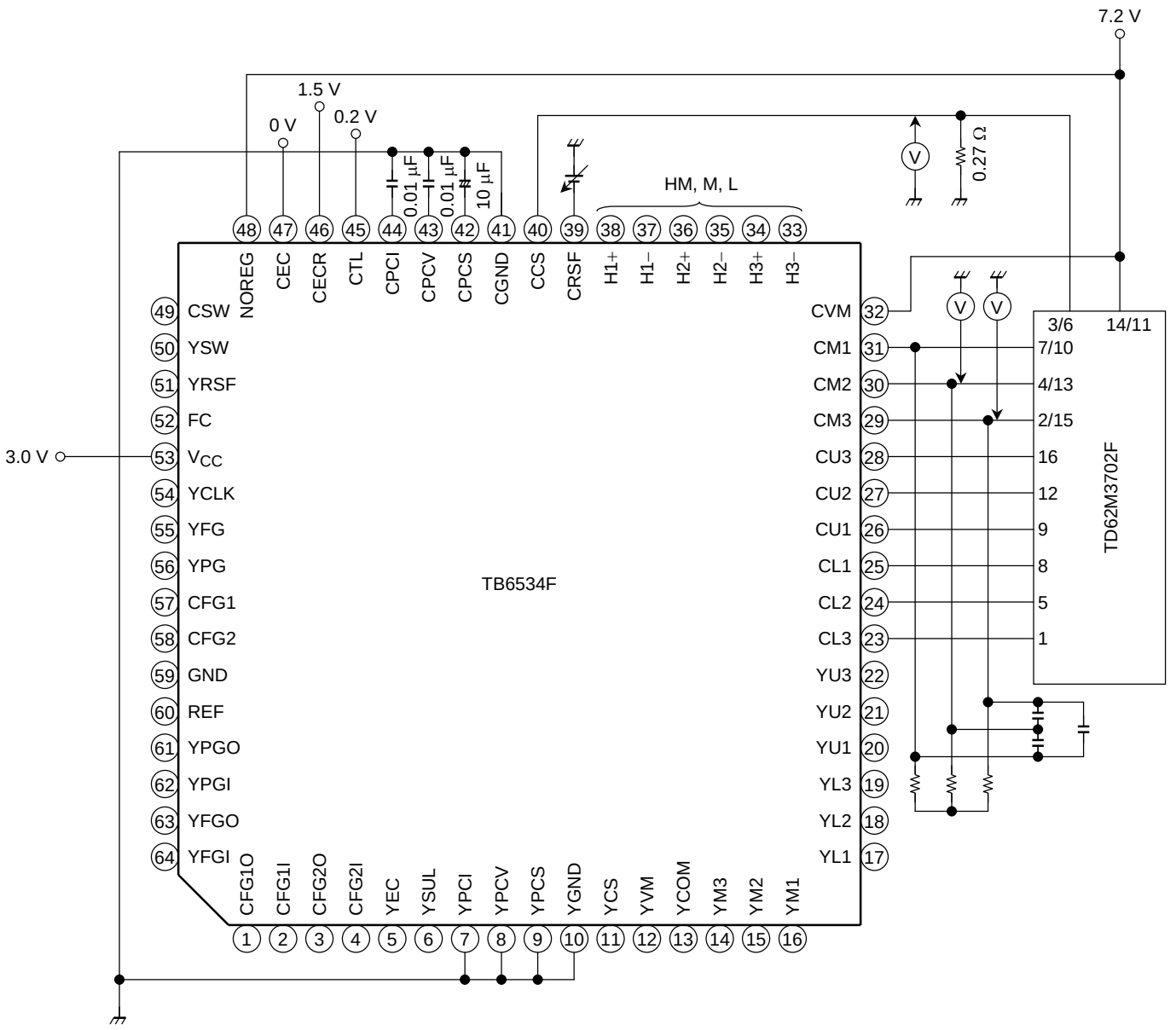
**Test Circuit 16 TLofs**




No.45 TLofs

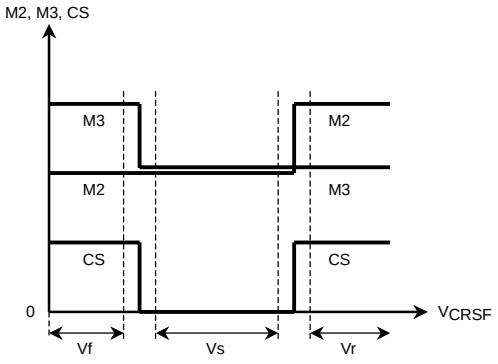
Measure the potential difference between the pin CTL and the pin CCS (CTL – CCS) when CTL = 20 mV.

**Test Circuit 17 CVf, CVs, CVr**

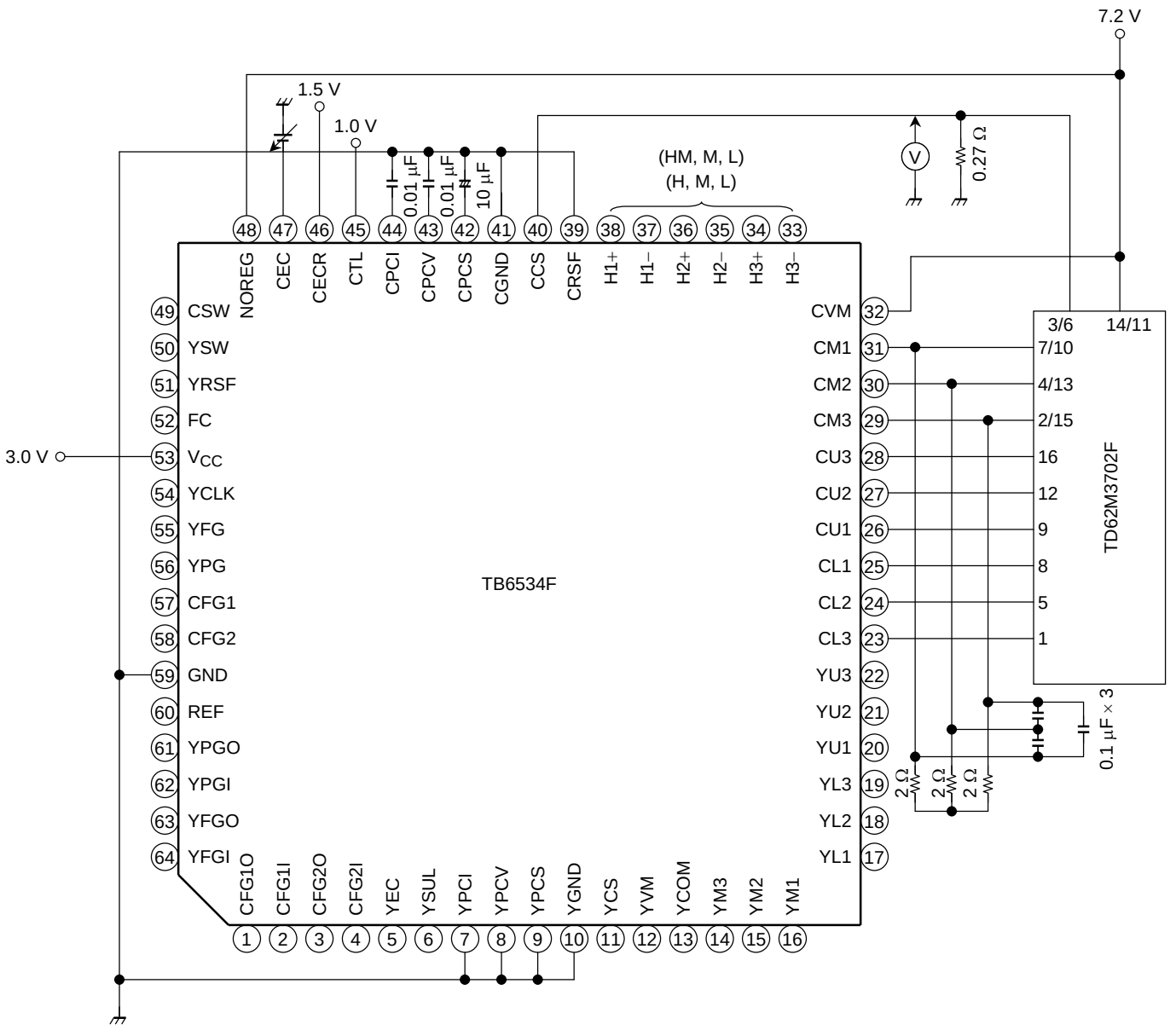



No.46 CVf, No.47 CVs, No.48 CVr

Change CRSF from 0 V to 3.0 V, acquire the characteristics as shown below, and measure the threshold voltage.



**Test Circuit 18 R**

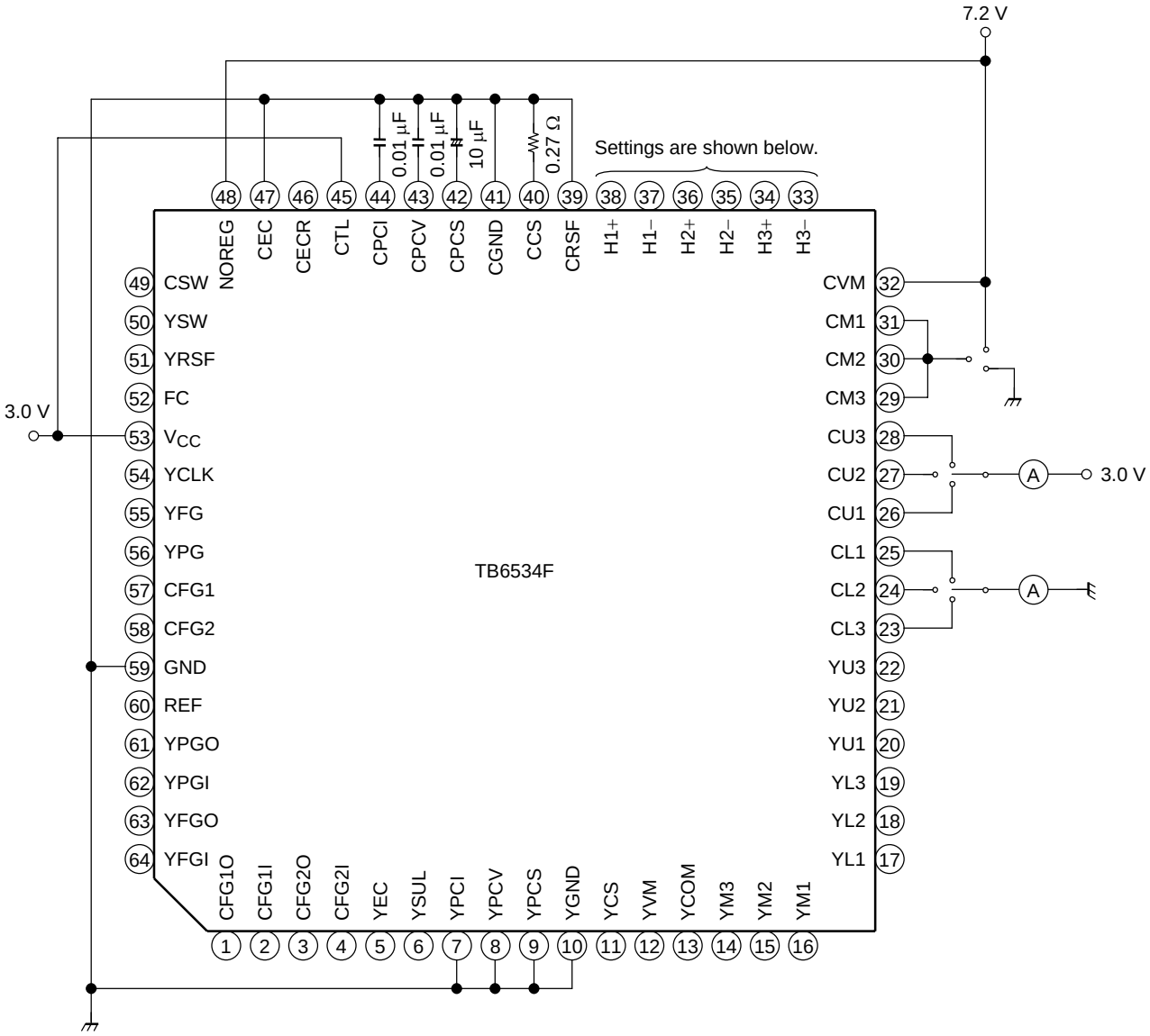



No.49 R

Adjust the CEC voltage so that CCS becomes 60 mV when H1+/–: “HM”, H2+/–: “HM”, and H3+/–: “L”. Then measure CCS potential (CSH) when H1+/–: “H”, H2+/–: “H”, and H3+/–: “L”.

$$R = \frac{CSH - 60\ mV}{60\ mV}$$

## Test Circuit 19 CIU, CIL

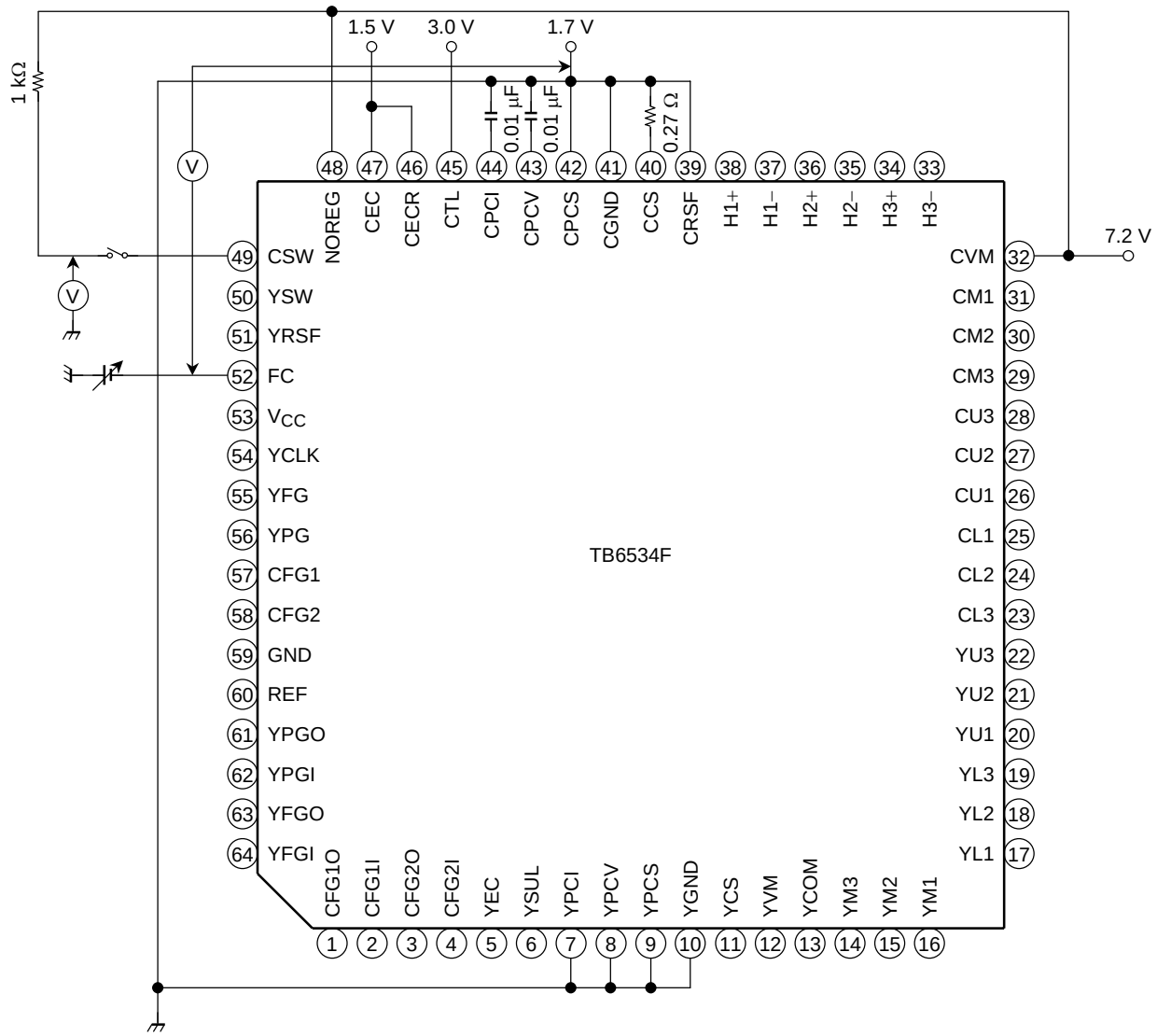



No.50 CIU, No.51 CIL

Perform the setting as shown below, measure the current to the pins CU1, CU2, CU3, CL1, CL2, and CL3.

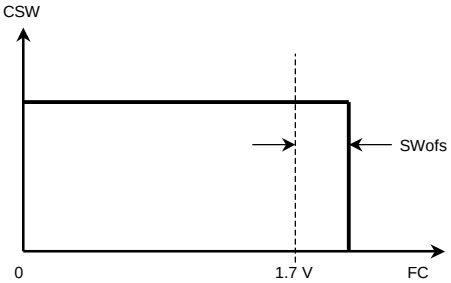
| | H1 | H2 | H3 | M1, M2, M3 | Test Pin |
|---|---|---|---|---|---|
| Setting 1 | L | H | M | GND | CU1 |
| Setting 2 | M | L | H | GND | CU2 |
| Setting 3 | H | M | H | GND | CU3 |
| Setting 4 | H | L | M | $V_M$ | CU1 |
| Setting 5 | M | H | L | $V_M$ | CU2 |
| Setting 6 | L | M | H | $V_M$ | CU3 |

## Test Circuit 20 CSWofs, IREG




No.52 CSWofs

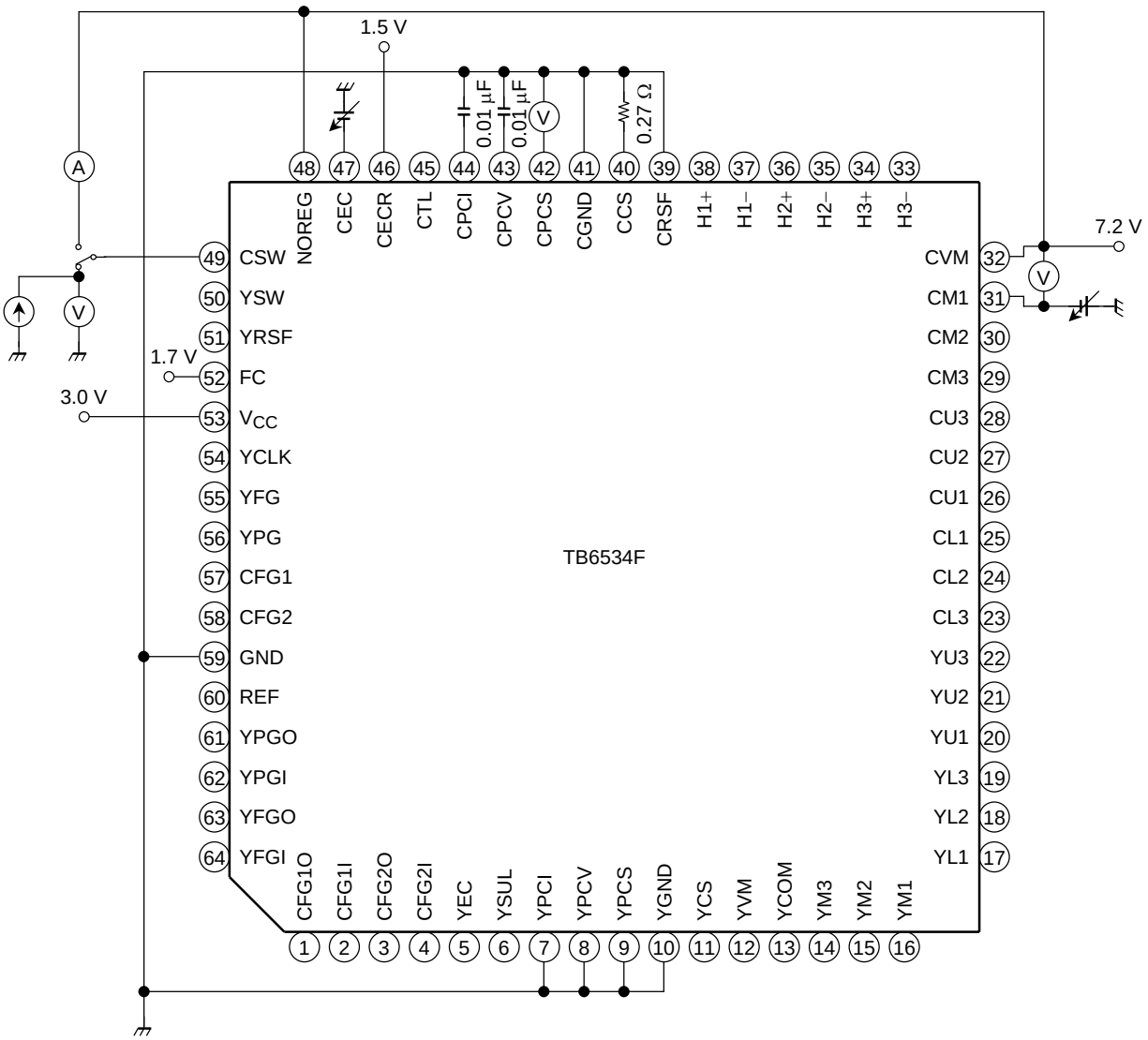
Set CPCS = 1.7 V, change FC from 0 V to 3.0 V, and measure the potential difference between the pins FC and CPCS (FC – CPCS) when CSW becomes Low from High.




No.63 IREG

Measure the current when CVM = 7.2 V, FC = 1.8 V, the pin CSW is open, and 7.2 V is applied from the pin NOREG.

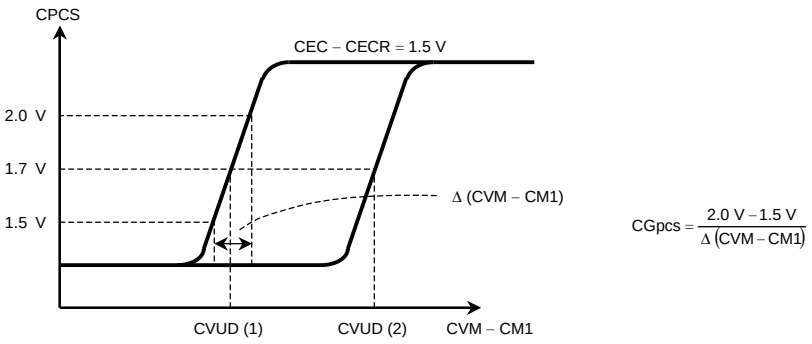
## Test Circuit 21 CGPCS, CVUD (1), CVUD (2), CISWB, CSWEC




No.53 CGPCS, No.54 CVUD (1), No.55 CVUD (2)

Set CEC = 0 V, change CM1 from 7.2 V to 6 V, and measure the potential difference between the pins CVM and CM1 (CVM – CM1).

Set CEC = CECR = 1.5 V, follow the steps described above to acquire the characteristic as shown below.

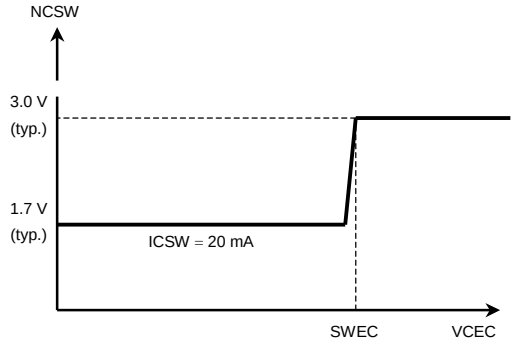


No.56 CISWB

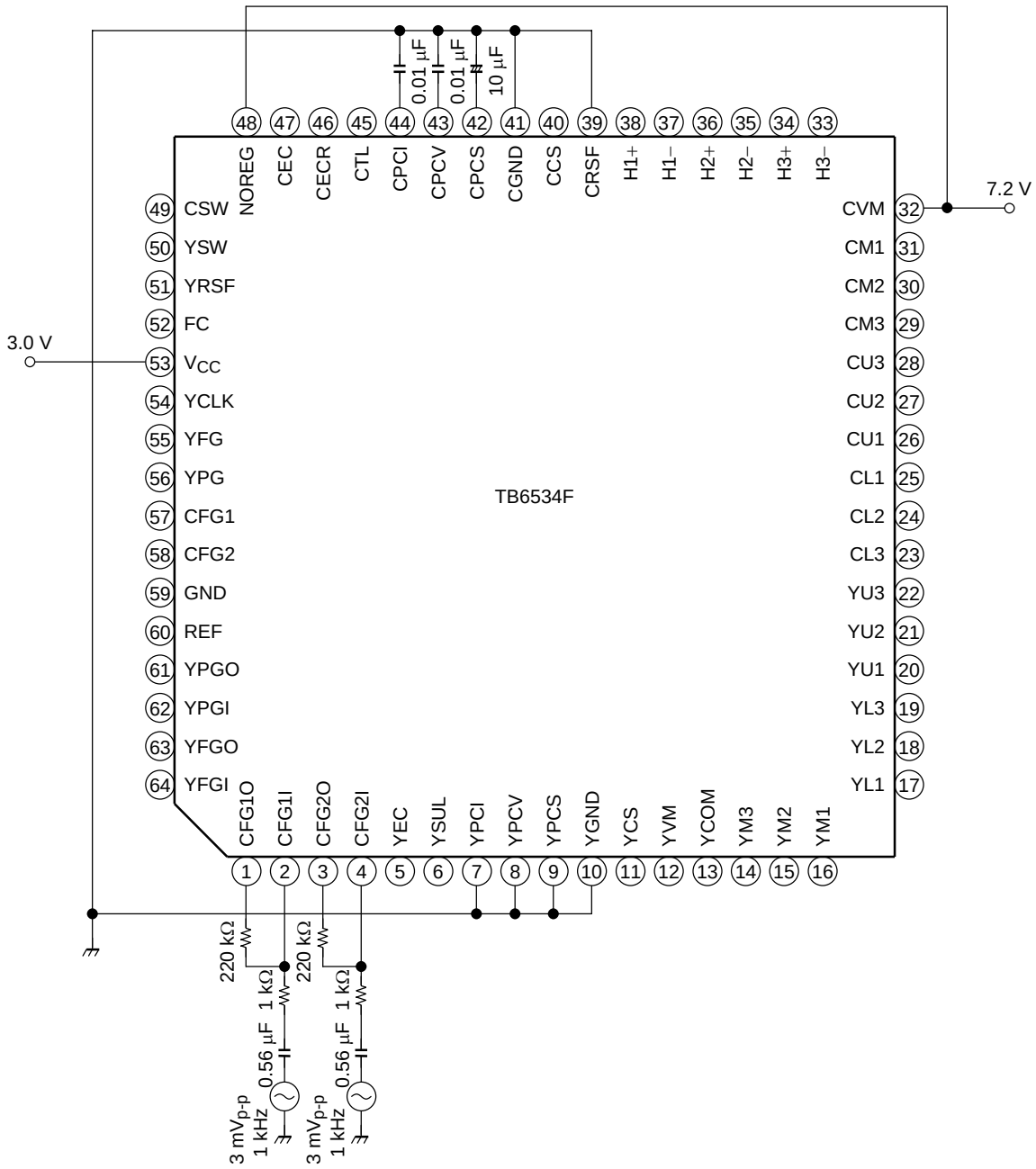
Set FC = 1.7 V, CEC = 0 V, and CM1 = 7.2 V, and measure the current to the pin CSW.

No.62 CSWEC

Apply 10 mA to the pin CSW, and apply voltage to pin CEC to acquire the characteristic as shown below.



## Test Circuit 22 CGFG, CFGH, CFGL

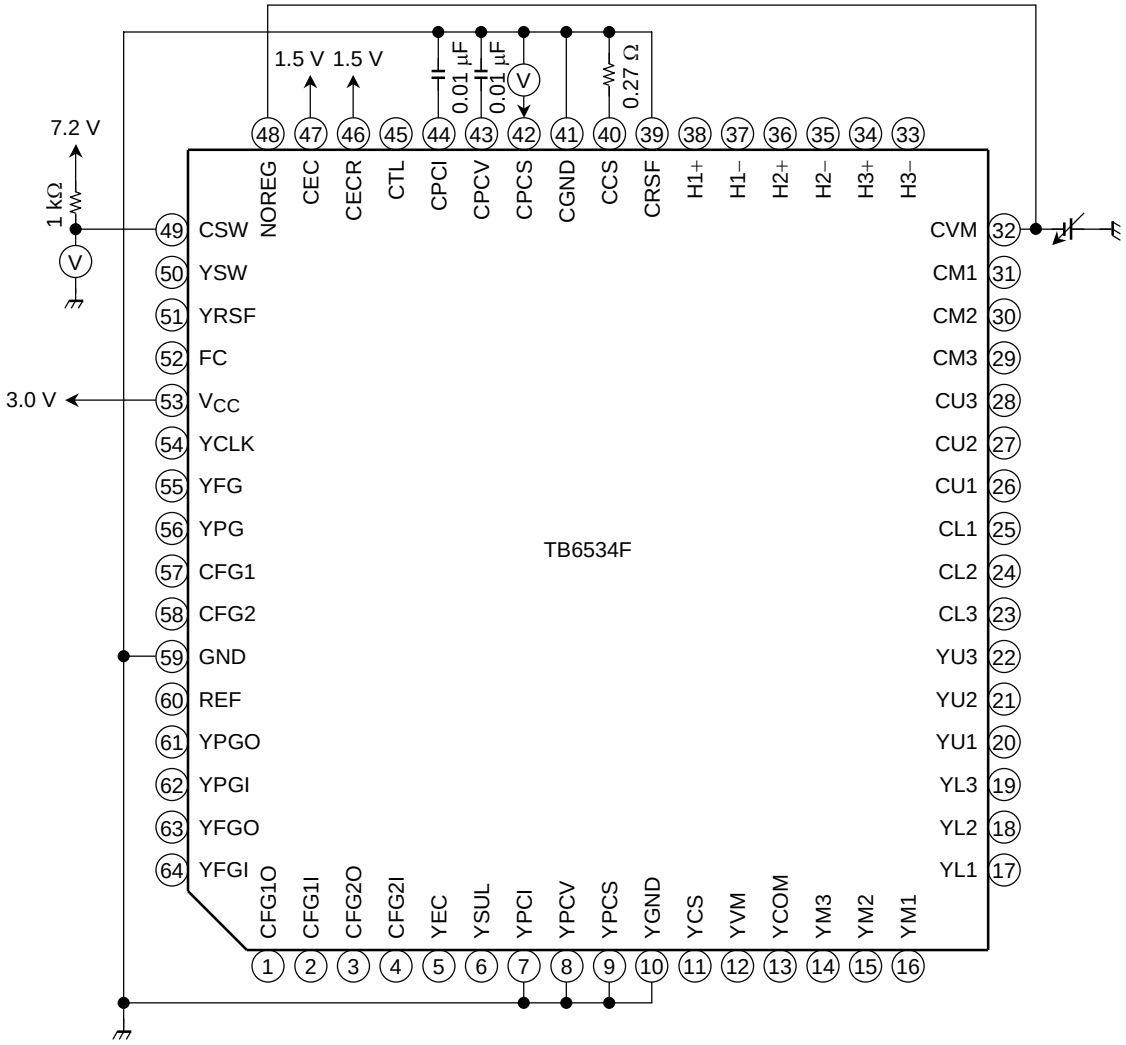



No.57 CGFG, No.58 CFGH, No.59 CFGL

Set CFGout = Vo, and measure Vo when $V_{in}$ = 3 $mV_{p\text{-}p}$, 1 kHz to acquire CGFG = 20 λog $\frac{Vo}{V_{in}}$.

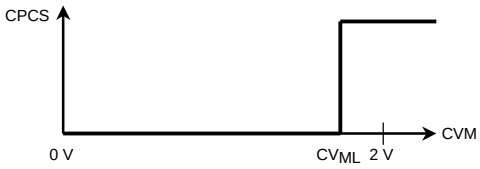
Also, acquire the characteristic as shown below, and measure the potential of High and Low levels of the pin CFG output waveform.

## Test Circuit 23 $CV_{ML}$, $CV_{MS}$



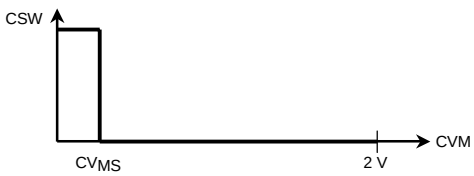

No.60 $CV_{ML}$

Change CVM from 2 V to 0 V, and acquire the characteristics as shown below.

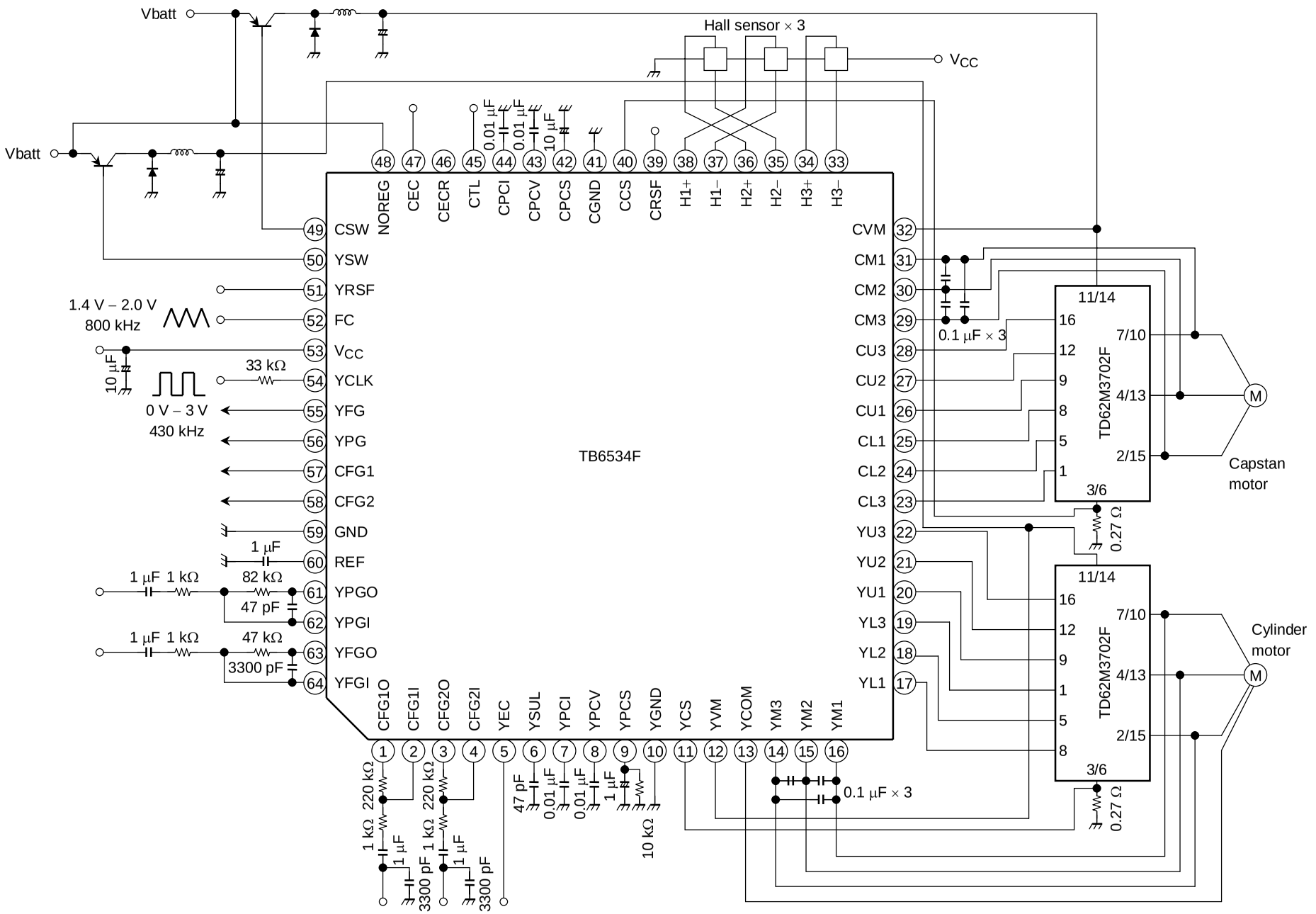



No.61 $CV_{MS}$

Change CVM from 2 V to 0 V, and acquire the characteristics as shown below.

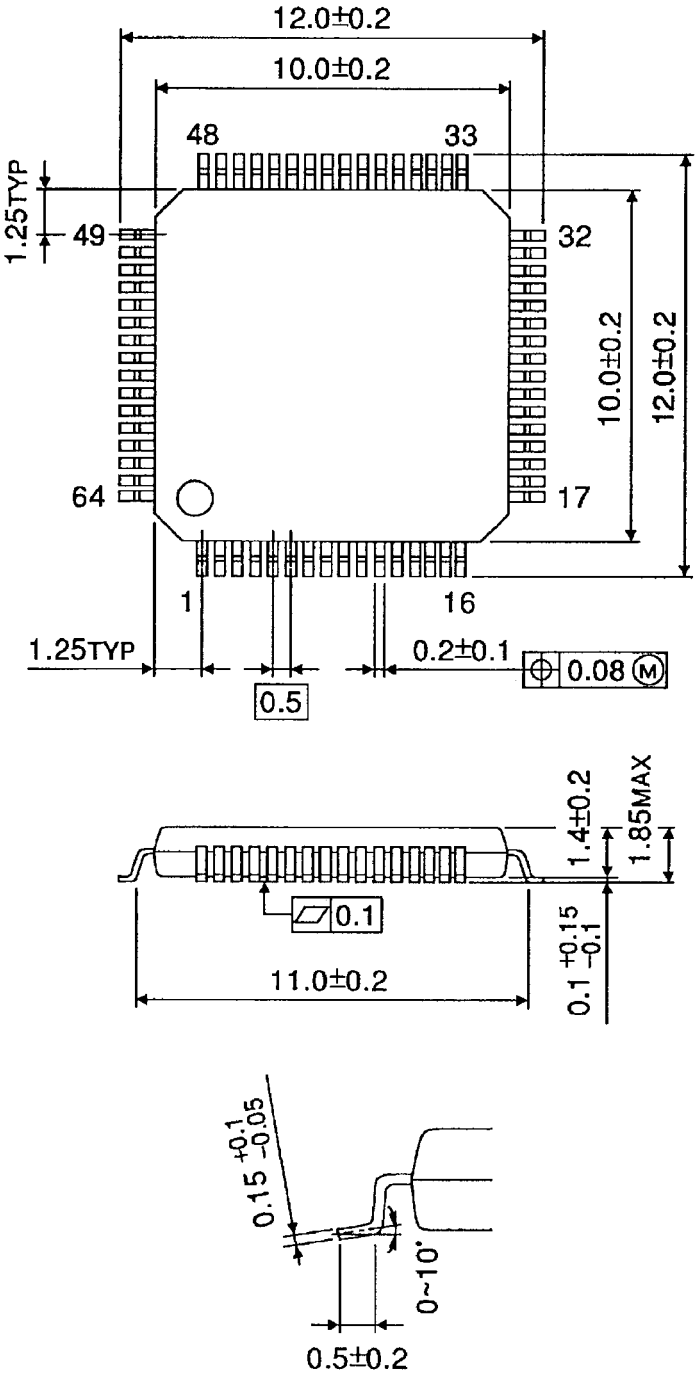


## Typical Application Diagram



## Package Dimensions

LQFP64-P-1010-0.50A Unit : mm




Weight: 0.34 g (typ.)

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