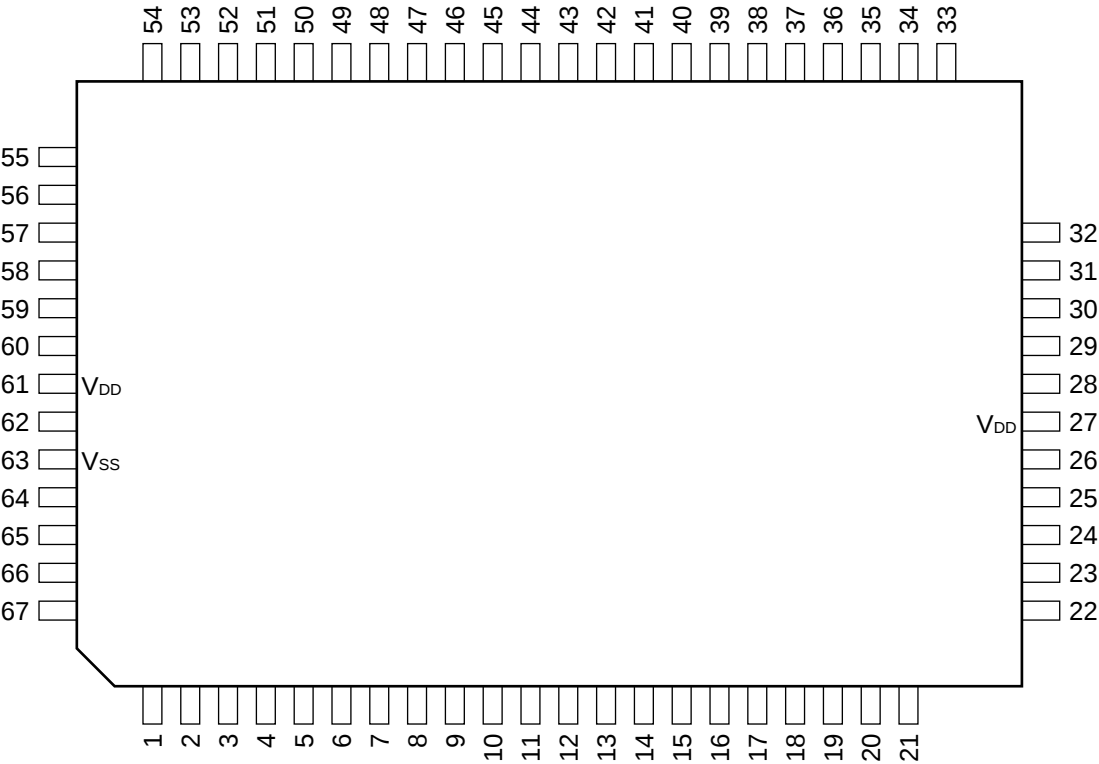
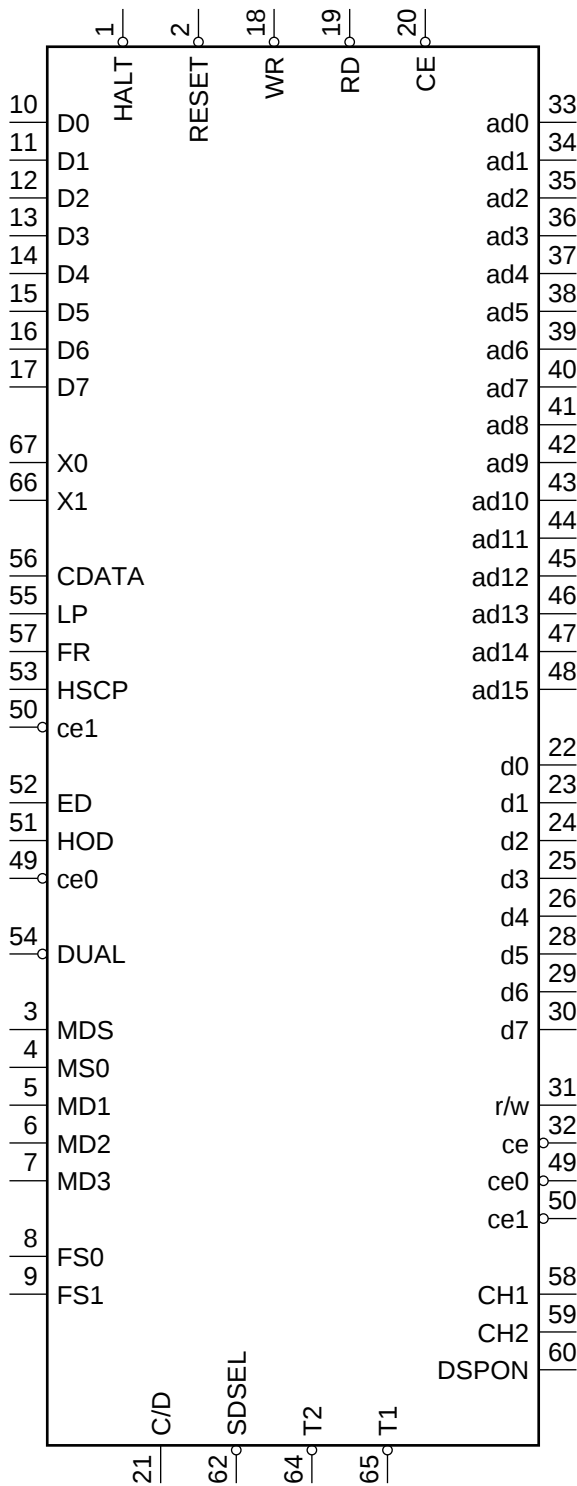

C-MOS DOT MATRIX LCD CONTROLLER

- TOP VIEW -





INPUT

C/D	; COMMAND/DATA SELECT
CE	; CHIP ENABLE
DUAL	; DUAL LCD SELECT
FS0, FS1	; FONT SELECT
HALT	; HALT
MDS	; DISPLAY COLUMN SELECT
MD0-3	; DISPLAY COLUMN SELECT
RD	; READ
RESET	; RESET
SDSEL	; INPUT DATA SELECT (NORMAL/DUAL)
T1, T2	; TEST1, 2
WR	; WRITE
X1	; CRYSTAL OSCILLATOR

OUTPUT

ad0-ad15	; ADDRESS BUS
CDATA	; SYNC
ce, ce0, ce1	; MEMORY CHIP ENABLE
CH1, CH2	; CHECK1, 2
DSPON	; EXTERNAL DC/DC CONVERTER CONTROL
ED	; SERIAL DATA FOR LCD
FR	; FRAME SIGNAL
HOD	; SERIAL DATA FOR UPPER LCD
HSCP	; SHIFT CLOCK PULSE
LP	; LATCH PULSE/CLOCK PULSE
r/w	; MEMORY READ/WRITE
X0	; CRYSTAL OSCILLATOR

INPUT/OUTPUT

D0-D7	; DATA BUS
d0-d7	; MEMORY DATA BUS

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I	$\overline{\text{HALT}}$	18	I	$\overline{\text{WR}}$	35	O	ad2	52	O	ED
2	I	$\overline{\text{RESET}}$	19	I	$\overline{\text{RD}}$	36	O	ad3	53	O	HSCP
3	I	MDS	20	I	$\overline{\text{CE}}$	37	O	ad4	54	I	$\overline{\text{DUAL}}$
4	I	MD0	21	I	C/D	38	O	ad5	55	O	LP
5	I	MD1	22	I/O	d0	39	O	ad6	56	O	CDATA
6	I	MD2	23	I/O	d1	40	O	ad7	57	O	FR
7	I	MD3	24	I/O	d2	41	O	ad8	58	O	CH1
8	I	FS0	25	I/O	d3	42	O	ad9	59	O	CH2
9	I	FS1	26	I/O	d4	43	O	ad10	60	O	DSPON
10	I/O	D0	27	–	V _{DD}	44	O	ad11	61	–	V _{DD}
11	I/O	D1	28	I/O	d5	45	O	ad12	62	I	$\overline{\text{SDSEL}}$
12	I/O	D2	29	I/O	d6	46	O	ad13	63	–	V _{ss}
13	I/O	D3	30	I/O	d7	47	O	ad14	64	I	$\overline{\text{T2}}$
14	I/O	D4	31	O	r/w	48	O	ad15	65	I	$\overline{\text{T1}}$
15	I/O	D5	32	O	ce	49	O	ce0	66	I	X1
16	I/O	D6	33	O	ad0	50	O	ce1	67	O	X0
17	I/O	D7	34	O	ad1	51	O	HOD	–	–	–

