Preliminary
SiI859 / SiI861 Data Sheet
Silicon Image Confidential Information

Silicon Image, Inc.

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1. Feature Review

- **Digital Visual Controller Architecture**
  - Consistent highest quality visual experience
  - Enables easy development of DVI compliant, pure digital LCD monitors
  - Eliminates analog image processing artifacts ("Pixel Dust")
  - Cost effective, single-chip solution lowers cost, increases reliability and saves board space to make product design easier
  - Easy firmware development – register compatible with SiI851
- **PixelPrecisionÔ Scaling Algorithm**
  - Finite impulse response filter provides high image quality for both text and graphics
  - Frame rate preservation locks outgoing frame rate with incoming frame rate to prevent temporal artifacts such as jutter (objects moving in abrupt steps across the screen) and tearing (the screen splits from one image to the next along a horizontal line).
  - Automatically upscales any lower resolution input to any output resolution up to UXGA without the use of a microcontroller
  - Automatically downscales any resolution up to UXGA to the output resoultion
  - Auto-detect functionality ensures rapid scaling of incoming images
- **Color Management**
  - Dithering engine to allow 24-bit color to be shown on 18-bit TFT panels
  - Two fully programmable look-up gamma tables are provided to allow adjustment of gamma, color temperature, color brightness, and contrast
- **Inputs**
  - PanelLink® Digital for guaranteed compatibility with DVI specification 1.0
  - Parallel 24-bit RGB digital input (861 only)
- **Outputs**
  - Flexible panel interface supports any panel interface up to 1600 horizontal pixels
  - Frequency range: 25MHz to 125MHz
  - Output data timing may be staggered in 2-pixel/clock mode to reduce ground bounce
  - 24-bit one-pixel/clock or 48-bit two-pixel/clock output for true color (16.7 million) support
  - Integrated LVDS transmitter (861 only)
- **On Screen Display (OSD)**
  - Fully programmable OSD support allows for localized messaging for specific regions and market segments
  - Character mapped OSD: RAM based, 16 color support per character with transparency. Up to 1024 characters can be displayed
  - Built-in loss-of-sync and out-of-range functions
  - Built in OSD mode that doesn't require a micro-controller for lower cost
- **Internal Clock Multiplier**
  - 5 X multiplier, allows use of lower cost, lower frequency crystal or oscillator
  - Crystal oscillator circuit (861 only)
- **Power Management**
  - Supports DVI power management functionality
- **High-bandwidth DigitalContent Protection**
  - PanelLink input supporting DVI content protection scheme (861 only)
- **Automatic PWM Control**
  - Pushbutton input monitoring adjusts PWM output to control backlight brightness and volume without microcontroller (861 only)

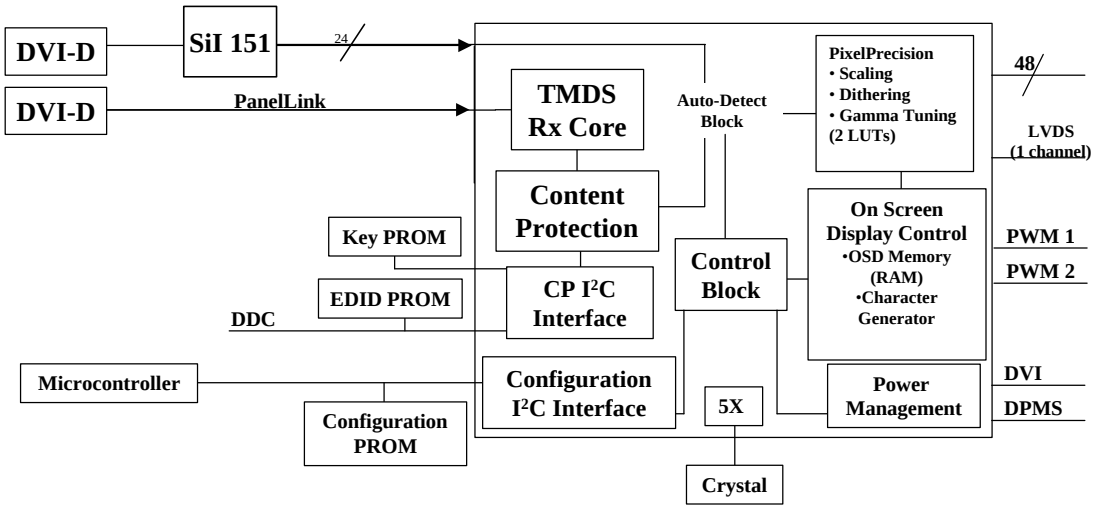


Figure 1. SiI861 Block Diagram

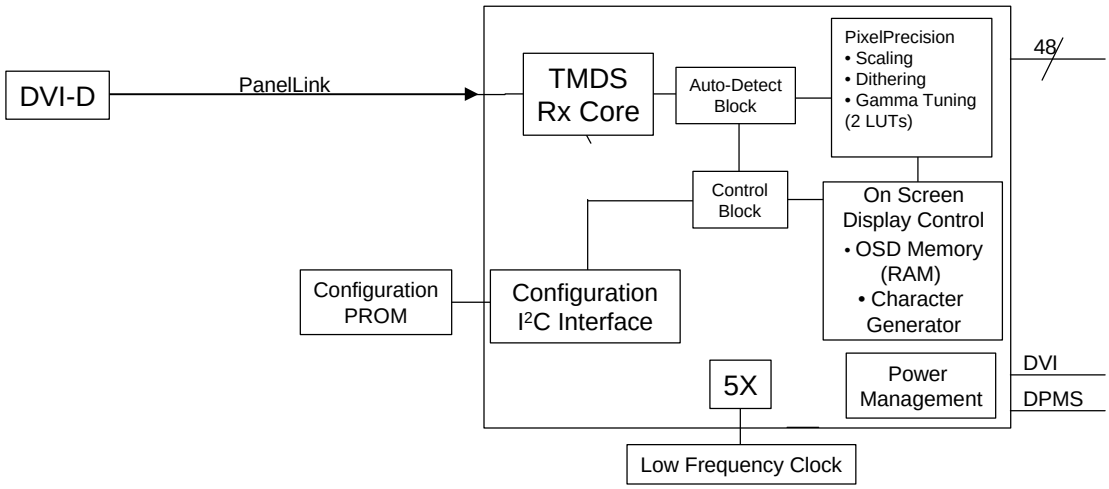


Figure 2. SiI859 Block Diagram

2. Pin Diagrams

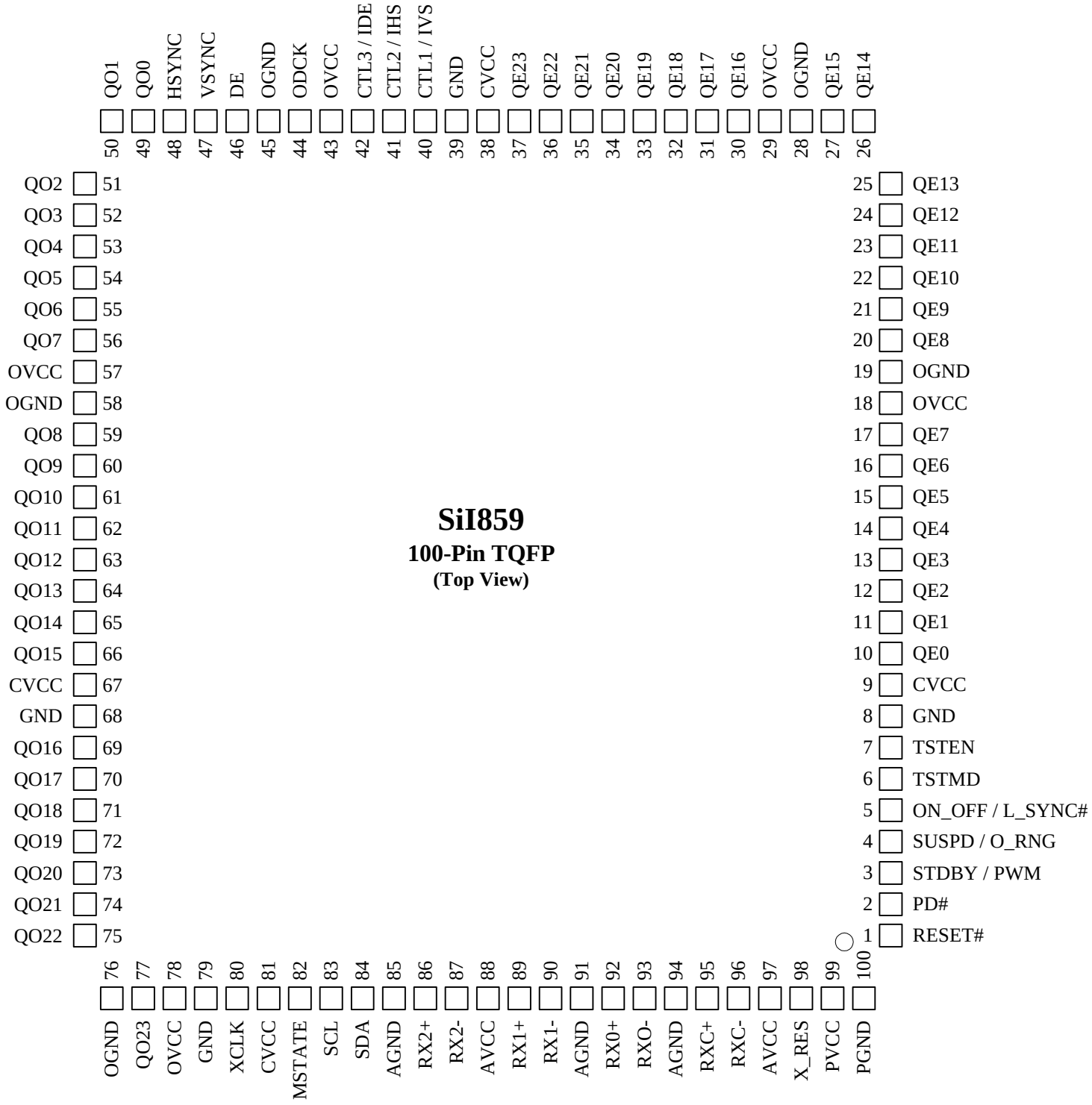


Figure 3. SiI859 Pin Diagram

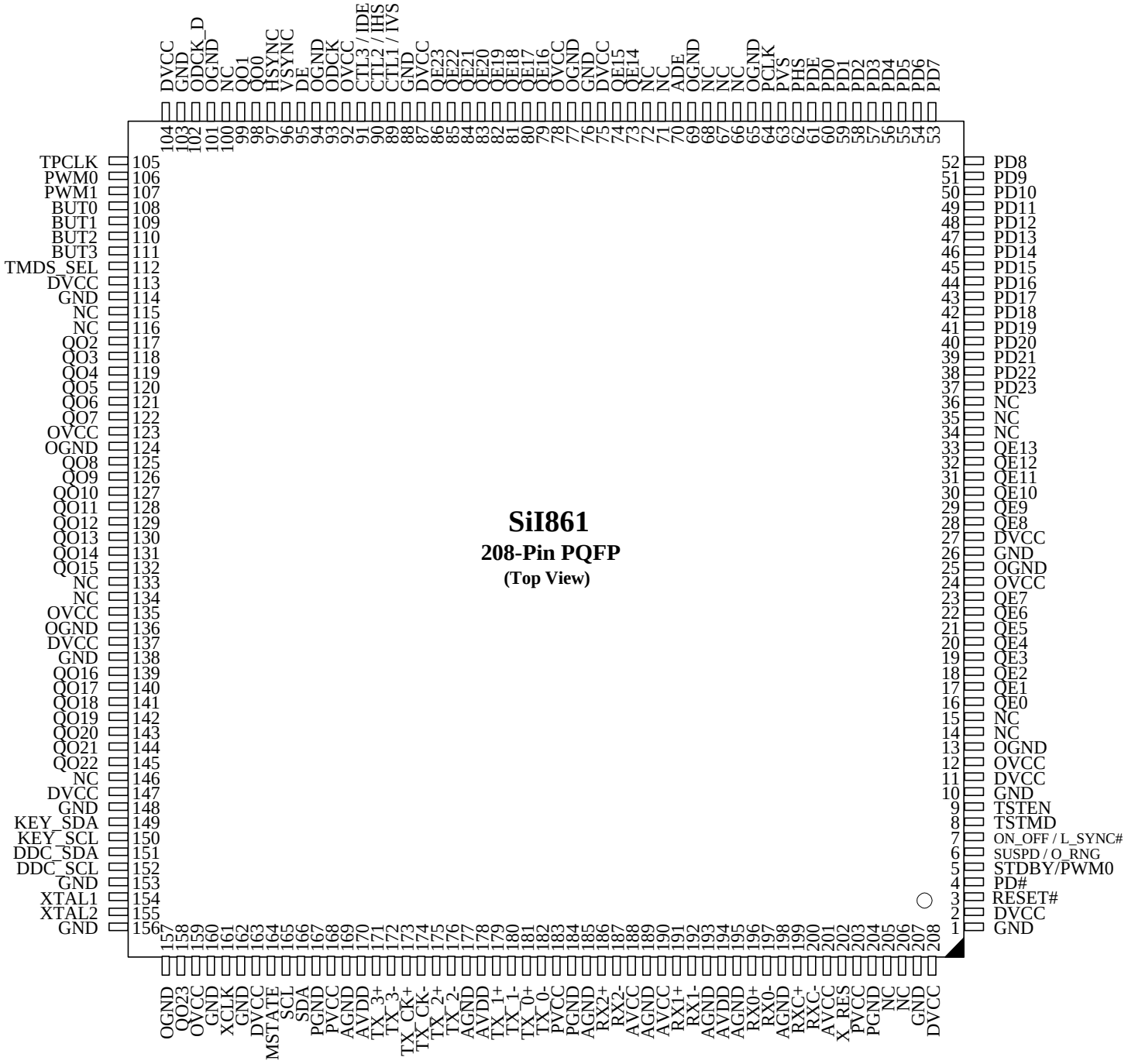


Figure 4. SiI861 Pin diagram

3. Pins Descriptions

Output Pins

Pin Name	859 Pin #	861 Pin #	Type	Description
QE[23-0]	37-30, 27-20, 17-10	86-79, 74-73, 33-28, 23-16	Out	Output Even Data[23:0] corresponds to 24-bit pixel data for 1-pixel/clock input mode and to the first 24-bit pixel data for 2-pixels/clock mode. Output data is synchronized with output data clock (ODCK). See section 1 on page 105 for the output data mapping of these pins.
QO[23:0]	77, 75-69, 66-59, 56-49	158, 145-139, 132-125, 122-117, 99-98	Out	Output Odd Data[23:0] corresponds to the second 24-bit pixel data for 2-pixels/clock mode. During 1-pixel/clock mode, these outputs are forced LOW. Output data is synchronized with output data clock (ODCK). See section 1 on page 105 for the output data mapping of these pins.
ODCK	44	93	Out	Output Data Clock.
ODCK_D	NA	102	Out	Output Data Clock Delayed. Controlled by register VSD1[3:2] on page 105.
DE	46	95	Out	Output Data Enable. This signal qualifies the active data area. A HIGH level signifies valid display time. A LOW level signifies a valid blanking time.
HSYNC	48	97	Out	Horizontal Sync control signal.
VSYNC	47	96	Out	Vertical Sync control signal.
CTL1 / IVS CTL2 / IHS CTL3 / IDE TPCLK	40 41 42 NA	89 90 91 105	Out Out Out Out	Control signals from the transmitter and internal XCLK or input HSYNC, input VSYNC, input DE and input CLOCK (ICLK). RMDT[7] determines the function of these pins. See section 1 for RMDT[7] control information. CTL3 is also used as a strapping option to enable/disable the 5x clock multiplier, high=bypass and low=enable 5x.

LVDS Output Pins

Pin Name	861 Pin #	Type	Description
TX_0- TX_0+ TX_1- TX_1+ TX_2- TX_2+ TX_3- TX_3+	182 181 180 179 176 175 172 171	Analog	LVDS output data pairs.
TX_CK- TX_CK+	174 173	Analog	LVDS output clock pair.

I^2C Pins

Pin Name	859 Pin #	861 Pin #	Type	Description
SCL	83	165	I/O	I^2C Clock. This pin is open drain.
SDA	84	166	I/O	I^2C Data. This pin is open drain.
MSTATE	82	164	Out	I^2C Bus Master. The pin goes HIGH upon RESET LOW and goes LOW after the SiI861 has finished mastering the I^2C bus.

Content Protection

Pin Name	861 Pin #	Type	Description
KEY_SCL	150	I/O	Cipher Key I^2C Clock. This pin is open drain.
KEY_SDA	149	I/O	Cipher Key I^2C Data. This pin is open drain.
DDC_SCL	152	I/O	DDC/Authentication I^2C Clock. This pin is open drain.
DDC_SDA	151	I/O	DDC/Authentication I^2C Data. This pin is open drain.

Power Management Pins

Pin Name	859 Pin #	861 Pin #	Type	Description
PD#	2	4	In	Power Down (active LOW). A HIGH level (3.3V) indicates normal operation and a LOW level indicates power down mode. Register FDIV[7] determines the power down mode entered: 1 = Power down, 0 = Pull down The I^2C register values are retained in Power Down mode but the I^2C interface is disabled.
ON_OFF / L_SYNC#	5	7	Out	On/Off / Loss of Sync. In non-DVI mode, a HIGH level indicates that the link from the transmitter to the SiI861 is active. A LOW level indicates that the link from the transmitter to the SiI861 is not active. In DVI mode, a HIGH level indicates that the link from the transmitter to the SiI861 is active. A LOW level indicates a “Loss of Sync” condition between the transmitter and the SiI861. Please refer to the Section 1. PD does not affect this output when operating in pull-down mode
STDBY/ PWM0	3	5	Out	Standby In non-DVI mode, a HIGH level indicates a standby condition. A LOW level indicates a normal active condition. In DVI mode, this pin is PWM0. Please refer to the Section 1. PD does not affect this output when operating in pull-down mode
SUSPD / O_RNG	4	6	Out	Suspend / Out of Range. In non-DVI mode, a HIGH level indicates a suspend condition. A LOW level indicates a normal active condition. In DVI mode, a HIGH level indicates an “Out of Range” condition. A LOW level indicates normal operation. Please refer to Section 1. PD does not affect this output.

PWM and Button Pins

Pin Name	861 Pin #	Type	Description
PWM0 PWM1	106 107	Out	Pulse Width Modulation. These pins can be used as the pulse width modulation signal to control the backlight brightness or volume. Please refer to the Section 1 for more information. PD# does not affect this output when in pull-down mode
BUT0 BUT1 BUT2 BUT3	108 109 110 111	In	These pins are used to monitor pushbuttons which can directly control the PWM0 and PWM1 outputs. These pins have internal 100K pull-down resistors.

Oscillator Pins

Pin Name	859 Pin #	861 Pin #	Type	Description
XCLK	80	161	In	External clock input. See Section 1 *External Clock Rate and Input Frame Rate*
XTAL1	NA	154	In	External crystal input to the inverting oscillator amplifier or clock oscillator input. This sets the output clock frequency to the panel, which will equal this frequency or be 5 times this frequency if the clock multiplier is used. This pin is 5V tolerant. See Section 1 *External Clock Rate and Input Frame Rate*.
XTAL2	NA	155	Out	Output from inverting oscillator amplifier when using on-chip crystal oscillator. No-connect when using external clock.

Reset Pin

Pin Name	859 Pin #	861 Pin #	Type	Description
RESET#	1	3	In	Reset (active LOW). When this pin is pulled LOW, the SiI861 will enter a reset state. When RESET goes HIGH, the SiI861 begins loading the internal I^2C registers automatically from the external configuration EEPROM.

Differential Signal Input Data Pins

Pin Name	859 Pin #	861 Pin #	Type	Description
RX0+	92	196	Analog	TMDS™ Low Voltage Differential Signal input data pairs.
RX0-	93	197	Analog	
RX1+	89	191	Analog	
RX1-	90	192	Analog	
RX2+	86	186	Analog	
RX2-	87	187	Analog	
RXC+	95	199	Analog	TMDS™ Low Voltage Differential Signal input clock pairs.
RXC-	96	200	Analog	
X_RES	98	202	Analog	Impedance Matching Control. Resistor value should be ten times the characteristic single-ended impedance of the cable. In the common case of 50Ω transmission line, an external 510Ω resistor must be connected between AVCC and this pin.

Parallel Input Pins

Pin Name	861 Pin #	Type	Description
TMDS_SEL	112	In	Selects PanelLink or Parallel as input source. High = PanelLink, Low = Parallel. This pin has an internal 100K pull-up resistor.
PD[23-0]	37-60	In	Corresponds to 24-bit pixel data for 1-pixel/clock input mode. These pins have internal 100K pull-down resistors.
PCLK	64	In	Input data clock for parallel input. This pin has an internal 100K pull-down resistor.
PDE	61	In	Input Data Enable for parallel input. This signal qualifies the active data area. A HIGH level signifies valid display time. A LOW level signifies a valid blanking time. This pin has an internal 100K pull-down resistor.
PHS	62	In	Horizontal Sync control signal input on parallel input.
PVS	63	In	Vertical Sync control signal input on parallel input. These pins have internal 100K pull-down resistors.
ADE	70	Out	An external DE signal is generated based on the parallel input IN_HSYNC and IN_VSYNC pins. If using an external component that does not generate DE, such as a TV decoder, this signal should be connected externally to IN_DE. The timing of this signal is controlled by register [TBD].

Test Pins

Pin Name	859 Pin #	861 Pin #	Type	Description
TSTMD	6	8	In	For TEST purposes only. Should be tied LOW.
TSTEN	7	9	In	For TEST purposes only. Should be tied LOW.

Power and Ground Pins

Pin Name	859 Pin #	861 Pin #	Type	Description
DVCC	9,38, 67,81	2,11,27, 75,87, 104,113 ,137, 147,163 ,208	Power	Digital Core VCC, must be set to 2.5V.
GND	8,39, 68,79	1,10,26, 76,88, 103,114 ,138, 148,153 ,156, 160,162 ,207	Ground	Digital GND.
OVCC	18,29 ,43,5 7,78	12,24, 78,92, 123,135 ,159	Power	Output Buffers VCC, must be set to 3.3V.
OGND	19,28 ,45,5 8,76	13,25, 65,69, 77,94, 101,124 ,136, 157	Ground	Output Buffer GND.
AVDD	NA	170, 178, 194	Power	Analog VCC, must be set to 3.3V.
AVCC	88,97	188, 190, 201	Power	Analog VCC, must be set to 3.3V.
AGND	85,91 ,94	169, 177, 185, 189, 193, 195, 198	Ground	Analog GND.
PVCC	99	168, 183, 203,	Power	PLL Analog VCC, must be set to 3.3V.
PGND	100	167, 184, 204	Ground	PLL Analog GND.

4. Strapping option on CTL3

The SiI 859/861 has a strapping option on pin CTL3, which selects whether to use the 5x clock multiplier: high = bypass, low = 5 x multiply. This strapping option was added to improve performance of loading the EEPROM after reset by using the appropriate clock divider circuit based on the input clock. This strapping option will set the internal register IDIV[7] = "strap value" immediately after reset. Therefore, the register bit for IDIV[7] in the configuration EEPROM must match the strapping value. If the clock multiplier is bypassed, a 4.7K pull-down resistor plus setting IDIV[7] = 0 in the EEPROM is required. Likewise, if the clock multiplier is enabled by strapping CTL3 high, then register IDIV[7]=1 in the EEPROM is required.

Pin Name	859 Pin #	861 Ball #	Type	Strap Option
CTL3	42	W13	Output 3.3V	Clock mode strap: 4.7K Pull-up = bypass 4.7K Pull-down = 5x

Table 1. Strapping option on CTL3

5. Control Signal Output Timing

HS, VS and DE active periods may not overlap.

VSYNC & HSYNC Timing

The Position, Width, and Polarity of VSYNC and HSYNC are adjustable by way of the I^2C registers. The output VSYNC occurs a fixed number of XCLK cycles after the last Output DE. The output HSYNC occurs a fixed number of XCLK cycles before the rising edge of the output DE signal.

The width of the output VSYNC pulse can be adjusted from 1 to $(2^{12} - 1)$ XCLK cycles using register VSW1 and VSW2. The delay of the output VSYNC pulse, with respect to the trailing edge of the last input DE, can also be adjusted from 1 to $(2^{18} - 1)$ XCLK cycles using register VSD1, VSD2, and VSD3. The polarity may be inverted using register POLT[3].

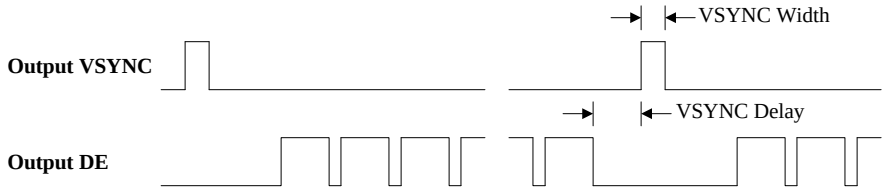


Figure 5. Output VSYNC Timing

The output HSYNC is generated from the output DE signal and begins from 1 to 511 XCLK cycles before the **rising edge of DE** using register HSDL. Please note that this is different than the reference edge for VSYNC and the Final HSYNC. The width can be adjusted from 1 to 254 XCLK cycles using register HSWD. The pulse must not overlap the rising edge of DE. The polarity may be inverted using register POLT[0].

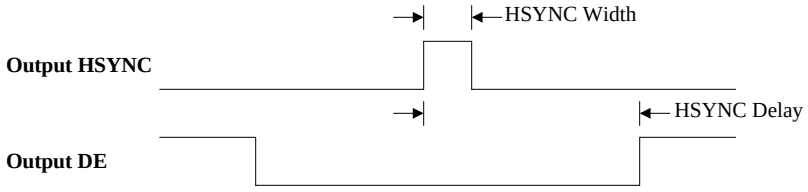


Figure 6. Output HSYNC Timing

HSYNC Inserted into Vertical Blanking Period

Some panels may require the insertion of horizontal sync pulses into the vertical blanking period. The 861 can be programmed to generate these pulses in either of two ways:

1. A fixed number of pulses after the end of a frame, determined by register VBN1,2
2. Fill from beginning of frame backwards. Pulses will be inserted until the previous Hsync. The previous Hsync can be from the last displayed line, or if VBN1,2 is used it will be the last inserted pulse. RMDT[5] enables this mode.

The timing on these pulses can either be a fixed number of XCLKs or can be determined from the last line. If the number from the previous line is used, the timing may vary slightly from line to line. Moreover, the fixed number of pulses must be small enough that they do not overlap the DE pulses from the next frame. VHD should be an even number for 2 pixel per clock output.

Two registers (VHD1 and VHD2) are used to give the period of the pulses inserted into the blanking period and control the operation. Another register (VBN1,2) sets the number of pulses inserted. The pulse width is the normal HSync width. The first pulse starts the horizontal final delay after the final DE.

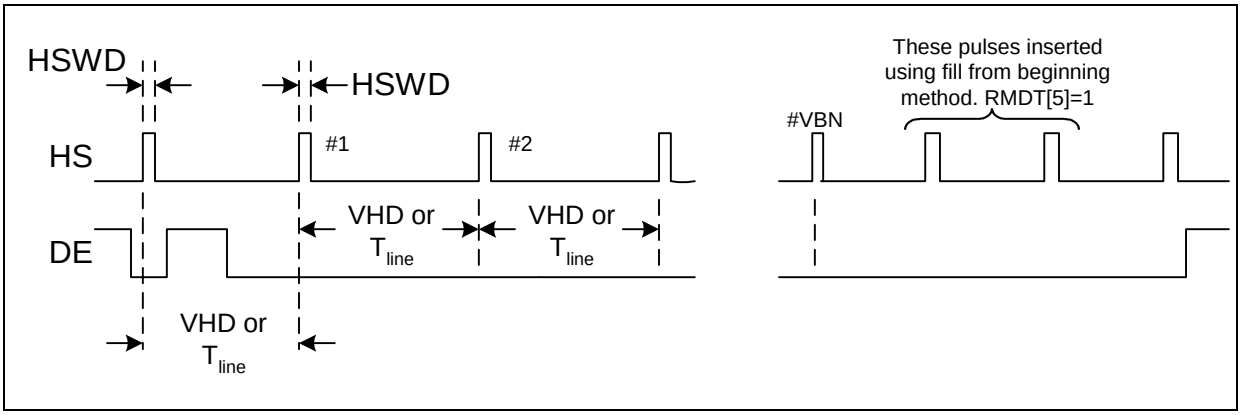


Figure 7: HSync in VBlank

Output DE Timing

The line time of the output lines is not identical. The output has the same number of pixels during DE high (active display time), but the length of the blanked period (DE low) may vary by up to 3 input ICLK clock cycles (RXC clock cycles) in order to keep the input and output synchronized. This is shown in the figure below.

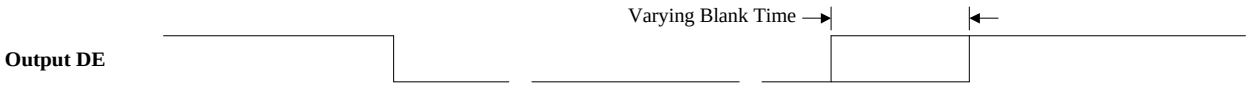


Figure 8. Output DE Timing

6. External Clock Rate and Input Frame Rate

To support full screen expansion and frame rate matching, the external clock must be at a high enough rate for the output to keep up with the input. In the SiI 861 architecture, the active time of the input is equal to the active time of the output. This is expressed in the following equations:

$$(\text{Input Line Time}) * (\text{Rows}_{In}) = (\text{Output Line Time}) * (\text{Rows}_{out})$$

$$1/f_{in} * (\text{Column}_{In} + \text{Blanking}_{In}) * (\text{Rows}_{In}) = 1/f_{XCLK} * (\text{Column}_{out} + \text{Blanking}_{out}) * (\text{Rows}_{out})$$

Using a typical 32 clock delay for Hsync before DE, the equation for deriving the minumum XCLK becomes:

$$\text{Minimum XCLK Frequency} = (\text{Column}_{out} + 32) * \text{Input Line Frequency} * \text{Rows}_{out} / \text{Rows}_{In}$$

The minimum XCLK clock rate for XGA with a HSYNC delay of 32 clocks is determined by the following equation:

$$f_{XCLK} = (\text{Input Line Rate} / \text{Minimum Input Rows}) * (1024 + 32) * 768$$

A XGA panel that supports such a frequency is required.

Example –

640 x 480 at 60Hz – Input Resolution, 31.5 KHz – Input Line Rate

f_{XCLK} = (Input Line Rate / Minimum Input Rows) x 811,008

f_{XCLK} = (31.5 KHz / 480) * 811,008

f_{XCLK} = 53.2 MHz

The minimum XCLK clock rate for SXGA with a HSYNC delay of 32 clocks is determined by the following equation:

f_{XCLK} = (Input Line Rate / Minimum Input Rows) * (1280 + 32) * 1024

A SXGA panel that supports such a frequency is required.

Example –

640 x 480 at 60Hz – Input Resolution, 31.5 KHz – Input Line Rate

f_{XCLK} = (Input Line Rate / Minimum Input Rows) * 1,343,488

f_{XCLK} = (31.5 KHz / 480) * 1,343,488

f_{XCLK} = 88.2 MHz

To support all possible input modes that the SiI861 can support, it is recommended that the maximum output frequency appropriate for the panel be used.

7. Input and Output Resolutions Supported

The 861 supports any output panel resolution up to 1600 horizontal pixels. The output resolution is configured by setting registers PLC1,2 to the output columns, and registers PLR1,2 to the output rows. The automatic scaling engine of the 861 will then scale up or scale down any incoming resolution to that of the output. This scaling function does not require an external microcontroller to operate – all calculations are performed by the 861.

8. Loss of Sync and Out of Range

Loss of Sync occurs when there is no valid incoming video signal, either on the PanelLink interface or the parallel interface of the 861. Out of Range occurs when there is an incoming video signal, but the timing is not within acceptable limits set by registers in the 859/861. The 859/861 can automatically be configured to generate a Loss of Sync OSD (LOS) or an Out of Range OSD (OOR) when one of these conditions occurs. Instead of instantly displaying these messages when a LOS or OOR condition exists, it may be desirable to add a delay before displaying any OSD. For example, this may be used when switching from one resolution (1024x768) to another (640x480) if the graphics controller does not always output stable video. With no delay, the 859/861 may display the Loss of Sync or Out of Range message for a brief time, thus alarming the end user. To add a delay, register OSDD is used. During this delay period, only the screen OSD background color is displayed with no alarming message. If the LOS or OOR condition continues to exist after this delay, then the appropriate OSD message (LOS or OOR) is displayed. lists the registers used to control Loss of Sync and Out of Range behavior. For a description of OSD functionality, please see section 1, . The L_SYNC# pin is asserted low when a Loss of Sync occurs, and the O_RNG pin is asserted high when an Out of Range occurs.

Register Name	Function
OSDE[5]	Enable Loss of Sync OSD when video lost. 1 = enable, 0 = disable
OSDE[4]	Enable Out of Range OSD when out of limits. 1 = enable, 0 = disable
OSDE[3]	Loss of Sync status. 1 = no incoming video, 0 = valid incoming video (monitors DE)
OSDE[2]	Out of Range status. 1 = out of range, 0 = in range
OSDE[1]	Detection method of Loss of Sync. 1 = SCDT from PanelLink, 0 = monitor DE. See page 105.
LOSD	Loss of Sync delay. 4-bit number determines delay when transitioning from Loss of Sync to active display state. Increments are approximately ¼ second.
OSDD	OSD delay. 8-bit number of frames to delay before displaying Loss of Sync or Out of Range OSD.
FLR1[6]	Enable frame rate checking using registers FFR1,2 and SFR1,2 to detect Out of Range conditions. 1 = enable, 0 = disable.
FLR1[5]	Enable line rate checking on output to panel using registers FLR1,2 and SLR1,2. NOTE: This measures the output line rate to the panel, not the input line rate of the PanelLink receiver.
FLR1[4:0], FLR2	Fast Line Rate in number of XCLKs to check for out of range conditions. 13-bits
SLR1[3:0], SLR2	Slow Line Rate in number of XCLKs to check for out of range conditions. 12-bits
FFR1,2,3	Fast Frame Rate in number of XCLKs to check for out of range conditions. 24-bits
SFR1,2,3	Slow Frame Rate in number of XCLKs to check for out of range conditions. 24-bits
OFSH,OFSL	Address to fetch OSD character bitmap and message memory from. 16-bits.

Table 2. Loss of Sync and Out of Range Registers

9. Dithering

The SiI861 Dithering Engine increases the perceived color depth of an 18-bit TFT panel so that 24-bit colors can be shown. A proprietary dithering technique is used to preserve the image resolution while increasing the perceived color depth. The TFT Dithering Engine includes a set of 4 different dithering patterns that combine a proprietary frame rate control and spatial dithering algorithm. Dithering can be enabled via register POLT[6].

10. Color Management

Flat panels have no standardization when it comes to color management. Each panel manufacturer has a different gamma curve for each panel type and resolution that responds differently to temperature. CRTs and flat panels may have different gamma curves. Video images and graphics images also have different gamma curves. Therefore, to be able to show a quality image on a flat panel monitor as is shown on a CRT or television no matter the image source, temperature variation or some form of color management may be needed on the flat panel monitor. The SiI859/861 has two integrated gamma tables, one before the scaling engine (GAMMA1) and one after the scaling engine (GAMMA2). Both of these gamma tables are 8-bit lookup tables with 256 entries per color as shown in and can be bypassed through register ICC1[4] for input and ICC1[5] for output (1=disabled, 0=enabled).

Having the color management capabilities on the flat panel monitor allows the flat panel monitor manufacturer to fine tune the monitor to show the best possible image to the viewer. It also allows the viewer to be able to see the same high quality image on the monitor no matter which system it is connected to.

The SiI859/861 has six fully programmable 8-bit 256 look-up tables, two for each of the primary colors (RED, GREEN, and BLUE) that allow adjustment of gamma. The 8-bit incoming value for each color is mapped into the lookup table, the 8-bit value in that location of the table is then output as the color.

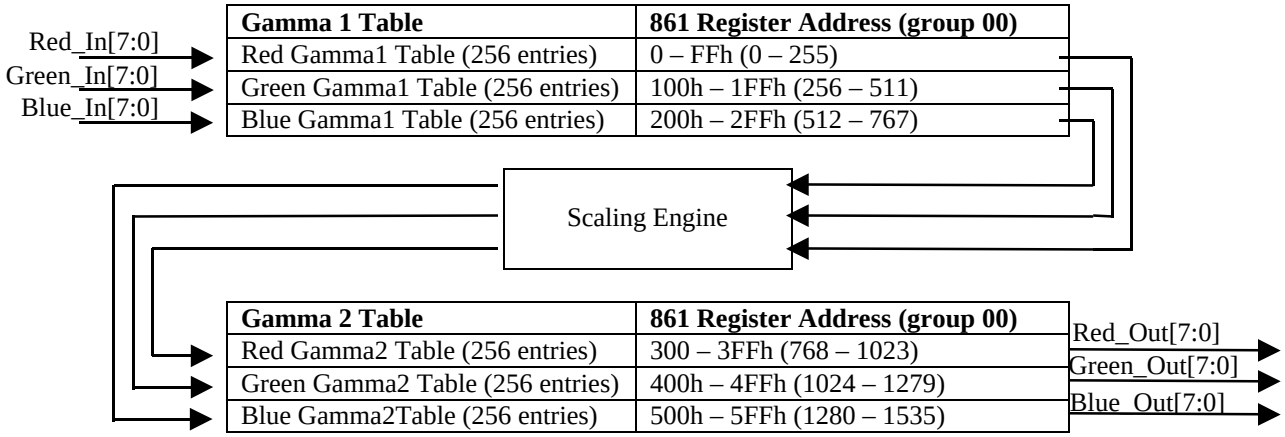


Table 3. Gamma Tables

Gamma correction can be disabled by setting ICC1[4] = 1 for GAMMA1 and ICC1[5] for GAMMA2, in which case both GAMMA1 and GAMMA2 are bypassed.

11. XTAL1 and XTAL2 Clock Input and Clock Multiplier

The 861 contains an on-chip crystal oscillator which generates an input clock from a crystal connected to pins XTAL1 and XTAL2. When the crystal oscillator is used, XCLK should be tied to ground. If this oscillator is not used, a clock input should be connected to XCLK, with X1 tied to ground while X2 should be left open. The 861 also contains an internal PLL clock generator that can be enabled to multiply the input clock by 5 if IDIV[7] = 0.The clock input to the chip can be directed into the internal clock generator or directly to the logic. When using the clock in the direct mode, the frequency must match the frequency of the panel being used. illustrates the clock input options that can be used.

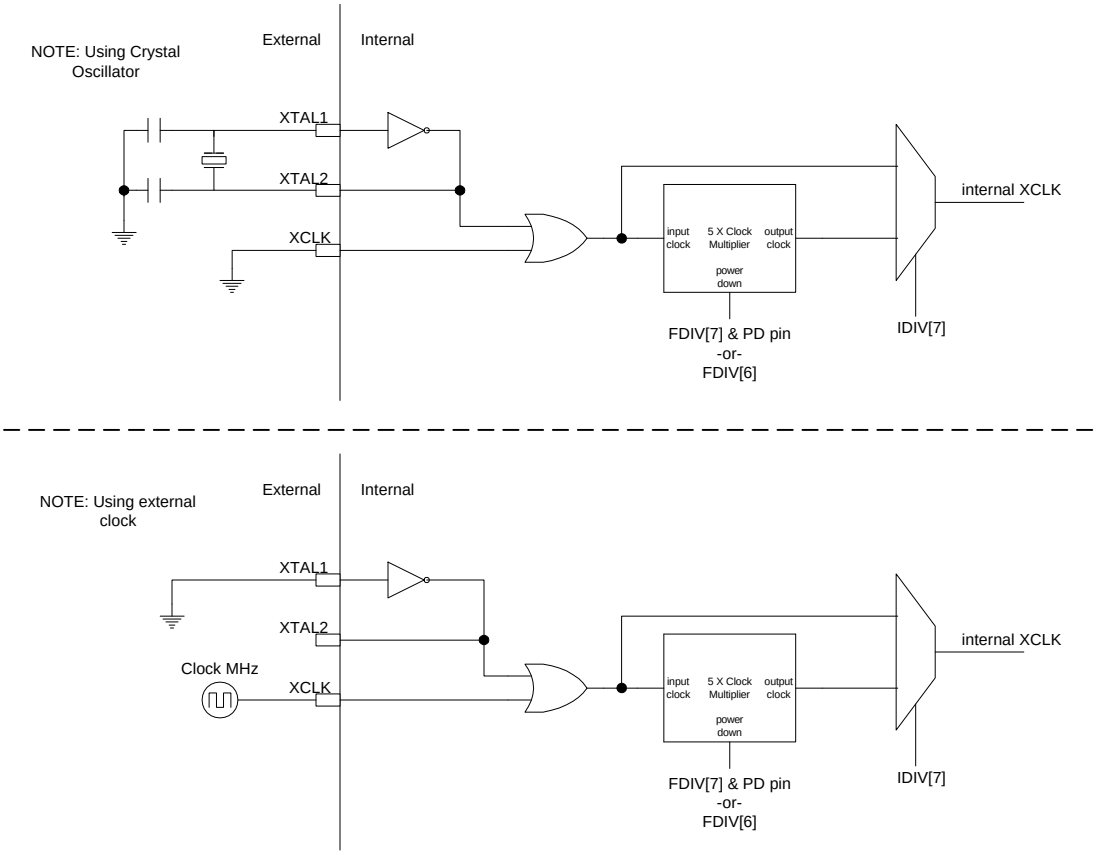


Figure 9. Clock Input Options

0 = “Pull down”.
In full power down the entire chip is powered off, including the core, the scaling, the clock multiplier, the power management, and the I^2C interface. The outputs are pulled down. The state of the registers and the memory are retained. This mode might be used if an extremely low power consumption mode is desired. In this case, a microcontroller could be used to put the 861 in “power down” mode by asserting PD#. Because the core is not active, by the 861 until PD# is de-asserted. To accomplish this, a timer can be used by the microcontroller to periodically wake up the 861 and then check the “Loss of Sync” pin or read the status register. The outputs of the 861 will be valid 2 frames after PD# goes high – at 60 Hz this equals .033 seconds. If there is no incoming active video, the 861 can be powered down again by asserting PD# low.
In pull down mode the only change to operation is that the panel outputs are pulled low. These pins are even and odd data outputs, ODCK, HSYNC, VSYNC, and ODE. The rest of the chip remains active. In this mode the “Loss of Sync” pin remains operational and can be used to detect an active video signal.

Clock Multiplier and LVDS Transmitter Power Down

Both the clock multiplier circuit and LVDS transmitter can be powered down through register control. Register FDIV[6] can be used to power down the clock multiplier: 1 = power down clock multipler, 0 = normal operation. Register POLT[5] can be used to power down the LVDS transmitter: 1 = power down LVDS, 0 = normal operation.

13. Pulse Width Modulation

The 861 has two pulse width modulation (PWM) outputs that can be used for control of backlight brightness and volume control. These PWM outputs can be adjusted by writing to the PWM control registers, usually by a microcontroller, or automatically by having the 861 monitor pushbutton inputs. When the 861 is configured to automatically adjust the PWM signals, an internal state machine will monitor the pushbutton input pins and adjust the duty cycle output of the PWM in steps when a button is pressed. The step registers of the backlight and audio PWM functions (BLST and AUST) determine these steps.

The PWM signals can be set to be always HIGH, always LOW, or through a large range of frequencies and duty cycles. The frequency and duty cycle can be controlled through the I^2C registers. The timing of this PWM output can be reset at the beginning of each frame (to synchronize the backlight to the frame rate) or the output can be free running.

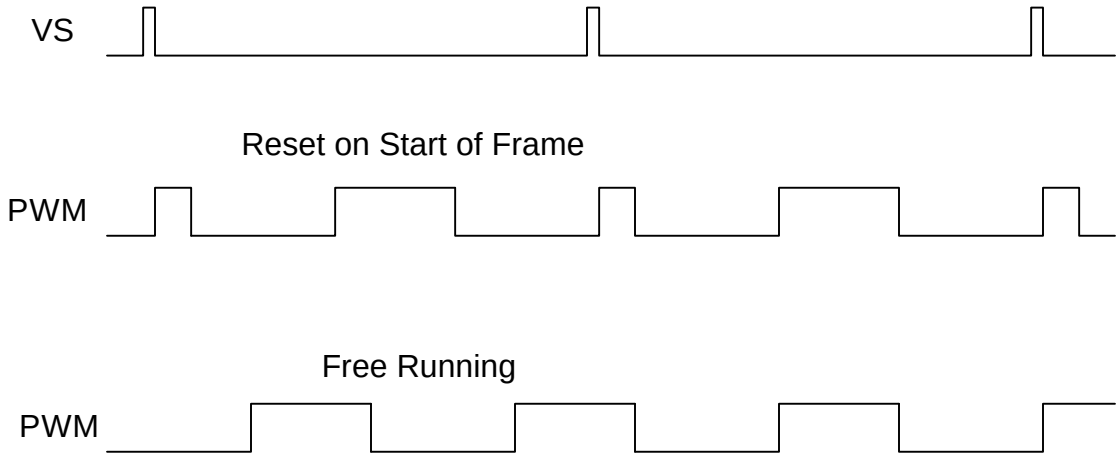
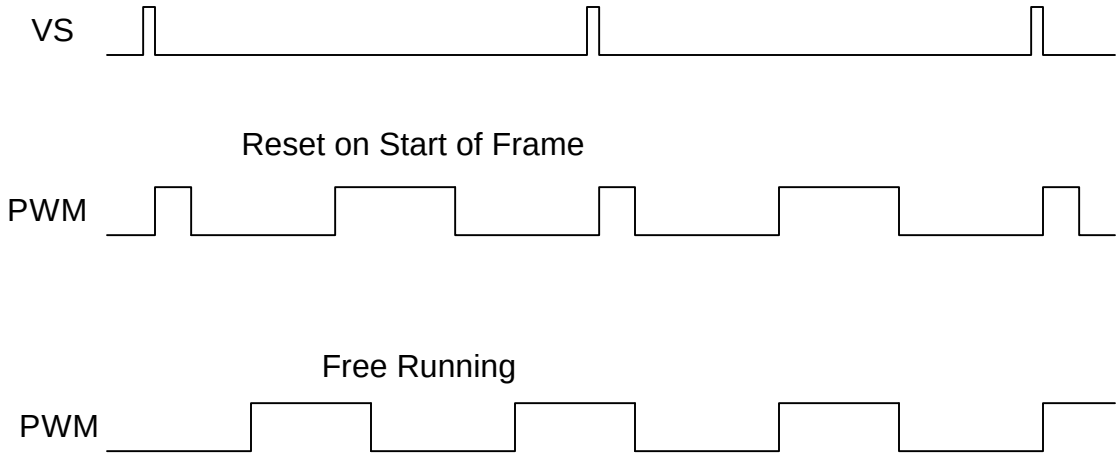


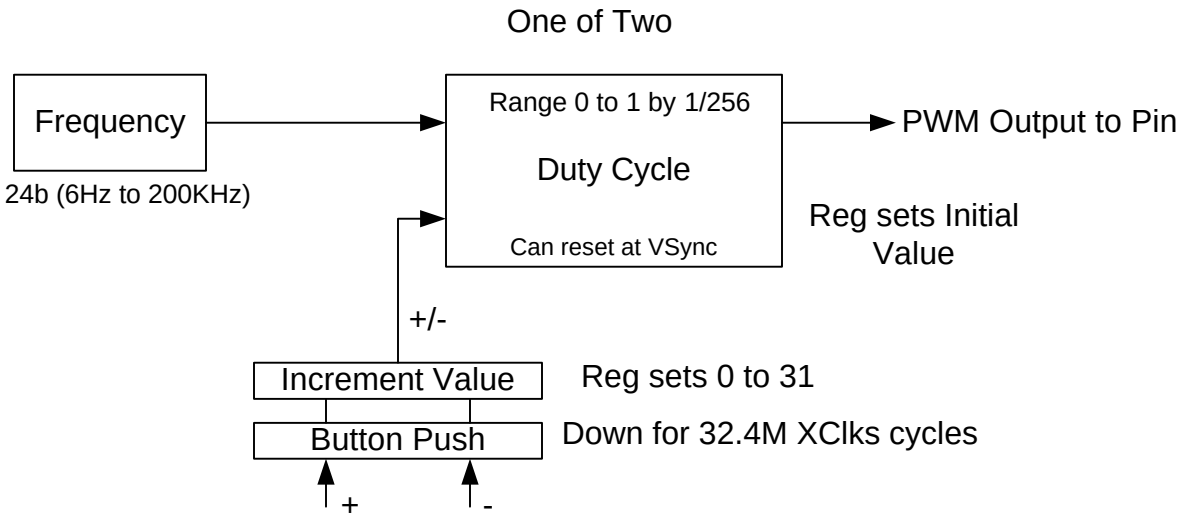
Figure 10. PWM Timing

14. Pushbutton Interface

The chip provides two pulse width modulation (PWM) outputs for control of backlight or speaker volume. These may be programmed on the I^2C bus or by a button interface. It can be set to be always high, always low, or through a large range of frequencies and duty cycles. The timing can be reset at the beginning of the frame (to synchronize to the backlight to the output frame rate) or the output can be free running.



The button interface is programmed through registers. It is possible to set the frequency, initial duty cycle, and the change in duty cycle caused by a button push. The frequency is set by 24 bits which are counted in XCLK cycles. The output can be from 6 Hz to 200 KHz, given the nominal range of XCLK frequencies. The duty cycle can be adjusted in up to 256 steps from all high to all low. The change in duty cycle for each button push may be set by a 5 bit register. Therefore, the change in duty cycle of the PWM for each button push can be from 1/256 to 1/32.



The button is considered to have been pushed when it is high for 32.4 million internal XCLK cycles. The external button circuit should have proper debounce to guaranteed a false trigger does not occur. When the duty cycle reaches 100% or 0%, further raising or lowering, respectively, will not change the output.

15. CTL[3:1], IXCLK / IVS, IHS, IDE, ICLK Options

The control lines can be passed directly from the PanelLink receiver to these outputs without modification. The outputs can also be switched to provide IVS (internal vertical sync.), IHS (internal horizontal sync.), IDE (internal display enable) signals, and ICLK (clock from PanelLink receiver). Which signals are output is controlled by the register RMDT[7]. IVS, IHS and IDE are timed with reference to received differential clock (RXC).
IXCLK refers to the internal XCLK, or the pixel clock used to control the panel. In 1 pixel/clock mode, XCLK equals the output clock, ODCK. In 2 pixel/clock mode, XLCK equals twice the frequency of ODCK.
ICLK refers to the PanelLink receiver clock, or the clock that is re-generated from the incoming PanelLink serial stream. This clock is useful when measuring DVI compliance and eye diagrams at the receiver side.

Pin	RMDT[7] = 1	RMDT[7] = 0
CTL1	CTL1	IVS
CTL2	CTL2	IHS
CTL3	CTL3	IDE
TPCLK	IXCLK	ICLK

16. I²C PROM Mapping

The SiI861 I²C PROM memory address space is organized into three regions: OSD Space, Color Look-up Tables Space, and Configuration/Control Space as shown in the Figure below. After reset, the SiI861 becomes a master on the I²C bus and reads the Configuration and Control, Color Look-up Tables, and OSD Message data from an external I²C ROM at address A0h. The OSD space can be skipped and not loaded if OSDE[7] = 0. The OSD Space requires 7Kbytes. The Color Look-up Tables Space requires 1536 bytes. The Configuration/Control space requires 2704 bytes.

Table 5. PROM Content Layout

Decimal Address		Hexadecimal Address
11919 : 10896	**OSD Message Memory 1024 Bytes**	2E8F : 2A90
10895 : 4752	**OSD Character Bitmap Memory 6144 Bytes**	2A8F : 1290
4751 : 3984	**Gamma 2 Table 768 Bytes (3 x 256)**	128F : F90
3983 : 3216	**Gamma 1 Table 768 Bytes (3 x 256)**	F8F : C90
3215 : 768	**Scaling Weight Table 2448 Bytes**	C8F : 300
767 : 512	**Configuration and Control Space 256 Bytes**	2FF : 200
511 : 0	**Unused 512 Bytes**	1FF : 0

[1] Refer to the Register Index for a detailed description of the configuration/Control registers.

17. I²C Interface

When the SiI859/861 is an I²C master the frequency of the I²C clock is equal to XCLK / 512. The SiI859/861 I²C interface supports the Fast Mode I²C Interface timings when acting as a slave. Please consult the Philips Semiconductor I²C Specification for electrical information. After reset, the 861 will become an I²C master and read from an external EEPROM at device address A0h. The 861 will begin to load all of its registers from this external EEPROM. If there is no EEPROM present at address A0h, the 861 will timeout and default to slave address 1C0h. If this happens, the 861 will be unconfigured and must be loaded externally from a microcontroller. The 861 has one deviation from the standard I²C interface – it does not support arbitration when it becomes a master on the I²C bus. For this reason, there is an additional pin (MSTATE) that should be monitored when an external I²C master device wishes to share the I²C bus with the 861. This pin is asserted by the 861 when it is reset and stays high until the 861 has finished mastering the I²C bus – this is the only time the 861 becomes an I²C master and this pin gets asserted. NOTE: 28 I²C clocks after being asserted, the MSTATE pin will go low for approximately one I²C clock, then it will remain high for the remainder of the EEPROM load.
The timing is shown in .

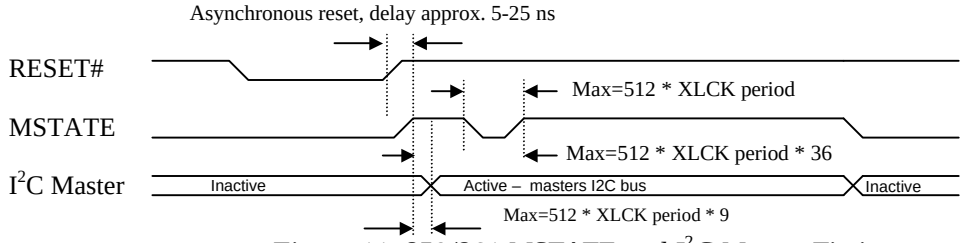


Figure 11. 859/861 MSTATE and I²C Master Timing

I²C Register Addresses

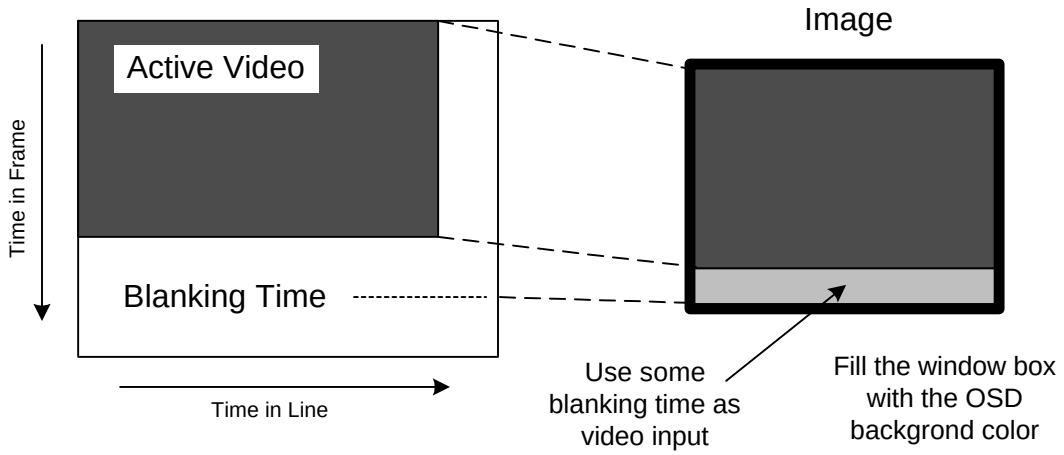
The 861 has four groups of registers, group 0-3, that can be accessed over the I²C bus. In order to access these registers, the 861 acts as a slave I²C device. The slave I²C address of the 861 is determined in one of two ways: 1) After reset, if there is no external EEPROM present, the 861 will timeout and default to slave address 1C0h; 2) If there is an EEPROM present, the 861 will begin to read in its configuration from the EEPROM, two bytes of this configuration (registers SAD1,2) determine the slave address of the 861 after it finishes mastering the I²C bus. It is recommended to use a slave address of 1C0h. The four groups of registers of the 861 are mapped internally using two bytes, the group number occupies the two most significant bits of the address as shown in .

Group	Register Address															
	High Byte – first byte on I2C bus								**Low Byte – second byte on I2C bus**							
#	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	0	0	Reserved				Gamma Tables									
1	0	1	Reserved						Control Registers							
2	1	0	Reserved				Scaling Weight Table									
3	1	1	Res	OSD Memory (Character bitmaps and message)												

Table 6. 861 Register Group Mapping

18. Window Boxing to reduce line rate

Certain panels cannot tolerate fast line time. Because the lower row count DOS resolution, such as 640x350, have long vertical blanking periods it is possible to reduce the line time by taking some of the VBlank as input. This causes the image to be "window boxed". The SiI 859/861 has the capability to perform this window boxing automatically, without using a microcontroller, by setting registers LWB1 and LWB2 in the configuration EEPROM.



The 861 supports three modes of window boxing, these modes are mutually exclusive, therefore only one mode should be enabled at a time. The three modes are:

1. Automatic Mode Once. If the line rate is too fast, a fixed number of rows, set by XIRW[7:0], will be added once to the input. To enable set register LWB1[4] = 1.
2. Automatic Mode Progressive. If the line rate is too fast, a fixed number of rows, set by XIRW[7:0], will be added. After adding these rows, if the line rate is still too fast, this process will be repeated up to 8 times until the line rate is within range. To enable set register LWB1[5] = 1
3. Manual Mode. This mode requires a microcontroller and is backward compatible with the SiI 851 window boxing implementation. To enable set XRW1[3] = 1.

Registers IRP1, IRP2, ICP1and ICP2 measure the input resolution counted even when the lock resolution bit RMDT[6] is set. They operate in the same way as IRC/ICC. Registers XRW1 and XRW2 are used in manual mode and give the row after which the image is filled with the color from the OSD background.

The procedure to initiate automatic mode window boxing is as follows:

1. Determine the maximum line rate period in XCLKS the panel can support. Set register LWB1,2 to this value.
2. Determine the number of rows to add to the input resolution at each step. Set register XIRW to this value.
3. Set register LWB1 to enable automatic window boxing, either once or progressive mode.

The procedure to initiate manual mode window boxing is as follows:

1. Detect a situation in which the line rate or other condition is not acceptable, either by monitoring registers ICC, IRC, or LWD.
2. Lock the resolution by setting RMDT[6]
3. Set the user resolution to a value with the same column count as the incoming image, but with a larger number of rows. Set the increments as well as the rows and columns.
4. Set IRC# and ICC# to match the user resolution.
5. Set FWB# to be the integer just below IRP/IRC * Output rows.

6. Enable window boxing by setting XRW[3] to 1.
7. Monitor IRP and ICP to detect another change in resolution and IFR and LWD for changes in input rate. If one occurs, unset RMDT[6]. If the new resolution is also too fast repeat the process.
8. Disable window boxing by setting XRW1[3] to 0.
9. Reprogram the user resolution to its new desired value.

19. Character based On Screen Display (OSD)

The OSD is based upon characters, which are 12 by 16 pixels. These characters may be letters or symbols. They could be a portion of a larger character or symbol if several were always used together. There are 64 characters total. The characters are loaded from the EEPROM by the SiI 861 after reset, and may be modified through the I^2C interface at any time. These characters form the alphabet from which the OSD messages are composed. When the EEPROM is loaded at reset, loading of the OSD space may be skipped in order to save time or EEPROM space. - this occurs if the bit OSDE[7] = 0

Each pixel in each character is one of sixteen colors. Fifteen of the colors are defined by a 24 bit RGB value and one "color" is transparent. The composition of the message is through the OSD Message Memory. This may be up to 1024 characters. The width and height, in pixels, defines the rectangle in which the OSD image is formed. The pixel width MUST be a multiple of 12, and the pixel height MUST be a multiple of 16. The upper left corner position is defined by registers OUL1-4.. The OSD image must not go off the boundaries of the screen. The horizontal position of the upper left corner is two pixels less than the value of OUL1,2, the horizontal position register.

There are three memory pointers for displaying the OSD messages: One for the User OSD, one for the Out of Range (OOR) OSD, and one for the Loss of Sync (LOS) OSD. More than one OSD message may be loaded at once filling up the 1024 bytes of message memory. The user OSD pointer can then be moved and the width and height changed to the content of the image very rapidly. Because the characters in the message are only a pointer to a 6 bit location (one of 64 characters), it is very fast to change the content. Each element of text also includes the double and highlight bits, so the actual size of each character is one byte. Because this one byte causes the display of a 12x16 character = 192 pixel image, the OSD can be changed very rapidly with no perceptible delay to the end user. The message may be doubled on a row by row basis. This makes the characters 24 by 32 with each pixel in the 12 by 16 character doubled in both directions. There is also a highlight option which causes the characters color map to change instantly, allowing for specified characters in the message to be highlighted – this is useful for doing menu selection OSDs.

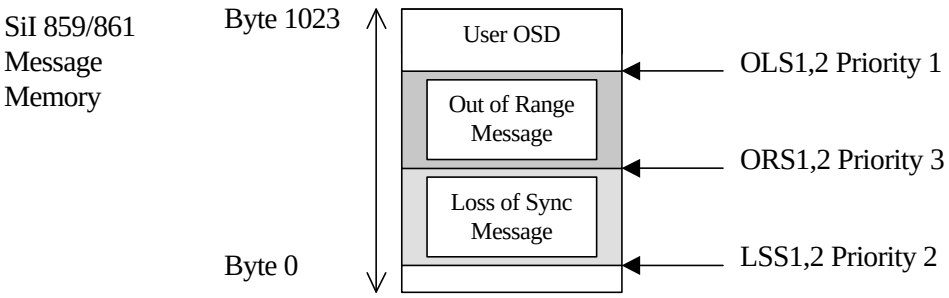


Figure 12. OSD Message Memory Pointers

OSD Control Registers and Memory Space

The "Loss of Sync" and "Out of Range" OSD messages can be used without a microcontroller, if enabled in the configuration EEPROM loaded by the 859/861 after reset, in which case these OSD messages will automatically be displayed by the 859/861 when one of these conditions occurs. The "User Mode" OSD requires the use of a

microcontroller to enable, disable, or load in new messages by using the I2C bus to access the appropriate 859/861 registers. In order to use the OSD features of the 859/861, there are four groups of registers that must be set correctly:

1. Control registers
2. Color look up table for character bitmap (15 entries)
3. Character bitmap memory (6144 bytes)
4. Message memory (1024 bytes)

These four groups of registers are loaded from the external configuration EEPROM. However, because they are RAM based, they can be updated at any time by using the I2C interface of the 859/861. shows the OSD structure describing these registers. Each of these four groups will be described below:

Control Registers:

These registers are used to control the basic operation of the OSD. Some of these registers occupy more than one byte – each byte must be programmed accordingly. lists these OSD control registers.

Register Name	Function					
OSDE[7:2] (bit register)	7	6	5	4	3	2
	Load OSD data at reset	Display User OSD	Enable Loss of Sync OSD	Enable Out of Range OSD	Loss of Sync Status	Out of Range Status
OUL1,OUL2	Horizontal position, upper left corner. 11-bits					
OUL3,OUL4	Vertical position, upper left corner. 11-bits					
OSW1,OSW2	Width of OSD message in pixels. Must be a multiple of 12. 11-bits.					
OSH1,OSH2	Height of OSD message in pixels. Must be a multiple of 16. 11-bits.					
OLS1,OLS2	Pointer to User OSD message in OSD Message Memory. 12-bits, range = 0-3FFh					
LLS1,LLS2	Pointer to Loss of Sync OSD message in OSD Message Memory. 12-bits, range = 0-3FFh					
ORS1,ORS2	Pointer to Out of Range OSD message in OSD Message Memory. 12-bits, range = 0-3FFh					
XRW1[5:4]	OSD transparency. (Opaque, 25%, 50%, 75%)					
OSBR,OSBG ,OSBB	Screen background color on Loss of Sync or Out of Range. 24-bit RGB value.					
LOSD[3:0]	Delay when transitioning from Loss of Sync state to active display state.					
OSDD	Delay before displaying Loss of Sync or Out of Range OSD.					
OFSH,OFSL	Address to fetch OSD character bitmap and message memory from. 16-bits.					

Table 7. OSD Control Registers

Color Look Up Table:

The color look up table registers are used to define the colors used by the characters. There are a total of 15 entries, each entry is a 24-bit RGB value. Each individual pixel that makes up the 12x16 character can be any one of these unique 15 colors (entry 1-Fh) or transparent (entry 0). NOTE: There is no entry for color ‘0’ this is the transparent color. lists these color look up registers.

Register Name	Function
CL[1:F]R	Red value color look up. Entries 1-F
CL[1:F]G	Green value color look up. Entries 1-F
CL[1:F]B	Blue value color look up. Entries 1-F

Table 8. Color Look Up Table Registers

There are two modes for operation of the color look up table: Normal and Highlight. These modes are selectable on a character by character basis in the Message memory area by bit-7 of the character to be displayed. Normal mode will cause the pixels in the character to take on the color based on the look up table mapping. Highlight mode will cause a change or reversal of this mapping for entries 2-Eh. This is shown in . Highlight mode is useful when displaying OSD menus or icons and a selection needs to be highlighted.

Entry #	Normal Mode Character[7] = 0	Highlight Mode Character[7] = 1
0	0	0
1	1	E
2	2	D
3	3	C
4	4	B
5	5	A
6	6	9
7	7	8
8	8	7
9	9	6
A	A	5
B	B	4
C	C	3
D	D	2
E	E	1
F	F	F

Table 9. Color Look Up Table Highlight Mode

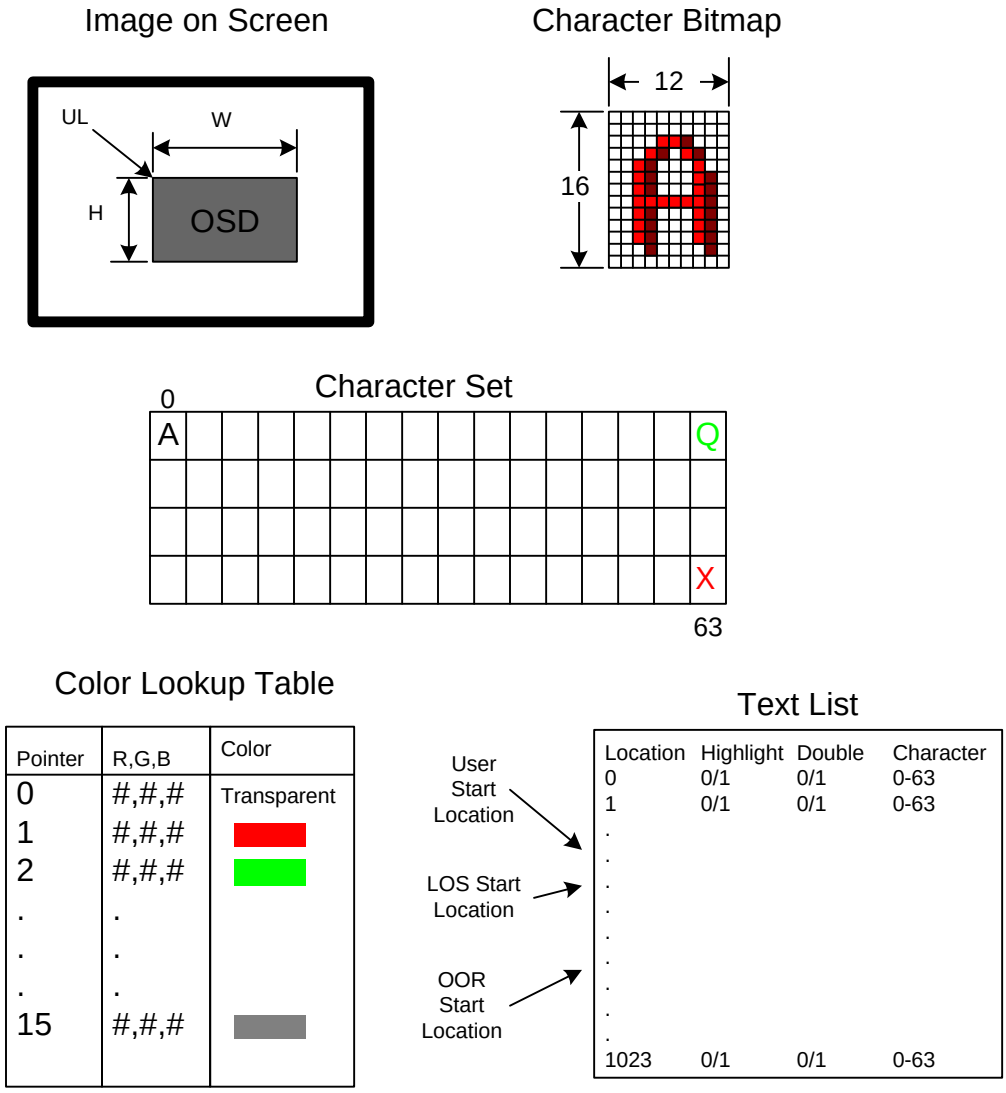


Figure 13. Character OSD Structure

Character Bitmap Memory:

The bitmaps for the character set are mapped from a 48 wide by 1024 high image. This represents one character wide times four bit planes (12 x 4 = 48) and 64 characters high (64 x 16 = 1024). This four bitplane image is mapped into the OSD character map memory as shown in . This bitmap is divided into six blocks, each block being 1 byte wide. These blocks are loaded into the SiI859/861 OSD memory space sequentially, starting from the first block up to the sixth block. For example, the bits which represent character # 0 are located in hexadecimal address ranges: 00-0F, 400-40F, 800-80F, C00-C0F, 1000-100F, and 1400-140F. also shows a graphical representation of this bit-plane arrangement.

Table 10. OSD character map memory configuration

Character # (hex)	Bitplane 0			Bitplane 1			Bitplane 2			Bitplane 3		
	First	Block	Second	Block	Third	Block	Fourth	Block	Fifth	Block	Sixth	Block
	Hex	addr	Hex	addr	Hex	addr	Hex	addr	Hex	addr	Hex	addr
0 (00)	00 -	0F	400 -	40F	800 -	80F	C00 -	C0F	1000 -	100F	1400 -	140F
1 (01)	10 -	1F	410 -	40F	810 -	81F	C10 -	C1F	1010 -	101F	1410 -	141F
2 (02)	20 -	2F	420 -	40F	820 -	82F	C20 -	C2F	1020 -	102F	1420 -	142F
3 (03)	30 -	3F	430 -	40F	830 -	83F	C30 -	C3F	1030 -	103F	1430 -	143F
4 (04)	40 -	4F	440 -	40F	840 -	84F	C40 -	C4F	1040 -	104F	1440 -	144F
5 (05)	50 -	5F	450 -	40F	850 -	85F	C50 -	C5F	1050 -	105F	1450 -	145F
6 (06)	60 -	6F	460 -	40F	860 -	86F	C60 -	C6F	1060 -	106F	1460 -	146F
7 (07)	70 -	7F	470 -	40F	870 -	87F	C70 -	C7F	1070 -	107F	1470 -	147F
8 (08)	80 -	8F	480 -	48F	880 -	88F	C80 -	C8F	1080 -	108F	1480 -	148F
9 (09)	90 -	9F	490 -	49F	890 -	89F	C90 -	C9F	1090 -	109F	1490 -	149F
10 (0A)	A0 -	AF	4A0 -	4AF	8A0 -	8AF	CA0 -	CAF	10A0 -	10AF	14A0 -	14AF
11 (0B)	B0 -	BF	4B0 -	4BF	8B0 -	8BF	CB0 -	CBF	10B0 -	10BF	14B0 -	14BF
12 (0C)	C0 -	CF	4C0 -	4CF	8C0 -	8CF	CC0 -	CCF	10C0 -	10CF	14C0 -	14CF
13 (0D)	D0 -	DF	4D0 -	4DF	8D0 -	8DF	CD0 -	CDF	10D0 -	10DF	14D0 -	14DF
14 (0E)	E0 -	EF	4E0 -	4EF	8E0 -	8EF	CE0 -	CEF	10E0 -	10EF	14E0 -	14EF
15 (0F)	F0 -	FF	4F0 -	4FF	8F0 -	8FF	CF0 -	CFF	10F0 -	10FF	14F0 -	14FF
16 (10)	100 -	10F	500 -	50F	900 -	90F	D00 -	D0F	1100 -	110F	1500 -	150F
17 (11)	110 -	11F	510 -	51F	910 -	91F	D10 -	D1F	1110 -	111F	1510 -	151F
18 (12)	120 -	12F	520 -	52F	920 -	92F	D20 -	D2F	1120 -	112F	1520 -	152F
19 (13)	130 -	13F	530 -	53F	930 -	93F	D30 -	D3F	1130 -	113F	1530 -	153F
20 (14)	140 -	14F	540 -	54F	940 -	94F	D40 -	D4F	1140 -	114F	1540 -	154F
21 (15)	150 -	15F	550 -	55F	950 -	95F	D50 -	D5F	1150 -	115F	1550 -	155F
22 (16)	160 -	16F	560 -	56F	960 -	96F	D60 -	D6F	1160 -	116F	1560 -	156F
23 (17)	170 -	17F	570 -	57F	970 -	97F	D70 -	D7F	1170 -	117F	1570 -	157F
24 (18)	180 -	18F	580 -	58F	980 -	98F	D80 -	D8F	1180 -	118F	1580 -	158F
25 (19)	190 -	19F	590 -	59F	990 -	99F	D90 -	D9F	1190 -	119F	1590 -	159F
26 (1A)	1A0 -	1AF	5A0 -	5AF	9A0 -	9AF	DA0 -	DAF	11A0 -	11AF	15A0 -	15AF
27 (1B)	1B0 -	1BF	5B0 -	5BF	9B0 -	9BF	DB0 -	DBF	11B0 -	11BF	15B0 -	15BF
28 (1C)	1C0 -	1CF	5C0 -	5CF	9C0 -	9CF	DC0 -	DCF	11C0 -	11CF	15C0 -	15CF
29 (1D)	1D0 -	1DF	5D0 -	5DF	9D0 -	9DF	DD0 -	DDF	11D0 -	11DF	15D0 -	15DF
30 (1E)	1E0 -	1EF	5E0 -	5EF	9E0 -	9EF	DE0 -	DEF	11E0 -	11EF	15E0 -	15EF
31 (1F)	1F0 -	1FF	5F0 -	5FF	9F0 -	9FF	DF0 -	DFF	11F0 -	11FF	15F0 -	15FF
32 (20)	200 -	20F	600 -	60F	A00 -	A0F	E00 -	E0F	1200 -	120F	1600 -	160F
33 (21)	210 -	21F	610 -	61F	A10 -	A1F	E10 -	E1F	1210 -	121F	1610 -	161F
34 (22)	220 -	22F	620 -	62F	A20 -	A2F	E20 -	E2F	1220 -	122F	1620 -	162F
35 (23)	230 -	23F	630 -	63F	A30 -	A3F	E30 -	E3F	1230 -	123F	1630 -	163F
36 (24)	240 -	24F	640 -	64F	A40 -	A4F	E40 -	E4F	1240 -	124F	1640 -	164F
37 (25)	250 -	25F	650 -	65F	A50 -	A5F	E50 -	E5F	1250 -	125F	1650 -	165F
38 (26)	260 -	26F	660 -	66F	A60 -	A6F	E60 -	E6F	1260 -	126F	1660 -	166F
39 (27)	270 -	27F	670 -	67F	A70 -	A7F	E70 -	E7F	1270 -	127F	1670 -	167F
40 (28)	280 -	28F	680 -	68F	A80 -	A8F	E80 -	E8F	1280 -	128F	1680 -	168F
41 (29)	290 -	29F	690 -	69F	A90 -	A9F	E90 -	E9F	1290 -	129F	1690 -	169F
42 (2A)	2A0 -	2AF	6A0 -	6AF	AA0 -	AAF	EA0 -	EAF	12A0 -	12AF	16A0 -	16AF
43 (2B)	2B0 -	2BF	6B0 -	6BF	AB0 -	ABF	EB0 -	EBF	12B0 -	12BF	16B0 -	16BF
44 (2C)	2C0 -	2CF	6C0 -	6CF	AC0 -	ACF	EC0 -	ECF	12C0 -	12CF	16C0 -	16CF
45 (2D)	2D0 -	2DF	6D0 -	6DF	AD0 -	ADF	ED0 -	EDF	12D0 -	12DF	16D0 -	16DF
46 (2E)	2E0 -	2EF	6E0 -	6EF	AE0 -	AEF	EE0 -	EEF	12E0 -	12EF	16E0 -	16EF
47 (2F)	2F0 -	2FF	6F0 -	6FF	AF0 -	AFF	EF0 -	EFF	12F0 -	12FF	16F0 -	16FF
48 (30)	300 -	30F	700 -	70F	B00 -	B0F	F00 -	F0F	1300 -	130F	1700 -	170F
49 (31)	310 -	31F	710 -	71F	B10 -	B1F	F10 -	F1F	1310 -	131F	1710 -	171F
50 (32)	320 -	32F	720 -	72F	B20 -	B2F	F20 -	F2F	1320 -	132F	1720 -	172F
51 (33)	330 -	33F	730 -	73F	B30 -	B3F	F30 -	F3F	1330 -	133F	1730 -	173F
52 (34)	340 -	34F	740 -	74F	B40 -	B4F	F40 -	F4F	1340 -	134F	1740 -	174F
53 (35)	350 -	35F	750 -	75F	B50 -	B5F	F50 -	F5F	1350 -	135F	1750 -	175F

Character # (hex)	Bitplane 0			Bitplane 1			Bitplane 2			Bitplane 3		
	First	Block	Second	Block	Third	Block	Fourth	Block	Fifth	Block	Sixth	Block
	Hex	addr	Hex	addr	Hex	addr	Hex	addr	Hex	addr	Hex	addr
54 (36)	360 -	36F	760 -	76F	B60 -	B6F	F60 -	F6F	1360 -	136F	1760 -	176F
55 (37)	370 -	37F	770 -	77F	B70 -	B7F	F70 -	F7F	1370 -	137F	1770 -	177F
56 (38)	380 -	38F	780 -	78F	B80 -	B8F	F80 -	F8F	1380 -	138F	1780 -	178F
57 (39)	390 -	39F	790 -	79F	B90 -	B9F	F90 -	F9F	1390 -	139F	1790 -	179F
58 (3A)	3A0 -	3AF	7A0 -	7AF	BA0 -	BAF	FA0 -	FAF	13A0 -	13AF	17A0 -	17AF
59 (3B)	3B0 -	3BF	7B0 -	7BF	BB0 -	BBF	FB0 -	FBF	13B0 -	13BF	17B0 -	17BF
60 (3C)	3C0 -	3CF	7C0 -	7CF	BC0 -	BCF	FC0 -	FCF	13C0 -	13CF	17C0 -	17CF
61 (3D)	3D0 -	3DF	7D0 -	7DF	BD0 -	BDF	FD0 -	FDF	13D0 -	13DF	17D0 -	17DF
62 (3E)	3E0 -	3EF	7E0 -	7EF	BE0 -	BEF	FE0 -	FEF	13E0 -	13EF	17E0 -	17EF
63 (3F)	3F0 -	3FF	7F0 -	7FF	BF0 -	BFF	FF0 -	FFF	13F0 -	13FF	17F0 -	17FF

continued…

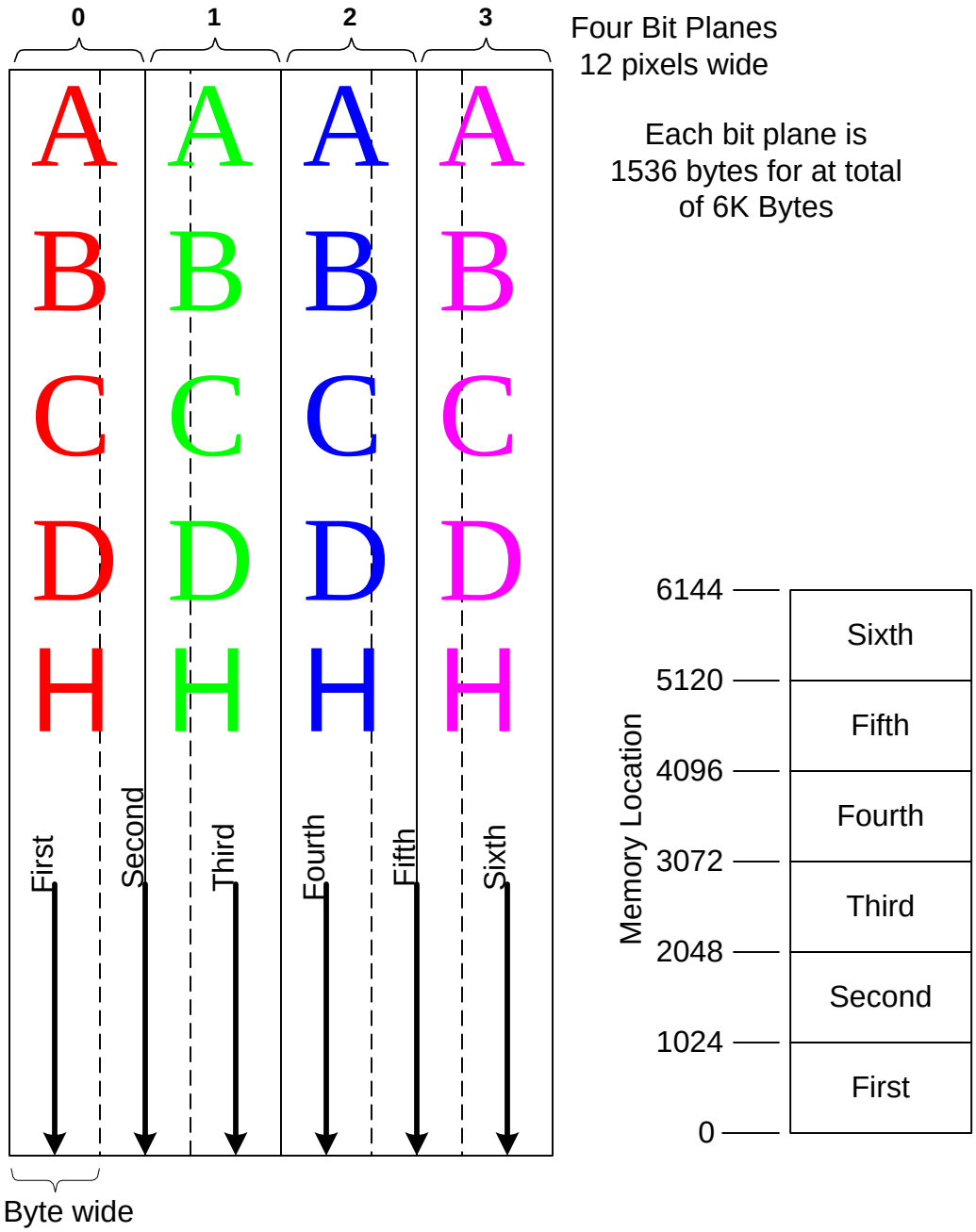


Figure 14. Character OSD Bitmap Structure

Message Memory:
The OSD Message Memory consists of 1024 bytes that are used to choose the characters to be displayed on screen. Each location is 1-byte, the lower 6-bits point to one of the 64 characters. Bit 6 is used to double the character (24x32 pixels) and Bit 7 is used to highlight the character (use reversed color look up table). When doubling a character, the entire row of the OSD must be doubled. describes the OSD Message Memory structure.

OSD Message Memory Space: 1024 bytes							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Highlight 1 = highlight 0 = normal	Double 1 = double 0 = normal	Character[5:0]. Points to one of the 64 characters.					

Table 11. OSD Message Memory

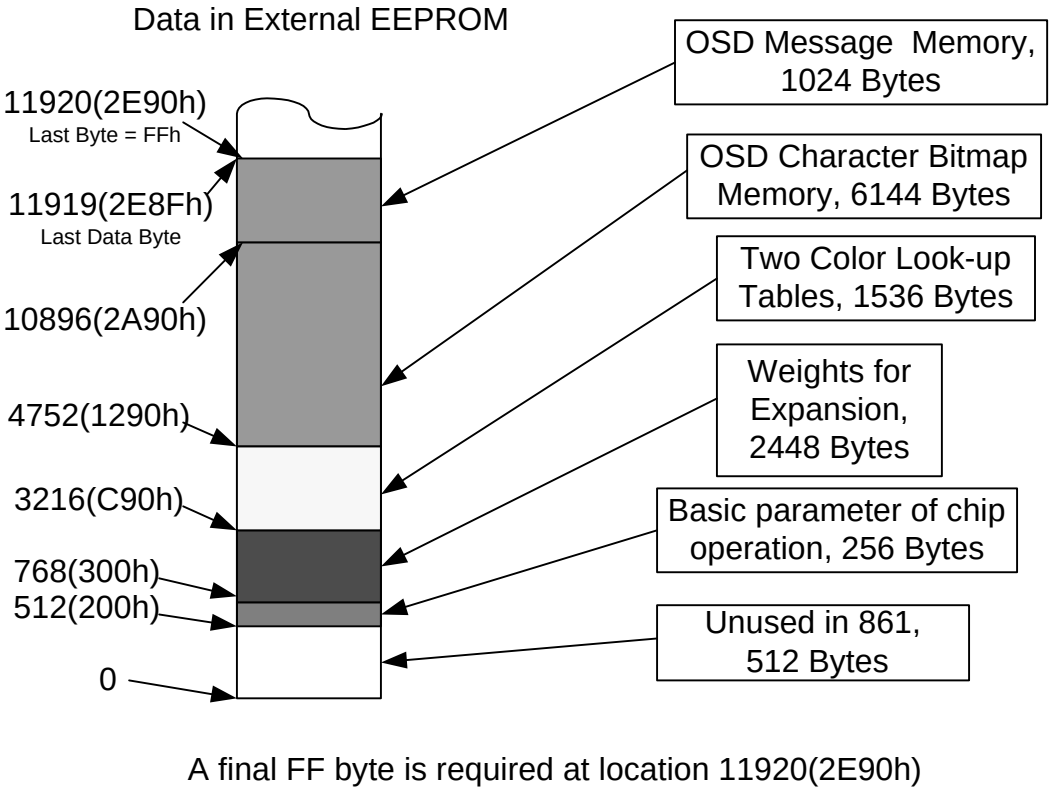


Figure 15. Character OSD PROM Mapping

20. High-bandwidth Digital Content Protection (HDCP)

The 861 implements HDCP according to the 1.0 specification. This specification is available at the Digital Content Protection website at: www.digital-cp.com. Designing a compliant HDCP system using the SiI861 is very straightforward, as shown in the figure below. Two dedicated I^2C buses are used for HDCP support, one bus connects to an external EEPROM which contains the HDCP keys, the other bus connects to the DDC bus and is used by the host transmitter side to control HDCP. These two I^2C buses are completely separate from the configuration I^2C bus that is used to configure the 861, which means the SiI861 has a total of three I^2C buses.

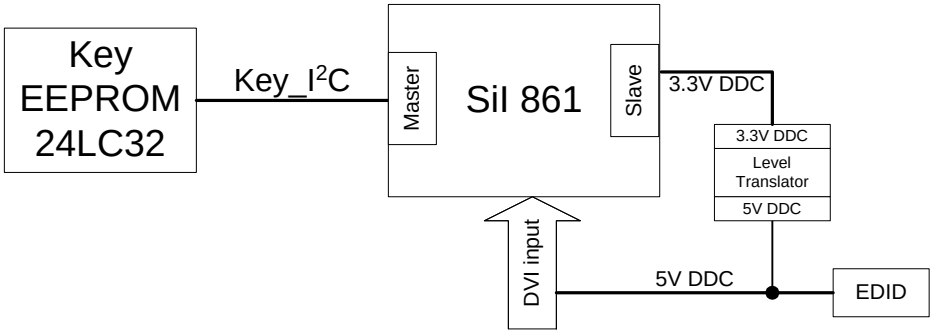


Figure 16. HDCP Implementation Block Diagram

HDCP Keys:
The 861 requires the HDCP keys to be stored in an external EEPROM that is compatible with a 24LC32. The I^2C device address of this EEPROM should be 0b1010011x (0xA6 hex). On a 24LC32 device, this will require the A0, A1, and A2 address pins to be connected as shown below.

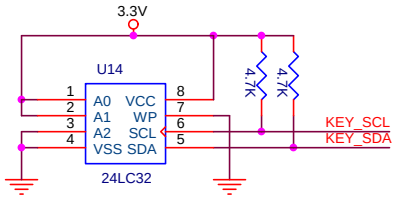


Figure 17. HDCP Serial EEPROM

After reset, the SiI861 will become a master on the Key_I2C bus and begin reading the HDCP keys, which are used in the cipher engine when HDCP is enabled. If there is no EEPROM present, the SiI861 will timeout on the Key_I2C bus – in this case the cipher engine will not have valid keys and will not be able to de-crypt any incoming HDCP data, however it will be able to accept and display any non-encrypted or normal data.

HDCP DDC / I^2C Port:
The HDCP protocol requires values to be exchanged between the video transmitter and video receiver. These values are exchanged over the DDC channel of the DVI interface. The DDC channel follows the I^2C serial protocol. The seven-bit device address of the video receiver on the primary link must be at address 0b0111010x, or 0x74 hex. In an SiI861 design, the SiI861 is the video receiver and will have a connection to the DDC bus with a slave address of 0x74 hex. The SiI861 cannot connect directly to the DDC bus because the DDC bus is a 5-volt level bus, and the inputs are not 5 volt tolerant. In order to interface the SiI861 with the DDC channel, a level translator circuit is required. One method of converting the voltage level is to use a dual N-channel transistor, Fairchild part # NDC7002N. This is shown in .

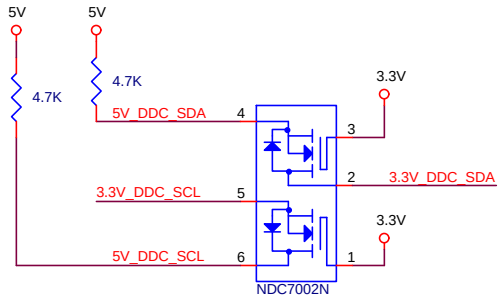


Figure 18. DDC Voltage Level Translation for HDCP I2C Port

HDCP Register Space

The register mapping of the HDCP registers accessed through the DDC bus at address 0x74 hex are shown in . These registers conform to the HDCP Revision 1.0 specification, please refer to that document for further information on the function and control of HDCP.

Table 12. HDCP Register Address Locations (Device address 0x74 hex)

Offset (hex)	Name	Size in Bytes	Rd/Wr	Function
0x00	*Bksv*	5	Rd	Video receiver KSV. This value must always be available for reading, and may be used to determine that the video receiver is HDCP capable
0x05	Rsvd	3	Rd	All byes read as 0x00
0x08	R_i'	2	Rd	Link verification response. Updated every 128th frame. It is recommended that graphics systems protect against errors in the I^2C transmission by re-reading this value when unexpected values are received. This calue must be available at all times between updates. R_0' must be available a maximum of 100 ms after *Aksv* is received. Subsequent R_i' values must be available a maximum of 128 pixel clocks following the assertion of CTL3.
0x0A	Rsvd	6	Rd	All bytes read as 0x00
0x10	*Aksv*	5	Wr	Video transmitter KSV. Writes to this multi-byte value are written least significant byte first. The final write to 0x14 triggers the authentication sequence in the display device.
0x15	RSVD	3	Rd	All bytes read as 0x00
0x18	*An*	8	Wr	Session random number. This multi-byte value must be written by the graphics system before the KSV is written.
0x20	*V*	20	Rd	Not used in SiI861 – for video repeaters only. Read as all 0's
0x34	Rsvd	12	Rd	All bytes read as 0x00
0x40	*Bcaps*	1	Rd	Bit 7: Reserved. Read as zero. Bit 6: Repeater,Video repeater capability. Read as 0 in SiI861, it does not support repeater function Bit 5: READY, KSV FIFO ready. Read as 0 in 861, only used for repeaters Bit 4: FAST. Read as 1, SiI861 supports 400 KHz transfers
0x41	*Bstatus*	2	Rd	Not used in SiI861 – for video repeaters only. Read as all 0's
0x43	KSV FIFO	1	Rd	Not used in SiI861 – for video repeaters only. Read as all 0's
0x44	Rsvd	179	Rd	All bytes read as 0x00
0xFF	dbg	1	Rd/Wr	Reserved debug register

21. Parallel Output Data Mapping

The following table shows the output data mapping in one pixel per clock mode for the SiI859/861. This output data mapping is dependent upon the SiI PanelLink transmitters having the exact same type of input data mappings. Please refer to the SiI PanelLink transmitter for the specific input data mappings.

	SiI859/861	
	1-Pixel/Clock Output	
	18bpp	**24bpp**
BLUE[7:0]	QE[7:2]	QE[7:0]
GREEN[7:0]	QE[15:10]	QE[15:8]
RED[7:0]	QE[23:18]	QE[23:16]

Table 21. One Pixel/Clock Mode Data Mapping

	SiI859/861		
	2-Pixel/Clock Output		
	18bpp	**24bpp**	
BLUE[7:0] - 0	QE[7:2]	QE[7:0]	First Pixel
GREEN[7:0] – 0	QE[15:10]	QE[15:8]	
RED[7:0] – 0	QE[23:18]	QE[23:16]	
BLUE[7:0] – 1	QO[7:2]	QO[7:0]	Second Pixel
GREEN[7:0] – 1	QO[15:10]	QO[15:8]	
RED[7:0] – 1	QO[23:18]	QO[23:16]	

Table 22. Two Pixel/Clock Mode Data Mapping

Note: For 18-bit mode, the Flat Panel Timing Controller interfaces to the SiI861 exactly the same as in the 24-bit mode; however, only 6-bits per channel (color) are interfaced instead of the full 8. As can be seen from the above table, the data mapping for less than 24-bit per pixel interfaces are MSB justified.

22. LVDS Output Data Mapping

The SiI861 has an integrated, one channel LVDS transmitter that can be used to drive a panel with a one channel, LVDS receiver. When using the internal LVDS transmitter, the output of the SiI861 should be in 1 pixel/clock mode. If a higher resolution panel is used which requires two LVDS channels, for example an SXGA panel with two receivers, then two external LVDS transmitters must be used by connecting them to the SiI861 parallel output which is set for 2 pixel/clock mode. This is required because the internal LVDS transmitter cannot be synchronized with an external transmitter.

The SiI861 supports two data mappings on the LVDS transmitter selectable by register RMDT[3]. The LVDS transmitter has four differential data pairs, each pair will serialize 7-bits of data. These data mappings must match the data mapping of the LVDS receiver. The data mappings are:

1. "MSB" (RMDT[3] = 1): This is backward compatible with 6-bit LVDS receivers and the most common. In this mode the first 6 MSB's for each of the colors is sent on data pairs TX_0, TX_1, and TX_2. The remaining two LSB's are sent on the fourth data pair, TX_3. Most panels use this mapping.
2. "LSB" (RMDT[3] = 0): In this mode the first 6 LSB's for each of the colors is sent on data pairs TX_0, TX_1, and TX_2. The remaining two MSB's are sent on the fourth data pair, TX_3.

LVDS MSB mapping RMDT[3] = 1	
Red[2:7], Green2	TX_0
Green[3:7],Blue[2:3]	TX_1
Blue[4:7],HSYNC, VSYNC,DE	TX_2
Red[0:1],Green[0:1], Blue[0:1]	TX_3

Table 21. LVDS MSB Data Mapping

LVDS LSB mapping RMDT[3] = 0	
Red[0:5], Green0	TX_0
Green[1:5],Blue[0:1]	TX_1
Blue[2:5],HSYNC, VSYNC,DE	TX_2
Red[6:7],Green[6:7], Blue[6:7]	TX_3

Table 22. LVDS LSB Data Mapping

23. Register Index

Table 13. Group 1 Register Address Locations

Hex	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
00	LIN1	LIN2	ICC1	ICC2	IRC1	IRC2	PLC1	PLC2	PLR1	PLR2		XIRW				
10					ICP1	ICP2	IRP1	IRP2								
20																
30													OFSH	OFSL	SAD1	SAD2
40	CL3R	CL3G	CL3B	CL4R	CL4G	CL4B	CL5R	CL5G	CL5B	CL6R	CL6G	CL6B	CL7R	CL7G	CL7B	CL8R
50	CL8G	CL8B	CL9R	CL9G	CL9B	CLAR	CLAG	CLAB	CLBR	CLBG	CLBB	CLCR	CLCG	CLCB	CLDR	CLDG
60	CLDB	CLER	CLEG	CLEB	CLFR	CLFG	CLFB									
70																
80	OSDE	OSBR	OSBG	OSBB	OUL1	OUL2	OUL3	OUL4	OSW1	OSW2	OSH1	OSH2	CL1R	CL1G	CL1B	CL2R
90	CL2G	CL2B	OLS1	OLS2	ADD1	ADD2	FLR1	FLR2	RMDT	VSW1	VSW2	VSD1	VSD2	VSD3	HSWD	HSDL
A0	POLT	ADE1	ADE2	AHDL	IFR1	IFR2	IFR3	LWD1	LWD2	ORS1	ORS2	LLS1	LLS2	BLP1	BLP2	BLP3
B0	BLPH	BLST	LOSD	FFR1	FFR2	FFR3	FDIV	IDIV	D4xx	D4xx	D4xx	D4xx	D4xx	D4xx	D4xx	D4xx
C0	D4xx	D4xx	D4xx	D4xx	D4xx	D4xx	D4xx	D4xx	D4xx	D4xx	D4xx	D4xx	D4xx	D4xx	D4xx	D4xx
D0	D4xx	D4xx	D4xx	D4xx	D4xx	D4xx	D4xx	D4xx	D2xx	D2xx	D2xx	D2xx	D2xx	D2xx	D2xx	D2xx
E0	VHD1	VHD2	VHBN	XRW1	XRW2	AHC1	AHC2	AVC1	AVC2	ADN1	ADN2	AUP1	AUP2	AUP3	AUPH	AUST
F0	HBN1	HBN2	VBN1	VBN2	SLR1	SLR2	SFR1	SFR2	SFR3	LWB1	LWB2	OSDD				

Table 14. Group 1 Bit Registers

Function	Name	Address	Setting	
Reset backlight PWM when Vsync occurs	BLST[7]	B1[7]	1	Reset counter when Vsync occurs
			0	Counter free runs
Backlight PWM always low	BLST[6]	B1[6]	1	Keep backlight PWM pin always low
			0	Output timing of PWM based on BLxx registers
Backlight PWM always high	BLST[5]	B1[5]	1	Keep backlight PWM pin always high
			0	Output timing of PWM based on BLxx registers
Reset audio PWM when Vsync occurs	AUST[7]	EF[7]	1	Reset counter when Vsync occurs
			0	Counter free runs
Audio PWM always low	AUST[6]	EF[6]	1	Keep backlight PWM pin always low
			0	Output timing of PWM based on BLxx registers
Audio PWM always high	AUST[5]	EF[5]	1	Keep backlight PWM pin always high
			0	Output timing of PWM based on BLxx registers
Enable frame rate checking using registers FFRx and SFRx	FLR1[6]	96[6]	1	Enable
			0	Disable
Enable line rate checking using registers FLRx and SLRx	FLR1[5]	96[5]	1	Enable
			0	Disable
Enable automatic window boxing progressive	LWB1[5]	F9[5]	1	Enable
			0	Disable
Enable automatic window boxing once	LWB1[4]	F9[4]	1	Enable
			0	Disable
CTL Output and TPCLK	RMDT[7]	98[7]	1	CLT[3:1] from transmitter are output on CTL[3:1]
			0	Input Vsync,Hsync, and DE are output on CTL[3:1]
Lock Resolution	RMDT[6]	98[6]	1	Disable update of input resolution, IRC and ICC
			0	Enable scaling to changed based on input resolution
Fill Hsync from beginning	RMDT[5]	98[5]	1	Enable inserting Hsync pulse in blanking period
			0	Disable filling Hsync pulses from beginning
Enable staggered clock	RMDT[4]	98[4]	1	Enable (only works in 2-pixels/clock mode)
			0	Disable

Function	Name	Address	Setting	
LVDS Data Mapping (see page 105)	RMDT[3]	98[3]	1	MSB LVDS mapping
			0	LSB LVDS mapping
Output Mode: 1 or 2 pixels/clock	RMDT[2]	98[2]	1	One pixel per clock
			0	Two pixels per clock
Enable negative weights	RMDT[1]	98[1]	1	Enable negative weight processing
			0	Disable negative weight processing
Load OSD from EEPROM	OSDE[7]	80[7]	1	Load OSD data (7 KB) after reset
			0	Disable loading of OSD data after reset
Enable User OSD	OSDE[6]	80[6]	1	Display User OSD on screen
			0	Do not display User OSD
Enable Loss of Sync OSD	OSDE[5]	80[5]	1	If DE input is lost, display Loss of Sync OSD
			0	Do not display Loss of Sync OSD
Enable Out of Range OSD	OSDE[4]	80[4]	1	If input is out of range, display Out of Range OSD
			0	Do not display Out of Range OSD
Sync Lost Status (Read Only)	OSDE[3]	80[3]	1	Input DE has been lost
			0	Input DE is present with active video coming in
Out of Range Status (Read Only)	OSDE[2]	80[2]	1	Input out of acceptable ranges
			0	Input within acceptable ranges
Detection Method of Loss of Sync	OSDE[1]	80[1]	1	Use SCDT from PanelLink receiver core
			0	Count timing of input DE
Power Management Mode	OSDE[0]	80[0]	1	Non-DVI
			0	DVI mode
Enable one-to-one Scaling	ICC1[7]	02[7]	1	Enable scaling filter to be used when input=output
			0	Disable scaling filter when input=output
Reset Cipher engine	ICC1[6]	02[6]	1	Reset Cipher engine
			0	Enable Cipher engine
Bypass Output Gamma Table	ICC1[5]	02[5]	1	Data bypasses output gamma table
			0	Data goes through gamma table
Bypass Input Gamma Table	ICC1[4]	02[4]	1	Data bypasses input gamma table
			0	Data goes through input gamma table
VHS Counted. Period of Hsync pulses in vertical blanking	VHD1[6]	E0[6]	1	Use VHD as the period in number of XCLKS
			0	Use the output line time
Panel Output Tristate	VHD1[5]	E0[5]	1	Output DE,Hsync,Vsync,ODCK and data tri-state
			0	Normal operation
Dithering	POLT[6]	A0[6]	1	Enable 18-bit to 24-bit dithering
			0	Disable
LVDS Disable	POLT[5]	A0[5]	1	Disable LVDS transmitter
			0	Enable LVDS transmitter
Bypass Mode (for testing only)	POLT[4]	A0[4]	1	PanelLink receiver core outputs directly to panel
			0	Normal operation
Vsync Polarity	POLT[3]	A0[3]	1	Active high
			0	Active low
DE polatiry	POLT[2]	A0[2]	1	Active high
			0	Active low
Clock polarity (ODCK)	POLT[1]	A0[1]	1	Data valid on falling edge
			0	Data valid on rising edge
Hsync polarity	POLT[0]	A0[0]	1	Active high
			0	Active low
Power down mode	FDIV[7]	B6[7]	1	Power down entire chip when PD# is asserted low
			0	Pull down panel outputs when PD# is asserted low

Function	Name	Address	Setting	
Clock multiplier (5x) power down	FDIV[6]	B6[6]	1	Power down 5x clock generator
			0	5x clock generator operational
Enable Mode Change Status	FDIV[5]	B6[5]	1	Enable mode change status clear bit using FDIV[4]
			0	Disable mode change status clear bit.
Mode Change Status	FDIV[4]	B6[4]	1	Set to 1 when input rows or columns changes
			0	Writing a 0 will clear this bit if FDIV[5]=1
Line Rate too Fast Status (read only)	FDIV[3]	B6[3]	1	Line rate is too fast
			0	Line rate in range
Frame Rate too Fast Status (read only)	FDIV[2]	B6[2]	1	Frame rate too fast
			0	Frame rate in range
Windox boxing OOR status (read only)	FDIV[1]	B6[1]	1	OOR due to window boxing
			0	Not OOR due to window boxing
XCLK too slow status (read only)	FDIV[0]	B6[0]	1	XCLK frequency is too slow to keep up with input
			0	XCLK frequency is not too slow
Bypass PLL clock generator	IDIV[7]	B7[7]	1	Bypass clock generator, internal XCLK = input
			0	XLCK generated by clock generator = 5 * input
Manual Window Box (Do not use with automatic modes)	XRW1[3]	E3[3]	1	Enable manual window boxing
			0	Disable manual window boxing

Register Definitions

Table 15. New Registers in 861

Name	Description	Page #	Access	Group Address	Register Address	PROM Address
PLC1	Upper 3-bits of 11-bit total panel size output columns	48	W	01	6(6h)	206h
PLC2	Lower 8-bits of 11-bit total panel size output columns	48	W	01	7(7h)	207h
PLR1	Upper 3-bits of 11-bit total panel size output rows	48	W	01	8(8h)	208h
PLR2	Lower 8-bits of 11-bit total panel size output rows	48	W	01	9(9h)	209h
LIN1	Upper 4-bits of 12-bit total TMDS line time	77	R	01	0(0h)	200h
LIN2	Lower 8-bits of 12-bit total TMDS line time	77	R	01	1(1h)	201h
RCTL	3-bit value [2:0]. Receiver sync off, receiver test, cksel. Set this register always to 07H.		W	01	10(Ah)	RESERVED 20Ah always =07h
HBN1	[10:0]. Fixed hblank in XCLKS	49	RW	01	240(F0h)	2F0h
HBN2	[10:0]. Fixed hblank in XCLKS	49	RW	01	241(F1h)	2F1h
VBN1	[10:0]. Fixed vblank in rows. VBN[10]=enable fix hblank	50	RW	01	242(F2h)	2F2h
VBN2	[10:0]. Fixed vblank in rows. VBN[10]=enable fix hblank	50	RW	01	243(F3h)	2F3h
LOSD	[3:0]. Ide-los de-assert delay msbs	51	W	01	178(B2h)	2B2h
ADD1	Tmds polarity, avs polarity, ahs polarity, ahs to ade high msb	92	W	01	148(94h)	294h
ADD2	ahs to ade high lsb	92	W	01	149(95h)	295h
ADE1	Ade high [10:0]	92	W	01	161(A1h)	2A1h
ADE2	Ade high [10:0]	92	W	01	162(A2h)	2A2h
AHDL	[6:0] number ahs between avs and ade	92	W	01	163(A3h)	2A3h
AHC1	[10:0] number of XCLKS between ahs	92	RW	01	229(E5h)	2E5h
AHC2	[10:0] number of XCLKS between ahs	92	RW	01	230(E6h)	2E6h
AVC1	[10:0] number ahs between avs	92	RW	01	231(E7h)	2E7h
AVC2	[10:0] number ahs between avs	92	RW	01	232(E8h)	2E8h
ADN1	[10:0] number of ade per avs	92	W	01	233(E9h)	2E9h
ADN2	[10:0] number of ade per avs	92	W	01	234(EAh)	2EAh
OSDD	Delay in los/oor displayed, counted in frames	51	W	01	251(FBh)	2FBh
P0P1	[23:0] PWM0 period	52	W	01	173(ADh)	2ADh
P0P2	[23:0] PWM0 period	52	W	01	174(AEh)	2AEh
P0P3	[23:0] PWM0 period	52	W	01	175(AFh)	2AFh
P0PH	PWM0 time high	53	RW	01	176(B0h)	2B0h
P0ST	PWM0 button control and change step	53	W	01	177(B1h)	2B1h
P1P1	[23:0] PWM1 Period	54	W	01	235(EBh)	2EBh
P1P2	[23:0] PWM1 Period	54	W	01	236(ECh)	2ECh
P1P3	[23:0] PWM1 Period	54	W	01	237(EDh)	2EDh
P1PH	PWM1 time high	55	RW	01	238(EEh)	2EEh
P1ST	PWM1 button control and change step	55	W	01	239(EFh)	2EFh
FLR1	[15:0] Fast line rate limit	56	W	01	150(96h)	296h
FLR2	[15:0] Fast line rate limit	56	W	01	151(97h)	297h
SLR1	[12:0] Slow line rate limit	57	W	01	244(F4h)	2F4h
SLR2	[12:0] Slow line rate limit	57	W	01	245(F5h)	2F5h
SFR1	[23:0] Slow frame rate limit	58	W	01	246(F6h)	2F6h

Name	Description	Page #	Access	Group Address	Register Address	PROM Address
SFR2	[23:0] Slow frame rate limit	58	W	01	247(F7h)	2F7h
SFR3	[23:0] Slow frame rate limit	58	W	01	248(F8h)	2F8h
LWB1	[12:0] Automatic window box line rate	59	W	01	249(F9h)	2F9h
LWB2	[12:0] Automatic window box line rate	59	W	01	250(FAh)	2FAh
XIRW	Number of rows to add for window boxing	59	W	01	11(Bh)	20Bh
OFSH	[15:8] OSD re-download eeprom offset address, high order	60	R/W	01	60(3Ch)	23Ch
OFSL	[7:0] OSD re-download eeprom offset address, low order	60	R/W	01	61(3Dh)	23Dh

Table 16. Input / Output Configuration Register

Name	Description	Page #	Access	Group Address	Register Address	PROM Address
RMDT	Resolution, Mode, Drive, and Termination Settings	61	R/W	01	152(98h)	664(298h)

Table 17. OSD Registers

Name	Description	Page #	Access	Group Address	Register Address	PROM Address
OSDE	OSD Control and Activity Indicator	62	R/W	01	128(80h)	640(280h)
OSBR	Screen Background Color on Loss of Sync or Out of Range – 8-bit Red Component	64	W	01	129(81h)	641(281h)
OSBG	Screen Background Color on Loss of Sync or Out of Range – 8-bit Green Component	64	W	01	130(82h)	642(282h)
OSBB	Screen Background Color on Loss of Sync or Out of Range – 8-bit Blue Component	64	W	01	131(83h)	643(283h)
OUL1	Upper 3-bits of 11-bit total Upper Left Corner Position of OSD Message Window plus 2 pixels - Horizontal	65	W	01	132(84h)	644(284h)
OUL2	Lower 8-bits of 11-bit total Upper Left Corner Position of OSD Message Window plus 2 pixels - Horizontal	65	W	01	133(85h)	645(285h)
OUL3	Upper 2-bits of 10-bit total Upper Left Corner Position of OSD Message Window - Vertical	66	W	01	134(86h)	646(286h)
OLU4	Lower 8-bits of 10-bit total Upper Left Corner Position of OSD Message Window - Vertical	66	W	01	135(87h)	647(287h)
OSW1	Upper 3-bits of 11-bit total Width of OSD Message Window. Must be multiple of 12 for character based OSD.	67	W	01	136(88h)	648(288h)
OSW2	Lower 8-bits of 11-bit total Width of OSD Message Window. Must be multiple of 12 for character based OSD.	67	W	01	137(89h)	649(289h)
OSH1	Upper 2-bits of 10-bit total Height of OSD Message Window. Must be multiple of 16 for character based OSD.	68	W	01	138(8Ah)	650(28Ah)

Name	Description	Page #	Access	Group Address	Register Address	PROM Address
OSH2	Lower 8-bits of 10-bit total Height of OSD Message Window. Must be multiple of 16 for character based OSD.	68	W	01	139(8Bh)	651(28Bh)
OLS1	Upper 4-bits of 12-bit total OSD Message Window Starting Memory Location	69	W	01	146(92h)	658(292h)
OLS2	Lower 8-bits of 12-bit total OSD Message Window Starting Memory Location	69	W	01	147(93h)	659(293h)
LLS1	Upper 4-bits of 12-bit total “Loss of Sync” OSD Message Window Starting Memory Location	70	W	01	171(ABh)	683(2ABh)
LLS2	Lower 8-bits of 12-bit total “Loss of Sync” OSD Message Window Starting Memory Location	70	W	01	172(ACh)	684(2ACh)
ORS1	Upper 4-bits of 12-bit total “Out of Range” OSD Message Window Starting Memory Location	71	W	01	169(A9h)	681(2A9h)
ORS2	Lower 8-bits of 12-bit total “Out of Range” OSD Message Window Starting Memory Location	71	W	01	170(AAh)	682(2AAh)
O####	8-bit OSD Memory Content	72	W	11	0(00h) to 6143(17FFh)	2624(A40h) to 8768(2240h)

Table 18. Character Based OSD Registers

Name	Description	Page #	Access	Group Address	Register Address	PROM Address
T####	Character based text	90	R/W	11	6144(1800) to 7168(17FF)	8769(2241h) to 9791263Fh)
CL1R	OSD Red value color lookup table entry 1	91	W	01	140(8Ch)	140(28Ch)
CL1G	OSD Green value color lookup table entry 1	91	W	01	141(8Dh)	653(28Dh)
CL1B	OSD Blue value color lookup table entry 1	91	W	01	142(8Eh)	654(28Eh)
CL2R	OSD Red value color lookup table entry 2	91	W	01	143(8Fh)	655(28Fh)
CL2G	OSD Green value color lookup table entry 2	91	W	01	144(90h)	656(290h)
CL2B	OSD Blue value color lookup table entry 2	91	W	01	145(91h)	657(291h)
CL3R	OSD Red value color lookup table entry 3	91	W	01	64(40h)	576(240h)
CL3G	OSD Green value color lookup table entry 3	91	W	01	65(41h)	577(241h)
CL3B	OSD Blue value color lookup table entry 3	91	W	01	66(42h)	578(242h)
CL4R	OSD Red value color lookup table entry 4	91	W	01	67(43h)	579(243h)
CL4G	OSD Green value color lookup table entry 4	91	W	01	68(44h)	580(244h)
CL4B	OSD Blue value color lookup table entry 4	91	W	01	69(45h)	581(245h)
CL5R	OSD Red value color lookup table entry 5	91	W	01	70(46h)	582(246h)
CL5G	OSD Green value color lookup table entry 5	91	W	01	71(47h)	583(247h)
CL5B	OSD Blue value color lookup table entry 5	91	W	01	72(48h)	584(248h)
CL6R	OSD Red value color lookup table entry 6	91	W	01	73(49h)	585(249h)
CL6G	OSD Green value color lookup table entry 6	91	W	01	74(4Ah)	586(24Ah)
CL6B	OSD Blue value color lookup table entry 6	91	W	01	75(4Bh)	587(24Bh)
CL7R	OSD Red value color lookup table entry 7	91	W	01	76(4Ch)	588(24Ch)
CL7G	OSD Green value color lookup table entry 7	91	W	01	77(4Dh)	589(24Dh)
CL7B	OSD Blue value color lookup table entry 7	91	W	01	78(4Eh)	590(24Eh)
CL8R	OSD Red value color lookup table entry 8	91	W	01	79(4Fh)	591(24Fh)
CL8G	OSD Green value color lookup table entry 8	91	W	01	80(50h)	592(250h)
CL8B	OSD Blue value color lookup table entry 8	91	W	01	81(51h)	593(251h)
CL9R	OSD Red value color lookup table entry 9	91	W	01	82(52h)	594(252h)
CL9G	OSD Green value color lookup table entry 9	91	W	01	83(53h)	595(253h)
CL9B	OSD Blue value color lookup table entry 9	91	W	01	84(54h)	596(254h)
CLAR	OSD Red value color lookup table entry A	91	W	01	85(55h)	597(255h)
CLAG	OSD Green value color lookup table entry A	91	W	01	86(56h)	598(256h)
CLAB	OSD Blue value color lookup table entry A	91	W	01	87(57h)	599(257h)
CLBR	OSD Red value color lookup table entry B	91	W	01	88(58h)	600(258h)
CLBG	OSD Green value color lookup table entry B	91	W	01	89(59h)	601(259h)
CLBB	OSD Blue value color lookup table entry B	91	W	01	90(5Ah)	602(25Ah)
CLCR	OSD Red value color lookup table entry C	91	W	01	91(5Bh)	603(25Bh)
CLCG	OSD Green value color lookup table entry C	91	W	01	92(5Ch)	604(25Ch)
CLCB	OSD Blue value color lookup table entry C	91	W	01	93(5Dh)	605(25Dh)
CLDR	OSD Red value color lookup table entry D	91	W	01	94(5Eh)	606(25Eh)
CLDG	OSD Green value color lookup table entry D	91	W	01	95(5Fh)	607(25Fh)
CLDB	OSD Blue value color lookup table entry D	91	W	01	96(60h)	608(260h)
CLER	OSD Red value color lookup table entry E	91	W	01	97(61h)	609(261h)
CLEG	OSD Green value color lookup table entry E	91	W	01	98(62h)	610(262h)
CLEB	OSD Blue value color lookup table entry E	91	W	01	99(63h)	611(263h)
CLFR	OSD Red value color lookup table entry F	91	W	01	100(64h)	612(264h)
CLFG	OSD Green value color lookup table entry F	91	W	01	101(65h)	613(265h)
CLFB	OSD Blue value color lookup table entry F	91	W	01	102(66h)	614(266h)

Table 19. Input Resolution Count Registers

Name	Description	Page #	Access	Group Address	Register Address	PROM Address
ICC1	Upper 4-bits of 12-bit total Input Columns Counted on Last Frame	73	R/W	01	2(02h)	514(202h)
ICC2	Lower 8-bits of 12-bit total Input Columns Counted on Last Frame	73	R/W	01	3(03h)	515(203h)
IRC1	Upper 3-bits of 11-bit total Input Rows Counted on Last Frame	74	R/W	01	4(04h)	516(204h)
IRC2	Lower 8-bits of 11-bit total Input Rows Counted on Last Frame	74	R/W	01	5(05h)	517(205h)
IFR1	Upper 8-bits of 24-bit Input Frame Count	75	R	01	164(A4h)	676(2A4h)
IFR2	Middle 8-bits of 24-bit Input Frame Count	75	R	01	165(A5h)	677(2A5h)
IFR3	Lower 8-bits of 24-bit Input Frame Count	75	R	01	166(A6h)	678(2A6h)
LWD1	Upper 5-bits of 13-bit Input Line Count	76	R	01	167(A7h)	679(2A7h)
LWD2	Lower 8-bits of 13-bit Input Line Count	76	R	01	168(A8h)	680(2A8h)
FFR1	Upper 8-bits of 24-bit Minimum Frame Count to trigger “Out of Range” Condition	78	W	01	179(B3h)	691(2B3h)
FFR2	Middle 8-bits of 24-bit Minimum Frame Count to trigger “Out of Range” Condition	78	W	01	180(B4h)	692(2B4h)
FFR3	Lower 8-bits of 24-bit Minimum Frame Count to trigger “Out of Range” Condition	78	W	01	181(B5h)	693(2B5h)

Table 20. Output Control Timing Registers

Name	Description	Page #	Access	Group Address	Register Address	PROM Address
VSW1	Upper 4-bits of 12-bit total Vertical Sync Width	79	R/W	01	153(99h)	665(299h)
VSW2	Lower 8-bits of 12-bit total Vertical Sync Width	79	R/W	01	154(9Ah)	666(29Ah)
VSD1	Upper 1-bits of 17-bit total Vertical Sync Delay	80	R/W	01	156(9Bh)	668(29Bh)
VSD2	Middle 8-bits of 17-bit total Vertical Sync Delay	80	R/W	01	156(9Ch)	668(29Ch)
VSD3	Lower 8-bits of 17-bit total Vertical Sync Delay	80	R/W	01	157(9Dh)	669(29Dh)
HSWD	5-bit Horizontal Sync Width	81	R/W	01	158(9Eh)	670(29Eh)
HSDL	5-bit Horizontal Sync Delay	81	R/W	01	159(9Fh)	671(29Fh)
VHD1	Control and upper 3-bits of 11-bit total Horizontal Sync in Vertical Blank period	82	R/W	01	224(E0h)	736(2E0h)
VHD2	Lower 8-bits of 11-bit total Horizontal Sync in Vertical Blank period	82	R/W	01	225(E1h)	737(2E1h)
VHBN	Number of Horizontal pulses, minus 1, inserted in VBlank period	82	R/W	01	226(E2)	738(2E2h)
POLT	Vertical & Horizontal Sync, Data Enable, and Output Clock Polarity Control	83	R/W	01	160(A0h)	672(2A0h)

Table 21. Clock Multiplier Registers

Name	Description	Page #	Access	Group Address	Register Address	PROM Address
FDIV	PLL Feedback Divider	84	R/W	01	182(B6h)	694(2B6h)
IDIV	PLL Divider	84	R/W	01	183(B7h)	695(2B7h)

Table 22. Color Management Registers

Name	Description	Page #	Access	Group Address	Register Address	PROM Address
G1Rxxx	RED Gamma1 Table (xxx goes from 0 to 255)	86	W	00	0 to 255(FFh)	C90h to D8Fh
G1Gxxx	GREEN Gamma1 Table (xxx goes from 256 to 511)	86	W	00	256(100h) to 511(1FFh)	D90h to E8Fh
G1Bxxx	BLUE Gamma1 Table (xxx goes from 512 to 767)	86	W	00	512(200h) to 767(2FFh)	E90h to F8Fh
G2Rxxx	RED Gamma2 Table	86	W	00	300h to 3FFh	F90h to 108Fh
G2Gxxx	GREEN Gamma2 Table	86	W	00	400h to 4FFh	1090h to 118Fh
G2Bxxx	BLUE Gamma2 Table	86	W	00	500h to 5DDh	1190h to 128Fh
D4xx	Dithering Table Rows for 1/4 and 3/4 (XX is from 01 to 32)[1]	86	W	01	184(B8h) to 215(D7h)	696(2B8h) to 727(2D7h)
D2xx	Dithering Table Rows for 1/2 (XX is from 01 to 08)[1]	86	W	01	216(D8h) to 223(DFh)	728(2D8h) to 735(2DFh)

Notes 1) Default data provided by Silicon Image

Table 23. I²C Slave Address Registers

Name	Description	Page #	Access	Group Address	Register Address	PROM Address
SAD1	I²C Slave Address	85	W	01	62(3Eh)	574(23Eh)
SAD2	I²C Slave Address	85	W	01	63(3Fh)	575(23Fh)

Table 24. Window Box Registers

Name	Description	Page #	Access	Group Address	Register Address	PROM Address
ICP1	Upper 3-bits of 11-bit Input Columns Previous	87	R	01	20(14h)	532(214h)
ICP2	Lower 8-bits of 11-bit Input Columns Previous	87	R	01	21(15h)	533(215h)
IRP1	Upper 3-bits of 11-bit Input Rows Previous	88	R	01	22(16h)	534(214h)
IRP2	Lower 8-bits of 11-bit Input Columns Previous	88	R	01	23(17h)	535(215h)
XRW1	Upper 3-bits Fill Window Box and OSD selection	89	W	01	227(E3h)	740(2E4h)
XRW2	Lower 8-bits of 11-bit total for row after which background is used for image.	89	W	01	228(E4h)	741(2E5h)

Panel Output Columns – PLC1

Write at Address: 6(06h)
Reset Value: Undefined

7	6	5	4	3	2	1	0
Reserved					PLC1[10:8] - Output Columns		

7:3 Reserved

These bits must be set to 0.

2:0 Upper 3-bits of 11-bit Output Columns

PLC1[10:8] the upper 3-bits of a total 11-bit number of output columns to panel. Used with PLC2 to make 11-bit total.

Panel Output Columns – PLC2

Write at Address: 7(07h)
Reset Value: Undefined

7	6	5	4	3	2	1	0
PLC2[7:0] - Output Columns							

7:0 Lower 8-bits of 11-bit Output Columns

PLC2[7:0] the lower 8-bits of a total 11-bit number of columns counted in the previous frame. Used with PLC1 to make 11-bit total.

Panel Output Rows – PLR1

Write at Address: 8(08h)
Reset Value: Undefined

7	6	5	4	3	2	1	0
Reserved					PLR1[10:8] - Output Rows		

7:3 Reserved

These bits must be set to 0.

2:0 Upper 3-bits of 11-bit Output Rows

PLR1[10:8] the upper 3-bits of a total 11-bit number of output rows to panel. Used with PLR2 to make 11-bit total.

Panel Output Rows – PLR2

Write at Address: 9(09h)
Reset Value: Undefined

7	6	5	4	3	2	1	0
PLR2[7:0] - Output Rows							

7:0 Lower 8-bits of 11-bit Output Rows

PLR2[7:0] the lower 8-bits of a total 11-bit number of rows counted in the previous frame. Used with PLR1 to make 11-bit total.

Hsync during blank screen – HBN1

Read/Write at Address: 240(F0h)
Reset Value: Undefined

7	6	5	4	3	2	1	0
Reserved					HBN[10:8] - Output Rows		

7:3 Reserved

These bits must be set to 0.

2:0 Upper 3-bits of 11-bit DE low time in XCLKS

HBN[10:8] the upper 3-bits of a total 11-bit number of XCLKs that DE is low when the screen background is displayed due to an “out of range” or “loss of sync” condition.

Hsync during blank screen – HBN2

Read/Write at Address: 241(F1h)
Reset Value: Undefined

7	6	5	4	3	2	1	0
HBN[7:0] - Output Rows							

7:0 Lower 8-bits of 11-bit DE low time in XCLKS

HBN[7:0] the lower 8-bits of a total 11-bit number of XCLKs that DE is low when the screen background is displayed due to an “out of range” or “loss of sync” condition.

Vblank number of rows – VBN1

Read/Write at Address: 242(F2h)
Reset Value: Undefined

7	6	5	4	3	2	1	0
Reserved						VBN[9:8] - Output Rows	

7:2 Reserved

These bits must be set to 0.

1:0 Upper 2-bits of 10-bit rows to insert in Vblank period

VBN[10:8] the upper 2-bits of a total 10-bit number of rows to insert during the vertical blanking period. Set to 0 to disable inserting any Hsync pulses.

Vblank number of rows – VBN2

Read/Write at Address: 243(F3h)
Reset Value: Undefined

7	6	5	4	3	2	1	0
VBN[7:0] - Output Rows							

7:0 Lower 8-bits of 10-bit DE low time in XCLKS

VBN[7:0] the lower 8-bits of a total 11-bit number of rows to insert during the vertical blanking period. Set to 0 to disable inserting any Hsync pulses.

Loss of Sync delay – LOSD

Write at Address: 178(B2h)
Reset Value: Undefined

7	6	5	4	3	2	1	0
Reserved				LOSD[3:0] – De-assert delay			

7:4 Reserved

These bits must be set to 0.

3:0 4-bit delay when de-asserting "Loss of Sync"

LOSD[3:0] 4-bit number that determines delay when transitioning from "Loss of Sync" state to active display state. Increments are approximately ¼ second.

OSD delay – OSDD

Write at Address: 251(FBh)
Reset Value: Undefined

7	6	5	4	3	2	1	0
OSDD[7:0] – OSD message delay							

7:0 8-bit delay before displaying "Loss of Sync" or "Out of Range" OSD

OSDD[7:0] 8-bit number of frames to delay the display of the "Loss of Sync" or "Out of Range" message.

PWM0 period – P0P1

Write at Address: 173(ADh)
Reset Value: Undefined

7	6	5	4	3	2	1	0
P0P[23:16] –PWM0 period							

7:0 Upper 8-bits of 24-bit period in XLCKS of PWM0 output

P0P[23:16] the upper 8-bits of a total 24-bit number of XCLKs for the period of the PWM0 output

PWM0 period – P0P2

Write at Address: 174(AEh)
Reset Value: Undefined

7	6	5	4	3	2	1	0
P0P[15:8] – backlight PWM0 period							

7:0 Middle 8-bits of 24-bit period in XLCKS of PWM0 output

P0P[15:8] the middle 8-bits of a total 24-bit number of XCLKs for the period of the PWM0 output

PWM0 period – P0P3

Write at Address: 175(AFh)
Reset Value: Undefined

7	6	5	4	3	2	1	0
P0P[7:0] –PWM0 period							

7:0 Lower 8-bits of 24-bit period in XLCKS of PWM0 output

P0P[7:0] the lower 8-bits of a total 24-bit number of XCLKs for the period of the PWM0 output

PWM0 high time – P0PH

Read/Write at Address: 176(B0h)
Reset Value: Undefined

7	6	5	4	3	2	1	0
P0PH[7:0] –PWM0 high time							

7:0 8-bit high time in number of steps

P0PH[7:0] 8-bit number of steps that the PWM0 is high. Steps are determined by register P0ST.

PWM0 step increment and control – P0ST

Write at Address: 177(B1h)
Reset Value: Undefined

7	6	5	4	3	2	1	0
Reset at output VS	Always low	Always high	P0ST[4:0] – number of XCLKS per step				

7 Reset when output Vsync occurs

1 Reset counter when output Vsync occurs.

0 Counter free runs

6 Always low

1 Keep PWM0 pin always low

0 Output timing of PWM0 pin determined by P0Px registers

5 Always high

1 Keep backlight PWM0 pin always high

0 Output timing of PWM0 pin determined by P0Px registers

4:0 5-bit number of XCLKS per step when controlling PWM0

P0ST[4:0] 5-bit number of XCLKs for the step to adjust the PWM0 output high time. This adjustment can be done automatically when a button is pressed, or by a microcontroller.

PWM1 period – P1P1

Write at Address: 235(EBh)
Reset Value: Undefined

7	6	5	4	3	2	1	0
P1P[23:16] –PWM1 period							

7:0 Upper 8-bits of 24-bit period in XLCKS of PWM1 output

P1P[23:16] the upper 8-bits of a total 24-bit number of XCLKs for the period of the PWM1 output

PWM1 period – P1P2

Write at Address: 236(ECh)
Reset Value: Undefined

7	6	5	4	3	2	1	0
P1P[15:8] –PWM1 period							

7:0 Middle 8-bits of 24-bit period in XLCKS of PWM1 output

P1P[15:8] the middle 8-bits of a total 24-bit number of XCLKs for the period of the PWM1 output

PWM1 period – P1P3

Write at Address: 237(EDh)
Reset Value: Undefined

7	6	5	4	3	2	1	0
P1P[7:0] –PWM1 period							

7:0 Lower 8-bits of 24-bit period in XLCKS of PWM1 output

P1P[7:0] the lower 8-bits of a total 24-bit number of XCLKs for the period of the PWM1 output

PWM1 high time – P1PH

Read/Write at Address: 238(EEh)
Reset Value: Undefined

7	6	5	4	3	2	1	0
P1PH[7:0] –PWM1 high time							

7:0 8-bit high time in number of steps

P1PH[7:0] 8-bit number of steps that PWM1 is high. Steps is determined by register P1ST.

PWM1 step increment and control – P1ST

Write at Address: 239(EFh)
Reset Value: Undefined

7	6	5	4	3	2	1	0
Reset at output VS	Always low	Always high	P1ST[4:0] – number of XCLKS per step				

7 Reset when output Vsync occurs

1 Reset counter when output Vsync occurs.

0 Counter free runs

6 Always low

1 Keep audio PWM1 pin always low

0 Output timing of audio pin determined by P1Px registers

5 Always high

1 Keep audio PWM1 pin always high

0 Output timing of PWM1 pin determined by P1Px registers

4:0 5-bit number of XCLKS per step when controlling PWM1

P1ST[4:0] 5-bit number of XCLKs for the step to adjust the PWM1 output high time. This adjustment can be done automatically when a button is pressed, or by a microcontroller.

Fast Line Rate – FLR1

Write at Address: 150(96h)
Group Address: 01
Reset Value: Undefined

7	6	5	4	3	2	1	0
Reserved	Enable frame rate checking	Enable line rate checking	FLR[12:8] – Fast line rate limit				

7 Reserved

This bit must be set to 1.

6 Enable frame rate checking

1 Enables frame rating checking using registers FFR and SFR

0 Disables frame rate checking

5 Enable line rate checking

1 Enables line rating checking using registers FLR and SLR

0 Disables line rate checking

4:0 Upper 5-bits of 13-bit line rate limit

FLR[12:8] the upper 5-bits of a total 13-bit number, at the XCLK rate, of the line rate to use when checking for out of range conditions.

Fast Line Rate – FLR2

Write at Address: 151(97h)
Group Address: 01
Reset Value: Undefined

7	6	5	4	3	2	1	0
FLR[7:0] – Fast line rate limit							

7:0 Lower 8-bits of 13-bit line rate limit

FLR[7:0] the lower 8-bits of a total 13-bit number, at the XCLK rate, of the line rate to use when checking for out of range conditions.

Slow Line Rate – SLR1

Write at Address: 244(F4h)
Group Address: 01
Reset Value: Undefined

7	6	5	4	3	2	1	0
Reserved				SLR[11:8] – Slow line rate limit			

7:4 Reserved

3:0 Upper 4-bits of 12-bit slow line rate limit

SLR[11:8] the upper 4-bits of a total 12-bit number, at the XCLK rate, of the slow line rate to use when checking for out of range conditions.

Slow Line Rate – SLR2

Write at Address: 245(F5h)
Group Address: 01
Reset Value: Undefined

7	6	5	4	3	2	1	0
SLR2[7:0] – Slow line rate limit							

7:0 Lower 8-bits of 13-bit line rate limit

SLR[7:0] the lower 8-bits of a total 12-bit number, at the XCLK rate, of the slow line rate to use when checking for out of range conditions.

Slow Frame Rate – SFR1

Write at Address: 246(F6h)
Group Address: 01
Reset Value: Undefined

7	6	5	4	3	2	1	0
SFR[23:16] – Slow frame rate limit							

7:0 Upper 8-bits of 24-bit slow frame rate limit

SFR[23:16] the upper 8-bits of a total 24-bit number, at the XCLK rate, of the slow frame rate to use when checking for out of range conditions.

Slow Frame Rate – SFR2

Write at Address: 247(F7h)
Group Address: 01
Reset Value: Undefined

7	6	5	4	3	2	1	0
SFR[15:8] – Slow frame rate limit							

7:0 Middle 8-bits of 24-bit slow frame rate limit

SFR[15:8] the middle 8-bits of a total 24-bit number, at the XCLK rate, of the slow frame rate to use when checking for out of range conditions.

Slow Frame Rate – SFR3

Write at Address: 248(F8h)
Group Address: 01
Reset Value: Undefined

7	6	5	4	3	2	1	0
SFR[7:0] – Slow frame rate limit							

7:0 Lower 8-bits of 24-bit slow frame rate limit

SFR[7:0] the lower 8-bits of a total 24-bit number, at the XCLK rate, of the slow frame rate to use when checking for out of range conditions.

Automatic Window Box Line Rate – LWB1

Write at Address: 249(F9h)
Group Address: 01
Reset Value: Undefined

7	6	5	4	3	2	1	0
Reserved		Enable Progressive	Enable Once	LWB[11:8] – line rate limit to trigger window boxing			

5 Enable automatic window boxing progressive

1 Enables automatic window boxing when line rate is too fast (LWB) by adding XIRW rows. If line rate is still too fast then XIRW rows will be added again, up to eight times.

0 Disables automatic window boxing once

4 Enable automatic window boxing once

1 Enables automatic window boxing when line rate is too fast (LWB) by adding XIRW rows

0 Disables automatic window boxing once

3:0 Upper 4-bits of 12-bit window box line rate limit

LWB[11:8] the upper 4-bits of a total 12-bit number, at the XCLK rate, of the fast line rate to use when triggering automatic window boxing

Automatic Window Box Line Rate – LWB2

Write at Address: 250(FAh)
Group Address: 01
Reset Value: Undefined

7	6	5	4	3	2	1	0
LWB[7:0] – line rate limit to trigger window boxing							

7:0 Lower 8-bits of 12-bit slow frame rate limit

LWB[7:0] the lower 7-bits of a total 12-bit number, at the XCLK rate, of the fast line rate to use when triggering automatic window boxing.

Rows to add to input when window boxing – XIRW

Write at Address: 11(Bh)
Group Address: 01
Reset Value: Undefined

7	6	5	4	3	2	1	0
XIRW[7:0] – number of rows to add when window boxing							

7:0 8-bit number of rows to add to input when window boxing

XIRW[7:0] 8-bit number of rows to add to the input when window boxing. This will reduce the output line rate by taking in extra lines during the vertical blanking period.

OSD Fetch base address high – OFSH

Read/Write at Address: 60(3Ch)
Group Address: 01
Reset Value: Undefined

7	6	5	4	3	2	1	0
OFSH[7:0] – high order byte of OSD address							

7:0 Upper 8-bits of 16-bit address to fetch OSD character map and message from

OFSH[7:0] the high order byte of the EEPROM address to automatically load in the 7KB of OSD data (character map and message).

OSD Fetch base address low – OFSL

Read/Write at Address: 61(3Dh)
Group Address: 01
Reset Value: Undefined

7	6	5	4	3	2	1	0
OFSL[7:0] – low order byte of OSD address							

7:0 Lower 8-bits of 16-bit address to fetch OSD character map and message from

OFSL[7:0] the low order byte of the EEPROM address to automatically load in the 7KB of OSD data (character map and message). After a microcontroller writes to this location, the 861 will master the I2C bus and load in the new OSD information.

Input/Output Configuration Register - RMDT

Read/Write Only at Address: 152(98h)
Group Address: 01
Reset Value: Undefined
This register determines the operation of the inputs and outputs.

7	6	5	4	3	2	1	0
CTL Output Mode	Lock Resolution	Fill Hsync from beginning	Staggered Clock	LVDS 6-bit enable	Output Mode	Enable negative weights	Reserved

7 CTL output control and TPCLK

1 CTL[3:1] from the transmitter are output on the CTL[3:1] control signals and internal XCLK

0 Input Control Signals are output on the CTL[3:1] control signals –

CTL1 : Input Vertical Sync

CTL2 : Input Horizontal Sync

CTL3 : Input DE.

TPCLK: ICLK (PanelLink receiver clock)

6 Lock Resolution

1 Disable update of input resolution counted, IRC and ICC, registers.

0 Enable scaling to change based upon the input resolution.

5 Fill Hsync from beginning

1 Insert Hsync pulse in the vertical blanking time. Start filling from beginning of frame backwards, toward the last Hsync pulse of the frame. The last Hsync pulse may be an real line, or an inserted one using VHBN.

0 Disables fill Hsync from beginning

4 Enable Staggered Clock

1 Enable stagger output mode (This function can only be used in 2-pixels/clock).

0 Disable stagger output mode. Normal data output mode.

3 LVDS data mapping (see page 105)

1 MSB data mapping

0 LSB data mapping

2 Output Mode

1 One pixel per clock cycle (QE[23:0]).

0 Two pixels per clock cycle with the output clock running at half the rate (QE[23:0] and QO[23:0]).

1 Enable negative weights

1 Enable negative weight processing by scaling engine

0 Disable negative weight processing by scaling engine

0 Reserved

This bit must be set to 0.

OSD Registers – OSDE, OSBx, OULx, OSWx, OSHx, OO0X, OO1x, OLSx, LLSx, OSRx

Control Register - OSDE

Read/Write at Address: 128(80h), bits 2 and 3 are read only
Group Address: 01
Reset Value: Undefined

This sets the operation of the OSD and the state of the power management.

7	6	5	4	3	2	1	0
Load from I^2C PROM	Display User OSD	Enable Loss of Sync OSD	Enable Out of Range OSD	Loss of Sync Status	Out of Range Status	Detection Method of Loss of Sync	Power Management Mode

7 Load OSD from PROM

1 Load OSD data bytes from I^2C PROM at boot up.

0 Disable loading of OSD data from I^2C PROM upon boot up.

6 Enable User OSD

1 User OSD is displayed on the screen.

0 User OSD is not displayed. This bit does not affect the “Loss of Sync” and “O

5 Enable Loss of Sync Indicator

1 If DE signal from input is lost, “Loss of Sync” OSD is displayed.

0 Indicator disabled.

4 Enable Out of Range Indicator

1 If row and frame speed limits are enabled, enable OOR message when exceeding these limits.

0 Indicator disabled.

3 Sync Lost Status (Read Only)

1 Input DE has been lost.

0 Input DE is present.

2 Out of Range Status (Read Only)

1 Input mode outside of acceptable range.

0 Input mode within acceptable ranges.

OSDE Register definition continued on next page

Control Register – OSDE cont.

This sets the operation of the OSD and the state of the power management.

7	6	5	4	3	2	1	0
Load from I^2C PROM	Display User OSD	Enable Loss of Sync OSD	Enable Out of Range OSD	Loss of Sync Status	Out of Range Status	Detection Method of Loss of Sync	Power Management Mode

1 Detection Method of Loss of Sync

1 Logic controlled by counting incoming DE timing with respect to internal "XCLK". This method asserts "Loss of Sync" after counting the period of DE. DE "high" times or "low" times outside of a range expected for normal video signaling will immediately trigger "SCDT" low. More specifically, the "Loss of Sync" state will be entered on any of the following conditions:

Parameter	*Range of internal clock cycles*	*Example Clock*	*Example Min*	*Example Max*
Input DE high time	t_{High} >4096 OR t_{High} <256	66.6 MHz	4usec	61usec
Input DE low time	t_{low} >2^{20} OR t_{low} <32	66.6 MHz	<1usec	15.7msec

The "internal clock" is the pixel clock used to drive the panel.

0 Logic controlled by "SCDT" signal received internally from PanelLink receiver core. This method asserts "Loss of Sync" after a delay of 100ms or more. The logic delays assertion of SCDT to prevent short, non-functional transitions on DE from affecting the output.

0 Power Management Mode

1 non-DVI power management mode. Outputs are ON_OFF, STANDBY, and SUSPEND.

0 DVI power management mode. Outputs are SCDT ("Loss of Sync") and "Out of Range".

ON_OFF becomes SCDT

SUSPEND becomes "Out of Range"

STANDBY driven always low

Screen Background Color - OSBx

Write Only at Address: 129(81h) – 131(83h)
Group Address: 01
Reset Value: Undefined

These registers determine the color that appears as a screen background for the monitor in the case of “Loss of Sync” ut of Range” conditions.

Red Component - OSBR

Write Only at Address: 129(81h)
Reset Value: Undefined

7	6	5	4	3	2	1	0
OSBR[7:0] - Red Component							

7:0 Color Components

OSBR[7:0] 8-bit Red sub component.

Green Component - OSBG

Write Only at Address: 130(82h)
Reset Value: Undefined

7	6	5	4	3	2	1	0
OSBG[7:0] - Green Component							

7:0 Color Components

OSBG[7:0] 8-bit Green sub component.

Blue Component - OSBB

Write Only at Address: 131(83h)
Reset Value: Undefined

7	6	5	4	3	2	1	0
OSBB[7:0] - Blue Component							

7:0 Color Components

OSBB[7:0] 8-bit Blue sub component.

OSD Upper Left Corner Position - OULx

Write Only at Address: 132(84h) – 135(87h)
Grpup Address: 01
Reset Value: Undefined

These registers determine the starting position of the upper left corner of the OSD message window on the screen.

Horizontal Position – OUL1

Write Only at Address: 132(84h)
Reset Value: Undefined

7	6	5	4	3	2	1	0
Reserved					OUL1[10:8] – Horizontal Position		

7:3 Reserved

These bits must be set to 0.

2:0 Upper 3-bits of 11-bit Horizontal Position

OUL1[10:8] is the upper 3-bits of the total 11-bit horizontal position of the OSD message rectangle with respect to the upper left corner of the display plus two in pixels. Used with OUL2 to make 11-bit total.

Horizontal Position – OUL2

Write Only at Address: 133(85h)
Reset Value: Undefined

7	6	5	4	3	2	1	0
OUL2[7:0] – Horizontal Position							

7:0 Lower 8-bits of 11-bit Horizontal Position

OUL2[7:0] is the lower 8-bits of the total 11-bit horizontal position of the OSD message rectangle with respect to the upper left corner of the display plus two in pixels. Used with OUL1 to make 11-bit total.

Vertical Position – OUL3

Write Only at Address: 134 (86h)
Group Address: 01
Reset Value: Undefined

7	6	5	4	3	2	1	0
Reserved					OUL[10:8] – Vertical Position		

7:3 Reserved

These bits must be set to 0.

2:0 Upper 2-bits of 10-bit Vertical Position

OUL[10:8] is the upper 3-bits of the 11-bit total vertical position of the OSD message rectangle with respect to the upper left corner of the display in pixels. Used with OUL4 to make 11-bit total.

Vertical Position – OUL4

Write Only at Address: 135(87h)
Reset Value: Undefined

7	6	5	4	3	2	1	0
OUL[7:0] – Vertical Position							

7:0 Vertical Position

OUL[7:0] is the lower 8-bits of the 11-bit total vertical position of the OSD message rectangle with respect to the upper left corner of the display in pixels. Used with OUL3 to make 11-bit total.

OSD Width and Height – OSWx and OSHx

Write Only at Address: 136(88h) – 139(8Bh)
Group Address: 01
Reset Value: Undefined

These registers determine the width and height of the OSD message window to be displayed on the monitor.

Width – OSW1

Write Only at Address: 136(88h)
Reset Value: Undefined

7	6	5	4	3	2	1	0
Reserved					OSW1[10:8] – Width		

7:3 Reserved

These bits must be set to 0.

2:0 Upper 3-bits of 11-bit total OSD message Width

OSW1[10:8] is the upper 3-bits of an 11-bit total width of the OSD message overlay rectangle in pixels. Used with OSW2 to make 11-bit total.

Width – OSW2

Write Only at Address: 137(89h)
Reset Value: Undefined

7	6	5	4	3	2	1	0
OSW2[7:0] – Width							

7:0 Lower 8-bits of 11-bit total OSD message Width

OSW2[7:0] is the lower 8-bits of an 11-bit total width of the OSD message overlay rectangle in pixels. Used with OSW1 to make 11-bit total.

Height – OSH1

Write Only at Address: 138(8Ah)
Reset Value: Undefined

7	6	5	4	3	2	1	0
Reserved					OSH[10:8] - Height		

7:3 Reserved

These bits must be set to 0.

2:0 Upper 2-bits of 10-bit total OSD message Height

OSH1[2:0] is the upper 3-bits of a 11-bit total height of the OSD message overlay rectangle in pixels. Used with OSH2 to make 11-bit total.

Height – OSH2

Write Only at Address: 139(8Bh)
Reset Value: Undefined

7	6	5	4	3	2	1	0
OSH[7:0] – Height							

7:0 Height in Pixels

OSH2[7:0] is the lower 8-bits of a 11-bit total height of the OSD message overlay rectangle in pixels. Used with OSH1 to make 11-bit total.

OSD Memory Location - OLSx

Write Only at Address: 146(92h) – 147(93h)
Group Address: 01
Reset Value: Undefined

These registers set the location within the OSD memory where the user OSD overlay message beginsThis location must be within the first 1024(400h) bytes, address range 0-3FFh).

Starting Location – OLS1

Write Only at Address: 146(92h)
Reset Value: Undefined

7	6	5	4	3	2	1	0
Reserved				OLS1[11:8] - Starting Position			

7:4 Reserved

These bits must be set to 0.

3:0 Starting Position

OLS1[11:8] is the upper 4-bits of a 12-bit total starting byte location of the OSD message within the OSD memory. Used with OLS2 to make 12-bit total.

Starting Location – OLS2

Write Only at Address: 147(93h)
Reset Value: Undefined

7	6	5	4	3	2	1	0
OLS2[7:0] - Starting Position							

7:0 Starting Position

OLS2[7:0] is the lower 8-bits of a 12-bit total starting byte location of the OSD message within the OSD memory. Used with OLS1 to make 12-bit total.

Loss of Sync OSD Starting Location - LLSx

Write Only at Address: 171(ABh) – 172(ACh)
Group Address: 01
Reset Value: Undefined

These registers set the location within the OSD memory where the "Loss of Sync" OSD overlay message begins. This location must be within the first 1024(400h) bytes, address range 0-3FFh).

Loss of Sync OSD Starting Location – LLS1

Write Only at Address: 171(ABh)
Group Address: 01
Reset Value: Undefined

7	6	5	4	3	2	1	0
Reserved				LLS1[11:8] - Starting Position			

7:4 Reserved

These bits must be set to 0.

3:0 Starting Position

LLS1[11:8] is the upper 4-bits of a 12-bit total starting byte location of the OSD message within the OSD memory. Used with LLS2 to make 12-bit total.

Loss of Sync OSD Starting Location – LLS2

Write Only at Address: 172(ACh)
Reset Value: Undefined

7	6	5	4	3	2	1	0
LLS2[7:0] - Starting Position							

7:0 Starting Position

LLS2[7:0] is the lower 8-bits of a 12-bit total starting byte location of the OSD message within the 6143(17FFh) bytes of OSD memory. Used with LLS1 to make 12-bit total.

Out of Range OSD Starting Location - ORSx

Write Only at Address: 169(A9h) – 170(AAh)
Group Address: 01
Reset Value: Undefined

These registers set the location within the OSD memory where the "Out of Range" OSD overlay message begins. This location must be within the first 1024(400h) bytes, address range 0-3FFh).

Out of Range OSD Starting Location – ORS1

Write Only at Address: 169(A9h)
Group Address: 01Reset Value: Undefined

7	6	5	4	3	2	1	0
Reserved				ORS1[11:8] - Starting Position			

7:4 Reserved

These bits must be set to 0.

3:0 Starting Position

ORS1[11:8] is the upper 4-bits of a 12-bit total starting byte location of the OSD message within the OSD memory. Used with ORS2 to make 12-bit total.

Out of Range OSD Starting Location – ORS2

Write Only at Address: 170(AAh)
Reset Value: Undefined

7	6	5	4	3	2	1	0
ORS2[7:0] - Starting Position							

7:0 Starting Position

ORS2[7:0] is the lower 8-bits of a 12-bit total starting byte location of the OSD message within the OSD memory. Used with ORS1 to make 12-bit total.

OSD Memory Registers

Write Only at Address: 0 (0h) to 6143 (17FFh)
Group Address: 11
Reset Value: Undefined

These registers give the data for the OSD memory. It may or may not be loaded depending on the “Load from PROM” bit of OSDE register.

7	6	5	4	3	2	1	0
O####[7:0] - Memory Data							

7:0 Memory Data

The OSD data; #### ranges from 0 to 6143.. The data is the character bitmap consisting of 64 characters used for displaying OSD messages - up to 1024 of these characters. Please refer to the OSD register table for EEPROM byte address range.

Input Resolution Count Registers – ICCx, IRCx, IFRx, LWDx, FFRx

Read at Address: 2(02h) – 5(05h)
Read Only at Address: 164(A4h) – 168(A8h), 179(B3h) – 181(B5h)
Group Address: 01
Reset Value: Undefined

These registers give the measured incoming resolution.

Input Columns – ICC1

Read at Address: 2(02h)
Reset Value: Undefined

7	6	5	4	3	2	1	0
One-to-One Scaling	Reset Cipher Engine	Bypass Output Gamma	Bypass Input Gamma	Reserved	ICC1[10:8] - Input Columns		

7 Enable one-to-one Scaling

1 Turn on scaling engine when in native mode of panel. Can be used for sharpening effect

0 Scaling engine is not used when input is same as panel output.

6 Reset Cipher Engine to Idle

1 Disable the HDCP Cipher engine

0 Enable the HDCP Cipher Engine

5 Bypass Output Gamma Table (Write Only)

1 Data bypasses the gamma table.

0 Data goes through the gamma table.

4 Bypass Input Gamma Table (Write Only)

1 Data bypasses the gamma table.

0 Data goes through the gamma table.

3 Reserved

This bit must be set to 0.

2:0 Upper 3-bits of 11-bit Input Columns (Read Only)

ICC1[10:8] the upper 4-bits of a total 11-bit number of pixels counted **minus one** in the most recent row of input data. Used with ICC2 to make 11-bit total.

Input Columns – ICC2

Read at Address: 3(03h)
Reset Value: Undefined

7	6	5	4	3	2	1	0
ICC2[7:0] - Input Columns							

7:0 Lower 8-bits of 11-bit Input Columns (Read Only)

ICC2[7:0] the lower 8-bits of a total 11-bit number of pixels counted **minus one** in the most recent row of input data. Used with ICC1 to make 11-bit total.

Input Rows – IRC1

Read at Address: 4(04h)
Reset Value: Undefined

7	6	5	4	3	2	1	0
Reserved					IRC1[10:8] - Input Rows		

7:3 Reserved

These bits must be set to 0.

2:0 Upper 3-bits of 11-bit Input Rows

IRC1[10:8] the upper 3-bits of a total 11-bit number of rows counted in the previous frame. Used with IRC2 to make 11-bit total.

Input Rows – IRC2

Read at Address: 5(05h)
Reset Value: Undefined

7	6	5	4	3	2	1	0
IRC2[7:0] - Input Rows							

7:0 Lower 8-bits of 11-bit Input Rows

IRC2[7:0] the lower 8-bits of a total 11-bit number of rows counted in the previous frame. Used with IRC1 to make 11-bit total.

Input Frame Time – IFR1

Read at Address: 164(A4h)
Group Address: 01
Reset Value: Undefined

7	6	5	4	3	2	1	0
IFR1[23:16] - Input Frame Count							

7:0 Upper 8-bits of 24-bit Input Frame Count

IFR1[23:16] the upper 8-bits of a total 24-bit number, at the XCLK rate, of the frame measured between the end of frame condition on the previous frame. Used with IFR2 and IFR3 to make 24-bit total.

Input Frame Count – IFR2

Read at Address: 165(A5h)
Group Address: 01
Reset Value: Undefined

7	6	5	4	3	2	1	0
IFR2[15:8] - Input Frame Count							

7:0 Middle 8-bits of 24-bit Input Frame Count

IFR2[15:8] the middle 8-bits of a total 24-bit number, at the XCLK rate, of the frame measured between the end of frame condition on the previous frame. Used with IFR1 and IFR3 to make 24-bit total.

Input Frame Count – IFR3

Read at Address: 166(A6h)
Group Address: 01
Reset Value: Undefined

7	6	5	4	3	2	1	0
IFR3[7:0] - Input Frame Count							

7:0 Lower 8-bits of 24-bit Input Frame Count

IFR3[7:0] the lower 8-bits of a total 24-bit number, at the XCLK rate, of the frame measured between the end of frame condition on the previous frame. Used with IFR1 and IFR2 to make 24-bit total.

Input Line Time – LWD1

Read at Address: 167(A7h)
Group Address: 01
Reset Value: Undefined

7	6	5	4	3	2	1	0
Reserved			LWD1[12:8] - Input Line Time				

7:5 Reserved

These bits must be set to 0.

4:0 Upper 5-bits of 13-bit Input Rows

LWD1[12:8] the upper 5-bits of a total 13-bit number of XCLKS/row counted in the previous frame. Used with LWD2 to make 13-bit total.

Input Line Time – LWD2

Read at Address: 168(A8h)
Group Address: 01
Reset Value: Undefined

7	6	5	4	3	2	1	0
LWD2[7:0] - Input Line Time							

7:0 Lower 8-bits of 13-bit Input Rows

LWD2[7:0] the lower 8-bits of a total 13-bit number of XCLKS/row counted in the previous frame. Used with LWD1 to make 13-bit total.

TMDS Line Time – LIN1

Read at Address 0(00h)
Group Address: 01
Reset Value: Undefined

7	6	5	4	3	2	1	0
Reserved				LIN1[11:8] - TMDS Line Time			

7:4 Reserved

These bits must be set to 0.

3:0 Upper 4-bits of 12-bit number if ICLKS per row

LIN1[11:8] the upper 4-bits of a total 12-bit number of ICLKs (TMDS receiver clocks) counted per line. This time includes both DE high and DE low time, that is the time between DE high to DE high.. Used with LIN2 to make a 12-bit total.

TMDS Line Time – LIN2

Read at Address: 1(01h)
Group Address: 01
Reset Value: Undefined

7	6	5	4	3	2	1	0
LIN2[7:0] - TMDS Line Time							

7:0 Lower 8-bits of 12-bit number if ICLKS per row

LIN2[11:8] the lower 8-bits of a total 12-bit number of ICLKs (TMDS receiver clocks) counted per line. This time includes both DE high and DE low time, that is the time between DE high to DE high.. Used with LIN1 to make a 12-bit total.

g too high a frame rate. Used with FFR2 and FFR3 to make 24-bit total.

Minimum Frame Count – FFR2

Read/Write at Address: 180(B4h)
Group Address: 01
Reset Value: Undefined

7	6	5	4	3	2	1	0
FFR2[15:8] - Minimum Frame Count							

7:0 Middle 8-bits of 24-bit Minimum Frame Count

FFR2[15:8] the middle 8-bits of a total 24-bit number, at the XCLK rate, of the frame time that triggers and "Out of Range" condition reflecting too high a frame rate. Used with FFR1 and FFR3 to make 24-bit total.

Minimum Frame Count – FFR3

Read/Write at Address: 181(B5h)
Group Address: 01
Reset Value: Undefined

7	6	5	4	3	2	1	0
FFR3[7:0] - Minimum Frame Count							

7:0 Lower 8-bits of 24-bit Minimum Frame Count

FFR3[7:0] the lower 8-bits of a total 24-bit number, at the XCLK rate, of the frame time that triggers and "Out of Range" condition reflecting too high a frame rate. Used with FFR1 and FFR2 to make 24-bit total.

Vertical Sync Width – VSW1

Read/Write Only at Address: 153(99h)
Group Address: 01
Reset Value: Undefined

7	6	5	4	3	2	1	0
Reserved				VSW1[11:8] - VS width			

7:4 Reserved

These bits must be set to 0.

3:0 Upper 4-bits of 12-bit Output Vertical Sync Width

VSW1[11:8] is the upper 4-bits of a total 12-bit width of the output vertical sync, VSYNC, in XCLK clock cycles. Minimum width is 1. Zero is prohibited. The timing is not effected by the single or double pixel per clock setting. For 2 pixel per clock mode the value must be even. Used with VSW2 to make 12-bit total.

Vertical Sync Width – VSW2

Read/Write Only at Address: 154(9Ah)
Group Address: 01
Reset Value: Undefined

7	6	5	4	3	2	1	0
VSW2[7:0] - VS width							

7:0 Lower 8-bits of 12-bit Output Vertical Sync Width

VSW2[7:0] is the lower 8-bits of total 12-bit width of the output vertical sync, VSYNC, in XCLK clock cycles. Minimum width is 1. Zero is prohibited. The timing is not affected by the single or double pixel per clock setting. For 2 pixel per clock mode the value must be even. Used with VSW1 to make 12-bit total.

Vertical Sync Delay – VSD1

Read/Write Only at Address: 155(9Bh)
Group Address: 01
Reset Value: Undefined

7	6	5	4	3	2	1	0
Reserved				**Clock skew control**		VSD1[17:16] - VS delay	

7:4 Reserved

These bits must be set to 0.

3:2 Clock skew control

Amount of delay to add to ODCLK_D in approximately 1ns increments. Delay can be 0,1,2 or 3 ns.

1:0 Upper 1-bit of 17-bit Output Vertical Sync Delay

VSD1 [16] is the upper 1-bit of a total 17-bit delay of the output vertical sync, VSYNC, in XCLK clock cycles. Minimum width is 1. Zero is prohibited. The timing is not effected by the single or double pixel per clock setting. For 2 pixel per clock mode the value must be even. Used with VSD2 and VSD3 to make 17-bit total.

Vertical Sync Delay – VSD2

Read/Write Only at Address: 156(9Ch)
Group Address: 01
Reset Value: Undefined

7	6	5	4	3	2	1	0
VSD2[15:8] - VS delay							

7:0 Middle 8-bits of 17-bit Output Vertical Sync Delay

VSD2 [15:8] is the middle 8-bits of a total 17-bit delay of the output vertical sync, VSYNC, in XCLK clock cycles. Minimum width is 1. Zero is prohibited. The timing is not effected by the single or double pixel per clock setting. For 2 pixel per clock mode the value must be even. Used with VSD1 and VSD3 to make 17-bit total.

Vertical Sync Delay – VSD3

Read/Write Only at Address: 157(9Dh)
Group Address: 01
Reset Value: Undefined

7	6	5	4	3	2	1	0
VSD3[7:0] - VS delay							

7:0 Lower 8-bits of 17-bit Output Vertical Sync Delay

VSD3 [7:0] is the lower 8-bits of a total 17-bit delay of the output vertical sync, VSYNC, in XCLK clock cycles. Minimum width is 1. Zero is prohibited. The timing is not effected by the single or double pixel per clock setting. For 2 pixel per clock mode the value must be even. Used with VSD1 and VSD2 to make 17-bit total.

Horizontal Sync Width – HSWD

Read/Write Only at Address: 158(9Eh)
Group Address: 01
Reset Value: Undefined

7	6	5	4	3	2	1	0
HSWD[7:0] - HS width							

7:0 Output Horizontal Sync Width

HSWD[7:0] is the width of the output horizontal sync, HSYNC, in XCLK clock cycles. Minimum width is 1. Zero is prohibited. The timing is not effected by the single or double pixel per clock setting. For 2 pixel per clock mode the value must be even.

Horizontal Sync Delay – HSDL

Read/Write Only at Address: 159(9Fh)
Group Address: 01
Reset Value: Undefined

7	6	5	4	3	2	1	0
HSDL[7:0] - HS delay							

7:0 Output Horizontal Sync Delay

HSDL[7:0] is the lower 7-bits of an 8-bit total for the delay of the output horizontal sync, HSYNC, in XCLK clock cycles with respect to the rising edge of DE. HSDL[8] is located in register VHD1[4]. Minimum width is 1. Zero is prohibited. The timing is not effected by the single or double pixel per clock setting. For 2 pixel per clock mode the value must be even.

HS in VBlank Period – VHD1

Write at Address: 224 (E0h)
Group Address: 01
Reset Value: 00h

7	6	5	4	3	2	1	0
Reserved	VHS counted	Panel Outputs Tristate	HSD MSB	VHD[11:8] – HS period			

7 Reserved

This bit must be set to 0.

6 VHS Counted

1 Use VHD as the number in internal XCLK cycles for the period of the HSync pulses in VBlank.

0 Use the output line time as the period of the HSync pulses in the VBlank.

5 Panel Output Tristate

1 Normal operation

0 Output DE, HS, VS, ODCK, and output data are tri-stated

4 HSD MSB

The most significant bit of the horizontal width delay. This is used with register HSDL to give up to a full 511 clock cycles delay on regular HSync pulses.

3:0 VHD[10:8]

The most significant bit of the horizontal width period for the VBlank. This is used with register VHD2 to give up to a the 11 bit value for the period.

HS in VBlank Period – VHD2

Read at Address: 225 (E1h)
Group Address: 01
Reset Value: 00h

7	6	5	4	3	2	1	0
VHD[7:0] – HS period							

7:0 Lower 8-bits of 11-bit HS in VBlank period

VHD[7:0] is the lower 8 bits of the HSync period for the VBlank. Used with VHD1 to make 11-bit total.

HS in VBlank Count – VHBN

Read at Address: 226 (E2h)
Reset Value: 00h

7	6	5	4	3	2	1	0
VHBN[7:0] – HS Count							

7:0 HS Count

VHBN[7:0] is one less than the number of HS pulses inserted into the VBlank period.

Polarity for Output Control Signals - POLT

Write Only at Address: 160(A0h)
Group Address: 01
Reset Value: Undefined

This register controls the polarity of the control signals.

7	6	5	4	3	2	1	0
Reserved	Enable Dithering	LVDS Disable	Bypass Mode	VSP	DEP	CKP	HSP

7 Reserved - LVDS Latching, 1=rising, 0=falling

Set this bit equal to **TBD**

6 Dithering

1 Enable Dithering.

0 Disable Dithering.

5 LVDS Disable

1 Disable LVDS transmitter

0 Enable LVDS Transmitter

4 Bypass Mode

1 The data and control outputs of the receiver core are output to the panel pins directly. 1 or 2 pixels per clock is determined by its register. This mode for testing.

0 Data is scaled, normal operation.

3 VSP

This bit determines the polarity of VSYNC.

1 Active high

0 Active low

2 DEP

This bit determines the polarity of DE.

1 Active high

0 Active low

1 CKP

This bit determines the polarity of ODCK.

1 Data valid on falling edge

0 Data valid on rising edge

0 HSP

This bit determines the polarity of HSYNC.

1 Active high

0 Active low

Internal Clock Multiplier Registers – FDIV, IDIV

Write Only at Address: 182(B6h) and 183(B7h)
Group Address: 01
Reset Value: Undefined

Power Down Register – FDIV

Read/Write Only at Address: 182(B6h)
Reset Value: Undefined

7	6	5	4	3	2	1	0
Power Down	CLK Mult.	Enable Mode Status	Mode Status	Line Rate too Fast	Frame Rate too Fast	Window Box OOR	XCLK too slow

7 Power Down Mode

1 Power down all of chip at PD pin asserted low.

0 Pull down the panel output at PD pin asserted low.

6 5x Clock Multiplier power down

1 Power down 5x clock multiplier

0 Enable 5x clock multiplier

5 Enable Mode Change Status

1 Enable Mode Change Status clear bit. FDIV[4] needs to be cleared by writing a zero

0 Disable Mode Change Status. FDIV[4] will be cleared automatically at the end of each frame

4 Mode Change Status

1 Set to 1 when the input rows or columns changes by 4 pixels or more from previous frame

0 Writing a zero to this bit will clear it if Mode Change Status is enabled

3 Line Rate too Fast Status: 1=too fast, 0=in range

2 Frame Rate too Fast Status: 1=too fast, 0=in range

1 Out of Range due to window boxing Status: 1=Out of Range, 0=in range

0 XCLK too slow Status: 1=too slow, 0=in range

Clock Multiplier Register – IDIV

Read/Write Only at Address: 183(B7h)
Group Address: 01
Reset Value: Undefined

7	6	5	4	3	2	1	0
Bypass PLL	Reserved						

7 Bypass PLL

1 Bypass he clock generator, internal XCLK equals external XCLK.

0 Internal XCLK generated by the clock generator. Clock multiplier is fixed at 5

I²C Slave Address Registers - SADx

Write Only at Address: 62(3Eh) – 63(3Fh)
Group Address: 01
Reset Value: Undefined

These registers determine the I²C slave mode address. The 10-bit value in these registers must be even. The suggested value is 1C0.

I²C Upper Slave Address – SAD1

Write Only at Address: 62(3Eh)
Reset Value: Undefined

7	6	5	4	3	2	1	0
Reserved						SAD1[9:8] - Slave Address	

7:2 Reserved

These bits must be set to 0.

1:0 Upper 2-bits of 10-bit SAD1[9:0] Slave Address

The upper 2-bits of a total 10 bit slave address for I²C operation. Used with SAD2 to make 10-bit address.

I²C Lower Slave Address – SAD2

Write Only at Address: 63(3Fh)
Reset Value: Undefined

7	6	5	4	3	2	1	0
SAD2[7:0] - - Slave Address							

7:0 Lower 8-bits of 10-bit SAD2[9:0] Slave Address

The lower 8-bits of a total 10 bit slave address for I²C operation. Used with SAD1 to make 10-bit address. Please refer to the I²C slave address table for the PROM byte address.

Gamma Table Registers – G1###, G2###

Read or Write at address: 00 (00h) to 1535 (5FFh) in Group address 00. The order is red, green, blue.
Group Address: 00
Reset value is undefined.
.

7	6	5	4	3	2	1	0
G###[7:0] – Gamma Value							

Figure XXX: G### register

7:0 Gamma Table Entry

Values of ### from 0 to 255 are for the red table gamma1, for 256 to 511 are for the green table gamma1 and from 512 to 767 are for the Blue table gamma1. Values of ### from 768 to 1023 are for the red table gamma2, for 1024 to 1279 are for the green table gamma2 and for 1280 to 1535 are for the Blue table gamma2. The values are the output level for the corresponding input.

Note that the Bypass Bit for the Gamma1 Table is ICC1[4] and for Gamma2 Table is ICC1[5].

Dithering Table Registers – D4##, D2##

Read and Write at address: 184 (68h) to 215 (D7h) for D4## and 216 (D8h) to 223 (DFh) for D2##.
Reset value is undefined.

Dithering Registers – D4##

These registers set the pattern for dithering.

7	6	5	4	3	2	1	0
D4##[7:0] – Dithering pattern							

Figure XXX: D4## register

7:0 D4##

Dithering pattern when ## goes from 01 to 32. This pattern generates the ¼ and ¾ levels.

Dithering Registers – D2##

These registers set the pattern for dithering.

7	6	5	4	3	2	1	0
D2##[7:0] – Dithering pattern							

Figure XXX: D4## register

7:0 D2##

Dithering pattern when ## goes from 01 to 08. This pattern generates the ½ level.

Window Boxing Registers – ICPx, IRPx, XRWx

Input Columns Previous – ICP1

Read at Address: 20 (14h)
Group Address: 01
Reset Value: undefined

7	6	5	4	3	2	1	0
Reserved					ICP1[10:8] - Input Columns		

7:3 Reserved

These bits must be set to 0.

2:0 Upper 3-bits of 11-bit Input Columns (Read Only)

ICP1[10:8] the upper 3-bits of a total 11-bit number of pixels counted **minus one** in the most recent row of input data. Used with ICP2 to make 11-bit total.

Input Columns Previous – ICP2

Read at Address: 21 (15h)
Group Address: 01
Reset Value: undefined

7	6	5	4	3	2	1	0
ICP2[7:0] - Input Columns							

7:0 Lower 8-bits of 12-bit Input Columns (Read Only)

ICP2[7:0] the lower 8-bits of a total 11-bit number of pixels counted **minus one** in the most recent row of input data. Used with ICP1 to make 11-bit total.

Note that update of the above registers is NOT affected by register RMDT[6].

Input Rows – IRP1

Read at Address: 22 (16h)
Group Address: 01
Reset Value: Undefined

7	6	5	4	3	2	1	0
Reserved					IRP1[10:8] - Input Rows		

7:3 Reserved

These bits must be set to 0.

2:0 Upper 3-bits of 11-bit Input Rows (Read Only)

IRP1[10:8] the upper 3-bits of a total 11-bit number of rows counted in the previous frame. Used with IRP2 to make 11-bit total.

Input Rows – IRP2

Read at Address: 23 (17h)
Group Address: 01
Reset Value: Undefined

7	6	5	4	3	2	1	0
IRP2[7:0] - Input Rows							

7:0 Lower 8-bits of 11-bit Input Rows (Read Only)

IRP2[7:0] the lower 8-bits of a total 11-bit number of rows counted in the previous frame. Used with IRP1 to make 11-bit total.

Fill Window Box – XRW1

Read/Write at Address: 227 (E3h)
Group Address: 01
Reset Value: Undefined

7	6	5	4	3	2	1	0
Reserved		Transparency		Window Box	XRW1[10:8] - Row		

7:6 Reserved

These bits must be set to 0.

5:4 OSD Transparency

00 Opaque

01 25% transparent

10 50% transparent

11 75% transparent

3 Manual Window Box

1 Enable Manual Window Boxing. Do not enable with automatic window boxing mode.

0 Disable Manual Window Boxing

2:0 Upper 3-bits of 11-bit Row

XRW1[10:8] the upper 3-bits of a total 11-bit number for the row after which the OSD background is used for the image. Used with FWB2 to make 11-bit total.

Fill Window Box – XRW2

Read/Write at Address: 228 (E4h)
Group Address: 01
Reset Value: Undefined

7	6	5	4	3	2	1	0
XRW2[7:0] - Row							

7:0 Lower 8-bits of 10-bit Row

XRW2[7:0] the lower 8-bits of a total 11-bit number for the row after which the OSD background is used for the image. Used with XRW1 to make 11-bit total.

Character Based Text Registers – T####

Write at Address: 6144 (1800h) to 7168 (1C00h)
Group Address: 11
Reset Value: Undefined

7	6	5	4	3	2	1	0
Highlight	Double	Character[5:0]					

7 Highlight

1 Highlight color by flipping color table

0 normal color

6 Double

1 Enable Doubling Pixel size. Entire row must be doubled.

0 normal 12x16 character size

5:0 Character[5:0]

The character in the character set from 0 to 63.

OSD Character Color Lookup Tables – CL1x, CL2x, CL[3:F]X

Write Only at Address: 140(8Ch) – 142(8Eh), 143(8Fh) – 145(91h), 64(40h) – 102(66h)
Group Address: 01
Reset Value: Undefined

These registers make up the color lookup table used by the character based OSD. There are a total of 15 colors, thus there are 15 entries in the table. There is no entry 0, as this is the transparent color. Each of the entries consists of a 24-bit RGB value. The address locations of the entries in this table are shown in *Table 12: Character Based OSD.*

Red Component – Character Color Lookup Table

Write Only at Address:
Reset Value: Undefined

7	6	5	4	3	2	1	0
RED[7:0] - Red Component							

7:0 Color Components

RED[7:0] 8-bit Red sub component.

Green Component – Character Color Lookup Table

Write Only at Address:
Reset Value: Undefined

7	6	5	4	3	2	1	0
GREEN[7:0] - Green Component							

7:0 Color Components

GREEN[7:0] 8-bit Green sub component.

Blue Component – Character Color Lookup Table

Write Only at Address:
Reset Value: Undefined

7	6	5	4	3	2	1	0
BLUE[7:0] - Blue Component							

7:0 Color Components

BLUE[7:0] 8-bit Blue sub component.

DE Generation Registers for Parallel Input

DE register names and addresses

Addr. Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
94h ADD1	RSVD	DE_GEN (RW)	VS_POL (RW)	HS_POL (RW)	RSVD			DE_ DLY[8] (RW)
95h ADD2	DE_DLY[7:0] (WO)							
A1 ADE1	RSVD					DE_CNT[10:8] (WO)		
A2h ADE2	DE_CNT[7:0] (WO)							
A3h AHDL	RSVD	DE_TOP[6:0] (WO)						
E5h AHC1	RSVD					H_RES[10:8] (RO)		
E6h AHC2	H_RES[7:0] (RO)							
E7h AVC1	RSVD					V_RES[10:8] (RO)		
E8h AVC2	V_RES[7:0] (RO)							
E9h ADN1	RSVD					DE_LIN[10:8] (WO)		
EAh ADN2	DE_LIN[7:0] (WO)							

Notes: [1] All values are Bit 7 [MSB] and Bit 0 [LSB]. [2] RW = Read/Write register, RO = Read Only register.

DE register definitions

Function	Access	Description
DE_DLY[8:0]	WO	Defines the width of the area to the left of the active display. The unit of measurement is pixels. This register should be set to the sum of the (horizontal sync width + horizontal back porch + horizontal left border).
HS_POL	RW	Horizontal Sync Polarity: 1: Positive polarity (leading edge rises) 0: Negative polarity (leading edge falls)
VS_POL	RW	Vertical Sync Polarity: 1: Positive polarity (leading edge rises) 0: Negative polarity (leading edge falls)
DE_GEN	RW	Generate DE: 1: DE generator enabled. External DE signal ignored. 0: DE generator disabled. External DE signal used.
DE_TOP[6:0]	WO	Defines the height of the area above the active display. The unit of measurement is lines (HSYNC pulses). This register should be set to the sum of the (vertical sync width + vertical back porch + vertical top border).
DE_CNT[10:0]	WO	Defines the width of the active display. The unit of measurement is pixels. This register should be set to the desired horizontal resolution.
DE_LIN[10:0]	WO	Defines the height of the active display area. The unit of measurement is lines (HSYNC). This register should be set to the desired vertical resolution.
H_RES[10:0]	RO	Measured time between two consecutive HSYNC pulses. The unit of measurement is pixels.
V_RES[10:0]	RO	Measured time between two consecutive VSYNC pulses. The unit of measurement is lines (HSYNC pulses).

DE Generator

This chip contains a DE generator state machine, which is used when the original video source does not provide a DE signal. The DE generator must be programmed via the I^2C interface. There are a number of registers associated with the DE generator, and their functions are graphically represented in Figure 19.

The V_RES and H_RES registers are outputs, and represent the total vertical and horizontal resolutions, respectively. SiI861 counts these and makes them available at all times, whether or not the DE generator is active. Note that as the Figure shows, these values will be larger than the actual display area.

The rest of the registers are inputs to the DE generator function, and they define the boundaries of the display area. By definition, these delays are measured from the leading edge of the vertical or horizontal sync pulse, as appropriate. Note that the leading edge may be the rising or the falling edge, depending on signal polarity (as defined by the VS_POL and HS_POL control bits).

The DE_TOP register defines the top border. The unit of measurement is lines (HSYNC pulses). This register should be set to the sum of the (vertical sync width + vertical back porch + vertical top border). The DE_LIN register then defines the desired vertical resolution, also in line units.

The DE_DLY register defines the left border. The unit of measurement is pixels. This register should be set to the sum of the (horizontal sync width + horizontal back porch + horizontal left border). The DE_CNT register then defines the desired horizontal resolution, also in pixel units.

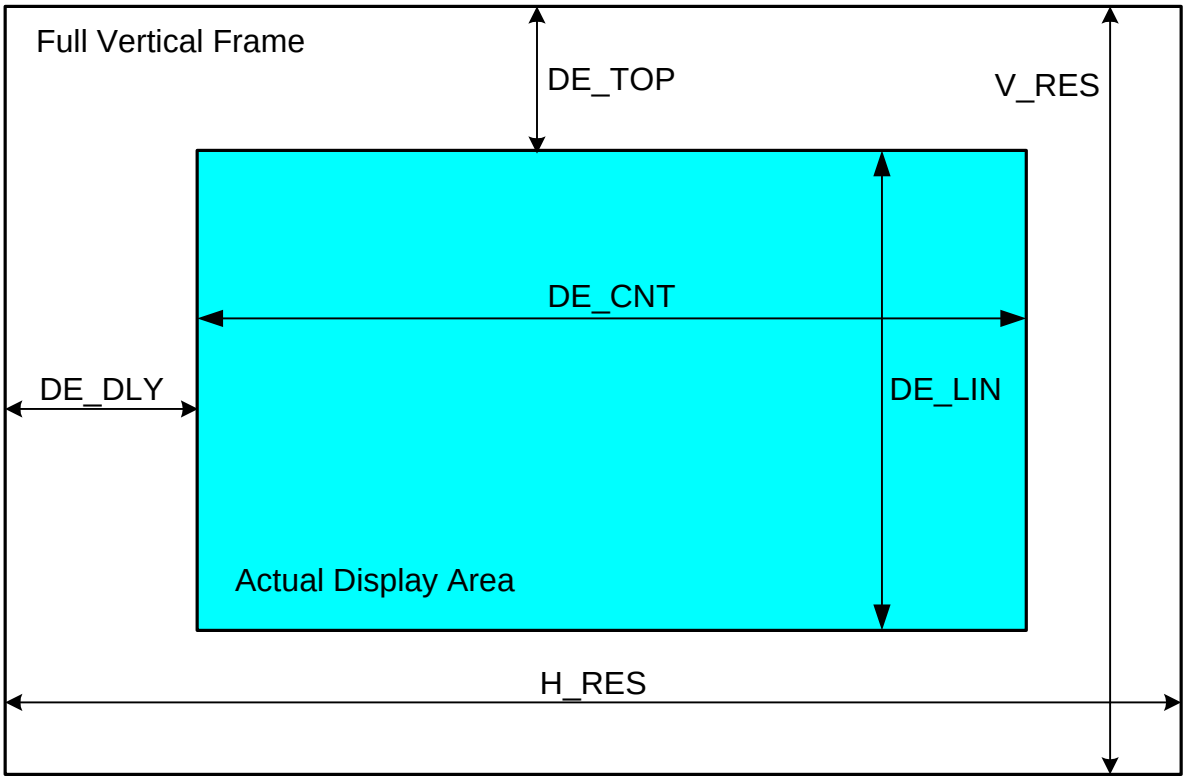


Figure 19. DE Generator Register Functions

24. Electrical Specifications

Absolute Maximum Conditions

Table 25. Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage 3.3V	-0.3		4.0	V
V_I	Input Voltage	-0.3		V_{CC}+ 0.3	V
V_O	Output Voltage	-0.3		V_{CC}+ 0.3	V
T_A	Ambient Temperature (with power applied)	-25		105	°C
T_{STG}	Storage Temperature	-40		125	°C

Notes: Permanent device damage may occur if absolute maximum conditions are exceeded.
Functional operation should be restricted to the conditions described under Normal Operating Conditions.

Table 26. Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage [1]	3.00	3.3	3.60	V
V_{CCN}	Supply Voltage Noise[1, 2]			100	mV_{P-P}
T_A	Ambient Temperature (with power applied)	0	25	70	°C
Θ_{Ja}	859: Thermal Resistance (Theta Ja) [3] Bottom epad not soldered to PCB			25	°C/W
Θ_{Ja}	859: Thermal Resistance (Theta Ja) [3] Bottom epad soldered to PCB			19	°C/W
Θ_{Ja}	861: Thermal Resistance (Theta Ja) [3]			20	°C/W

Note:
[1] Applies to all supply pins.
[2] Guaranteed by design.
[3] Airflow is 0 m/s.

Table 27. DC Digital I/O Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High-level Input Voltage		2			V
V_{IL}	Low-level Input Voltage				0.8	V
V_{OH}	High-level Output Voltage		2.4			V
V_{OL}	Low-level Output Voltage				0.4	V
I_{IL}	Input Leakage Current		-10uA		+10uA	µA

Under normal operating conditions unless otherwise specified.

DC Specifications

Table 28. DC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{OHD}	Output Drive	$V_{OUT} = V_{OH}$		-4		mA
		$V_{OUT} = V_{OL}$		4		
V_{ID}	Differential Input Voltage (Single Ended Amplitude)		TBD		TBD	mV
I_{PD}	Power-down Current[2]	XGA (65MHz) / SXGA (56MHz)			TBD	mA
I_D	Pull-down Current[3]	XGA (65MHz)			TBD	mA
I_D	Pull-down Current[3]	SXGA (56MHz)			TBD	mA
I_{CCR}	Receiver Supply Current[4]	ODCK = 65MHz R_{EXT_SWING} = 680Ω, C_L = 10pF Worst Case Pattern[1]			TBD	mA
I_{CCR}	Receiver Supply Current	ODCK = 56MHz, 2-pixel/clock mode, R_{EXT_SWING} = 680Ω, C_L = 10pF Worst Case Pattern[1]			TBD	mA
P_{CCR}	Power	ODCK = 65MHz[4] R_{EXT_SWING} = 680Ω, C_L = 10pF Worst Case Pattern[1]			TBD	W
P_{CCR}	Power	ODCK = 56MHz, 2-pixel/clock mode, R_{EXT_SWING} = 680Ω, C_L = 10pF Worst Case Pattern[1]			TBD	W

Under normal operating conditions unless otherwise specified.

Note:
[1] Black and white checkerboard pattern, each checker is one pixel wide.
[2] FDIV[7] = 1, PD pin = 0 (See Power Management section)
[3] FDIV[7] = 0, PD pin = 0 (See Power Management section)
[4] Operation in both 1-pixel/clock and 2-pixel/clock modes

AC Specifications

Table 29. AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{DPS}	Intra-Pair (+ to -) Differential Input Skew[1]	112 MHz One pixel / clock			TBD	ps
T_{CCS}	Channel to Channel Differential Input Skew[1]	112 MHz One pixel / clock			TBD	ns
T_{IJIT}	Worst Case Differential Input Clock Jitter Tolerance[2,3]	112 MHz One pixel / clock			TBD	ps
D_{LHT}	Output Low to High Transition Time	C_L = 10pF			TBD	ns
D_{HLT}	Output High to Low Transition Time	C_L = 10pF			TBD	ns
T_{SOF}	Data and Controls Setup Time to ODCK 1 pixel/clock, XCLK at 50% duty cycle[5]	65 MHz C_L = 10pF	TBD			ns
	2-pixel/clock	112 MHz C_L = 10pF	TBD			ns
T_{HOF}	Data and Controls Hold Time to ODCK 1 pixel/clock, XCLK at 50% duty cycle[5]	65 MHz C_L = 10pF	TBD			ns
	2-pixel/clock	112 MHz C_L = 10pF	TBD			ns
R_{CIP}	ODCK Cycle Time[1], 1-pixel/clock		TBD		TBD	ns
F_{CIP}	ODCK Frequency[1], 1-pixel/clock		TBD		TBD	MHz
R_{CIP}	ODCK Cycle Time[1], 2-pixel/clock		TBD		TBD	ns
F_{CIP}	ODCK Frequency[1], 2-pixel/clock		TBD		TBD	MHz
R_{XIP}	XCLK Cycle Time[1] (Direct)		TBD		TBD	ns
F_{XIP}	XCLK Frequency[1] (Direct)		TBD		TBD	MHz
R_{XIP}	XCLK Cycle Time[1] (Using Clock Generator)		TBD		TBD	ns
F_{XIP}	XCLK Frequency[1] (Using Clock Generator)		TBD		TBD	MHz
R_{XIH}	XCLK High Time[1] (Staggered Output Mode)		TBD			ns
R_{XIL}	XCLK Low Time[1] (Staggered Output Mode)		TBD			ns
T_{SSF}	Data and Controls Setup Time to ODCK Staggered Output Mode – 2-pixels/clock, XCLK at 50% duty cycle[5]	112 MHz C_L = 10pF	TBD			ns
T_{HSF}	Data and Controls Hold Time to ODCK Staggered Output Mode – 2-pixels/clock, XCLK at 50% duty cycle[5]	112 MHz C_L = 10pF	TBD			ns
T_{ST}	ODCK high to even data output[1], XCLK at 50% duty cycle[5]		TBD			ns
T_{PDL}	Delay from PD Low to Latched Outputs[1]				TBD	R_{XIP}[4]
T_{RST}	RESET Low		TBD			R_{XIP}[4]

Under normal operating conditions unless otherwise specified.

Notes:
[1] Guaranteed by design.
[2] Jitter defined as per DVI 1.0 Specification, Section 4.6 *Jitter Specification.*
[3] Jitter measured with Clock Recovery Unit as per DVI 1.0 Specification, Section 4.7 *Electrical Measurement Procedures.*
[4] R_{XIP} is period of XCLK input clock.
[5] XCLK duty cycle determines ODCK duty cycle and staggered output mode setup time, T_{ST} .

25. Timing Diagrams

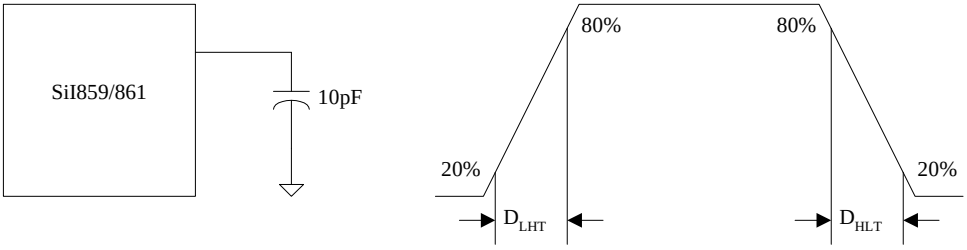


Figure 20. Digital Output Transition Times

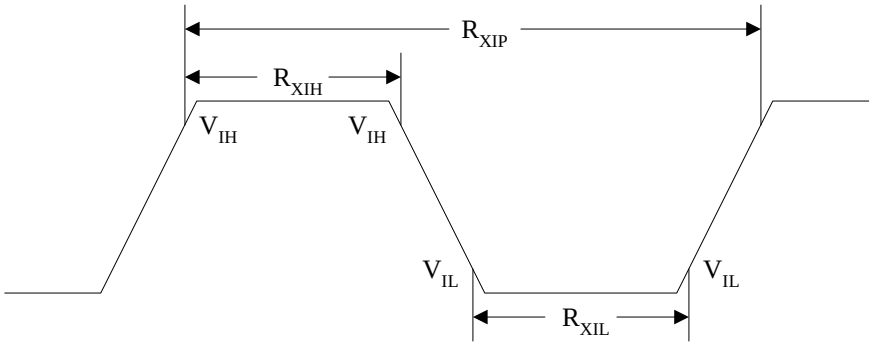


Figure 21. XCLK Input Clock Cycle/High/Low Times

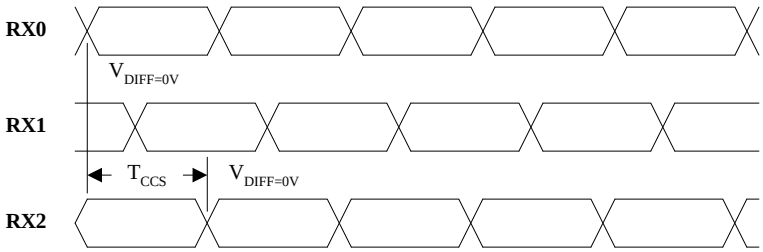
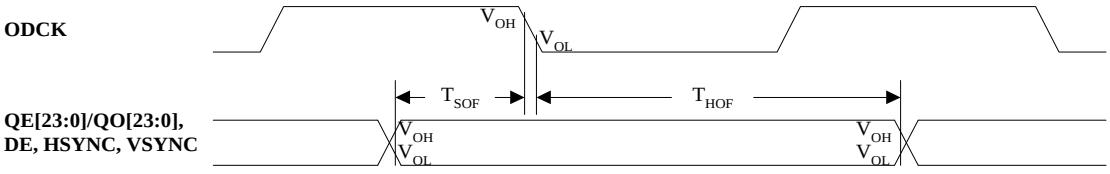


Figure 22. Channel-to-Channel Skew Timing

Output Timing



Please note that ODCK clock polarity may be inverted using POLT register. Setup and Hold times are always relative to active edge.

Figure 23. Data and Control Signals Setup/Hold Times to ODCK Falling Edge

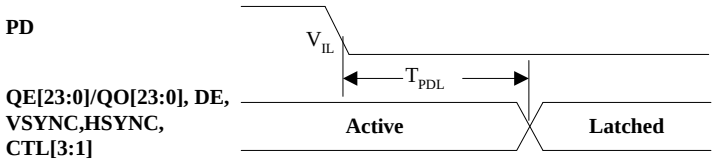
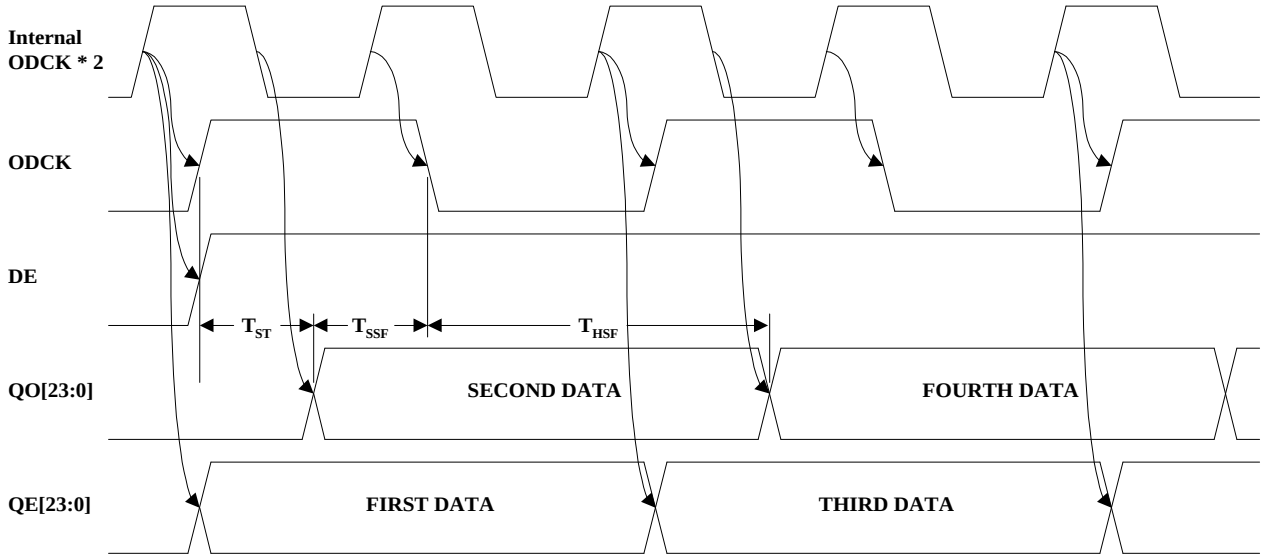


Figure 24. Output Signals Latched Timing from PD Active



Please note that ODCK clock and DE polarity may be inverted using POLT register. Setup and Hold times are always relative to active edge.

Figure 25. Staggered Output Timing

26. Package Dimensions

208-pin PQPF Thermally Enhanced Package Dimensions

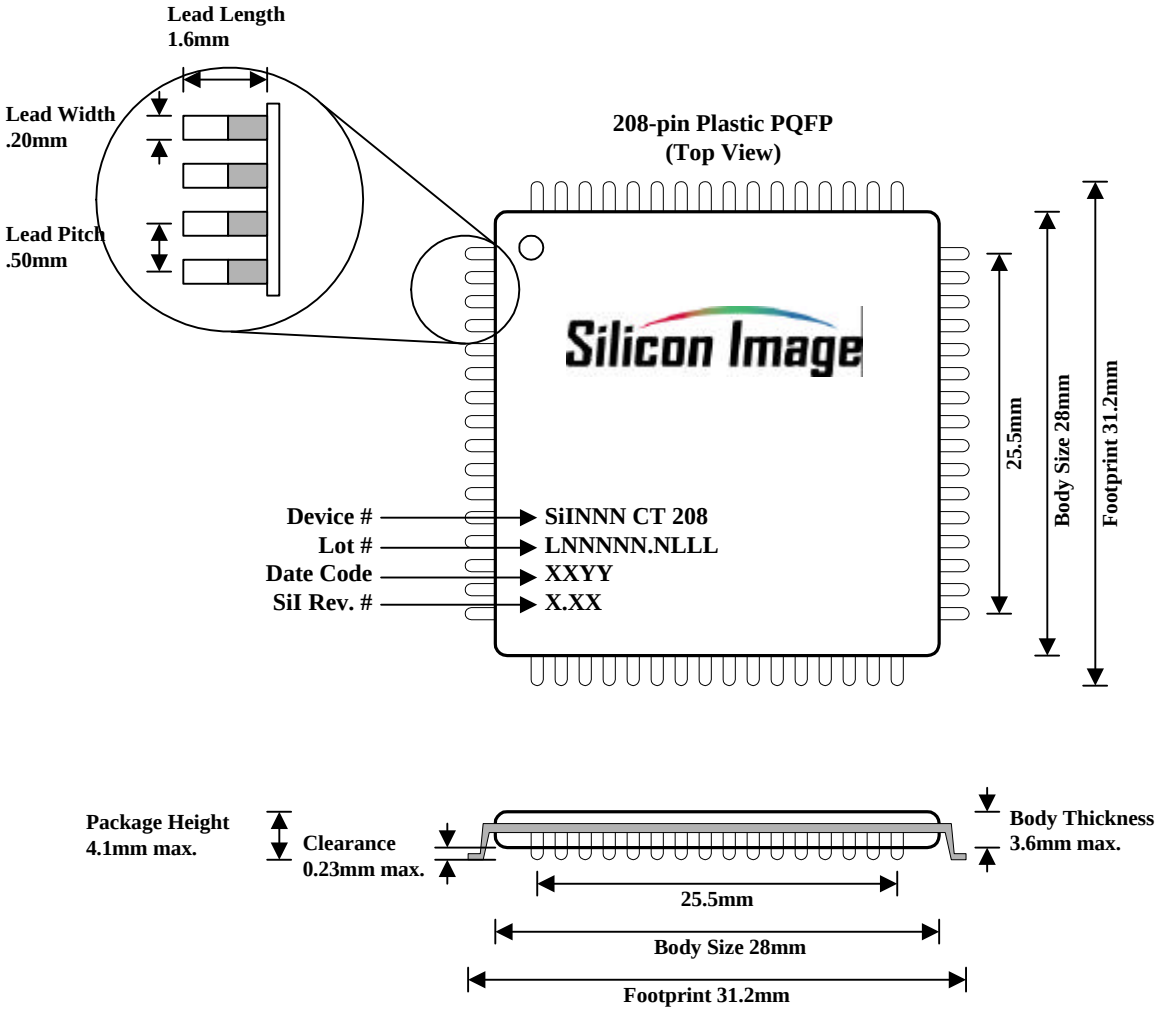


Figure 26. 208-pin PQFP Package Dimensions

100-pin TQPF Thermally Enhanced Package Dimensions

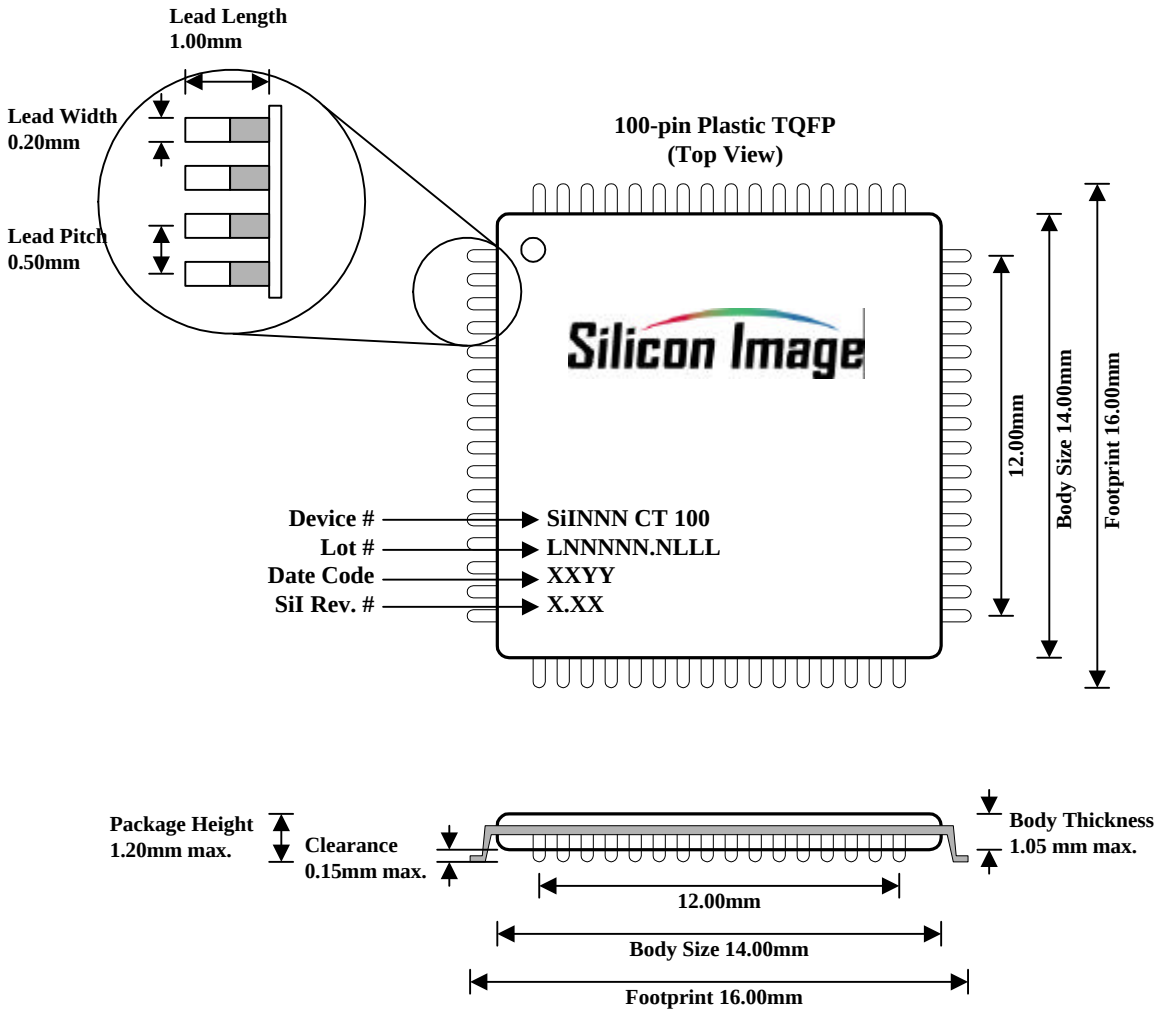


Figure 27. 100-pin TQFP Package Dimensions

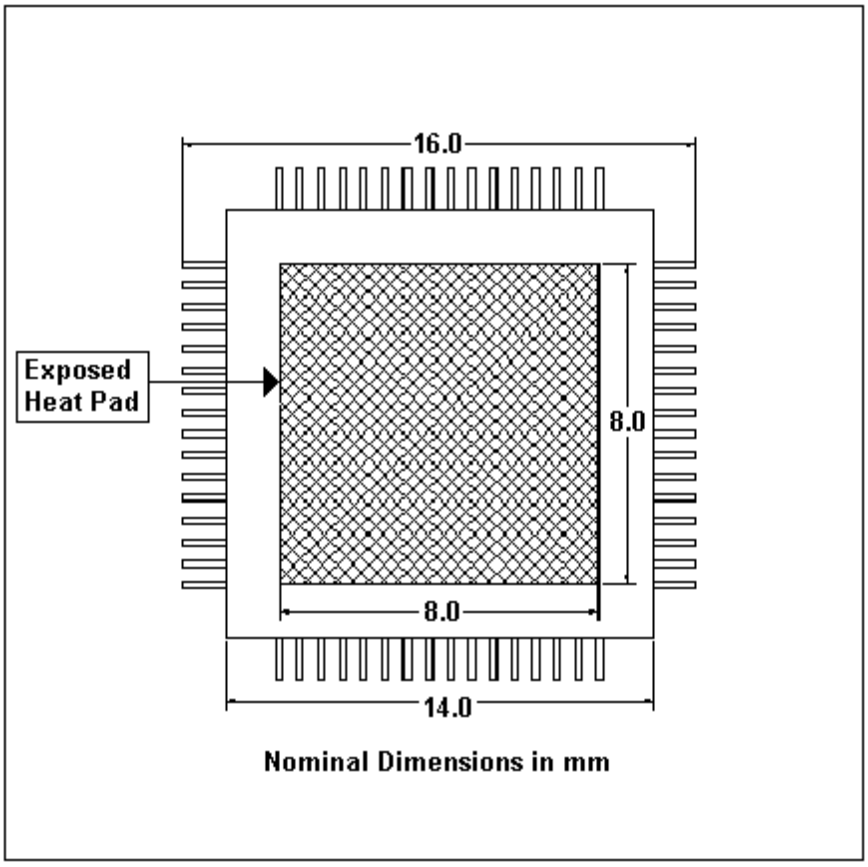


Figure 28. Bottom View of Thermally Enhanced 100-pin TQFP Package

27. 859 PCB Design Requirements

In order to remove the heat from the package, it is required that a thermal land be incorporated on the PCB within the footprint of the package corresponding to the exposed metal pad on the package, as shown in . Although the size of this thermal land can be larger than the exposed pad on the package, the solderable area, as defined by the solder mask, should be at least the same as the exposed pad area on the package. A clearance of at least 0.25 mm should be designed on the PCB between the outer edges of the thermal land and the inner edges of pad pattern for the leads to avoid any shorts.

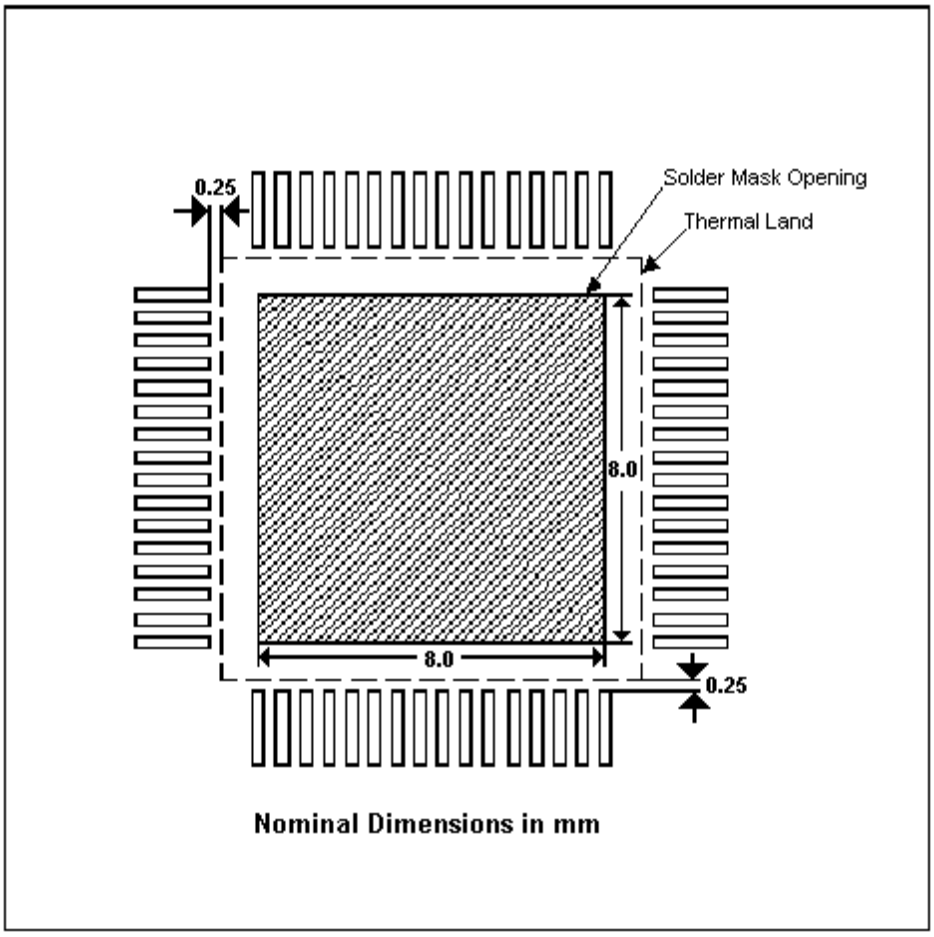


Figure 29. TQFP Thermal Land Design on PCB

While the thermal land on the PCB provides a means of heat transfer from the package to the board through a solder joint, thermal vias are required to remove the heat from the PCB. It is recommended that these vias connect to the ground plane of the PCB. These vias provide a heat transfer path from the top surface of the PCB to the inner layers and the bottom surface of the package. An array of vias should be incorporated in the thermal pad at 1.2 mm pitch grid, as shown in . It is also recommended that the via diameter should be around 12 to 13 mils (0.30 to 0.33 mm) and the via barrel should be plated with 1 oz copper to plug the via. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad and the thermal land. If the copper plating does not plug the vias, the thermal vias can be “tented” with solder mask on the top surface of the PCB to avoid solder wicking inside the via during assembly. The solder mask diameter should be at least 4 mils (0.1 mm) larger than the via diameter.

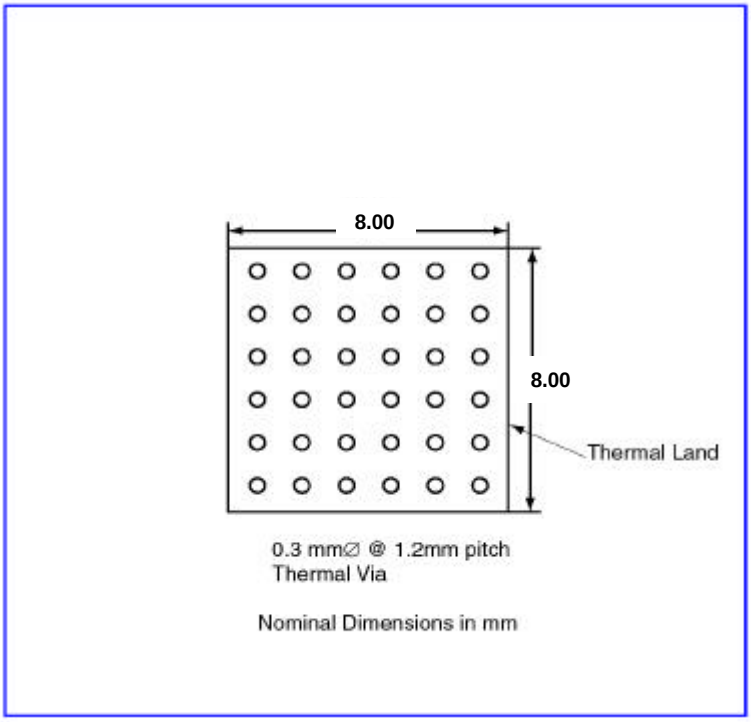


Figure 30. Thermal Pad Via Grid

Board Mounting Guidelines

The following are general recommendations for mounting exposed pad leadframe devices on the motherboard. This should serve as the starting point in assembly process development and it is recommended that the process should be developed based on past experience in mounting standard, non-thermally enhanced packages.

Stencil Design:

For proper heat transfer, it is required that the exposed pad on the package be soldered to the thermal land on the PCB. This requires solder paste application not only on the pad pattern for lead attachment but also on the thermal land using the stencil. While for standard (non-thermally enhanced) leadframe based packages the stencil thickness depends on the lead pitch and package coplanarity only, the package standoff also needs to be considered for the thermally enhanced packages to determine the stencil thickness. For a nominal standoff of 0.1 mm, the stencil thickness of 5 to 8 mils (depending upon the pitch) should still provide good solder joint between the exposed pad and the thermal land. The aperture openings should be the same as the solder mask opening on the thermal land. Since a large stencil opening may result in poor release, the aperture opening can be subdivided into an array of smaller openings, similar to the thermal land pattern shown in . The above guidelines will result in the solder joint area to be about 80 to 90% of the exposed pad area.

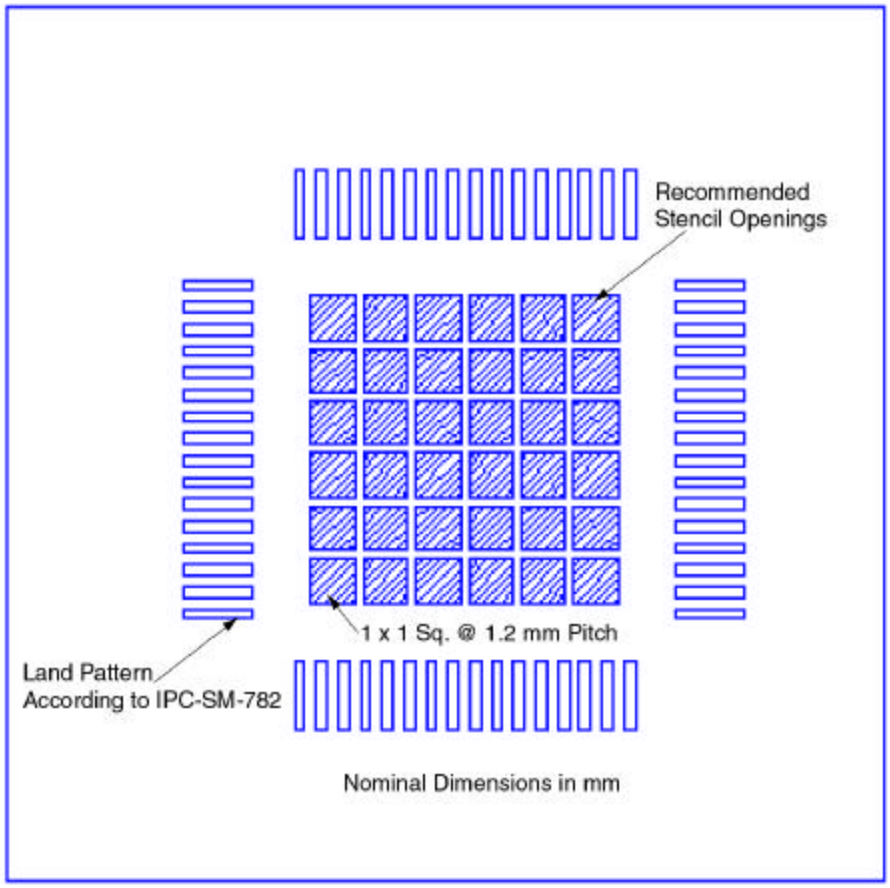


Figure 31. Recommended Stencil Design

Trademark Acknowledgment

Disclaimer

Revision History

Revision	Date	Comment
0.0	1/00	First Draft
0.1	2/00	Internal Release. Added corrections.
0.2	3/00	Internal Release for review. 859 added to databook. Pinout for 859 and 861 added. Crystal Oscillator explained. Pin numbers added for 859 and 861. Analog power pin connections still need to be added. Operation of ADC needs to be added. Character OSD needs to be re-written more clearly: Need to add info on highlight, transparency, and delay for LOS and OOR Register tables need to be organized more logically. Need to add which pins are 5V tolerant.
0.3	4/00	Character OSD section expanded. Added changes based on feedback from internal review. Pin names changed slightly for parallel input. Fixed pinout for I2C interface on Cipher and DDC bus. Added small HDCP section may need to be expanded. Added explanation of delay for Loss of Sync and Out of Range. Updated pinout for 861/859. Need to add: package for 208PQFP, register control for EDE pin.
0.4	4/00	Fixed pinout for LVDS transmitter. + and – were incorrect and needed to be swapped.
0.5	8/00	Removed 208 PQFP package. Added HDCP section. Added BGA pinout diagram. Added alphabetical BGA pin list. Added BGA package dimension drawing. Corrected OSD character bitmap structure – this has changed from the 851, also added table with memory addresses. Added CTL3 strapping section. Updated all 861 pin definition to reflect BGA package. Errors in Word Document: Figure and Tables are not numbered sequentially correctly. Added LVDS data mapping section. Added 859 block diagram.
0.6	11/00	Removed BGA package. Added 208 PQFP package and pinout info. Added DE generator registers. Change FFR1 registers to be fixed at 0Fh. Changed timing of MSTATE. Changed gamma table addresses.