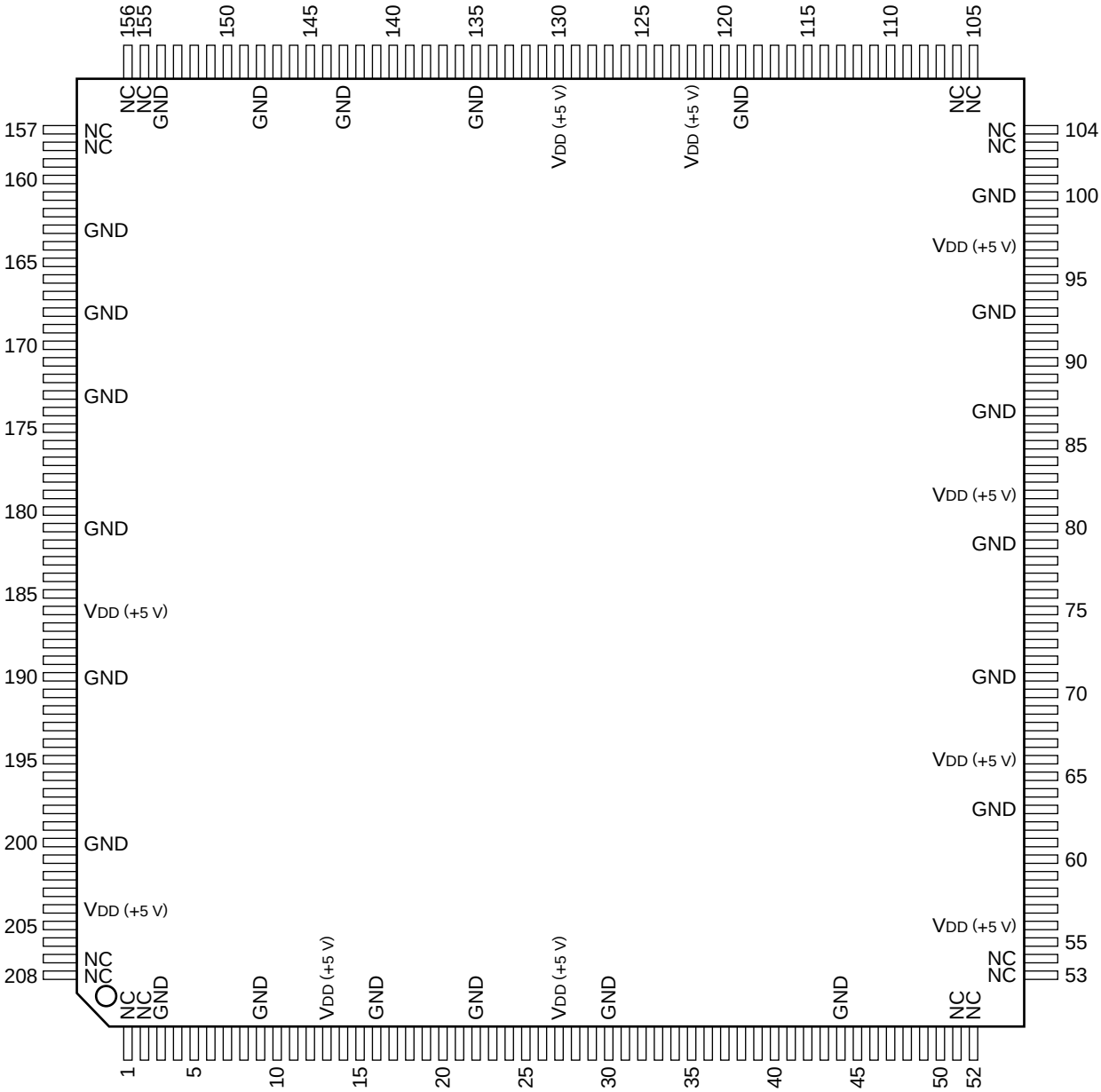
C-MOS SCSI I/O PROCESSOR

—TOP VIEW—



∗ SLAVE, Z = HIGH IMPEDANCE (V_{DD} = +5 V)

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	—	NC	53	—	NC	105	—	NC	157	—	NC
2	—	NC	54	—	NC	106	—	NC	158	—	NC
3	—	GND	55	O	$\overline{\text{MASTER}}$	107	I/O	D0	159	I/O	$\overline{\text{ATN}}$
4	∗ I, O	A10	56	—	V_{DD}	108	I/O	DP0	160	I/O	$\overline{\text{SDP0}}$
5	∗ I, O	A11	57	O	$\overline{\text{TIP}}$	109	I	DLE	161	I/O	$\overline{\text{SD7}}$
6	∗ I, O	A12	58	I	BCLK	110	∗ Z, O	SC0	162	I/O	$\overline{\text{SD6}}$
7	∗ I, O	A13	59	I/O	D31	111	∗ Z, O	SC1	163	—	GND
8	∗ I, O	A14	60	I/O	D30	112	I	BS0	164	I/O	$\overline{\text{SD5}}$
9	—	GND	61	I/O	D29	113	I	BS1	165	I/O	$\overline{\text{SD4}}$
10	∗ I, O	A15	62	I/O	D28	114	I	BS2	166	I/O	$\overline{\text{SD3}}$
11	∗ I, O	A16	63	—	GND	115	O	$\overline{\text{READYO}}$	167	I/O	$\overline{\text{SD2}}$
12	∗ I, O	A17	64	I/O	D27	116	I	$\overline{\text{CS}}$	168	—	GND
13	—	V_{DD}	65	I/O	D26	117	I	$\overline{\text{RESET}}$	169	I/O	$\overline{\text{SD1}}$
14	∗ I, O	A18	66	—	V_{DD}	118	I	$\overline{\text{BOFF}}$	170	I/O	$\overline{\text{SD0}}$
15	∗ I, O	A19	67	I/O	D25	119	—	GND	171	I/O	$\overline{\text{SDP1}}$
16	—	GND	68	I/O	D24	120	O	$\overline{\text{FETCH}}$	172	I/O	$\overline{\text{SD15}}$
17	∗ I, O	A20	69	I/O	$\overline{\text{DP3/ABRT}}$	121	∗ Z, I/O	$\overline{\text{BB}}$	173	—	GND
18	∗ I, O	A21	70	I/O	D23	122	—	V_{DD}	174	I/O	$\overline{\text{SD14}}$
19	∗ I, O	A22	71	—	GND	123	I	$\overline{\text{HLDAI}}$	175	I/O	$\overline{\text{SD13}}$
20	∗ I, O	A23	72	I/O	D22	124	O	$\overline{\text{HOLD}}$	176	I/O	$\overline{\text{SD12}}$
21	∗ I, O	A24	73	I/O	D21	125	I	SCLK	177	O	SDIRP0
22	—	GND	74	I/O	D20	126	O	$\overline{\text{IRQ}}$	178	O	SDIR7
23	∗ I, O	A25	75	I/O	D19	127	I	$\overline{\text{AUTO}}$	179	O	SDIR6
24	∗ I, O	A26	76	I/O	D18	128	I	DIFFSENS	180	O	SDIR5
25	∗ I, O	A27	77	I/O	D17	129	O	TGS	181	—	GND
26	O	$\overline{\text{MAC}}$	78	O	TSTOUT	130	—	V_{DD}	182	I	$\overline{\text{TSTIN}}$
27	—	V_{DD}	79	—	GND	131	O	IGS	183	O	SDIR4
28	∗ I, O	A28	80	I/O	D16	132	O	SELDIR	184	O	SDIR3
29	∗ I, O	A29	81	I/O	DP2	133	O	RSTDIR	185	O	SDIR2
30	—	GND	82	—	V_{DD}	134	O	BSYDIR	186	—	V_{DD}
31	∗ I, O	A30	83	I/O	D15	135	—	GND	187	O	SDIR1
32	∗ I, O	A31	84	I/O	D14	136	O	SDIR11	188	O	SDIR0
33	∗ I, O	$\overline{\text{ADS}}$	85	I/O	D13	137	O	SDIR10	189	O	SDIRP1
34	∗ I, O	$\overline{\text{BE3}}$	86	I/O	D12	138	O	SDIR9	190	—	GND
35	∗ I, O	$\overline{\text{BE2}}$	87	—	GND	139	O	SDIR8	191	O	SDIR15
36	∗ Z, O	FC2	88	I/O	D11	140	I/O	$\overline{\text{SD11}}$	192	O	SDIR14
37	∗ Z, O	FC1	89	I/O	D10	141	I/O	$\overline{\text{SD10}}$	193	O	SDIR13
38	∗ Z, O	FC0	90	I/O	D9	142	I/O	$\overline{\text{SD9}}$	194	O	SDIR12
39	I	GPI0	91	I/O	D8	143	—	GND	195	∗ I, O	$\overline{\text{BE0}}$
40	I	GPI1	92	I/O	DP1	144	I/O	$\overline{\text{SD8}}$	196	∗ I, O	$\overline{\text{BE1}}$
41	I	GPI2	93	—	GND	145	I/O	I/O	197	∗ I, O	A2
42	I	GPI3	94	I/O	D7	146	I/O	$\overline{\text{REQ}}$	198	∗ I, O	A3
43	O	GPO	95	I/O	D6	147	I/O	$\overline{\text{C/D}}$	199	∗ I, O	A4
44	—	GND	96	I/O	D5	148	—	GND	200	—	GND
45	∗ I, O	W/$\overline{\text{R}}$	97	—	V_{DD}	149	I/O	$\overline{\text{SEL}}$	201	∗ I, O	A5
46	∗ Z, O	$\overline{\text{TT1}}$	98	I/O	D4	150	I/O	$\overline{\text{MSG}}$	202	∗ I, O	A6
47	∗ Z, O	$\overline{\text{TT0}}$	99	I/O	D3	151	I/O	$\overline{\text{RST}}$	203	∗ I, O	A7
48	∗ O, I	$\overline{\text{TBI}}$	100	—	GND	152	I/O	$\overline{\text{ACK}}$	204	—	V_{DD}
49	I	$\overline{\text{READY1}}$	101	I/O	D2	153	I/O	$\overline{\text{BSY}}$	205	∗ I, O	A8
50	∗ O, I	$\overline{\text{TEA}}$	102	I/O	D1	154	—	GND	206	∗ I, O	A9
51	—	NC	103	—	NC	155	—	NC	207	—	NC
52	—	NC	104	—	NC	156	—	NC	208	—	NC

INPUT

$\overline{\text{AUTO}}$	: SCRIPTS AUTO-START MODE
BCLK	: BUS CLOCK
BOFF	: BACK OFF
BS0 - BS2	: BUS MODE SELECT
$\overline{\text{CS}}$	: CHIP SELECT
DLE	: DATA LATCH ENABLE
DIFFSENS	: DIFFERENTIAL SENSE
GPI0 - GPI3	: GENERAL PURPOSE
$\overline{\text{HLDAI}}$	: HOLD ACKNOWLEDGE
$\overline{\text{READYI}}$	: READY
$\overline{\text{RESET}}$	: CHIP RESET
SCLK	: SCSI CLOCK
$\overline{\text{TBI}}$	: TRANSFER BURST INHIBIT
$\overline{\text{TEA}}$	: TRANSFER ERROR ACKNOWLEDGE
$\overline{\text{TSTIN}}$	: TEST

OUTPUT

A2 - A31	: ADDRESS BUS
$\overline{\text{ADS}}$	: ADDRESS STROBE
$\overline{\text{BE0}}$ - $\overline{\text{BE3}}$	: BYTE ENABLE
BSYDIR	: DRIVER ENABLE CONTROL FOR SCSI BSY SIGNAL
FC0 - FC2	: FUNCTION CODES TRANSFER MODIFIER
$\overline{\text{FETCH}}$	: FETCHING OP CODE
GPO	: GENERAL PURPOSE
$\overline{\text{HOLD}}$	: HOLD
IGS	: INITIATOR DRIVER DIRECT CONTROL
$\overline{\text{IRQ}}$	: INTERRUPT REQUEST
$\overline{\text{MAC}}$	: MEMORY ACCESS CONTROL
$\overline{\text{MASTER}}$	: MASTER STATUS
READYO	: READY
RSTDIR	: DRIVER ENABLE CONTROL FOR SCSI RST SIGNAL
SC0, SC1	: SNOOP CONTROL
SDIR0 - SDIR15	: DRIVER DIRECTION CONTROL FOR SCSI DATA LINES
SDIRP0, SDIRP1	: DRIVER DIRECTION CONTROL FORSCSI PARITY SIGNAL
SELDIR	: DRIVER ENABLE CONTROL FOR SCSI SEL SIGNAL
TGS	: TRIGGER DRIVER DIRECT CONTROL
$\overline{\text{TIP}}$	: TRANSFER IN PROGRESS
TSTOUT	: TEST
$\overline{\text{TT0}}$, $\overline{\text{TT1}}$	: TRANSFER TYPE
W/$\overline{\text{R}}$	: READ/WRITE

INPUT/OUTPUT

$\overline{\text{ACK}}$	: DATA HANDSHAKE SIGNAL
$\overline{\text{ATN}}$	: ATTENTION
$\overline{\text{BB}}$	: BUS BUSY
$\overline{\text{BSY}}$	: SCSI BUS ARBITRATION SIGNAL
$\overline{\text{C/D}}$	: SCSI PHASE LINE COMMUNICATION DATA
D0 - D31	: HOST DATA BUS
DP0 - DP2	: HOST BUS DATA PARITY
$\overline{\text{DP3/ABRT}}$	: HOST BUS DATA PARITY
$\overline{\text{MSG}}$	: SCSI PHASE LINE MESSAGE
$\overline{\text{REQ}}$	: DATA HANDSHAKE SIGNAL
$\overline{\text{RST}}$	: SCSI BUS RESET
$\overline{\text{SD0}}$ - $\overline{\text{SD15}}$	: 16-BIT SCSI DATA BUS
$\overline{\text{SDP0}}$, $\overline{\text{SDP1}}$	: SCSI DATA PARITY BIT
$\overline{\text{SEL}}$	: SCSI BUS ARBITRATION SIGNAL SELECT DEVICE