



STY100NS20FD

N-CHANNEL 200V - 0.022Ω - 100A Max247
MESH OVERLAY™ Power MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D
STY100NS20FD	200V	< 0.024Ω	100 A

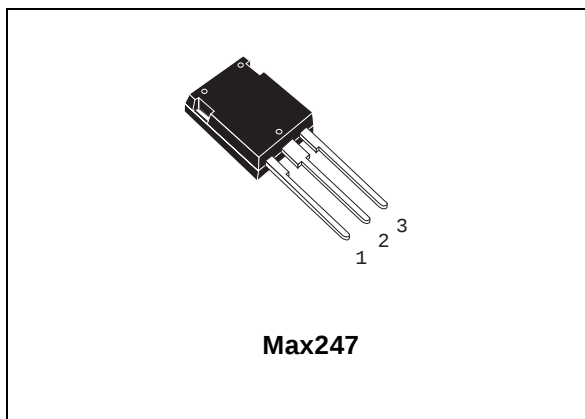
- TYPICAL R_{DS(on)} = 0.022Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- GATE CHARGE MINIMIZED
- ± 20V GATE TO SOURCE VOLTAGE RATING
- LOW INTRINSIC CAPACITANCE
- FAST BODY-DRAIN DIODE: LOW t_{rr}, Q_{rr}

DESCRIPTION

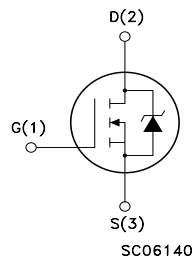
Using the latest high voltage MESH OVERLAY™ process, STMicroelectronics has designed an advanced family of power MOSFETs with outstanding performances. The new patented STrip layout coupled with the Company's proprietary edge termination structure, gives the lowest RDS(ON) per area, exceptional avalanche and dv/dt capabilities and unrivalled gate charge and switching characteristics.

APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SWITCH MODE POWER SUPPLY (SMPS)
- DC-AC CONVERTER FOR WELDING EQUIPMENT AND UNINTERRUPTABLE POWER SUPPLY AND MOTOR DRIVE



INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	200	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	200	V
V _{GS}	Gate- source Voltage	±20	V
I _D	Drain Current (continuous) at T _C = 25°C	100	A
I _D	Drain Current (continuous) at T _C = 100°C	63	A
I _{DM} (•)	Drain Current (pulsed)	400	A
P _{TOT}	Total Dissipation at T _C = 25°C	450	W
	Derating Factor	3.6	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	25	V/ns
T _{stg}	Storage Temperature	–65 to 150	°C
T _j	Max. Operating Junction Temperature	150	°C

(•)Pulse width limited by safe operating area

(1)I_{SD} ≤ 100A, di/dt ≤ 200A/μs, V_{DD} ≤ V_{(BR)DSS}, T_j ≤ T_{JMAX}

STY100NS20FD

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case	Max	0.277	°C/W
Rthj-amb	Thermal Resistance Junction-ambient	Max	30	°C/W
T _I	Maximum Lead Temperature For Soldering Purpose		300	°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T _j max)	100	A
E _{AS}	Single Pulse Avalanche Energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	750	mJ

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 µA, V _{GS} = 0	200			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125 °C			10 100	µA µA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 20V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250µA	3	4	5	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10V, I _D = 50A		0.022	0.024	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (1)	Forward Transconductance	V _{DS} > I _{D(on)} × R _{DS(on)} max, I _D = 50A		30		S
C _{iss}	Input Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		7900		pF
C _{oss}	Output Capacitance			1500		pF
C _{rss}	Reverse Transfer Capacitance			460		pF

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.

ELECTRICAL CHARACTERISTICS (CONTINUED) SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 100V, I_D = 50A$		42		ns
t_r	Rise Time	$R_G = 4.7\Omega, V_{GS} = 10V$ (see test circuit, Figure 3)		140		ns
Q_g	Total Gate Charge	$V_{DD} = 100V, I_D = 100A,$ $V_{GS} = 10V$		360		nC
Q_{gs}	Gate-Source Charge			35		nC
Q_{gd}	Gate-Drain Charge			135		nC

SWITCHING OFF

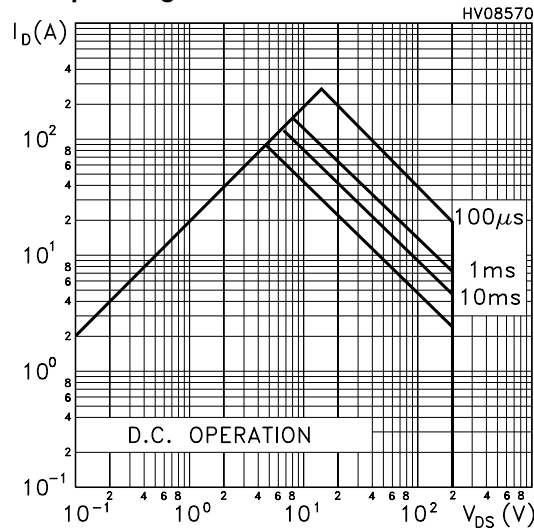
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_r(V_{off})$	Off-voltage Rise Time	$V_{DD} = 100V, I_D = 100A,$		245		ns
t_f	Fall Time	$R_G = 4.7\Omega, V_{GS} = 10V$ (see test circuit, Figure 5)		140		ns
t_c	Cross-over Time			220		ns

SOURCE DRAIN DIODE

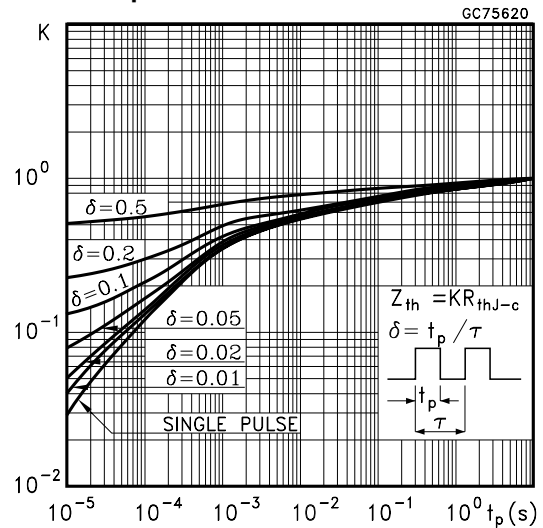
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				100	A
$I_{SDM} (2)$	Source-drain Current (pulsed)				400	A
$V_{SD} (1)$	Forward On Voltage	$I_{SD} = 100A, V_{GS} = 0$			1.6	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 100A, di/dt = 100A/\mu s,$ $V_{DD} = 160V, T_j = 150^\circ C$ (see test circuit, Figure 5)		225		ns
Q_{rr}	Reverse Recovery Charge			1.35		μC
I_{RRM}	Reverse Recovery Current			12		A

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

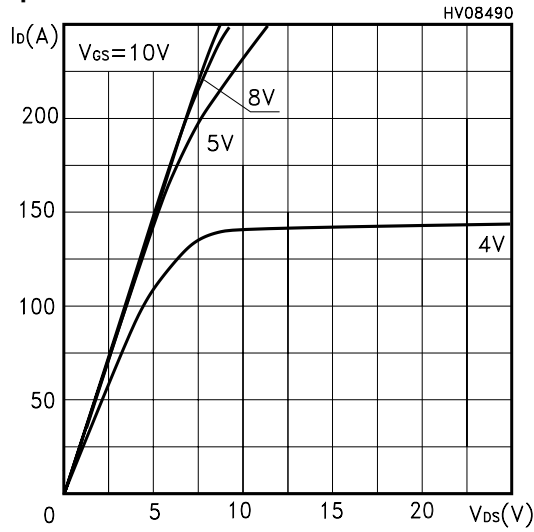
Safe Operating Area



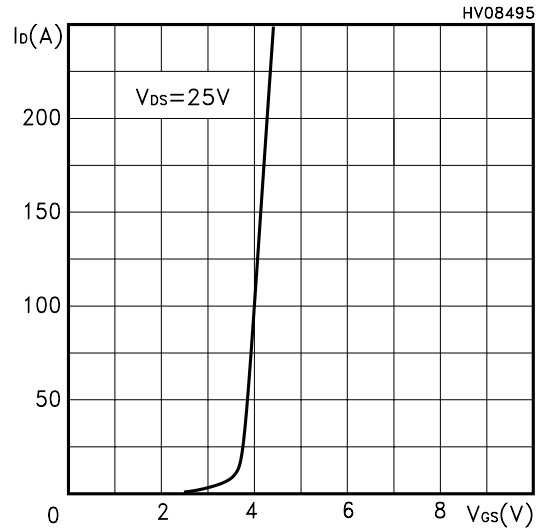
Thermal Impedance



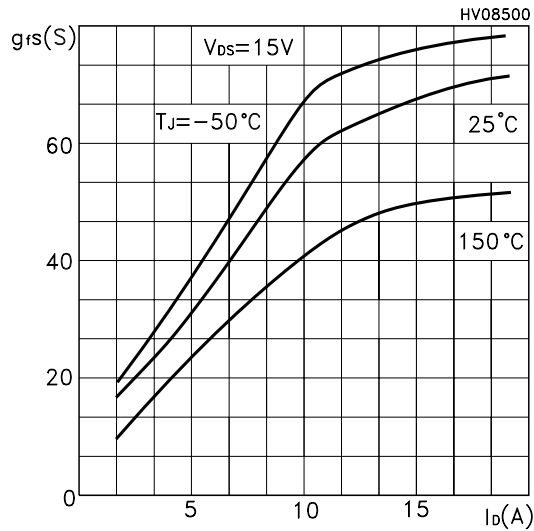
Output Characteristics



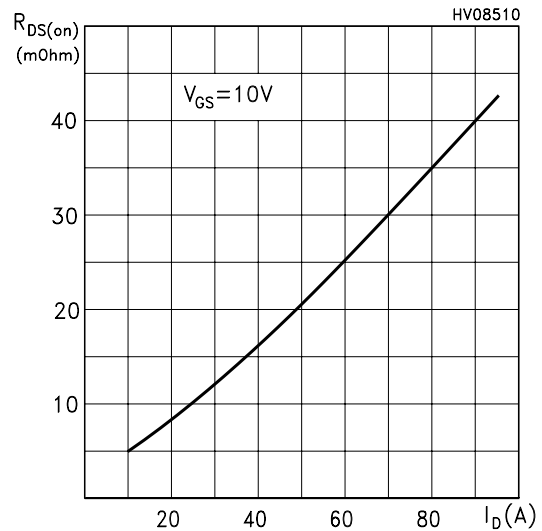
Transfer Characteristics



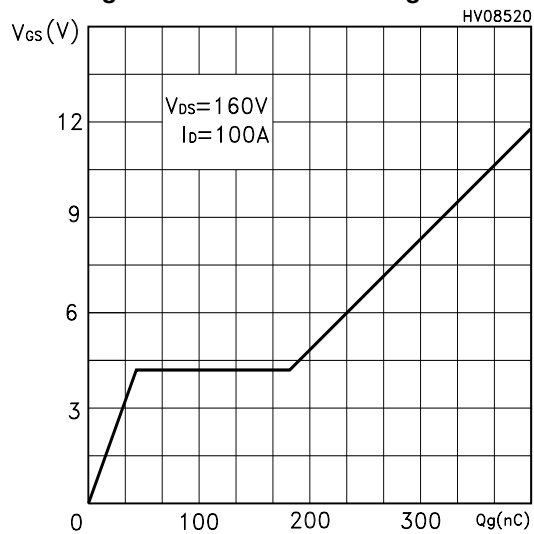
Transconductance



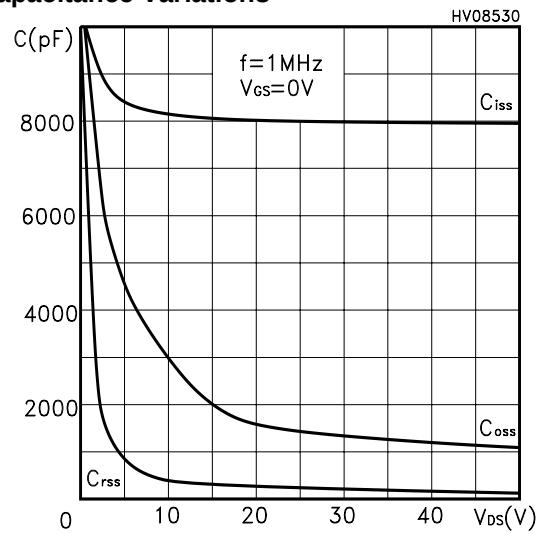
Static Drain-source On Resistance



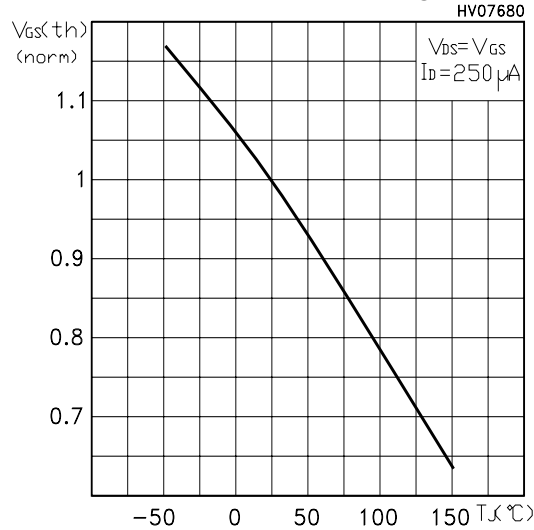
Gate Charge vs Gate-source Voltage



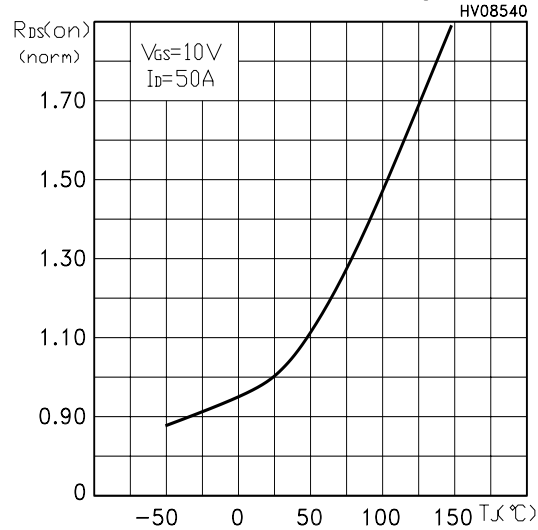
Capacitance Variations



Normalized Gate Thershold Voltage vs Temp.



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

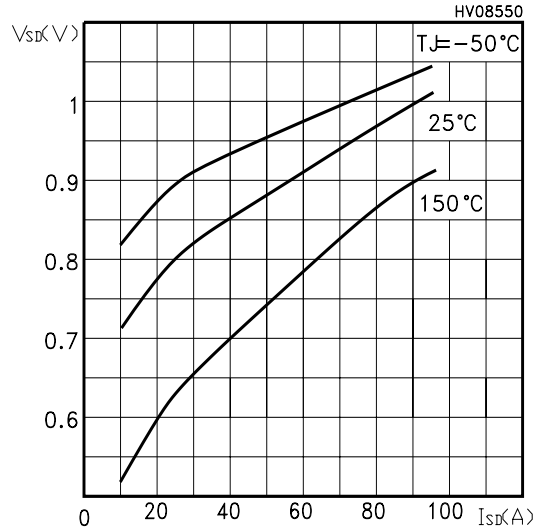


Fig. 1: Unclamped Inductive Load Test Circuit

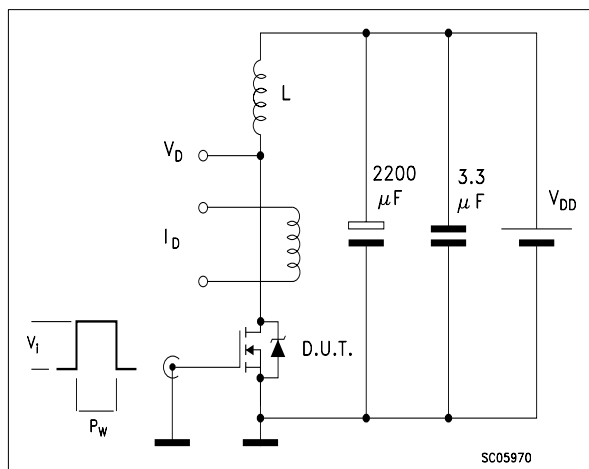


Fig. 2: Unclamped Inductive Waveform



Fig. 3: Switching Times Test Circuit For Resistive Load

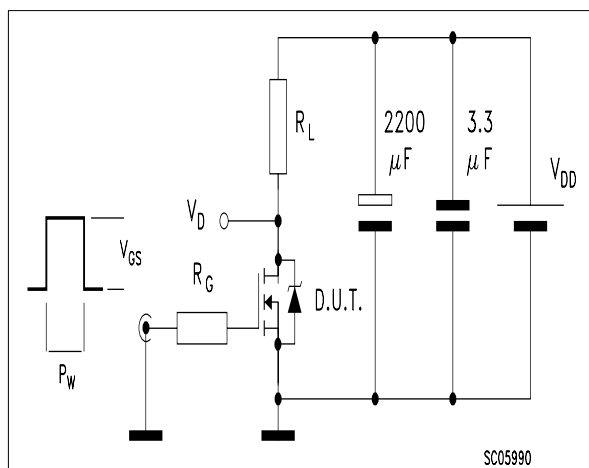


Fig. 4: Gate Charge test Circuit

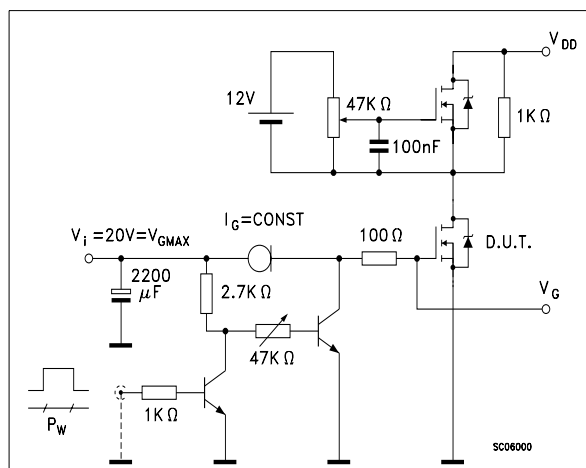
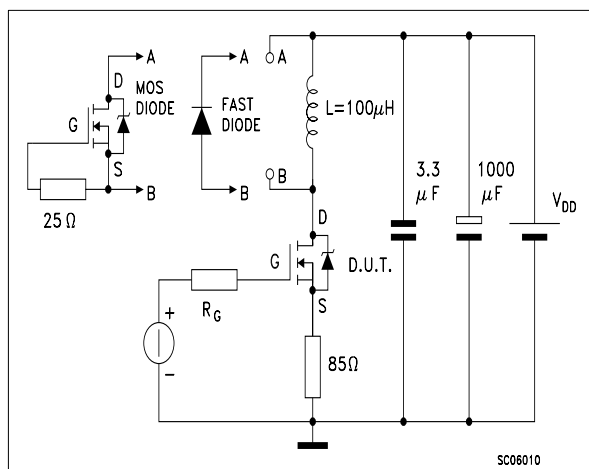
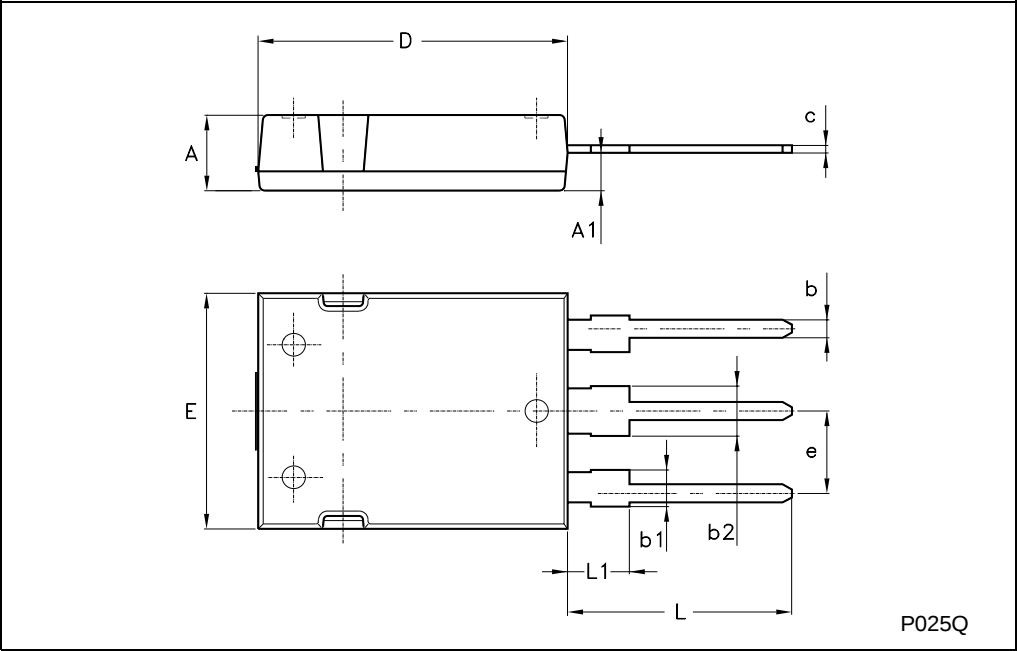


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



Max247 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.70		5.30			
A1	2.20		2.60			
b	1.00		1.40			
b1	2.00		2.40			
b2	3.00		3.40			
c	0.40		0.80			
D	19.70		20.30			
e	5.35		5.55			
E	15.30		15.90			
L	14.20		15.20			
L1	3.70		4.30			



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