



STW45NM50FD

N-CHANNEL 500V - 0.07Ω - 45A TO-247
FDmesh™ Power MOSFET (With FAST DIODE)

TYPE	V _{DSS}	R _{DS(on)}	I _D
STW45NM50FD	500V	< 0.1Ω	45 A

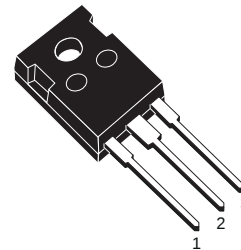
- TYPICAL R_{DS(on)} = 0.07Ω
- HIGH dv/dt AND AVALANCHE CAPABILITIES
- 100% AVALANCHE TESTED
- LOW INPUT CAPACITANCE AND GATE CHARGE
- LOW GATE INPUT RESISTANCE
- TIGHT PROCESS CONTROL AND HIGH MANUFACTURING YIELDS

DESCRIPTION

The FDmesh™ associates all advantages of reduced on-resistance and fast switching with an intrinsic fast-recovery body diode. It is therefore strongly recommended for bridge topologies, in particular ZVS phase-shift converters.

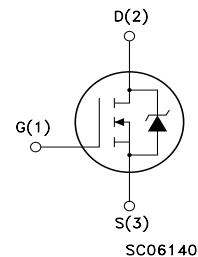
APPLICATIONS

- ZVS PHASE-SHIFT FULL BRIDGE CONVERTERS FOR SMPS AND WELDING EQUIPMENT



TO-247

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	500	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	500	V
V _{GS}	Gate- source Voltage	±30	V
I _D	Drain Current (continuous) at T _C = 25°C	45	A
I _D	Drain Current (continuous) at T _C = 100°C	28.4	A
I _{DM} (•)	Drain Current (pulsed)	180	A
P _{TOT}	Total Dissipation at T _C = 25°C	417	W
	Derating Factor	2.08	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	20	V/ns
T _{stg}	Storage Temperature	-65 to 150	°C
T _j	Max. Operating Junction Temperature	150	°C

(•) Pulse width limited by safe operating area

(1) I_{SD} ≤ 45A, di/dt ≤ 400A/μs, V_{DD} ≤ V_{(BR)DSS}, T_j ≤ T_{JMAX}.

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THERMAL DATA

Rthj-case	Thermal Resistance Junction-case	Max	0.3	°C/W
Rthj-amb	Thermal Resistance Junction-ambient	Max	30	°C/W
T _I	Maximum Lead Temperature For Soldering Purpose		300	°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T _j max)	22.5	A
E _{AS}	Single Pulse Avalanche Energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 35 V)	800	mJ

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED) OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 µA, V _{GS} = 0	500			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125 °C			10 100	µA µA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ±30V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250µA	3	4	5	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10V, I _D = 22.5A		0.07	0.10	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (1)	Forward Transconductance	V _{DS} > I _{D(on)} × R _{DS(on)} max, I _D = 22.5A		20		S
C _{iss}	Input Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		3600		pF
C _{oss}	Output Capacitance			680		pF
C _{rss}	Reverse Transfer Capacitance			82		pF
C _{oss} eq. (3)	Equivalent Output Capacitance	V _{GS} = 0V, V _{DS} = 0V to 400V		350		pF
R _G	Gate Input Resistance	f=1 MHz Gate DC Bias = 0 Test Signal Level = 20mV Open Drain		2		Ω

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.

ELECTRICAL CHARACTERISTICS (CONTINUED)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 250V$, $I_D = 22.5A$		28		ns
t_r	Rise Time	$R_G = 4.7\Omega$, $V_{GS} = 10V$ (see test circuit, Figure 3)		28		ns
Q_g	Total Gate Charge	$V_{DD} = 400V$, $I_D = 45A$, $V_{GS} = 10V$		92	120	nC
Q_{gs}	Gate-Source Charge			22		nC
Q_{gd}	Gate-Drain Charge			40		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	$V_{DD} = 400V$, $I_D = 45A$,		11		ns
t_f	Fall Time	$R_G = 4.7\Omega$, $V_{GS} = 10V$ (see test circuit, Figure 3)		25		ns
t_c	Cross-over Time			44		ns

SOURCE DRAIN DIODE

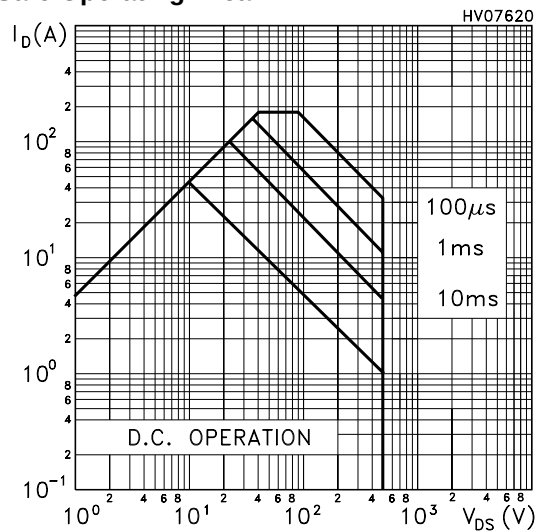
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				45	A
$I_{SDM(2)}$	Source-drain Current (pulsed)				180	A
$V_{SD(1)}$	Forward On Voltage	$I_{SD} = 45A$, $V_{GS} = 0$			1.5	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 45A$, $di/dt = 100A/\mu s$, $V_{DD} = 100V$ (see test circuit, Figure 5)		245		ns
Q_{rr}	Reverse Recovery Charge			2.2		μC
I_{RRM}	Reverse Recovery Current			18		A

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

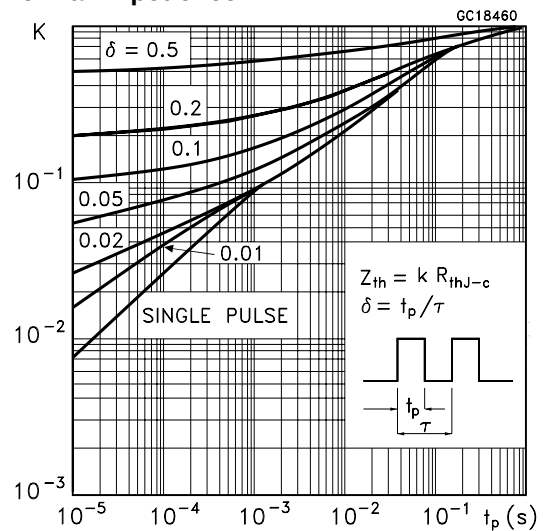
2. Pulse width limited by safe operating area.

3. $C_{oss eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

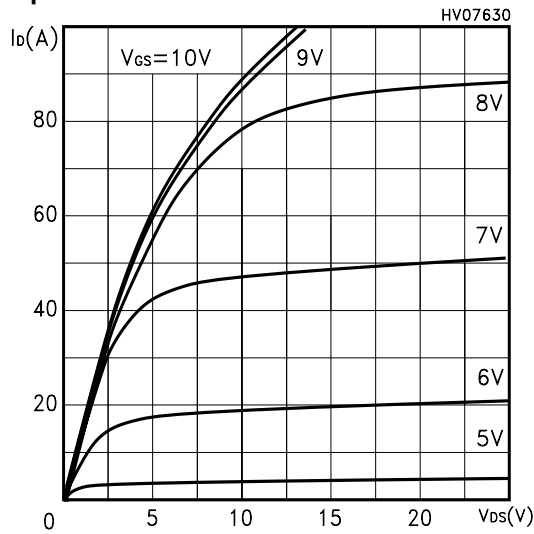
Safe Operating Area



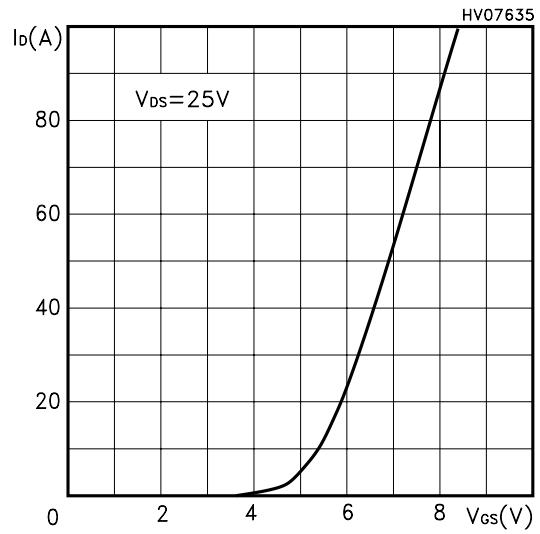
Thermal Impedance



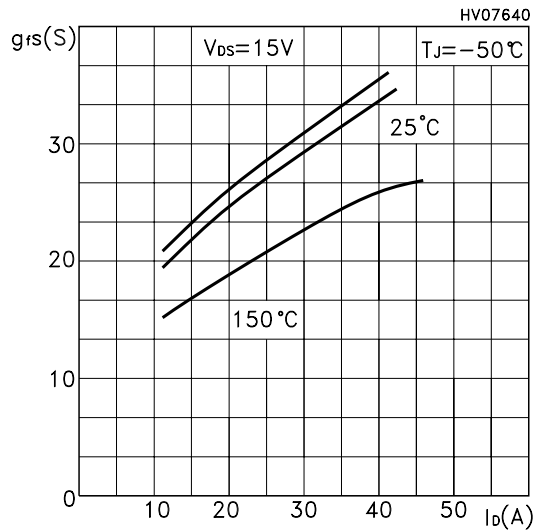
Output Characteristics



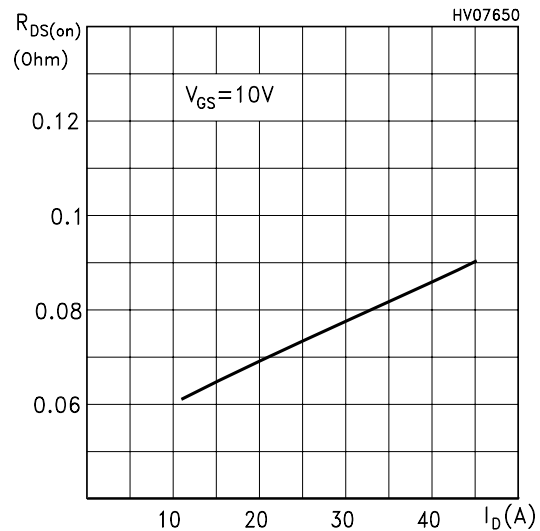
Transfer Characteristics



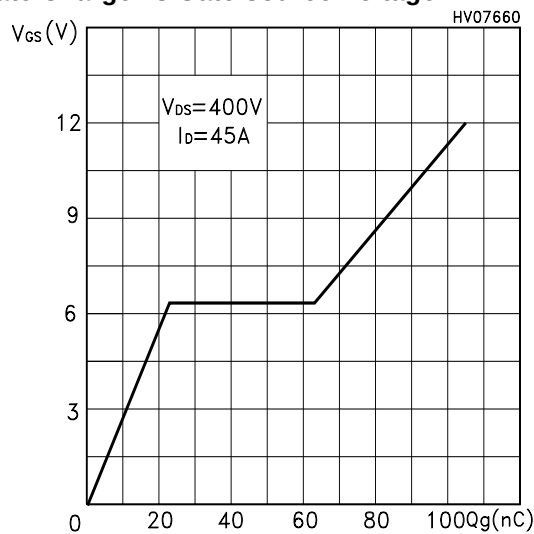
Transconductance



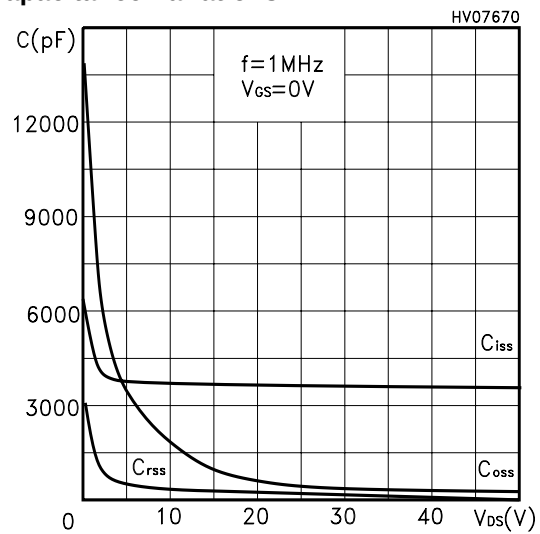
Static Drain-source On Resistance



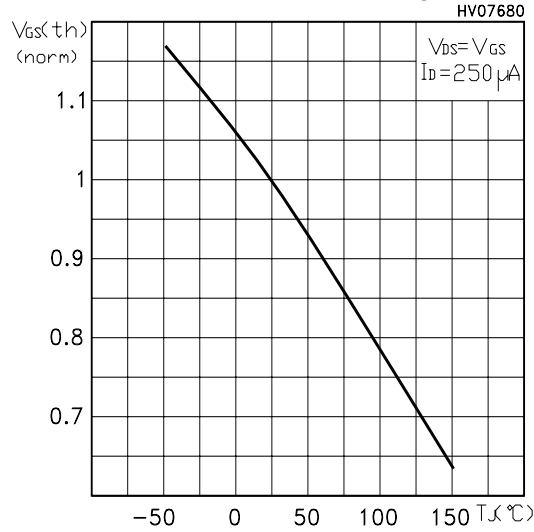
Gate Charge vs Gate-source Voltage



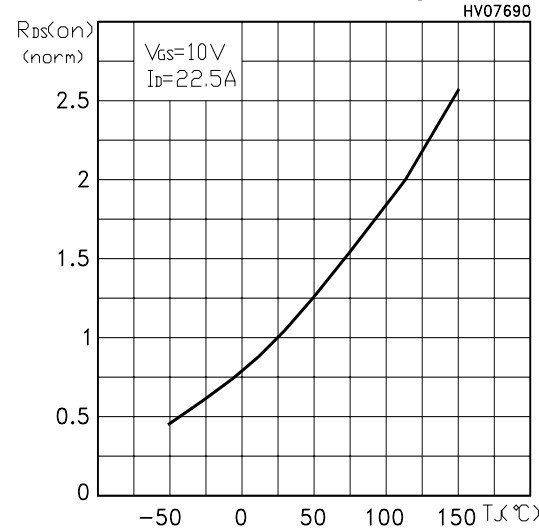
Capacitance Variations



Normalized Gate Thershold Voltage vs Temp.



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

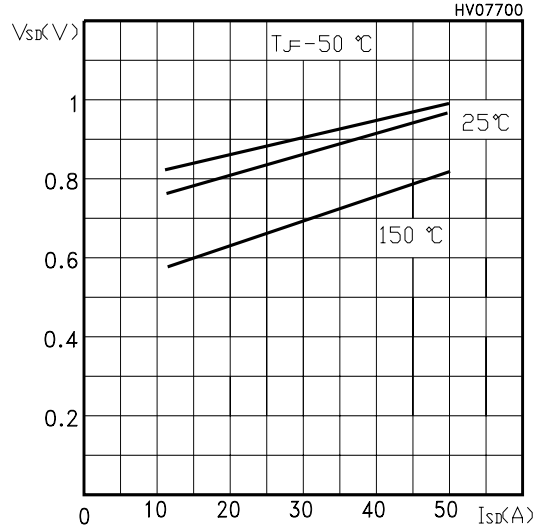


Fig. 1: Unclamped Inductive Load Test Circuit

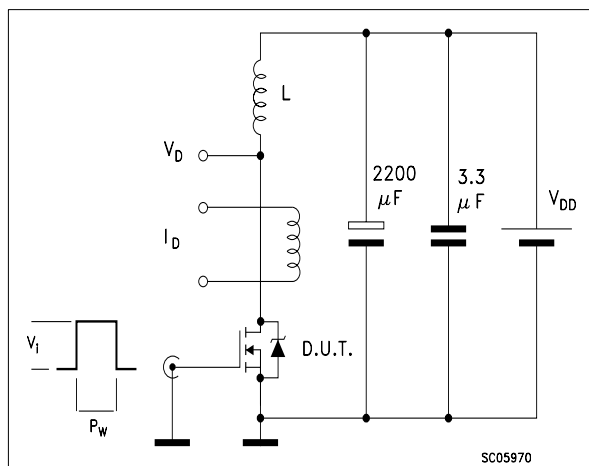


Fig. 2: Unclamped Inductive Waveform

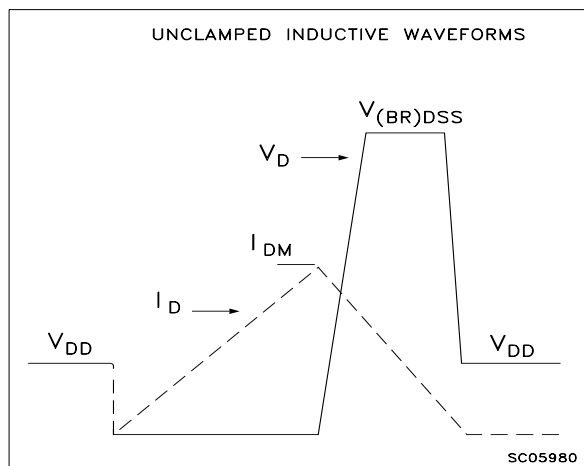


Fig. 3: Switching Times Test Circuit For Resistive Load

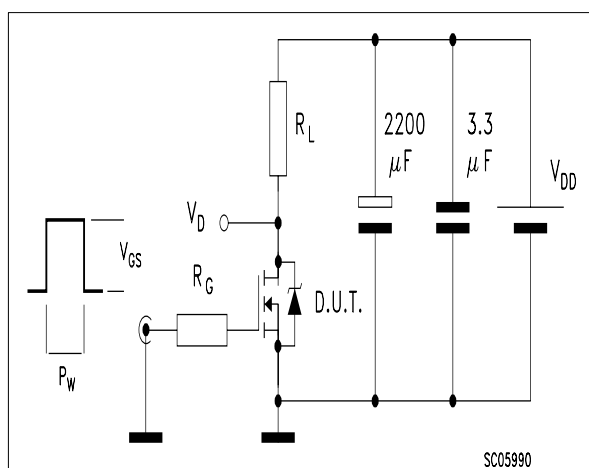


Fig. 4: Gate Charge test Circuit

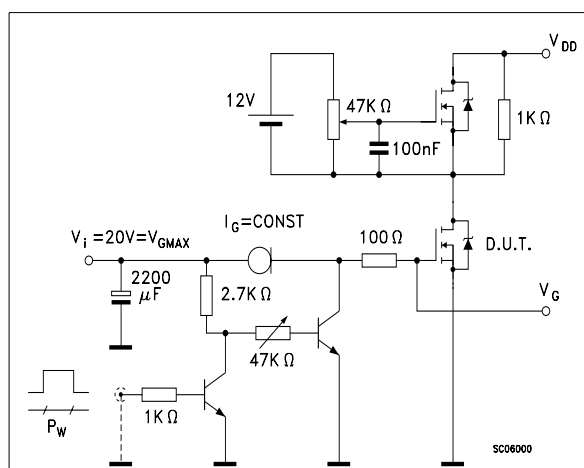
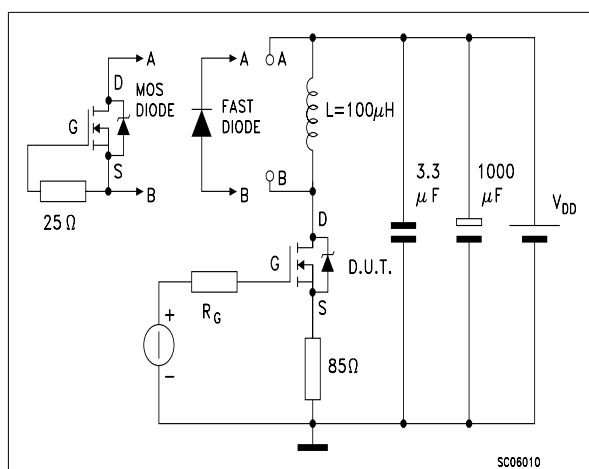
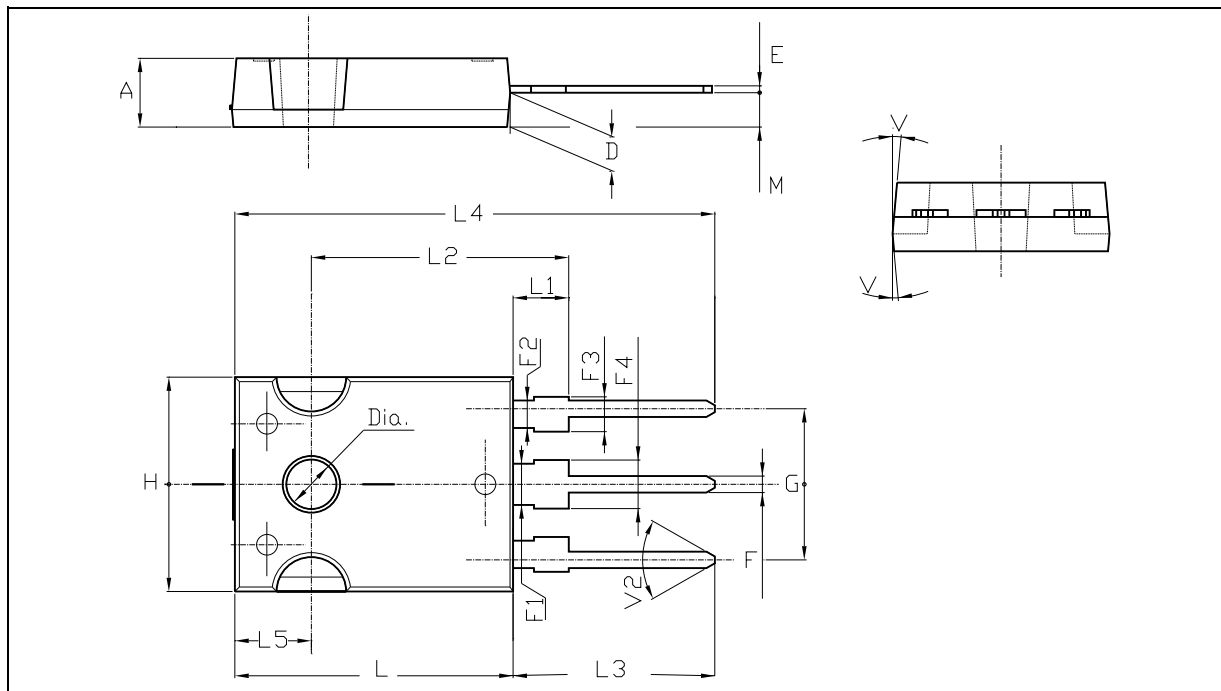


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-247 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.85		5.15	0.19		0.20
D	2.20		2.60	0.08		0.10
E	0.40		0.80	0.015		0.03
F	1		1.40	0.04		0.05
F1		3			0.11	
F2		2			0.07	
F3	2		2.40	0.07		0.09
F4	3		3.40	0.11		0.13
G		10.90			0.43	
H	15.45		15.75	0.60		0.62
L	19.85		20.15	0.78		0.79
L1	3.70		4.30	0.14		0.17
L2		18.50			0.72	
L3	14.20		14.80	0.56		0.58
L4		34.60			1.36	
L5		5.50			0.21	
M	2		3	0.07		0.11
V		5°			5°	
V2		60°			60°	
Dia	3.55		3.65	0.14		0.143



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