SGS-THOMSON MICROELECTRONICS

STV1602A

SERIAL INTERFACE TRANSMISSION DECODER

BUILT-IN AUTOMATIC EQUALIZER FOR UP TO 30dB ATTENUATION AT 135MHz (TYPICALLY 300m OF HIGH-GRADE COAXIAL CABLE), PLL CIRCUIT FOR RECLOCKING, AND SERIAL-PARALLEL CONVERSION CIRCUIT.
THIS SERIAL TRANSMISSION DECODER REQUIRES ONLY FEW EXTERNAL COMPONENTS.

OTHER RELATED IC's INCLUDE :

- STV1601A, A SERIAL TRANSMISSION ENCODER (PARALLEL-TO-SERIAL CONVERSION)
- STV1389AQ COAXIAL CABLE DRIVER

STRUCTURE

- Hybrid IC

APPLICATIONS

SERIAL DATA TRANSMISSION DECODER

- 100 to 270 Mb/s

APPLICATIONS EXAMPLES

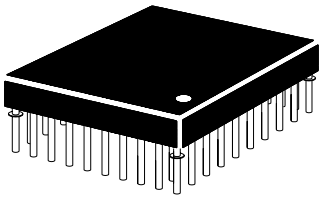
- Serial data transmission of digital television signals 525-625 lines
- 4:2:2 component 270Mb/s (10-bit)
- 4*fsc PAL composite 177Mb/s (10-bit)
- 4*fsc NTSC Composite 143Mb/s (10-bit)

FUNCTIONS

- Cable equalizer (maximum gain : 30dB at 135MHz)
- PLL for serial clock generation
- Reclocked repeater output (active loop through)
- Descrambler : modulo-2 multiplication by $G(x) = (x^9 + x^4 + 1)(x + 1)$
- Parallel-to-serial conversion
- Sync monitor output
- Eye pattern monitoring
- Input signal detector

DESCRIPTION

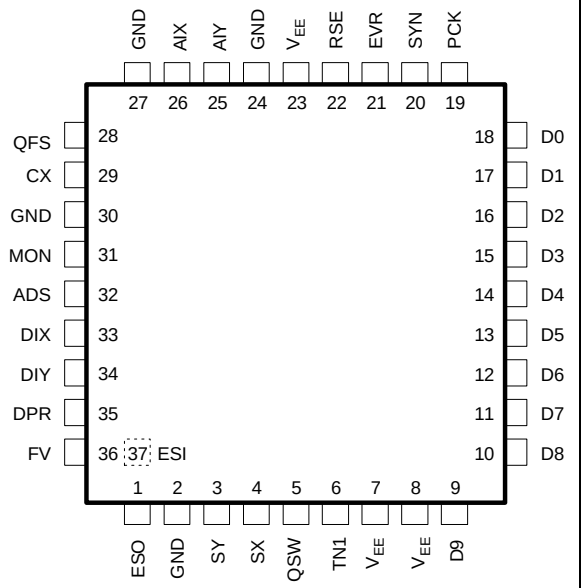
The STV1602A is a Hybrid IC decoder which converts serial data coming from a serial transmission line into parallel data.



PGA37
(Ceramic Package)

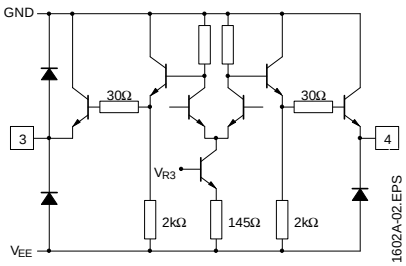
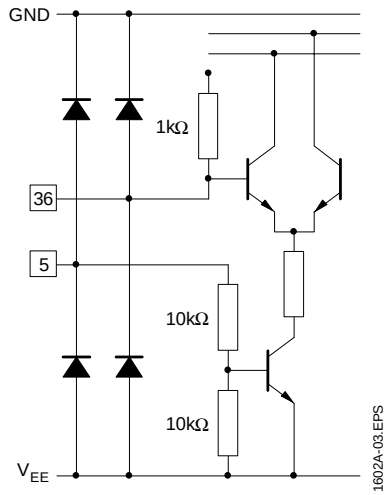
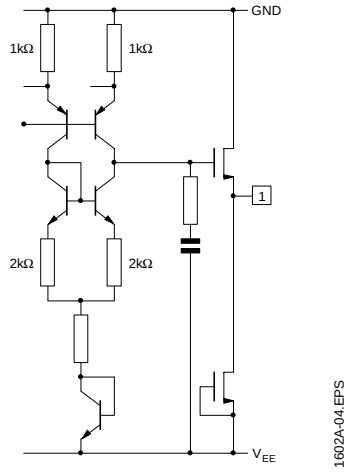
ORDER CODE : STV1602A

PIN CONNECTIONS



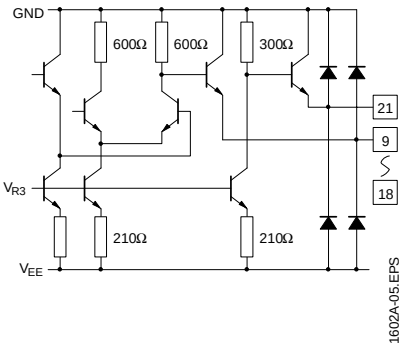
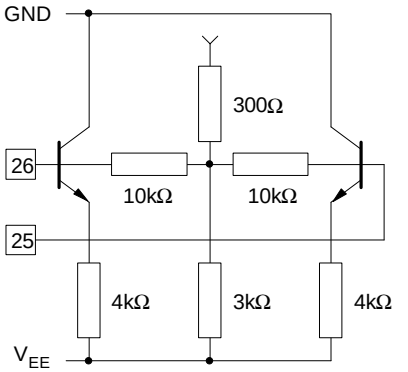
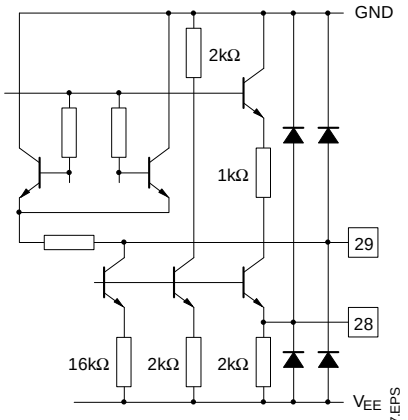
1601A-01.EPS

PIN DESCRIPTION

Pin N°	Symbol	Equivalent Circuit	Description	I/O	Standard			
					Min.	Typ.	Max.	Unit
3	SY		Reclocked serial data output in differential mode. SX and SY are disabled when TN1 is set High. In this case, SX is set High and SY is set Low H L	O		 -1.6 -2.4		 V V
4	SX							
5	QSW (GND)		To be connected to GND	I				
36	FV		Adjustment of VCO Free running frequency : V_{EE} level gives the lowest frequency. To adjust it, set TN1 High.	I				
1	ESO		Output of phase comparator : must be connected to ESI with the shortest distance	O		-3.2		V

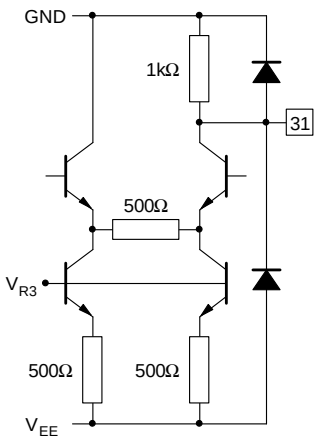
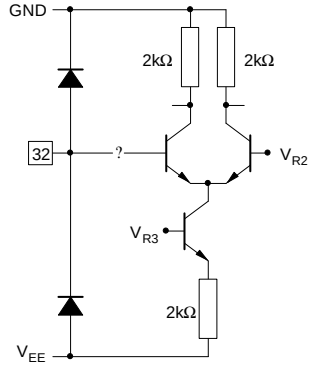
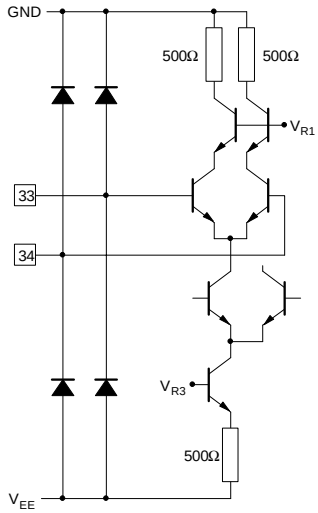
1602A-01.TBL

PIN DESCRIPTION (continued)

Pin N°	Symbol	Equivalent Circuit	Description	I/O	Standard			
					Min.	Typ.	Max.	Unit
9 to 18	D9 to D0		Parallel data output H L	O		 -0.8 -1.6		 V V
19	PCK		Parallel clock output (rising edge at data center) H L	O		 -0.8 -1.6		 V V
21	EVR		Data output reference potential	O		-1.2		V
26	AIX		Equalizer differential input	I		-2.0		V
25	AIY							
28	NC		To be left open	I		-4.6		V
29	CX		Equalizer detector output; Input signal : absent present	O		 -2.4 -2.0		 V V

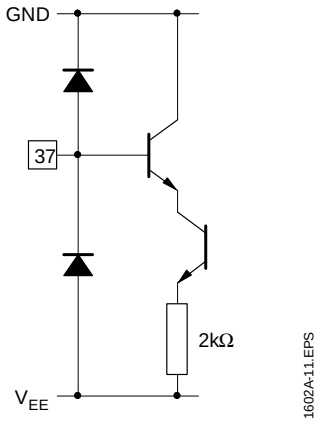
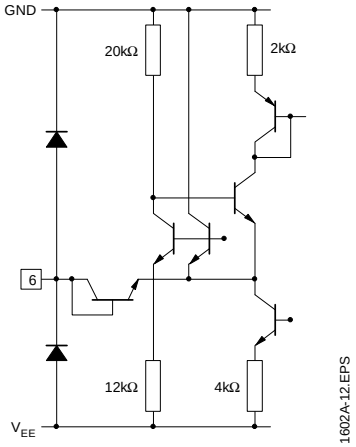
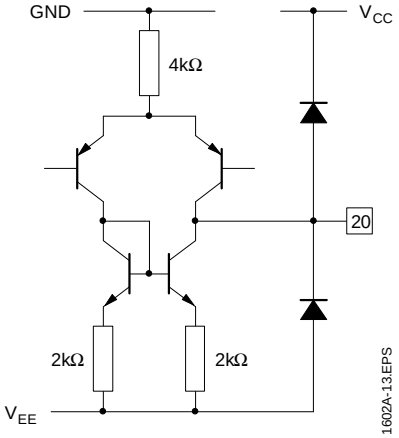
1602A-02.TBL

PIN DESCRIPTION (continued)

Pin N°	Symbol	Equivalent Circuit	Description	I/O	Standard			
					Min.	Typ.	Max.	Unit
31	MON		Equalizer monitor output. Connect 75Ω resistor between MON-GND. Observe using a 50Ω input oscilloscope at the 75Ω coaxial cable.	O		15		mV (pp)
32	ADS		Serial data input selection High : Digital input DIX/DIY Low : Equalizer input AIX/AIY H L	I	 -0.5		 -5	 V V
33	DIX		Serial data digital differential input	I				
34	DIY		Selected when ADS is High. H L		-1.0		-1.6	V V

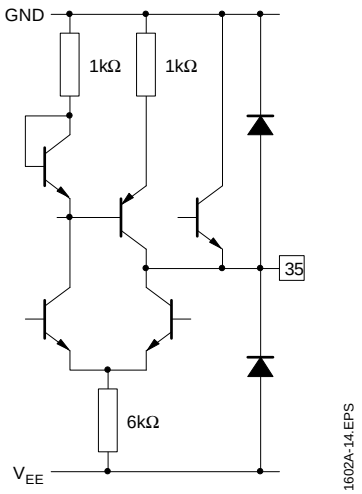
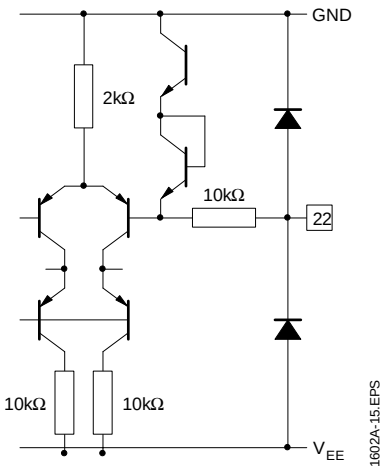
1602A-03.TBL

PIN DESCRIPTION (continued)

Pin N°	Symbol	Equivalent Circuit	Description	I/O	Standard			
					Min.	Typ.	Max.	Unit
37	ESI		PLL error signal input : must be connected to ESO with the shortest distance	i		-3.2		V
6	TN1		Serial data input activation High : Input disabled (VCO free running condition). Low : Input enabled. During switch-on phase, by temporarily hold High for quick start-up	I	-1.0		-4.0	V V
20	SYN		State changes at each TRS Sync word 3FFH 000H 000H H L	O	-1.0		-4.0	V V

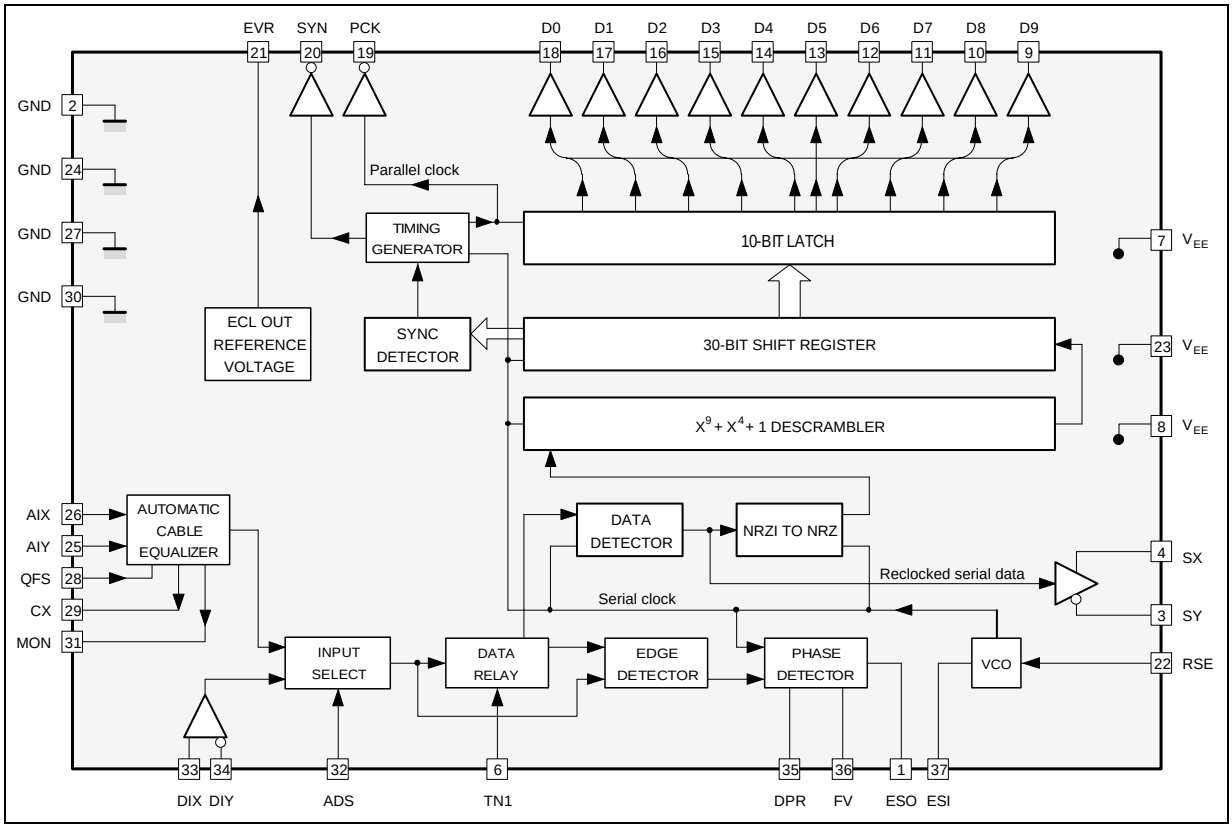
1602A-04.TBL

PIN DESCRIPTION (continued)

Pin N°	Symbol	Equivalent Circuit	Description	I/O	Standard			
					Min.	Typ.	Max.	Unit
35	DPR		Serial data detection output. When there is an input signal at the input side selected through ADS, this pin goes High. At no signal, it goes Low. H L i.e. - present : High - absent : Low	O	 -1.0		 -4.0	 V V
22	RSE		Selects VCO frequency range H : High range 140 to 270MHz L : Low range 100 to 145MHz H L	I	 -0.4		 -4.0	 V V
7 23	V_{EE}		-5V supply I/O buffer, PLL equalizer		-5.2	-5.0	-4.8	V
8	V_{EE}		-5V Supply Logic part		-5.2	-5.0	-4.8	V
2 24 27 30	GND		GND					

1602A-05.TBL

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Symbol	Parameter	Value	Unit
V_{EE}	Supply Voltage	-6	V
V_{IN}	Input Voltage	V_{EE} to 0	V
I_{OUT}	Output Current	-30	mA
T_{oper}	Operating Temperature	0 to 65	°C
T_{stg}	Storage Temperature	-50 to 125	°C
P_D	Allowable Power Dissipation	2.0	W

1602A-06.TBL

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{EE}	Supply Voltage	-4.8 to -5.2	V
T_{oper}	Operating Temperature	0 To 65	°C

1602A-07.TBL

ELECTRICAL CHARACTERISTICS (V_{EE} = -5V, T_A = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Test Circuit	Min.	TYp.	Max.	Unit
DC CHARACTERISTICS							
I_{EE}	Supply Current	V_{EE} = 5V	Figure 4		185		mA
V_{IH}	Input Voltage	Pin ADS		-0.4			V
V_{IL}						-1.5	V
V_{IH}		Pin RSE	Figure 10	-0.4			V
V_{IL}						-4.0	V
V_{IH}		Pin DIX, DIY		-1.0			V
V_{IL}						-1.6	V
I_{IH}	Input Current	Pin DIX, DIY	Figure 5			5.0	µA
I_{IL}				-1.0		+1.0	µA
V_{IH}	Input Voltage	Pin TN1	Figure 9	-1.0			V
V_{IL}						-4.6	V
V_{OH}	Output Voltage	Pin PCX, Dn R_P = 1kΩ			-0.8		V
V_{OL}					-1.6		V
V_M		Pin EVR, R_P = 1kΩ			-1.2		V
V_{OH}		Pin DPR, SYN I_{OH} = -10µA, I_{OL} = +10µA	Figure 7	-1.0			V
V_{OL}			Figure 8			-4.0	V
V_{OH}		Pin SX, SY R_P = 220Ω			-1.6		V
V_{OL}					-2.4		V
AC CHARACTERISTICS							
f_{MAX1}	VCO Max. Oscillation Frequency 1	RSE = "H"	Figure 6	30.0			MHz
f_{MIN1}	VCO Min. Oscillation Frequency 1	RSE = "H"				14.0	MHz
f_{MAX2}	VCO Max. Oscillation Frequency 2	RSE = "L"		15.0			MHz
f_{MIN2}	VCO Min. Oscillation Frequency 2	RSE = "L"				10.0	MHz
f_{HP1}	PLL Pull in Range	f signal = 270MHz RSE = "H"	Figure 3	27.7			MHz
f_{LP1}						25.5	MHz
f_{HP2}		f signal = 177MHz RSE = "H"		18.5			MHz
f_{LP2}						16.8	MHz
f_{HP3}		f signal = 143MHz RSE = "H"		15.0			MHz
f_{LP3}						13.3	MHz
f_{OP1}	PLL Generator Frequency	RSE = "H"		14.0		27.0	MHz
f_{OP2}		RSE = "L"		10.0		14.5	MHz

1602A-08.TBL

Frequency at 1/10 the value of signal frequency (Tested through Pin PCK)

SWITCHING CHARACTERISTICS (V_{EE} = -5V, T_A = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Test Circuit	Min.	Typ.	Max.	Unit
t_r	Rise Time	Pins PCK, Dn R_P = 1kΩ	Figure 3		0.8		nsec
t_f	Fall Time				1.4		nsec
t_r	Rise Time	Pins SX, SY R_P = 220Ω			0.7		nsec
t_f	Fall Time				0.7		nsec
t_d	Delay Time	Pins PCK, Dn		-3		+3	nsec

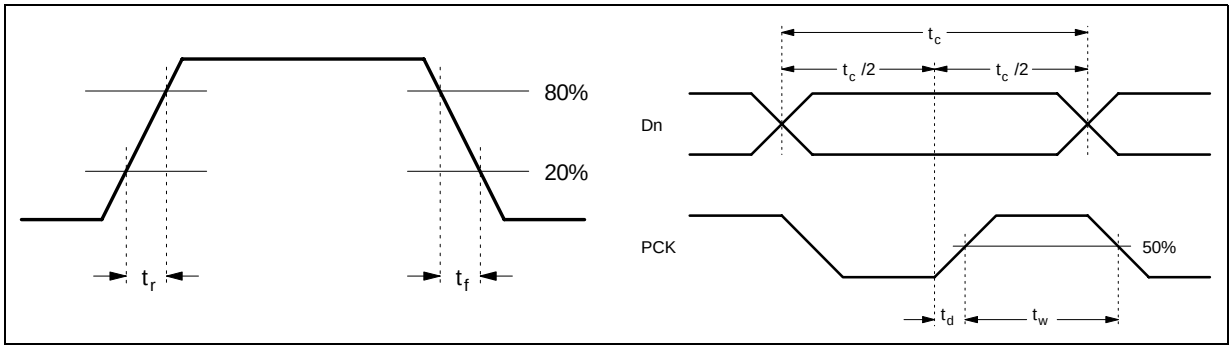
1602A-09.TBL

EQUALIZER (V_{EE} = -5V, T_A = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Test Circuit	Min.	Typ.	Max.	Unit
V_{MAX}	Equalizer Max. Input Voltage	Pins AIX, AIY	Figure 3	0.88			Vp-p
G_{MAX}	Equalizer Max. Gain				30		dB
C_{IN}	Input Capacity	Pins AIX, freq = 100MHz					pF
R_{IN}	Input Resistance	Pins AIX, freq = 100MHz					Ω

1602A-10.TBL

Figure 1 : t_r, t_f, t_c, t_d Definition



1602A-17.EPS / 1602A-18.EPS

SYN pin guaranteed operation range.

SYNC pin and serial to parallel conversion operate normally within the frequency and ambient temperature ranges according to the following considerations.

Reclocked output.

STV1602A may be used as a repeater. The reclocked output, providing characteristics almost identical to the serial output of STV1601A is available from SX (Pin 4) and SY (Pin 3).

When the reclocked output is used, it is recommended not to use simultaneously use the parallel outputs (data and clock) in order to avoid possible logic errors caused by an excessively high temperature which may result from additional power dissipation created by the reclocked output circuit under certain environnmental conditions.

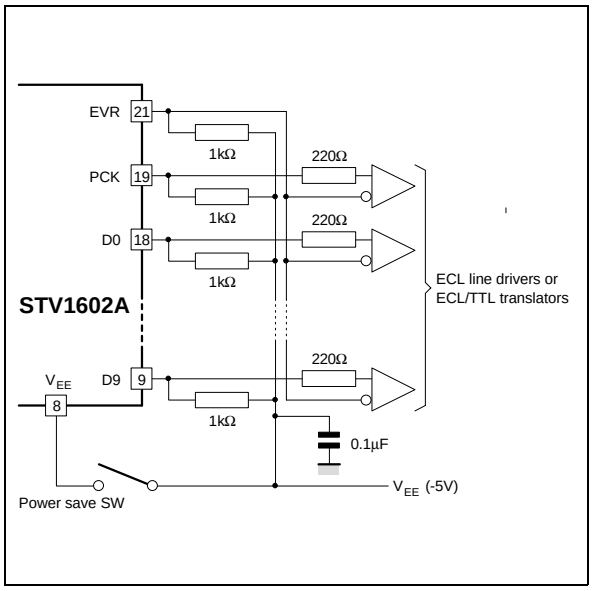
If, for the sake of a design convenience, both reclocked and parallel outputs are to be used, the ambient temperature has to be kept as low as possible or, at least, the airflow around STV1602A must be carefully considered. In addition, it is recommended to put 220Ω resistors on all parallel outputs including the clock as shown in Figure 2. This reduces the magnitude of the spike current resulting from the parallel output circuit inside the chip and helps reduce the probability of logic errors at high temperature.

Power saving in repeater mode

Since the parallell output is not always required for a reclocked repeater, the chip has been designed such that the uncessary parallel logic circuit can be disabled by disconnecting Pin 8, one of V_{EE}s, from the power supply. With this arrangement the power dissipation is reducible to about 45 percent of that of the fully functional mode.

In practice, a test switch should be provided so that some parallel signals may be available during adjustment procedures as shown in Figure 2.

Figure 2 : A Suggested Parallel Clock / Data Output Circuit



1602A-19.EPS

Figure 3 : Test Circuit Diagram Example

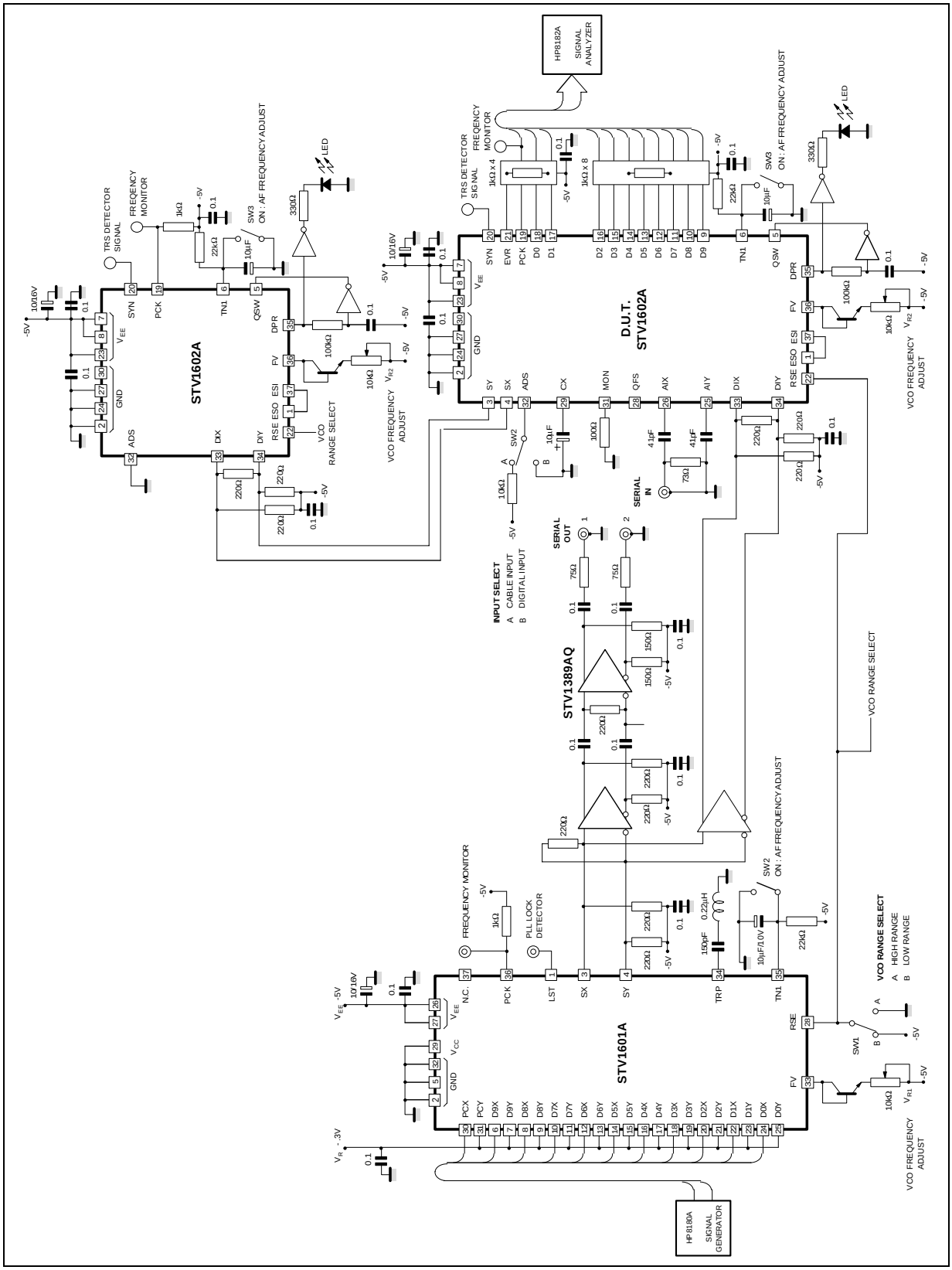


Figure 4

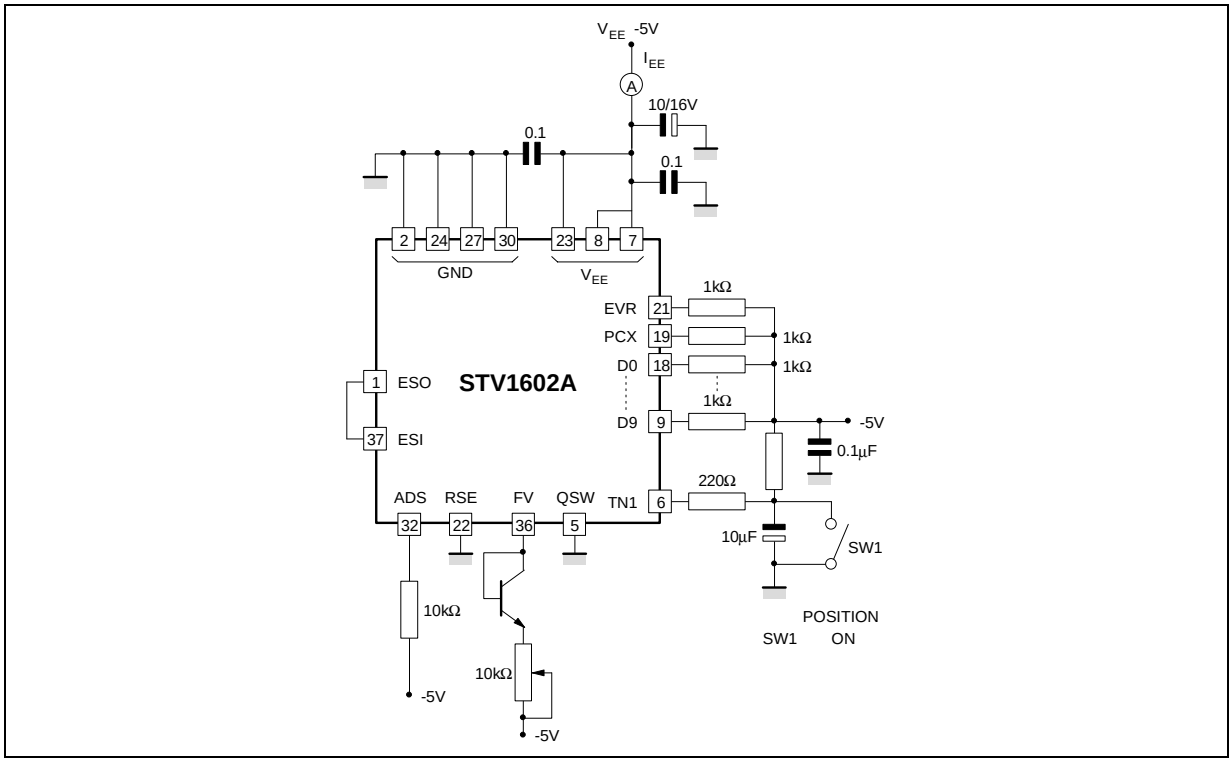


Figure 5

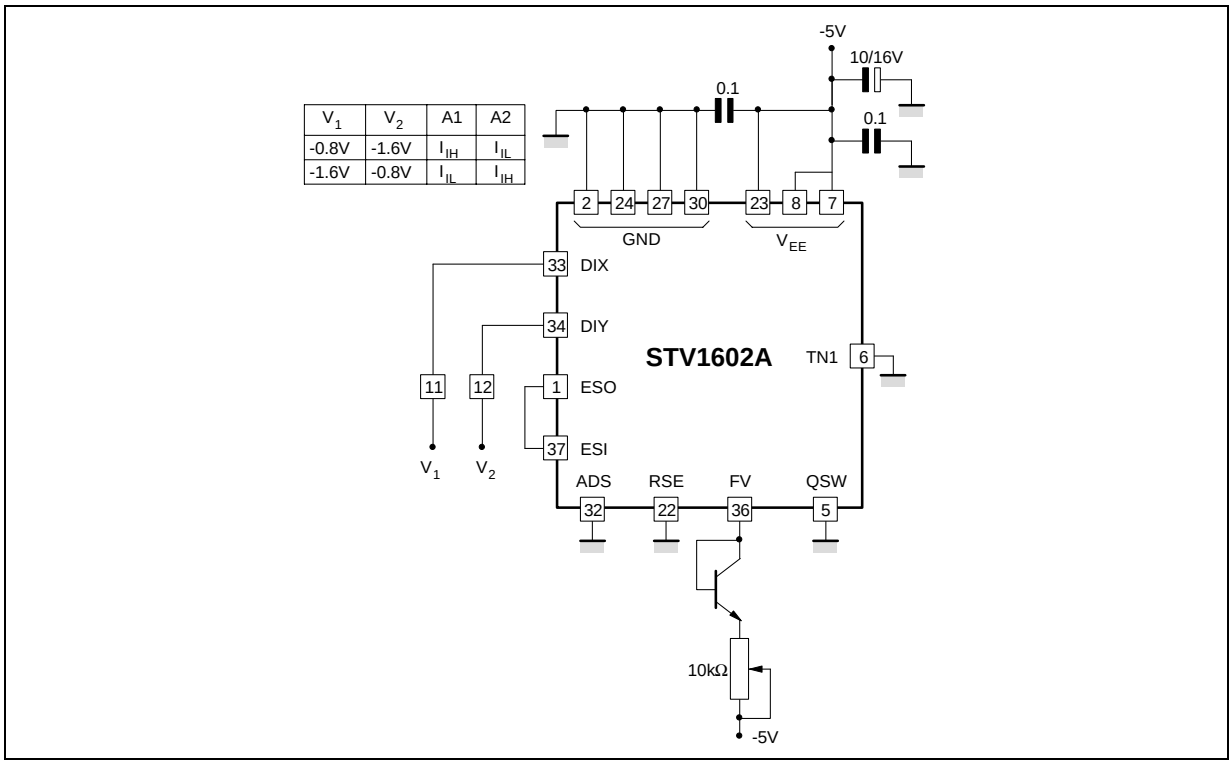


Figure 6

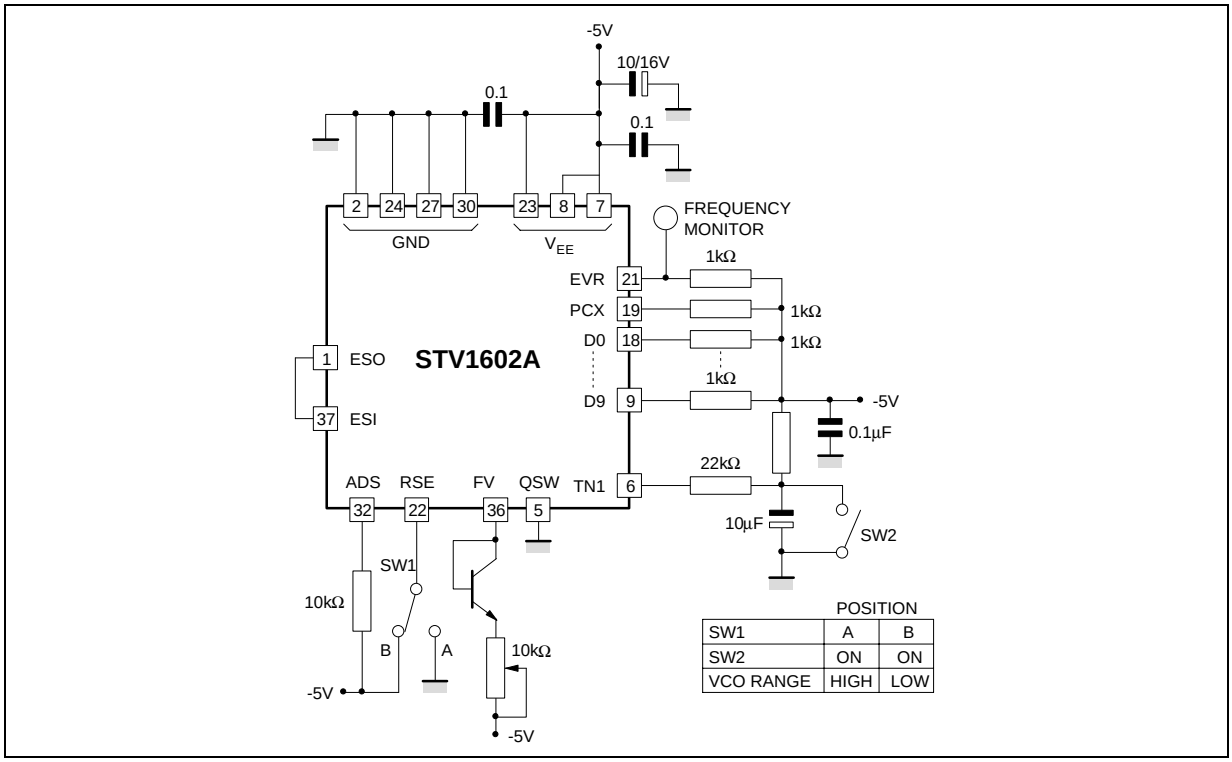


Figure 7

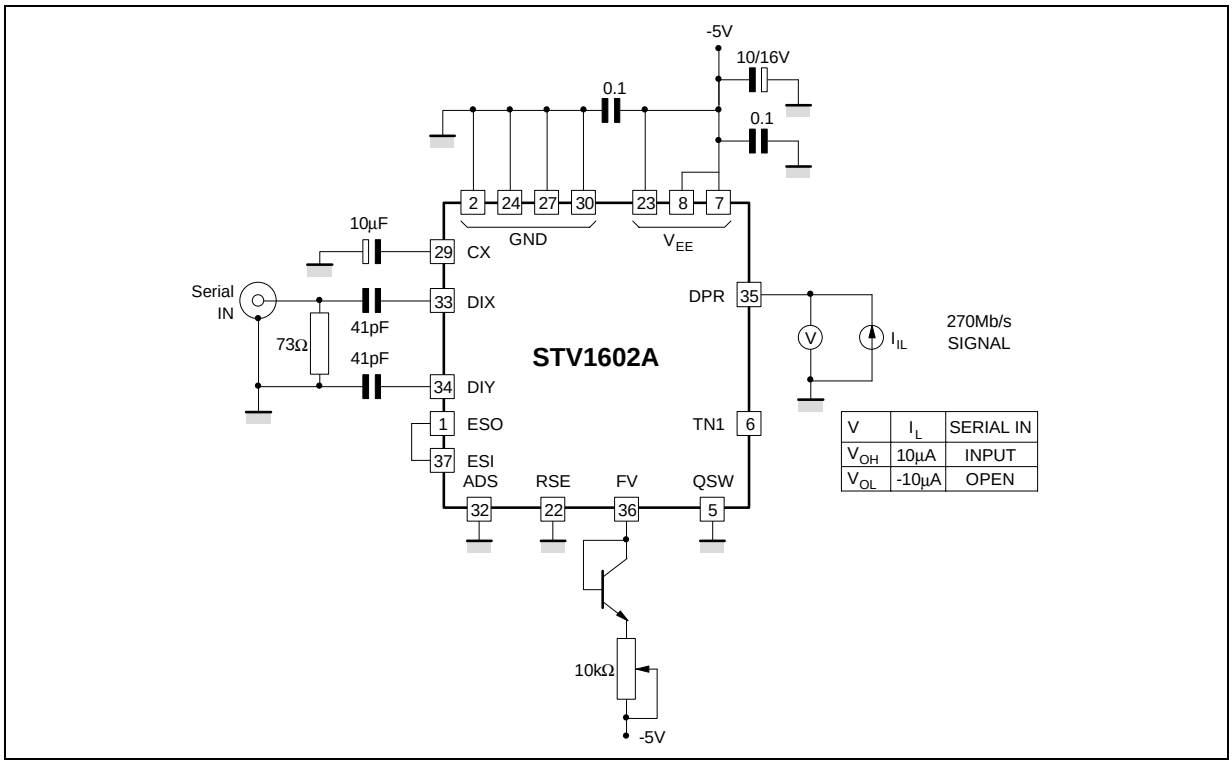


Figure 8

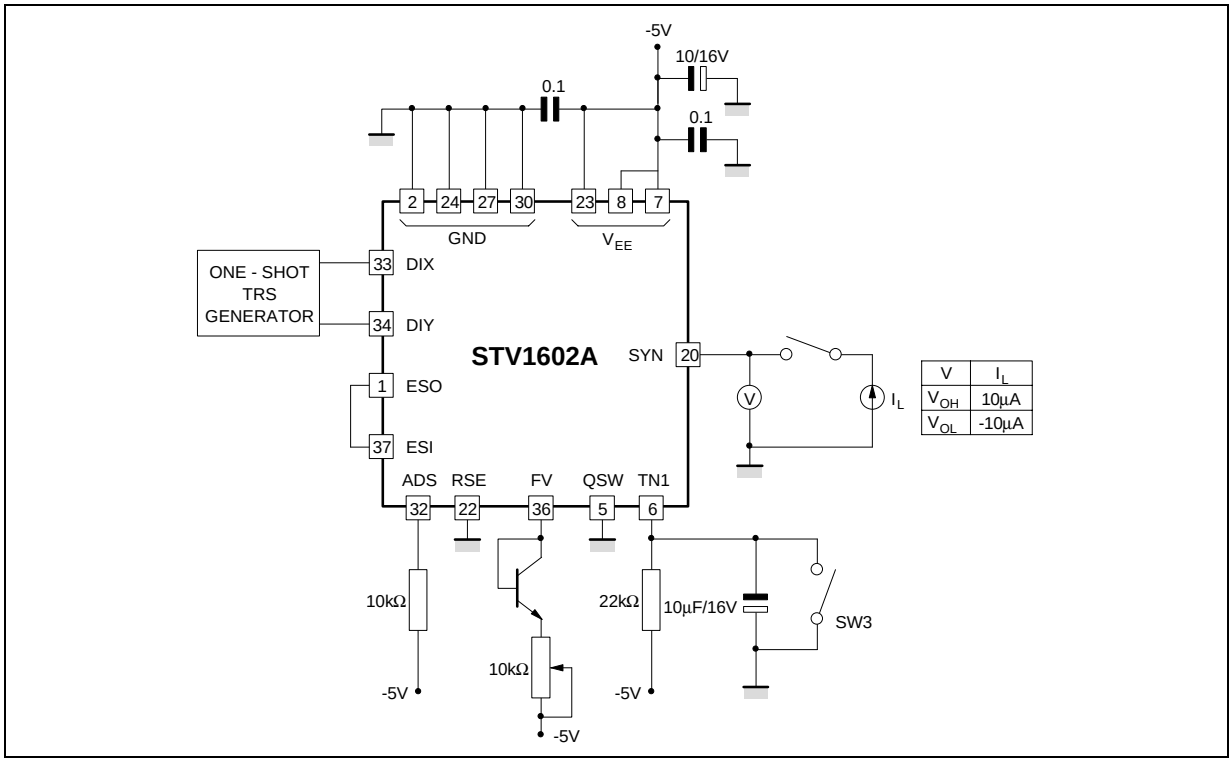


Figure 9

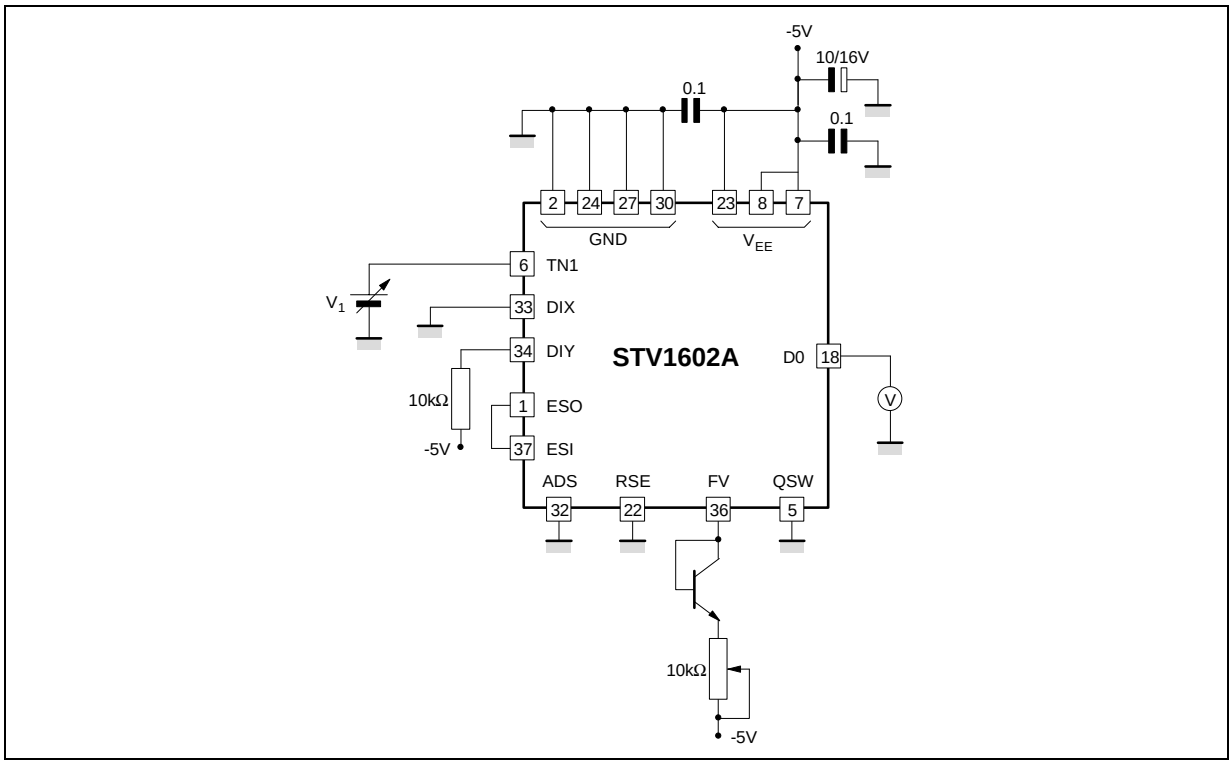
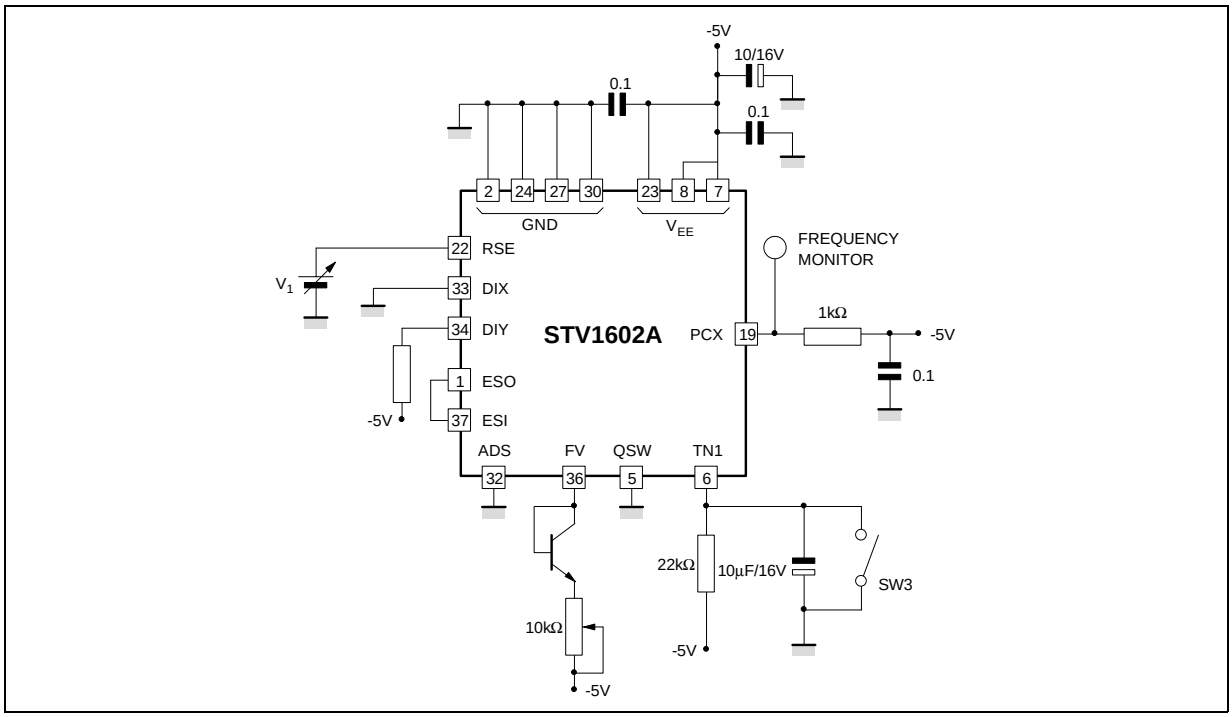


Figure 10



STV1602A GENERAL

As shown in the overall block diagram on page 7, STV1602A is composed of the following functions :

(1) Analog input as a primary input with automatic equalizer to meet the loss characteristics of coaxial cable
(2) Digital input as a secondary input to receive the encoded signal from short distances within the same printed circuit board or the same equipment
(3) Phase locked loop (PLL) variable oscillator
(4) Reclocked serial output
(5) Serial descrambler
(6) SYNC detector
(7) Deserializer
(8) Parallel output buffer amplifiers
(9) Three diagnostic signals : eye monitor, SYNC monitor and input data presence monitor

A brief explanation of each function is given in the following sections.

1. Cable equalizer

Transmission of high speed digital data by means of coaxial cable can greatly attenuate high frequency components. According to the cable length, received signals can widely differ from those sent; in such conditions, clock extraction and data identification could be difficult.

The cable equalizer overcomes this problem.

The IC performs up to 30dB (typical) equalization at 135MHz, typically 300m of high-grade coaxial cable. The equalization is automatically performed according to the coaxial cable length.

The input signal can be delivered either through a transformer or through a capacitor.

When the digital input is selected, the equalizer is disabled. Typical characteristics of the equalization are given in Figure 31.

Figure 11 : Equalizer Capacitor Coupling Input Circuit

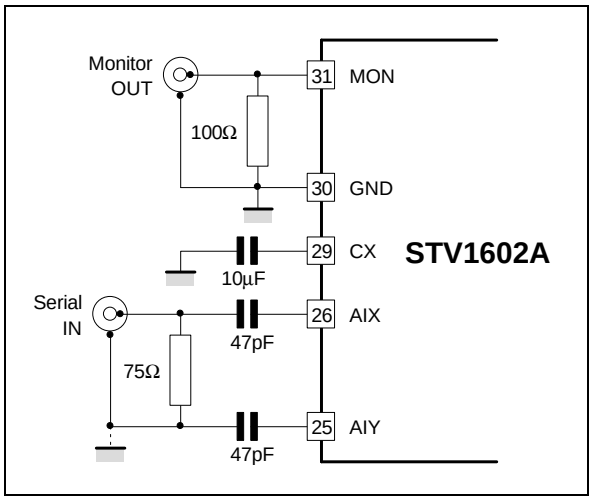
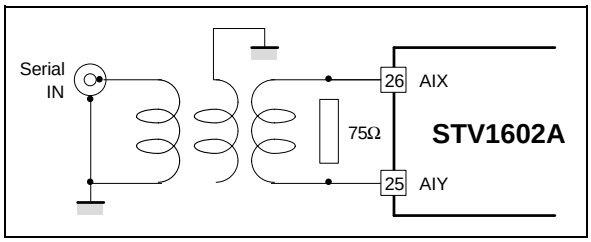
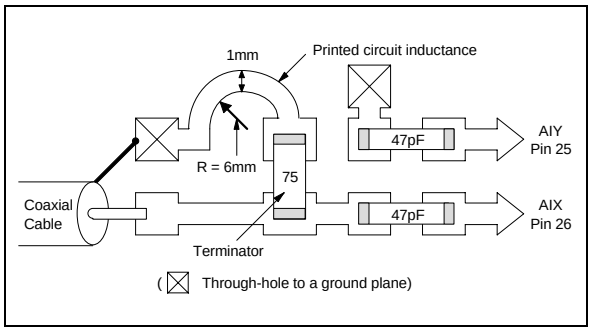


Figure 12 : Equalizer Transformer Input Circuit



In both input circuit configurations, a consideration is required in a practical design to obtain a sufficient return-loss (at least 15dB over a frequency range of 5MHz to the bit rate frequency used). To achieve this, it is effective to add a small inductance in series with the 75Ω termination resistor. Figure 13 shows an implementation example.

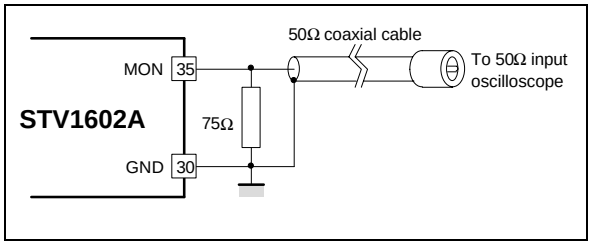
Figure 13 : An example of technique to improve the return-loss figure for the capacitor coupling input case



MON Pin (31)

Equalized signals can be observed at this pin by connecting an oscilloscope input (50Ω).

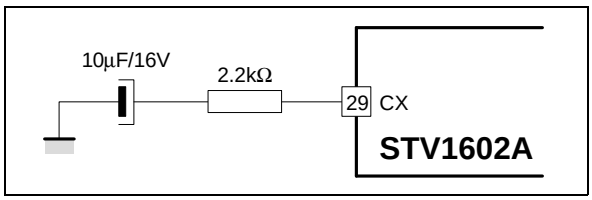
Figure 14 : Equalized Waveforms Monitoring



CX Pin (29) Equalizer AGC time constant

Connect a 10µF capacitor in serial with 2.2kΩ resistor between this pin and GND in order to obtain stable operation at all times. According to input signals, voltage changes from -2V to -2.4V can occur.

Figure 15 : AGC Time Constant



2. Digital input

The serial data input can be used without the equalizer.

DIX (Pin 33) and DIY (Pin 34) are differential inputs for ECL signals.

From these pins, input signals are differentially amplified, therefore with no input signals, the data detection signals could go High and erroneous data would be transferred to the parallel output.

To avoid this, a voltage level conforming to ECL specifications must be applied between DIX and DIY pins.

Also, while the analog input is in use, digital input must be kept "quiet" in order to avoid possible errors caused by cross-talk. This cross-talk problem naturally gets most severe when the analog input cable length is close to the limit of the transmission capability.

3. Serial input selection

Selection of the serial input is performed by ADS (Pin 32); when High the digital input is enabled; this input can be used for very short transmission lines. When Low, the equalizer input is enabled; this input must be used for long transmission lines.

4. PLL

In order to extract clock signals from the equalized serial data, it is processed to generate edge signals which are sent to the phase comparator.

When the PLL is locked, the identifier clock (D - flipflop) will be in phase with the incoming clock. The identifier clock rises at the center of the data period for easy identification.

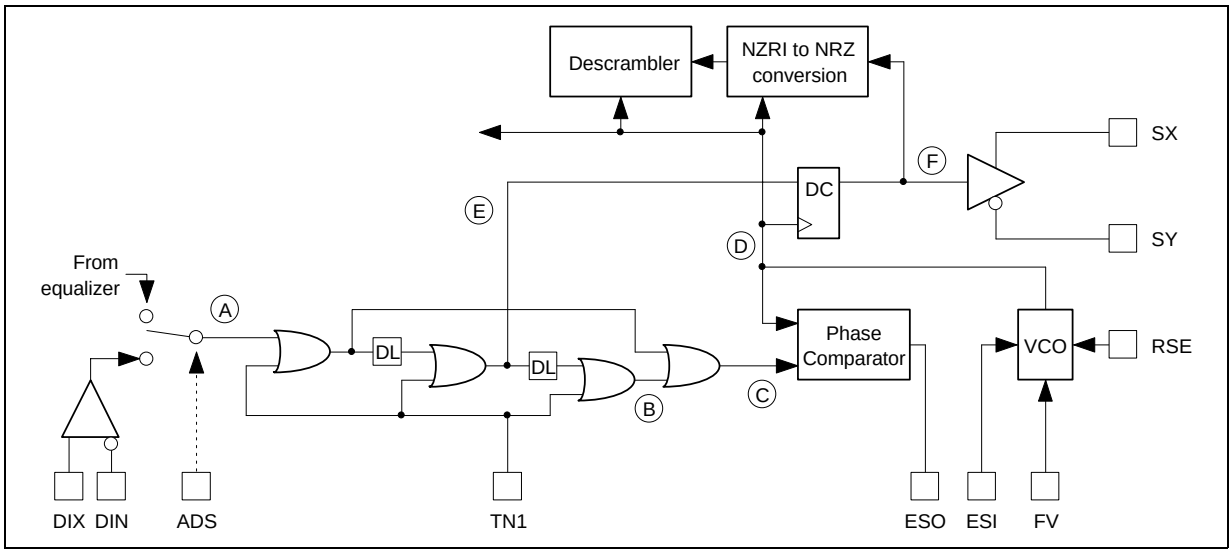
The PLL detailed block diagram is shown in Figure 16.

ESI is the VCO control input (Pin 37). Normally, the phase comparator output ESO (Pin 1) is connected to ESI.

Since the VCO employed has a very high sensitivity, those two nodes must be connected with a shortest distance and a minimum area of conductor

on the printed circuit board. Encircling those two nodes by a ground guarding is an efficient method to prevent errors caused by an "antenna effect".
Through FV (Pin 35) one can adjust the free running frequency; when the FV Voltage is equal to V_{EE}, the free running frequency is the lowest; the voltage adjustment can be performed by using a variable resistor connected between FV and VEE.
RSE (Pin 22) selects the VCO frequency range; High : 140 to 270MHz, Low : 100 to 145MHz.
When TN1 (Pin 6) is set High, input signals are disabled and the VCO free runs. The capacitor connected between TN1 and GND avoids mislocking problem when the power supply is switched on.

Figure 16 : Serial Data Input and PLL



Data detection

Serial data edges are detected and go through low pass filter. The processed signal is available at DPR (Pin 35).DPR goes High when an input signal is detected, otherwise it stays Low.

The driving capability of this pin is weak. It is recommended to load it with a high impedance CMOS or equivalent.

5. NRZI To NRZ conversion, descrambler

Serial data delivered by the identifier is available in differential mode, SX (Pin 4) and SY (Pin 3). At the same time, to recover the original data, NRZI to NRZ conversion and descrambling are performed.

Figure 17 : NRZI to NRZ conversion

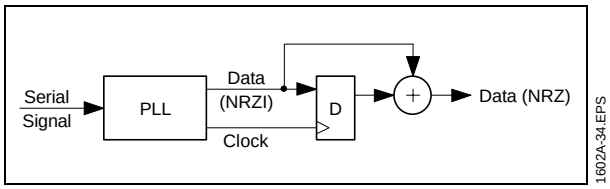


Figure 18 : $x^9 + x^4 + 1$ Descrambler

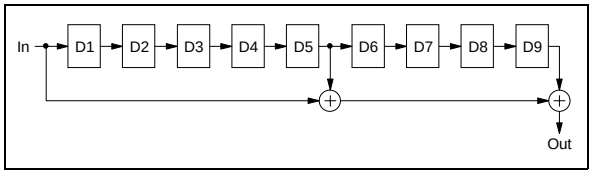
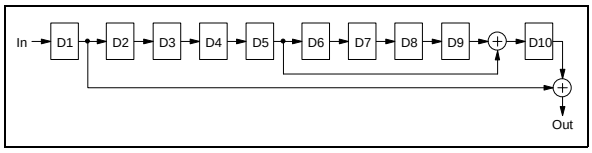


Figure 19 : Actual $x^9 + x^4 + 1$ Descrambler



6. Serial to parallel conversion

After descrambling, serial data is sent to a 30-bit register to detect the sync word (TRS). When the sequence 11111111110000000000000000000000 is detected, sync word detection signal is output, the counter which divides the clock frequency by 10 is initialized and data is converted to parallel (10-bit word) to be output.

Each time the sync word is detected, SYN (Pin 20) changes state as shown in Figure 20.

When a receiver using STV1602A is properly implemented and adjusted, the health of the implementation can be checked simply by looking at SYN (Pin 20) output while an encoded signal is present at the input.

SYN is an output of a flip-flop which toggles at each detection of TRS at the SYNC detector. Since the 4:2:2 signal contains two kinds of TRSs, SAV and EAV, when the output of SYN is observed by an oscilloscope it looks like either case A or case B as shown in Figure 20 depending upon the initial condition of the Flip-Flop.

When bit erros are occurring somewhere in the transmission path, SYN output is affected and looks like as shown in case C.

Figure 21 illustrates the case for 4 fsc (D2 NTSC and PAL).

Differing from the 4:2:2 case, SYN output has an equal mark and space ratio due to the periodic occurence (once per one TV line) of the TRS detection. However, transmission path bit errors will cause the SYN output to appear similar to the 4:2:2 case.

If SYN signal is used other than for monitoring purposes, buffering similar to that of DPR is required due to the high impedance nature of SYN output.

7. Phase relation ship between parallel data and parallel clock

Parallel data and clock are output so that the rising edge of the parallel clock is located at the center of the parallel data. Both parallel data and clock (nearly identical to that of single ECL) have DC levels depending on the temperature. In order to simplify the driving amplifier, a reference level (EVR) is available at Pin 21. PCX, Dn and EVR use pull down resistors (identical values). A peripheral circuit example is shown in Figure 23. Figure 24 shows a circuit to disable the parallel clock output.

Figure 20 : SYNC Output in 4:2:2 Case (not to scale)

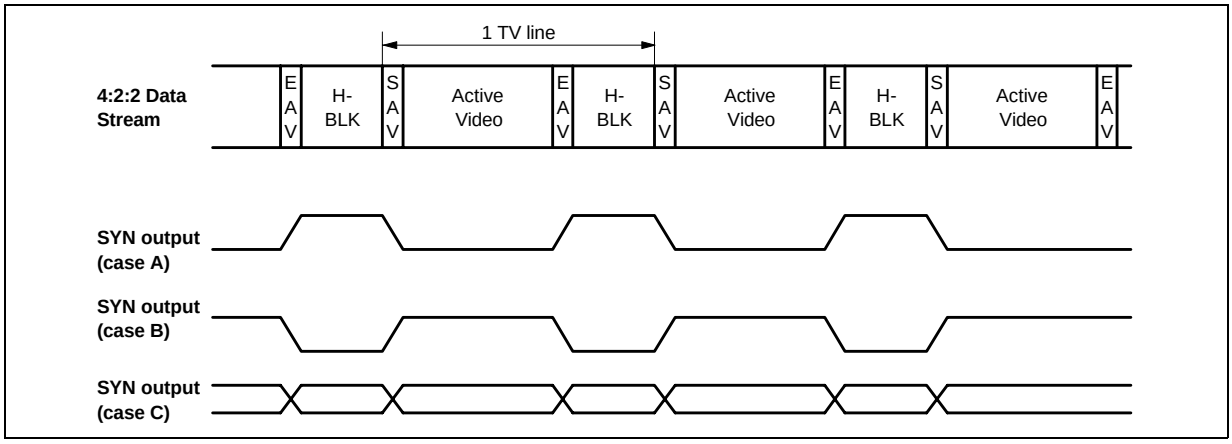


Figure 21 : SYNC Output in 4 fsc Case (not to scale)

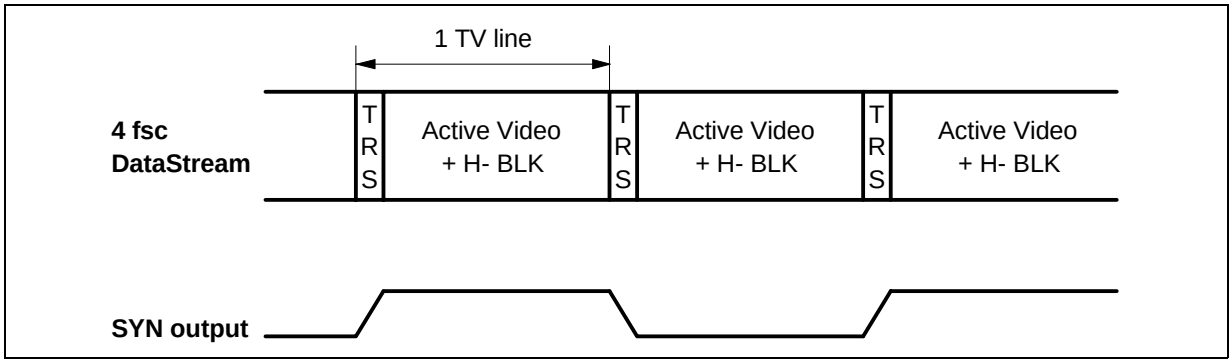


Figure 22 : Phase Relation of Parallel Clock, Data and EVR Voltage Level

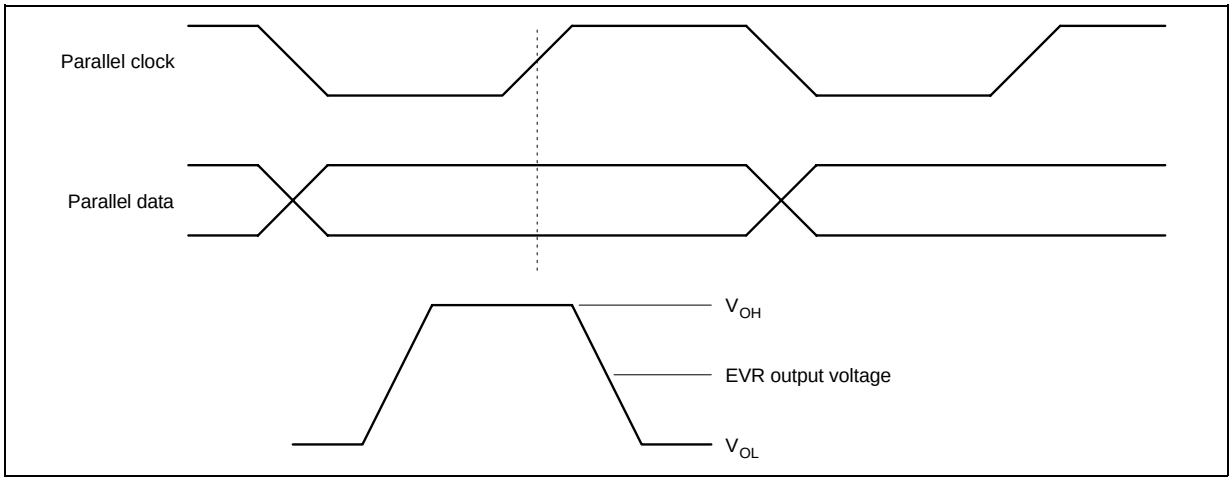


Figure 23 : Parallel Clock Data Output Circuit

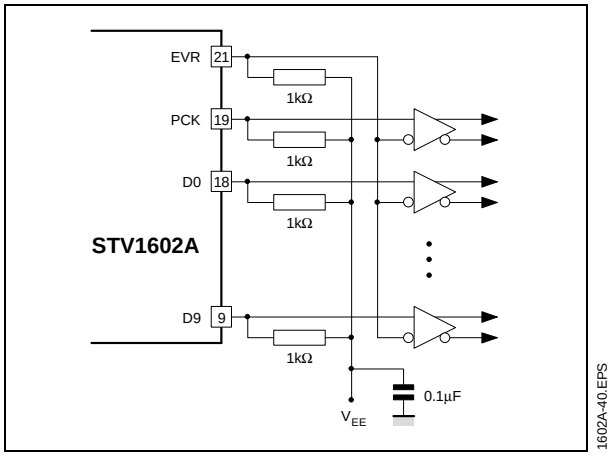
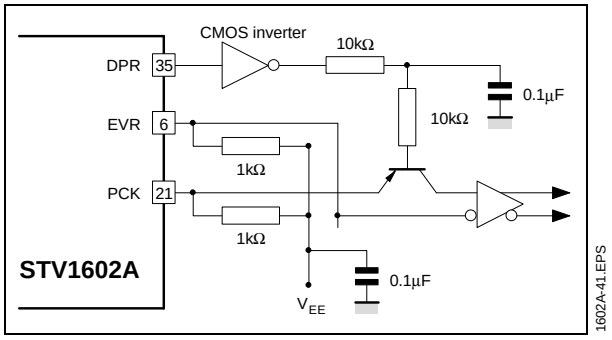


Figure 24 : A Circuit Example to Disable Parallel Clock



8. VCO temperature compensation and oscillation frequency adjustment.

VCO oscillation frequency depends on the temperature as shown in Figures 29 and 30 "Representative characteristics example". Within the normal range of operation, frequency increases with temperature.

FV pin voltage remains almost constant regardless of temperature.

Figure 25 shows an example of a temperature compensation circuit using a diode (transistor with C-B diode short-circuited) and a resistor between FV and V_{EE}.

PLL pull-in range (signal frequency 270, 177 and 143MHz) are given by Figures 32, 33 and 34.

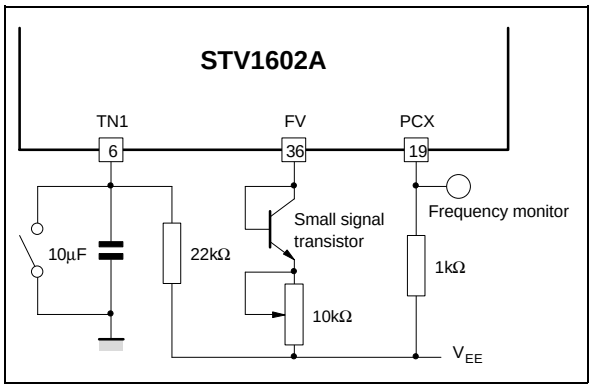
9. VCO free running frequency adjustment

VCO free running frequency adjustment is performed at room temperature.

If TN1 is set High, VCO is free running. Wait for 5 to 10 minutes after turning power supply ON (warm up time).

While monitoring PCK (Pin 19) output, adjust the signal frequency (within ±1%) with the variable resistor connected between FV and V_{EE}.

Figure 25 : VCO Temperature Compensation and Free Running Frequency Adjustment



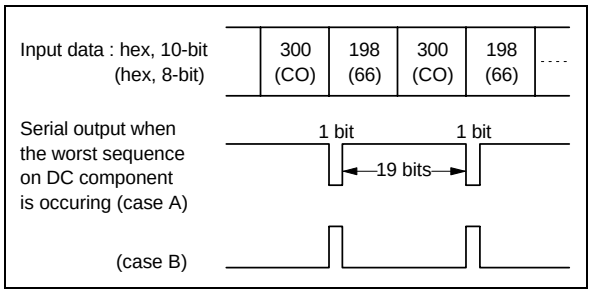
Using particular codes to check overall performance

Althrough the scrambling method employed effectively randomizes the incoming data and puts out a signal with a nearly uniform spectrum, there still exist some combinations of codes that give somewhat unfriendly conditions to the transmission path in terms of low frequency component or of a long run without any transitions.

As shown in Figure 26, it is known that if the code words 300, 198 (hex, 10-bit) are given alternately to the parallel input of the encoder, the largest amount of DC component (nearly one TV line period) can be produced at some place with a certain probability (such a sequence is, however, destroyed when different data is input to the encoder).

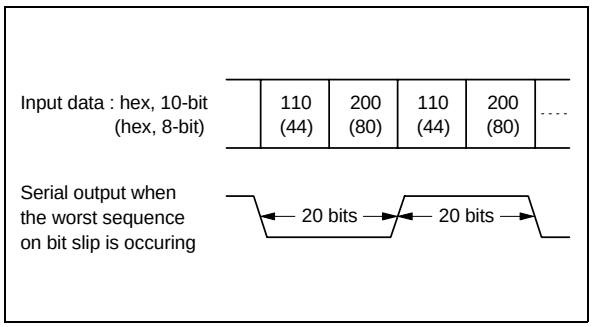
Even with such signals, error-free reception is possible with the STV1602A if a proper implementation is made (refer to section 12 for a recommended circuit).

Figure 26



Another particular combination of words, but with a different nature, is 200, 110 (hex, 10-bit) which can generate the sequence which is most vulnerable* to bit slip of nearly one TV line period. Figure 27 illustrates such a situation. Similar to the previous case, the worst sequence stops upon an arrival of a data other than the alternating 200, 110 at the input of the encoder.

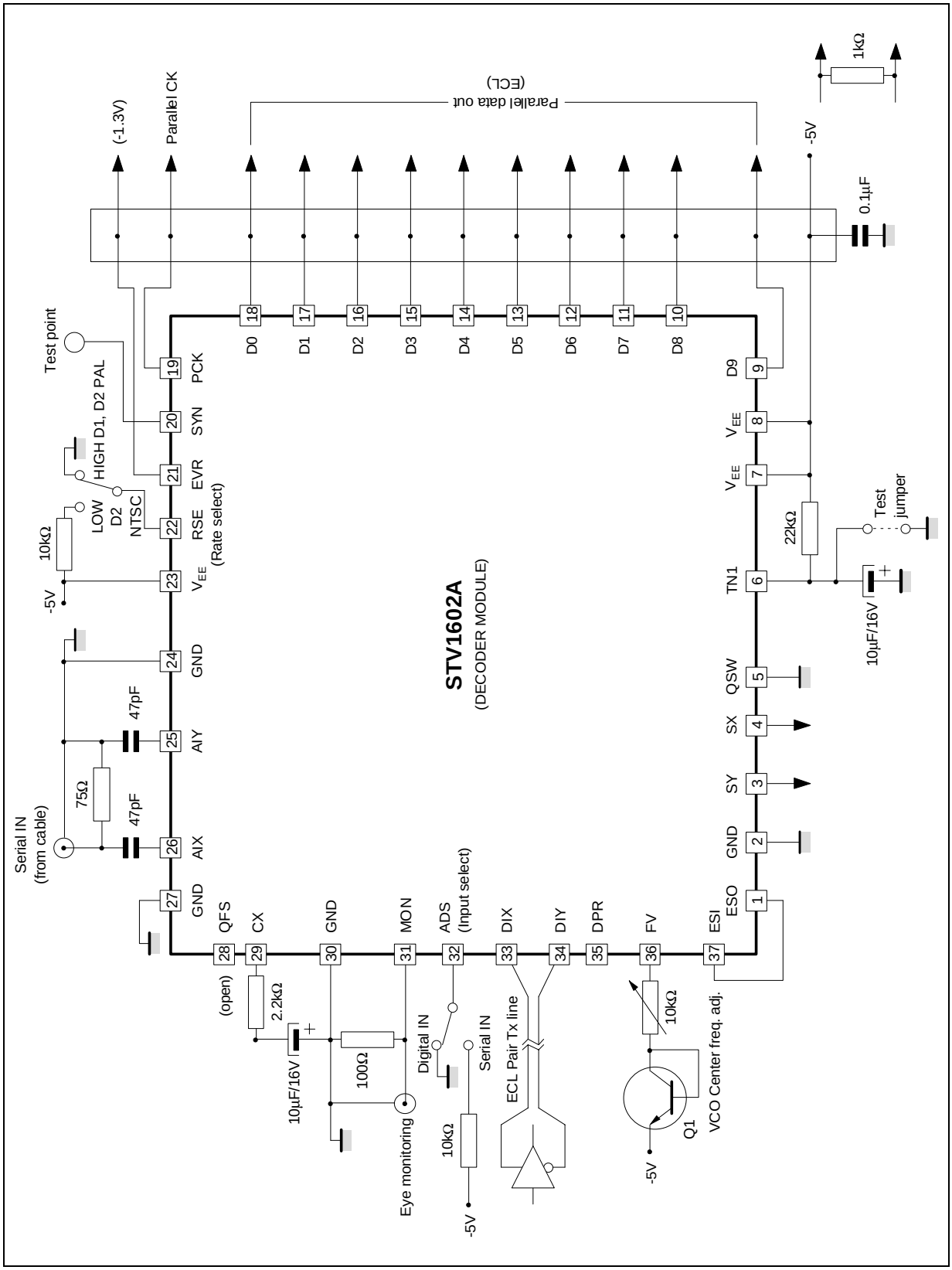
Figure 27 : Particular Data words for checking PLL bit slip



* Stricly speaking the longest isolated run is 38 clocks for 4:2:2 and 43 clocks for 4 fsc NTSC and PAL. However, the above sequence generally shows the most critical situation for the bit slip problem.

Note : Actually there exists a family of such particular code as above described. They will, however, create an identical sequence in the serial domain since the difference amongst the family is merely which bit is regarded as the start bit of a word.

Figure 28 : Application Circuit Example



REPRESENTATIVE CHARACTERISTICS EXAMPLE

Figure 29 : VCO Oscillation Frequency versus FV Pin Voltage

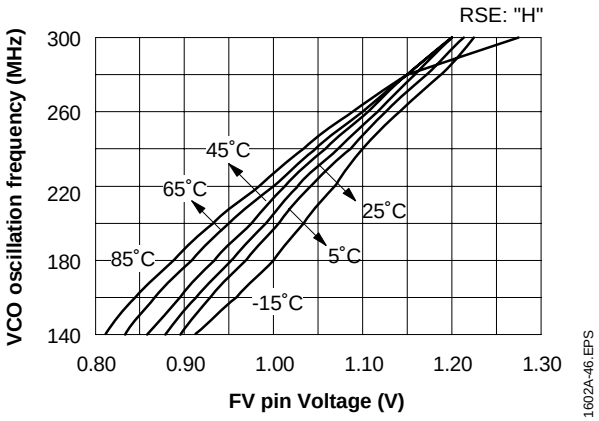


Figure 30 : VCO Oscillation Frequency versus FV Pin Voltage

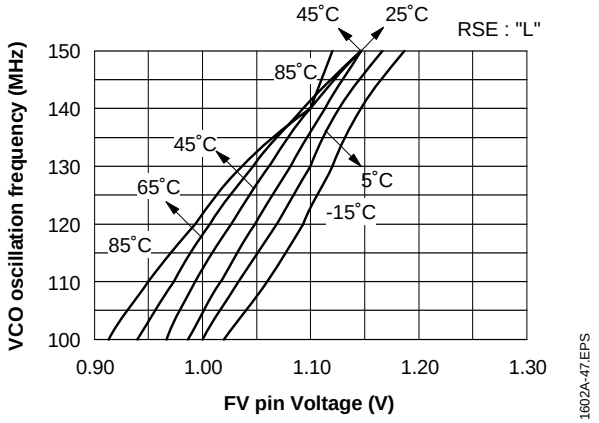


Figure 31 : An example of equalizer characteristics using 5C - 2V coaxial cable with respect to the gain for 0.5meter

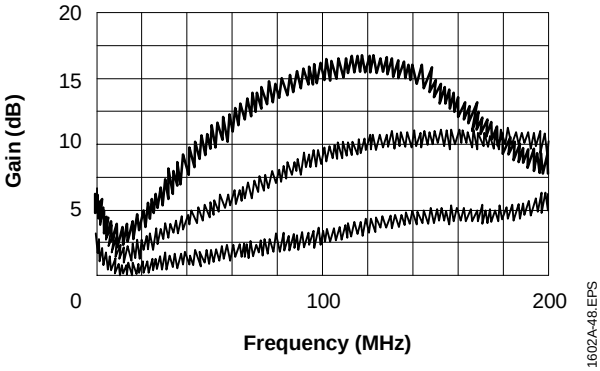


Figure 32 : Pull-in Range and Free Run Frequency (270Mb/s)

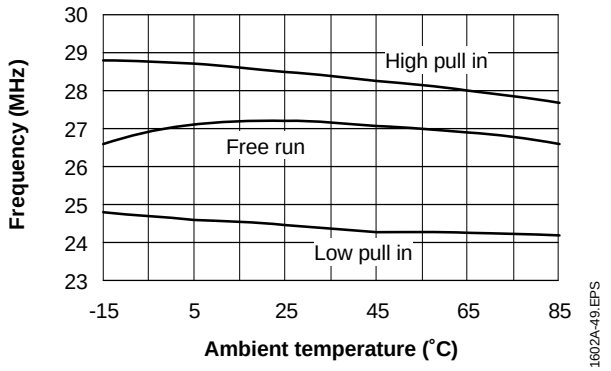


Figure 33 : Pull-in Range and Free Run Frequency (177Mb/s)

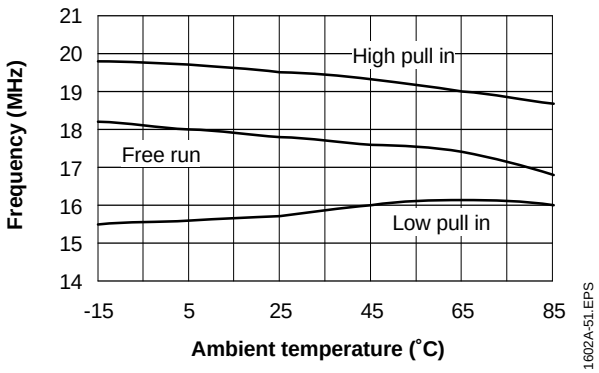
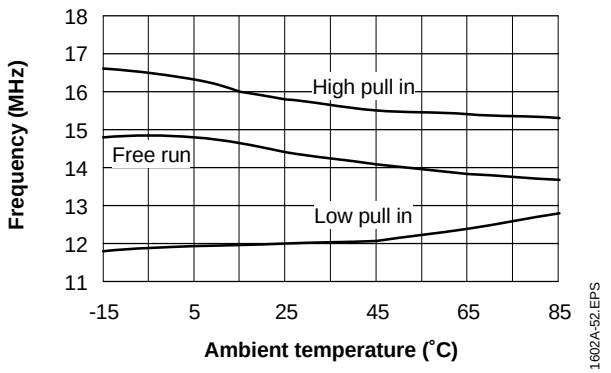
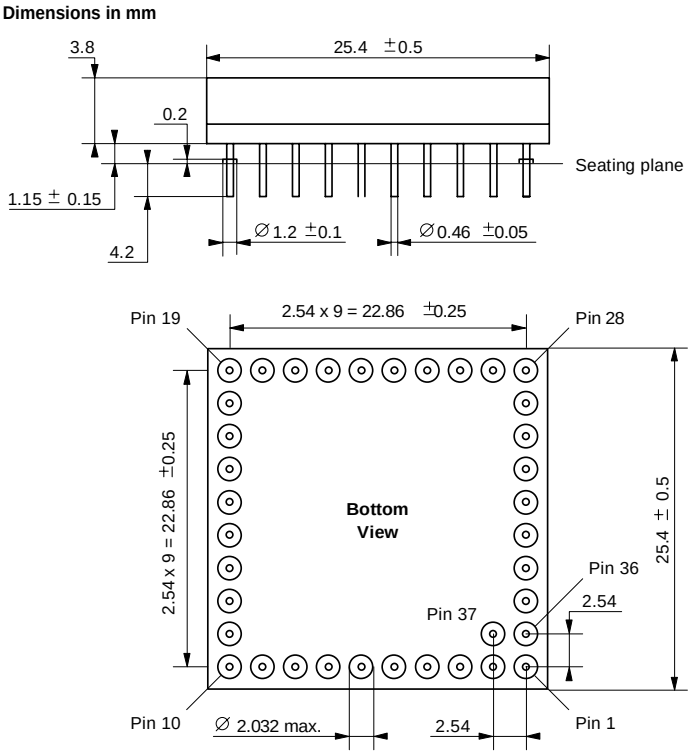


Figure 34 : Pull-in Range and Free Run Frequency (143Mb/s)



PACKAGE MECHANICAL DATA

37 PINS - CERAMIC PGA



PM-PGA37.EPS