



STSJ100NH3LL

N-CHANNEL 30V - 0.0027 Ω - 100A PowerSO-8™ STripFET™ III POWER MOSFET FOR DC-DC CONVERSION

PRELIMINARY DATA

TYPE	V _{DSS}	R _{DS(on)}	I _D
STSJ100NH3LL	30 V	<0.0035 Ω	100 A

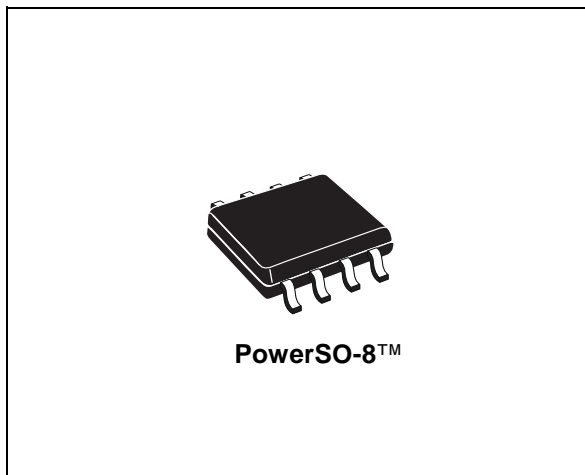
- TYPICAL R_{DS(on)} = 0.0027 Ω @ 10V
- OPTIMAL R_{DS(on)} x Q_g TRADE-OFF @ 4.5V
- CONDUCTION LOSSES REDUCED
- SWITCHING LOSSES REDUCED
- IMPROVED JUNCTION-CASE THERMAL RESISTANCE

DESCRIPTION

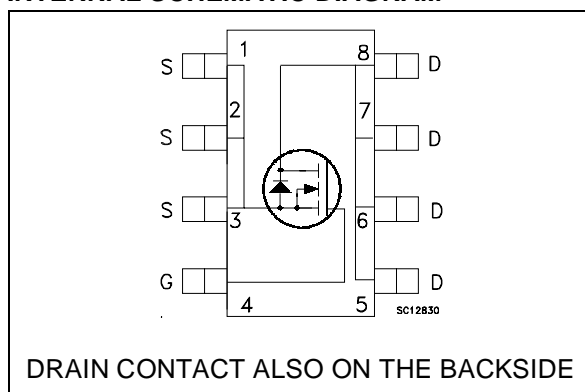
The STSJ100NH3LL utilizes the latest advanced design rules of ST's proprietary STripFET™ technology. This process complied to unique metallization techniques realizes the most advanced low voltage MOSFET in SO-8 ever produced. The exposed slug reduces the R_{thj-c} improving the current capability.

APPLICATIONS

- SPECIFICALLY DESIGNED AND OPTIMISED FOR HIGH EFFICIENCY CPU CORE DC/DC CONVERTERS FOR MOBILE PCs



INTERNAL SCHEMATIC DIAGRAM



Ordering Information

SALES TYPE	MARKING	PACKAGE	PACKAGING
STSJ100NH3LL	SJ100NH3LL	PowerSO-8	TAPE & REEL

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	30	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 k Ω)	30	V
V _{GS}	Gate- source Voltage	± 18	V
I _D	Drain Current (continuous) at T _C = 25°C	100	A
I _D	Drain Current (continuous) at T _C = 25°C (#)	22	A
I _D	Drain Current (continuous) at T _C = 100°C	62.5	A
I _{DM} (•)	Drain Current (pulsed)	400	A
P _{tot}	Total Dissipation at T _C = 25°C	70	W
	Total Dissipation at T _C = 25°C (#)	3	W

(•) Pulse width limited by safe operating area.

STSJ100NH3LL

THERMAL DATA

Rthj-c	Thermal Resistance Junction-case	Max	1.8	°C/W
Rthj-amb	(#)Thermal Resistance Junction-ambient	Max	42	°C/W
T _j	Maximum Operating Junction Temperature		150	°C
T _{stg}	Storage Temperature		-55 to 150	°C

(#) When Mounted on FR-4 board with 1 inch² pad, 2 oz of Cu and t ≤ 10 sec.

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0	30			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating T _C = 125°C			1 10	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 18 V			±100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} I _D = 250 μA	1			V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10 V I _D = 50 A V _{GS} = 4.5 V I _D = 50 A		0.0027 0.0035	0.0035 0.005	Ω Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (*)	Forward Transconductance	V _{DS} =10 V I _D = 12 A		30		S
C _{iss} C _{oss} C _{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		4450 655 50		pF pF pF

ELECTRICAL CHARACTERISTICS (continued)**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	$V_{DD} = 15\text{ V}$ $I_D = 50\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (Resistive Load, Figure 1)		18 50		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD}=15\text{V}$ $I_D=100\text{A}$ $V_{GS}=4.5\text{V}$ (see test circuit, Figure 2)		32 12.5 10	43	nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	$V_{DD} = 15\text{ V}$ $I_D = 50\text{ A}$ $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (Resistive Load, Figure 3)		75 8		ns ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}	Source-drain Current Source-drain Current (pulsed)				100 400	A A
$V_{SD}^{(*)}$	Forward On Voltage	$I_{SD} = 100\text{ A}$ $V_{GS} = 0$			1.2	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 100\text{ A}$ $di/dt = 100\text{A}/\mu\text{s}$ $V_{DD} = 25\text{ V}$ $T_j = 150^\circ\text{C}$ (see test circuit, Figure 3)		32 34 2.1		ns nC A

(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

(●) Pulse width limited by safe operating area.

Fig. 1: Switching Times Test Circuits For Resistive Load

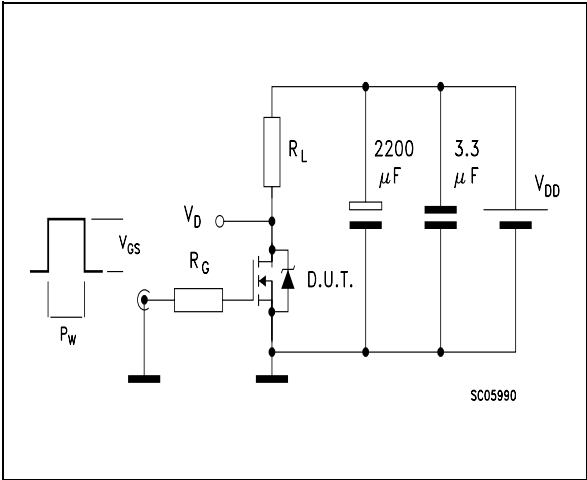


Fig. 2: Gate Charge test Circuit

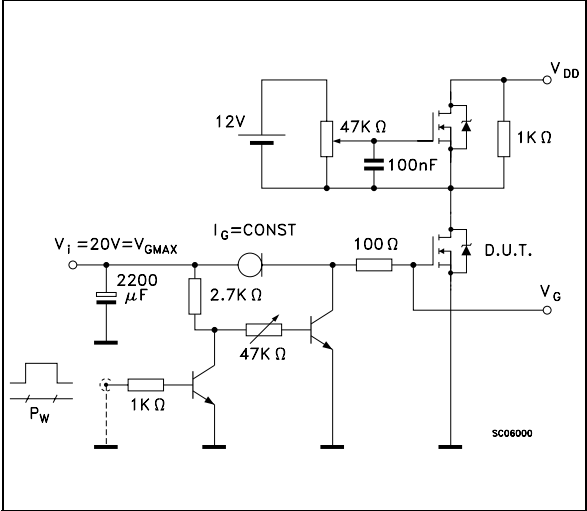
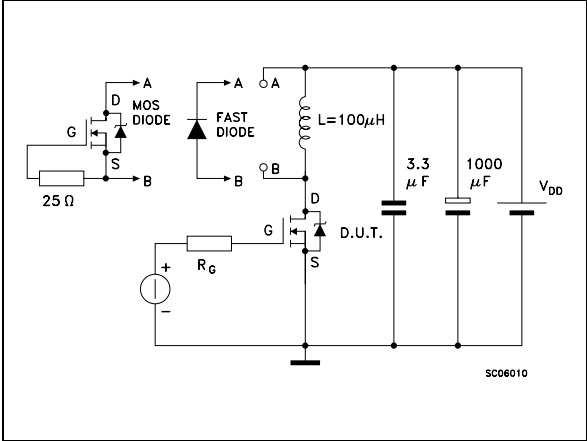
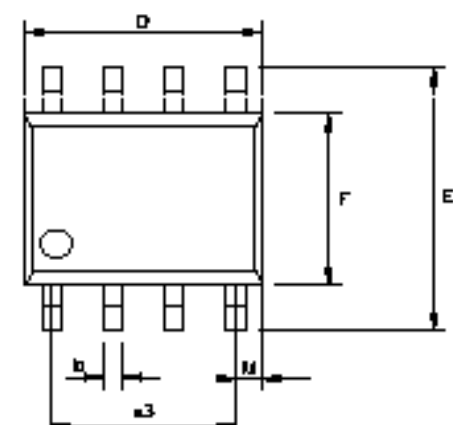


Fig. 3: Test Circuit For Diode Recovery Behaviour

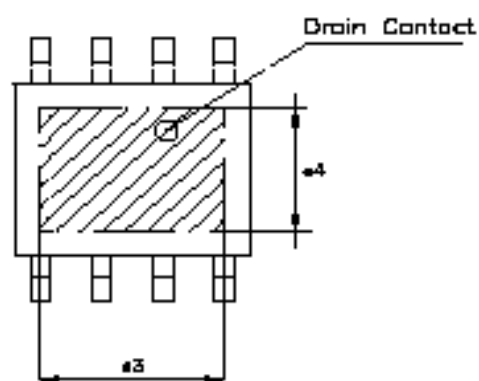


PowerSO-8™ MECHANICAL DATA

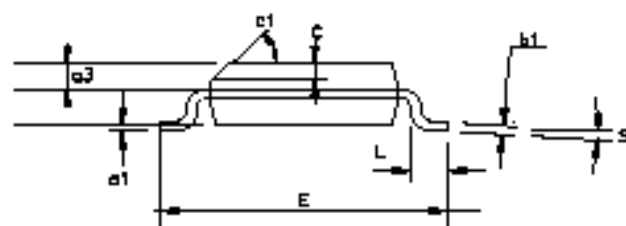
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45° (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
e4		2.79			0.110	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8° (max.)					



(Top View)



(Bottom View)



PowerSO-8

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