



STS2NF100

N-CHANNEL 100V - 0.23 Ω - 2A SO-8
STripFET™ II POWER MOSFET

| TYPE | V _{DSS} | R _{DS(on)} | I _D |
|-----------|------------------|---------------------|----------------|
| STS2NF100 | 100 V | <0.26 Ω | 2 A |

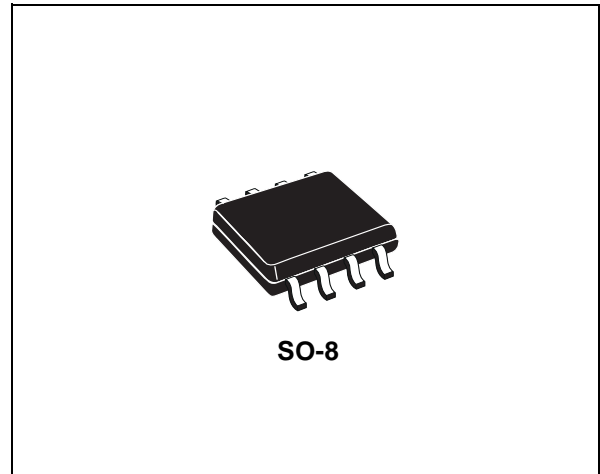
- TYPICAL R_{DS(on)} = 0.23 Ω
- EXCEPTIONAL dv/dt CAPABILITY
- 100 % AVALANCHE TESTED
- APPLICATION ORIENTED CHARACTERIZATION

DESCRIPTION

This MOSFET series realized with STMicroelectronics unique STripFET process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency, high-frequency isolated DC-DC converters for Telecom and Computer applications. It is also intended for any applications with low gate drive requirements.

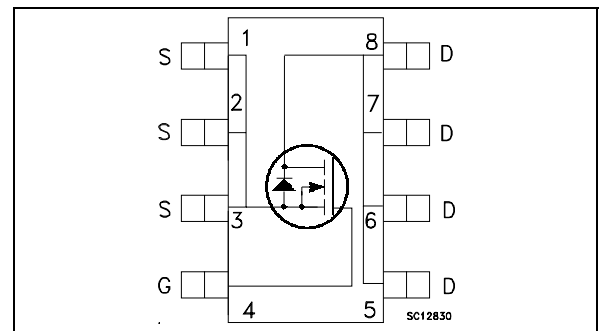
APPLICATIONS

- HIGH-EFFICIENCY DC-DC CONVERTERS
- UPS AND MOTOR CONTROL



SO-8

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---------------------|---|------------|------|
| V _{DS} | Drain-source Voltage (V _{GS} = 0) | 100 | V |
| V _{DGR} | Drain-gate Voltage (R _{GS} = 20 k Ω) | 100 | V |
| V _{GS} | Gate- source Voltage | ± 20 | V |
| I _{D(●)} | Drain Current (continuous) at T _C = 25°C | 2 | A |
| I _D | Drain Current (continuous) at T _C = 100°C | 1.3 | A |
| I _{DM(●●)} | Drain Current (pulsed) | 8 | A |
| P _{tot} | Total Dissipation at T _C = 25°C | 2.5 | W |
| | Derating Factor | 0.016 | W/°C |
| dV/dt (1) | Peak Diode Recovery voltage slope | 40 | V/ns |
| E _{AS} (2) | Single Pulse Avalanche Energy | 200 | mJ |
| T _{stg} | Storage Temperature | -65 to 175 | °C |
| T _j | Max. Operating Junction Temperature | | |

(●●) Pulse width limited by safe operating area.

(●) Current limited by the package

(1) I_{SD} \leq 2A, di/dt \leq 300A/ μ s, V_{DD} \leq V_{(BR)DSS}, T_j \leq T_{JMAX}

(2) Starting T_j = 25 °C, I_D = 3A, V_{DD} = 50V

STS2NF100

THERMAL DATA

| | | | |
|--|--|--------------------------------|------------------|
| Rthj-amb T _j T _{stg} | (*) Thermal Resistance Junction-ambient Thermal Operating Junction-ambient Storage Temperature | 50 -55 to 150 -55 to 150 | °C/W °C °C |
|--|--|--------------------------------|------------------|

(*) Mounted on FR-4 board (t ≤ 10 sec.)

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

OFF

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|----------------------|---|---|------|------|---------|----------|
| V _{(BR)DSS} | Drain-source Breakdown Voltage | I _D = 250 µA, V _{GS} = 0 | 100 | | | V |
| I _{DSS} | Zero Gate Voltage Drain Current (V _{GS} = 0) | V _{DS} = Max Rating V _{DS} = Max Rating T _C = 125°C | | | 1 10 | µA µA |
| I _{GSS} | Gate-body Leakage Current (V _{DS} = 0) | V _{GS} = ± 20 V | | | ±100 | nA |

ON (*)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---------------------|-----------------------------------|---|------|------|------|------|
| V _{GS(th)} | Gate Threshold Voltage | V _{DS} = V _{GS} I _D = 250 µA | 2 | 3 | 4 | V |
| R _{DS(on)} | Static Drain-source On Resistance | V _{GS} = 10 V I _D = 1 A | | 0.23 | 0.26 | Ω |

DYNAMIC

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|--|---|--|------|-----------------|------|----------------|
| g _{fs} (*) | Forward Transconductance | V _{DS} > I _{D(on)} × R _{DS(on)max} I _D = 1 A | | 1.5 | | S |
| C _{iss} C _{oss} C _{rss} | Input Capacitance Output Capacitance Reverse Transfer Capacitance | V _{DS} = 25V, f = 1 MHz, V _{GS} = 0 | | 280 45 20 | | pF pF pF |

ELECTRICAL CHARACTERISTICS (continued)**SWITCHING ON**

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|-------------------------------|--|---|------|----------------|------|----------------|
| $t_{d(on)}$ t_r | Turn-on Delay Time Rise Time | $V_{DD} = 50\text{ V}$ $I_D = 1\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (Resistive Load, Figure 3) | | 6 10 | | ns ns |
| Q_g Q_{gs} Q_{gd} | Total Gate Charge Gate-Source Charge Gate-Drain Charge | $V_{DD} = 80\text{ V}$ $I_D = 1\text{ A}$ $V_{GS} = 10\text{ V}$ | | 10 2.5 4 | | nC nC nC |

SWITCHING OFF

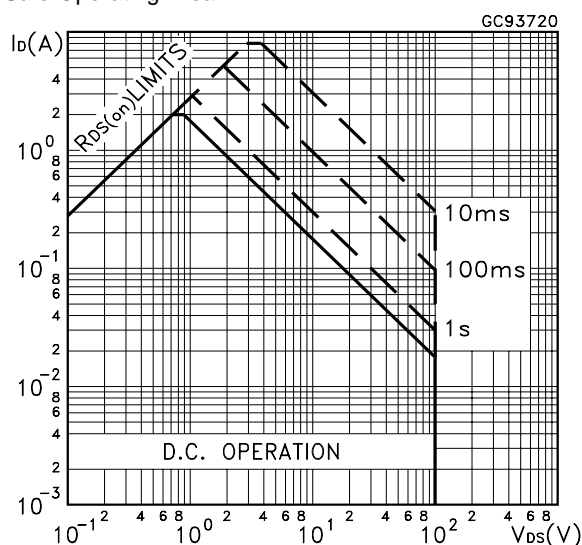
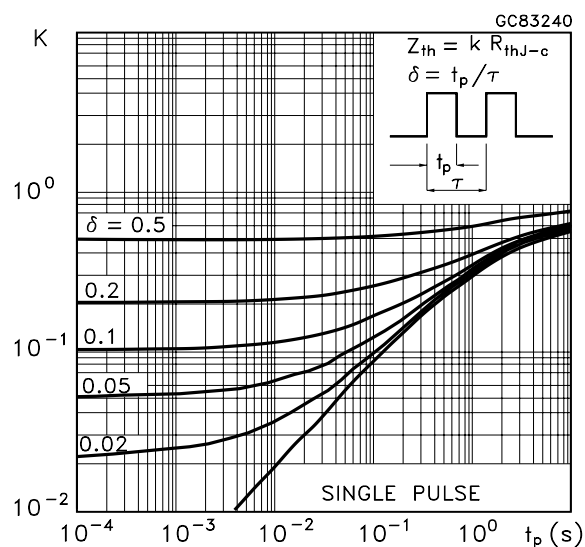
| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|----------------------------------|---|--|------|---------------|------|----------------|
| $t_{d(off)}$ t_f | Turn-off Delay Time Fall Time | $V_{DD} = 50\text{ V}$ $I_D = 1\text{ A}$ $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (Resistive Load, Figure 3) | | 20 3 | | ns ns |
| $t_r(V_{off})$ t_f t_c | Off-Voltage Rise Time Fall Time Cross-over Time | $V_{clamp} = 80\text{ V}$ $I_D = 1\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (Inductive Load, Figure 5) | | 19 8 15 | | ns ns ns |

SOURCE DRAIN DIODE

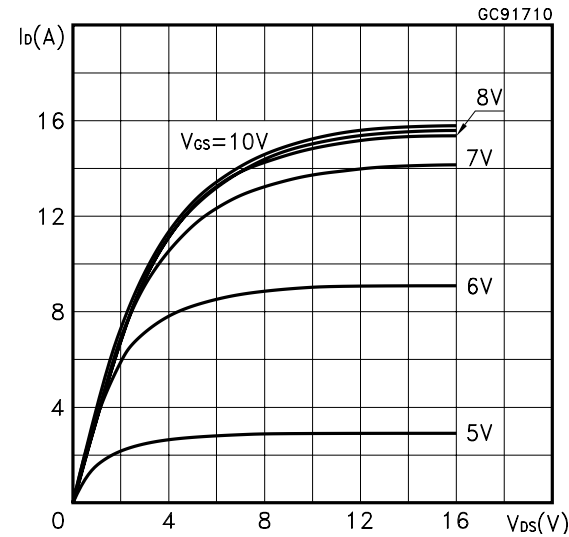
| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|-----------------------------------|--|--|------|----------------|--------|---------------|
| I_{SD} $I_{SDM}(\bullet)$ | Source-drain Current Source-drain Current (pulsed) | | | | 2 8 | A A |
| $V_{SD}(\ast)$ | Forward On Voltage | $I_{SD} = 2\text{ A}$ $V_{GS} = 0$ | | | 1.3 | V |
| t_{rr} Q_{rr} I_{RRM} | Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current | $I_{SD} = 2\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 10\text{ V}$ $T_j = 150^\circ\text{C}$ (see test circuit, Figure 5) | | 70 175 5 | | ns nC A |

(\ast) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

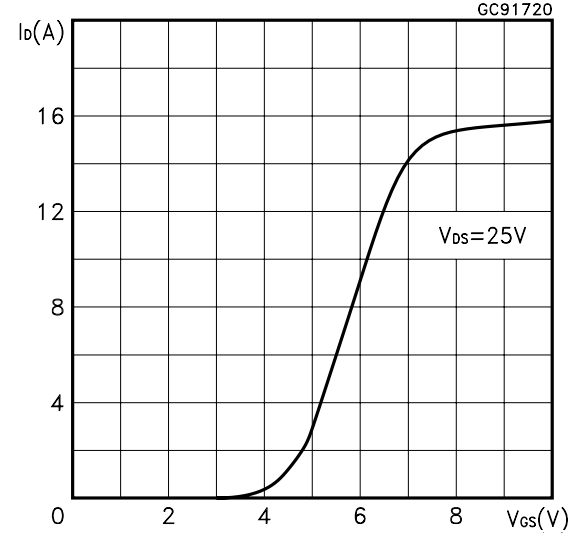
(\bullet) Pulse width limited by safe operating area.

Safe Operating Area**Thermal Impedance**

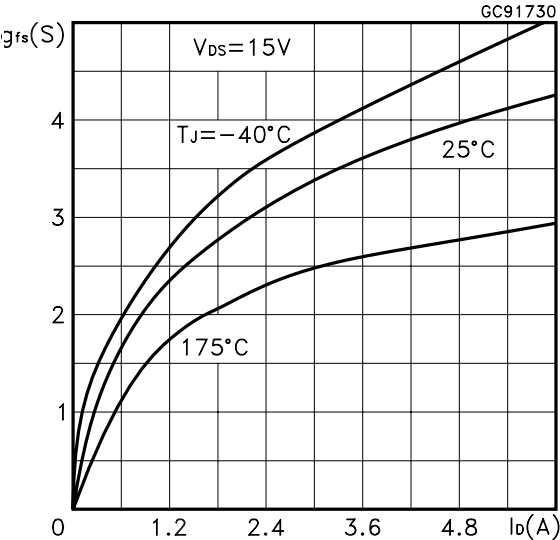
Output Characteristics



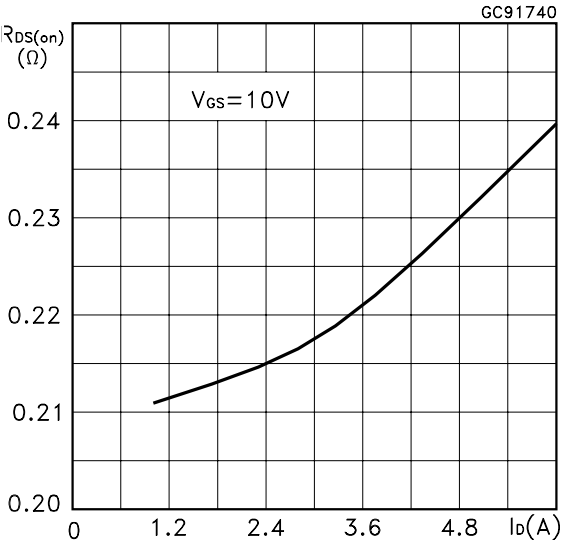
Transfer Characteristics



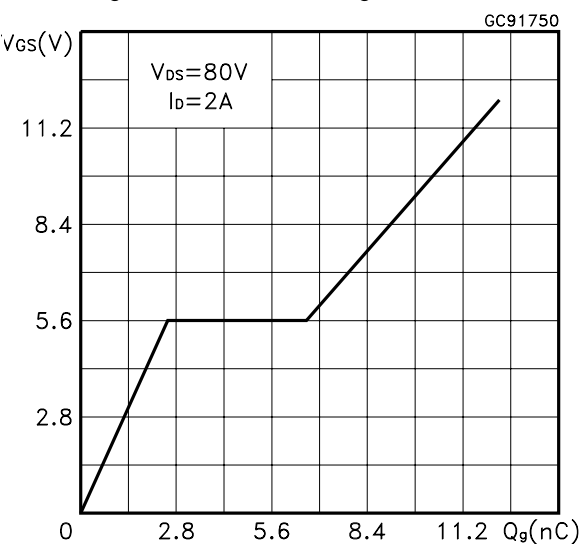
Transconductance



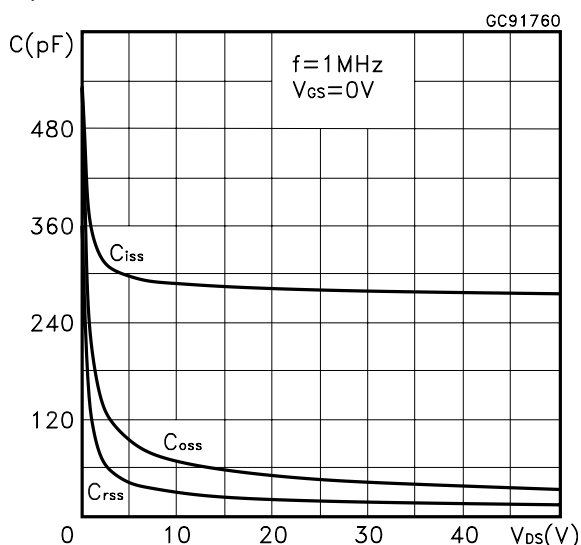
Static Drain-source On Resistance



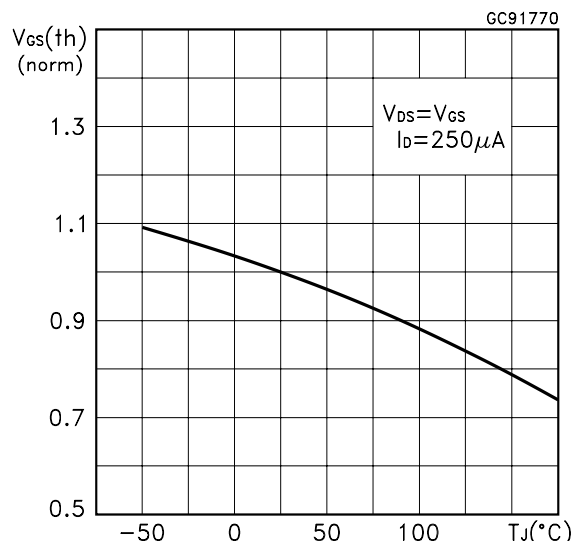
Gate Charge vs Gate-source Voltage



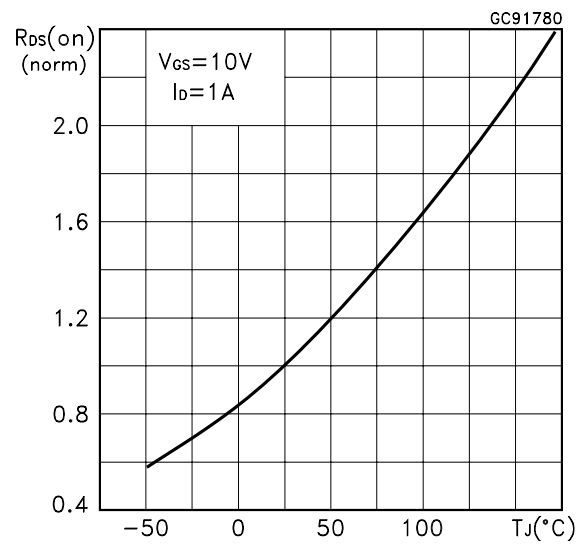
Capacitance Variations



Normalized Gate Threshold Voltage vs Temperature



Normalized on Resistance vs Temperature



Source-drain Diode Forward Characteristics

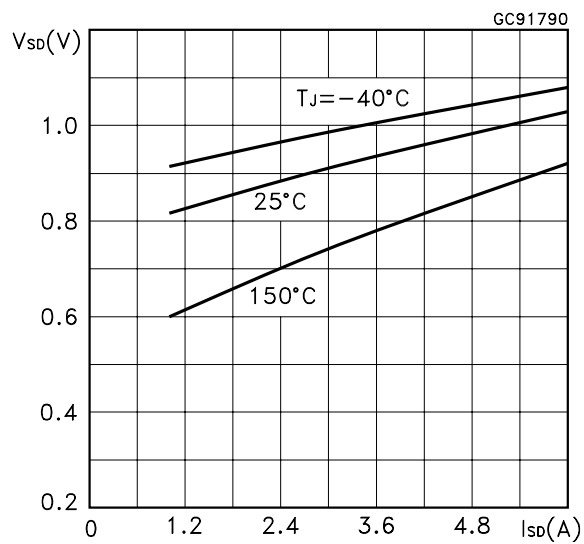


Fig. 1: Unclamped Inductive Load Test Circuit

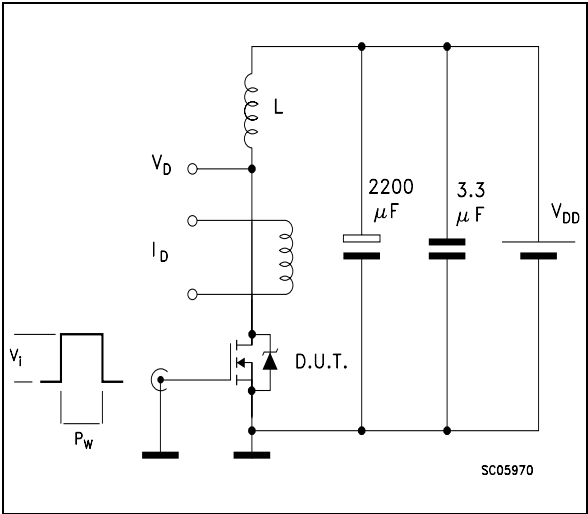


Fig. 2: Unclamped Inductive Waveform



Fig. 3: Switching Times Test Circuits For Resistive Load

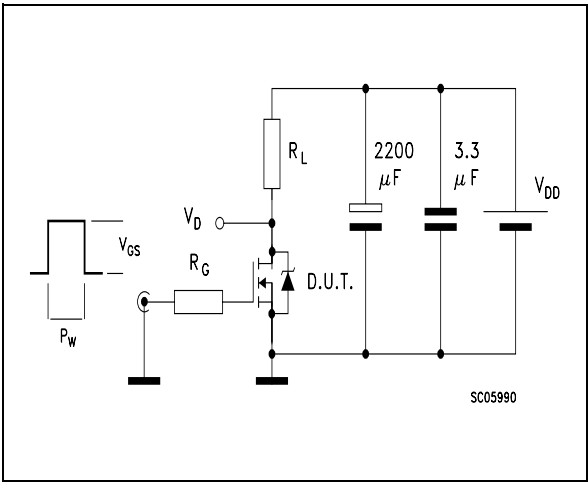


Fig. 4: Gate Charge test Circuit

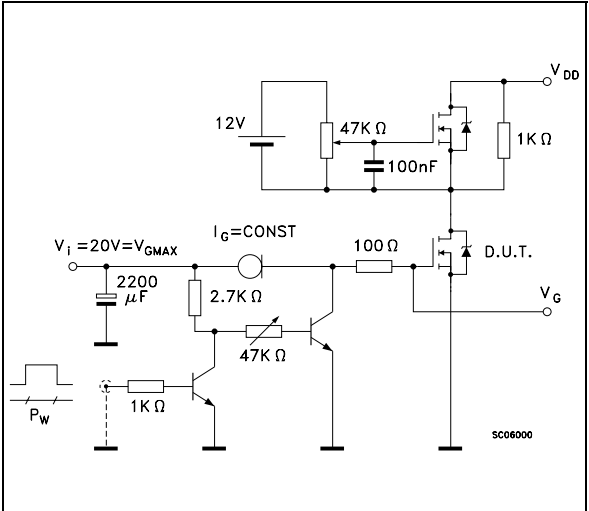
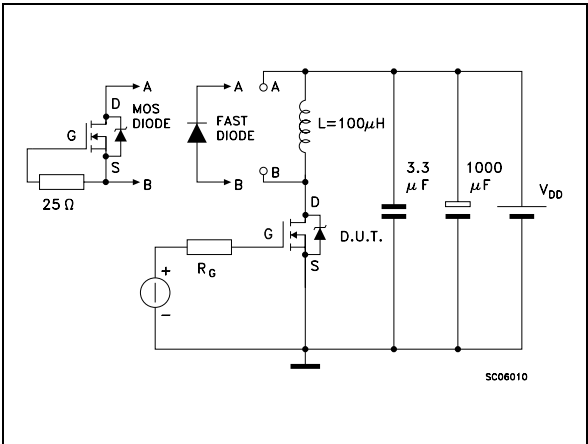
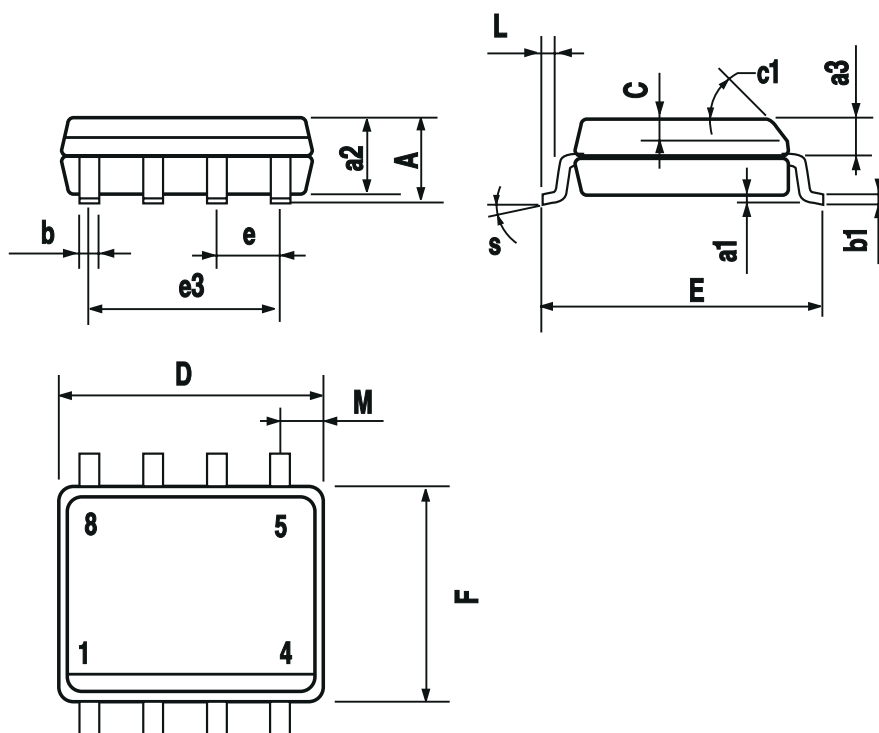


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



SO-8 MECHANICAL DATA

| DIM. | mm | | | inch | | |
|------|-----------|------|------|-------|-------|-------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | | 1.75 | | | 0.068 |
| a1 | 0.1 | | 0.25 | 0.003 | | 0.009 |
| a2 | | | 1.65 | | | 0.064 |
| a3 | 0.65 | | 0.85 | 0.025 | | 0.033 |
| b | 0.35 | | 0.48 | 0.013 | | 0.018 |
| b1 | 0.19 | | 0.25 | 0.007 | | 0.010 |
| C | 0.25 | | 0.5 | 0.010 | | 0.019 |
| c1 | 45 (typ.) | | | | | |
| D | 4.8 | | 5.0 | 0.188 | | 0.196 |
| E | 5.8 | | 6.2 | 0.228 | | 0.244 |
| e | | 1.27 | | | 0.050 | |
| e3 | | 3.81 | | | 0.150 | |
| F | 3.8 | | 4.0 | 0.14 | | 0.157 |
| L | 0.4 | | 1.27 | 0.015 | | 0.050 |
| M | | | 0.6 | | | 0.023 |
| S | 8 (max.) | | | | | |



0016023

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is registered trademark of STMicroelectronics
All other names are the property of their respective owners.

® 2003 STMicroelectronics - All Rights Reserved

STMicroelectronics GROUP OF COMPANIES

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan -
Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States.

www.st.com