



STS2DPF20V

DUAL P-CHANNEL 20V - 0.14Ω - 2A SO-8 2.7V-DRIVE STripFET™ II POWER MOSFET

PRELIMINARY DATA

TYPE	V _{DSS}	R _{DS(on)}	I _D
STS2DPF20V	20 V	<0.20Ω (@4.5V) <0.25Ω (@2.7V)	2 A

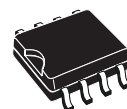
- TYPICAL R_{DS(on)} = 0.14Ω (@4.5V)
- TYPICAL R_{DS(on)} = 0.2Ω (@2.7V)
- ULTRA LOW THRESHOLD GATE DRIVE (2.7V)
- STANDARD OUTLINE FOR EASY AUTOMATED SURFACE MOUNT ASSEMBLY

DESCRIPTION

This Power MOSFET is the second generation of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

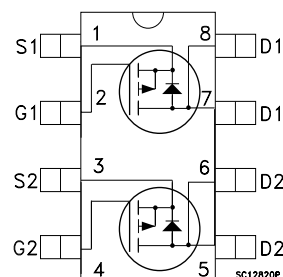
APPLICATIONS

- BATTERY MANAGMENT IN NOMADIC EQUIPMENT
- POWER MANAGMENT IN CELLULAR PHONES



SO-8

INTERNAL SCHEMATIC DIAGRAM



MOSFET ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	20	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	20	V
V _{GS}	Gate- source Voltage	± 12	V
I _D	Drain Current (continuos) at T _C = 25°C Single Operation Drain Current (continuos) at T _C = 100°C Single Operation	2 1.26	A A
I _{DM} (●)	Drain Current (pulsed)	8	A
P _{TOT}	Total Dissipation at T _C = 25°C Dual Operation Total Dissipation at T _C = 25°C Single Operation	1.6 2	W W

(●)Pulse width limited by safe operating area.

Note: For the P-CHANNEL MOSFET actual polarity of Voltages and current has to be reversed

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THERMAL DATA

Rthj-amb	(*)Thermal Resistance Junction-ambient Single Operation Dual Operation	62.5 78	°C/W °C/W
T _{stg}	Storage Temperature	-55 to 150	°C
T _j	Junction-ambient Temperature (*) When Mounted on 0.5 in ² of 2 oz. Copper	-55 to 150	°C

MOSFET ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED) OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 µA, V _{GS} = 0	20			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125 °C			1 10	µA µA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 12 V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250µA	0.6			V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 4.5 V, I _D = 1 A V _{GS} = 2.7 V, I _D = 1 A		0.14 0.20	0.20 0.25	Ω Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (1)	Forward Transconductance	V _{DS} = 15 V, I _D = 1.5 A		4.5		S
C _{iss}	Input Capacitance	V _{DS} = 15V, f = 1 MHz, V _{GS} = 0		315		pF
C _{oss}	Output Capacitance			87		pF
C _{rss}	Reverse Transfer Capacitance			17		pF

ELECTRICAL CHARACTERISTICS (CONTINUED)**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 10\text{ V}$, $I_D = 1.5\text{ A}$		38		ns
t_r	Rise Time	$R_G = 4.7\Omega$, $V_{GS} = 4.5\text{ V}$ (see test circuit, Figure 1)		30		ns
Q_g	Total Gate Charge	$V_{DD} = 10\text{ V}$, $I_D = 2\text{ A}$, $V_{GS} = 4.5\text{ V}$ (see test circuit, Figure 2)		3.8	4.8	nC
Q_{gs}	Gate-Source Charge			0.34		nC
Q_{gd}	Gate-Drain Charge			0.8		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off Delay Time	$V_{DD} = 10\text{ V}$, $I_D = 1\text{ A}$, $R_G = 4.7\Omega$, $V_{GS} = 4.5\text{ V}$ (see test circuit, Figure 1)		45		ns
t_f	Fall Time			11		ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				2	A
$I_{SDM} (2)$	Source-drain Current (pulsed)				8	A
$V_{SD} (1)$	Forward On Voltage	$I_{SD} = 2\text{ A}$, $V_{GS} = 0$			1.2	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 2\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 10\text{ V}$, $T_j = 150^\circ\text{C}$ (see test circuit, Figure 3)		15		ns
Q_{rr}	Reverse Recovery Charge			7.5		nC
I_{RRM}	Reverse Recovery Current			1		A

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

2. Pulse width limited by safe operating area.

Fig. 1: Switching Times Test Circuit For Resistive Load

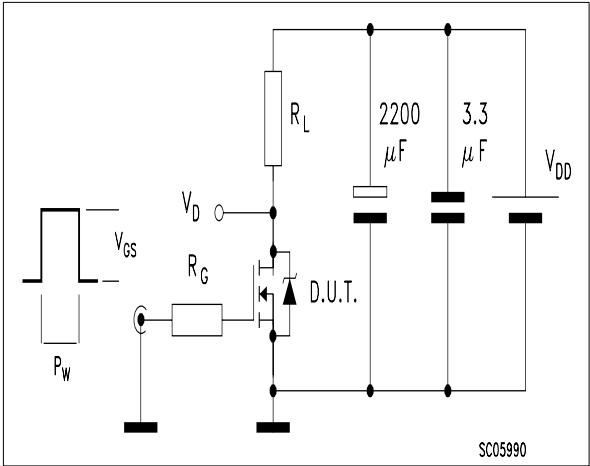


Fig. 2: Gate Charge test Circuit

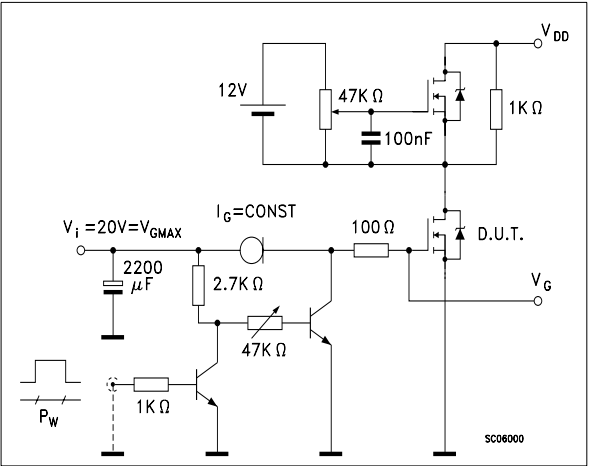
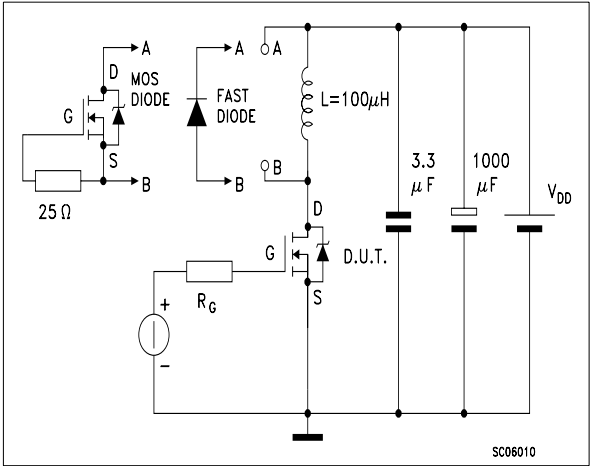
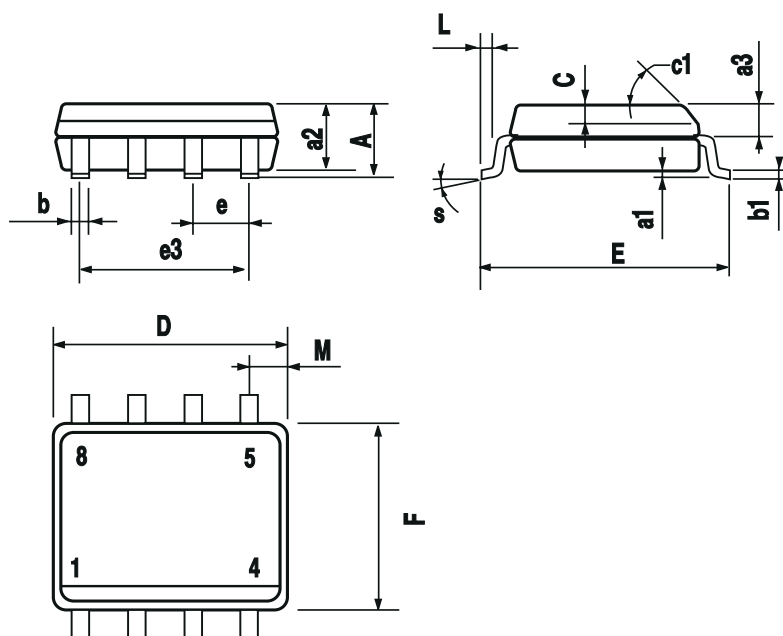


Fig. 3: Test Circuit For Diode Recovery Behaviour



SO-8 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



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