

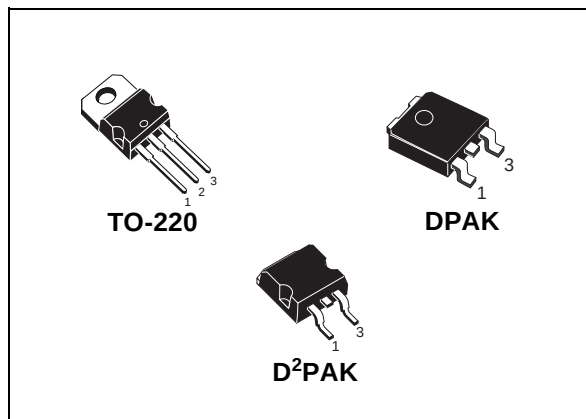


STP40NF10 STD40NF10 - STB40NF10

N-CHANNEL 100V - 0.024Ω - 50A TO-220/DPAK/D²PAK
LOW GATE CHARGE STripFET™ II POWER MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D
STP40NF10	100 V	< 0.028 Ω	50 A
STD40NF10	100 V	< 0.028 Ω	50 A
STB40NF10	100 V	< 0.028 Ω	50 A

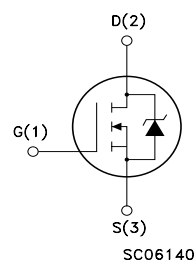
- TYPICAL R_{DS(on)} = 0.024Ω
- EXCEPTIONAL dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- APPLICATION ORIENTED CHARACTERIZATION
- ADD SUFFIX "T4" FOR ORDERING IN TAPE & REEL



DESCRIPTION

This Power MOSFET series realized with STMicroelectronics unique STripFET process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency isolated DC-DC converters for Telecom and Computer application. It is also intended for any application with low gate charge drive requirements.

INTERNAL SCHEMATIC DIAGRAM



APPLICATIONS

- HIGH-EFFICIENCY DC-DC CONVERTERS
- HIGH-CURRENT SWITCHING APPLICATIONS

ORDERING INFORMATION

SALES TYPE	MARKING	PACKAGE	PACKAGING
STP40NF10	P40NF10	TO-220	TUBE
STD40NF10T4	D40NF10	DPAK	TAPE & REEL
STB40NF10T4	B40NF10	D ² PAK	TAPE & REEL

STP40NF10 - STD40NF10 - STB40NF10**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value		Unit
		TO-220 - D ² PAK	DPAK	
V _{DS}	Drain-source Voltage (V _{GS} = 0)	100		V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	100		V
V _{GS}	Gate- source Voltage	± 20		V
I _D (*)	Drain Current (continuous) at T _C = 25°C	50		A
I _D	Drain Current (continuous) at T _C = 100°C	35		A
I _{DM} (•)	Drain Current (pulsed)	200		A
P _{TOT}	Total Dissipation at T _C = 25°C	150	125	W
	Derating Factor	1	0.83	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	20	35	V/ns
E _{AS} (2)	Single Pulse Avalanche Energy	150	135	mJ
T _{stg}	Storage Temperature	– 55 to 175		°C
T _j	Operating Junction Temperature			

(•) Pulse width limited by safe operating area

(*) Limited by Package

(1) I_{SD} ≤ 50A, di/dt ≤ 600 A/μs, V_{DD} ≤ V_{(BR)DSS}, T_j ≤ T_{JMAX}.(2) Starting T_j = 25°C, I_D = 50A, V_{DD} = 25V**THERMAL DATA**

		TO-220 - D ² PAK	DPAK	
R _{thj-case}	Thermal Resistance Junction-case Max	1	1.2	°C/W
R _{thj-amb}	Thermal Resistance Junction-ambient Max	62.5		°C/W
T _l	Maximum Lead Temperature For Soldering Purpose	300		°C

ELECTRICAL CHARACTERISTICS (T_{CASE} = 25 °C UNLESS OTHERWISE SPECIFIED)

ON/OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0	100			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125 °C			1 10	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 20V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	2	2.8	4	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10V, I _D = 25 A		0.024	0.028	Ω

ELECTRICAL CHARACTERISTICS (CONTINUED)
DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	$V_{DS} = 25V, I_D = 25 A$		20		S
C_{iss}	Input Capacitance	$V_{DS} = 25V, f = 1 MHz, V_{GS} = 0$		1780		pF
C_{oss}	Output Capacitance			265		pF
C_{rss}	Reverse Transfer Capacitance			112		pF

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 50 V, I_D = 25 A$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see test circuit, Figure 3)		28		ns
t_r	Rise Time			63		ns
Q_g	Total Gate Charge	$V_{DD} = 80V, I_D = 50A, V_{GS} = 10V$		60.6	80	nC
Q_{gs}	Gate-Source Charge			9.6		nC
Q_{gd}	Gate-Drain Charge			22.8		nC

SWITCHING OFF

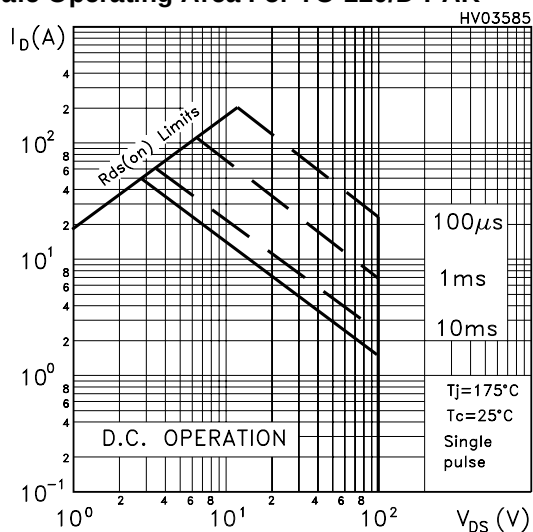
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off-Delay Time	$V_{DD} = 50 V, I_D = 25 A,$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see test circuit, Figure 3)		84		ns
t_f	Fall Time			28		ns

SOURCE DRAIN DIODE

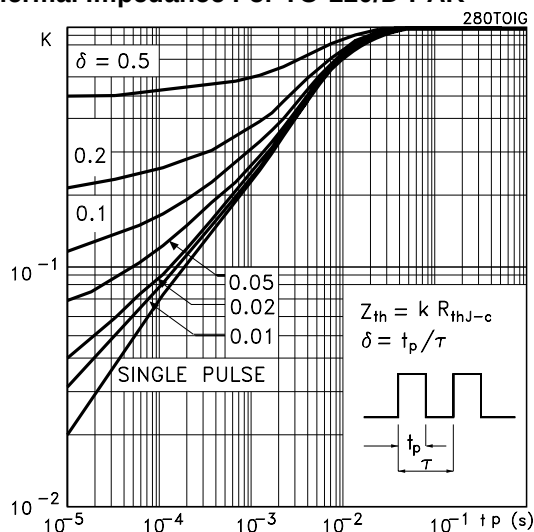
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				50	A
I_{SDM} (2)	Source-drain Current (pulsed)				200	A
V_{SD} (1)	Forward On Voltage	$I_{SD} = 50 A, V_{GS} = 0$			1.3	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 50 A, di/dt = 100A/\mu s,$ $V_{DD} = 25V, T_j = 150^\circ C$ (see test circuit, Figure 5)		114		ns
Q_{rr}	Reverse Recovery Charge			456		nC
I_{RRM}	Reverse Recovery Current			8		A

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%.
 2. Pulse width limited by safe operating area.

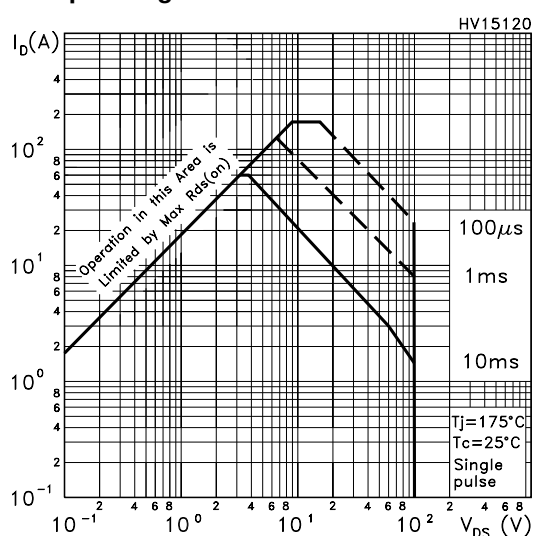
Safe Operating Area For TO-220/D²PAK



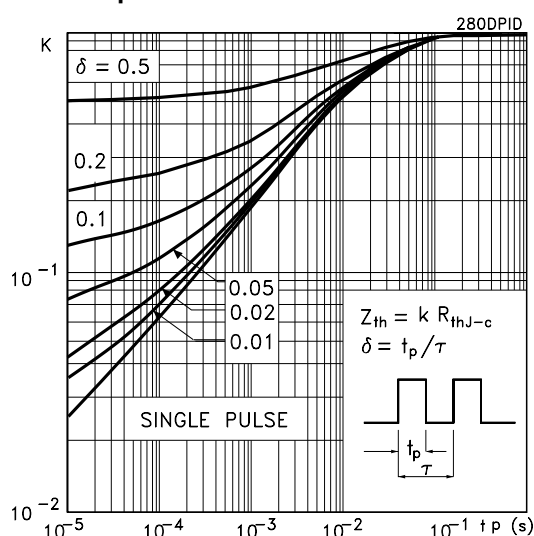
Thermal Impedance For TO-220/D²PAK



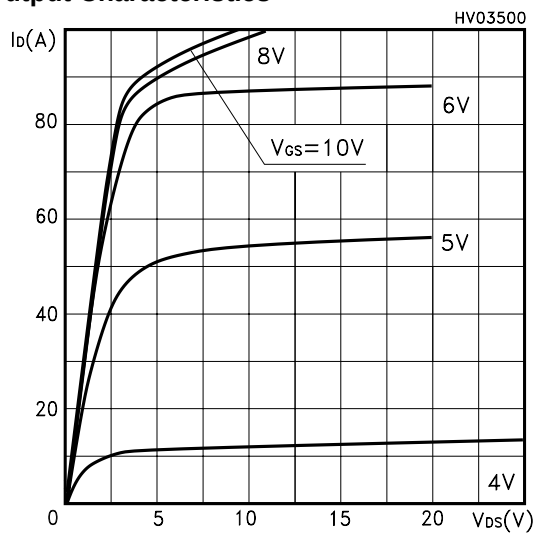
Safe Operating Area For DPAK



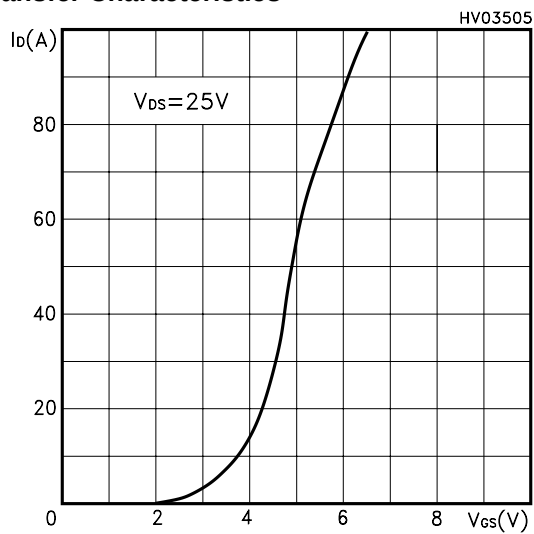
Thermal Impedance For DPAK



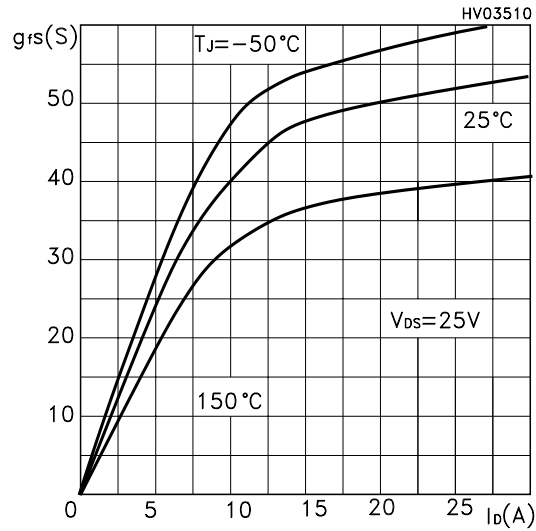
Output Characteristics



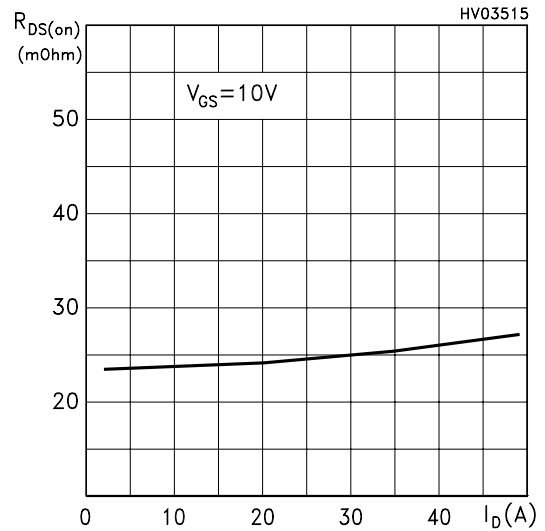
Transfer Characteristics



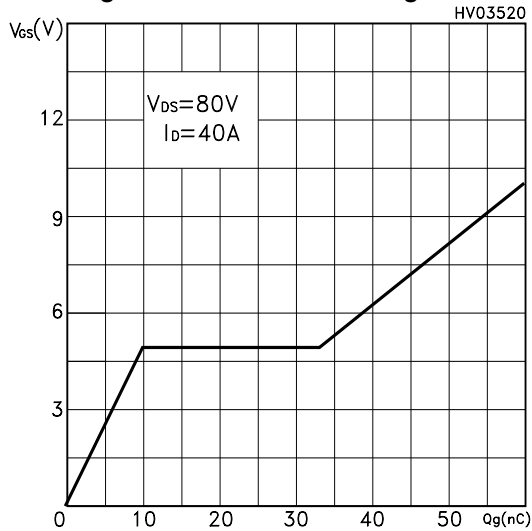
Transconductance



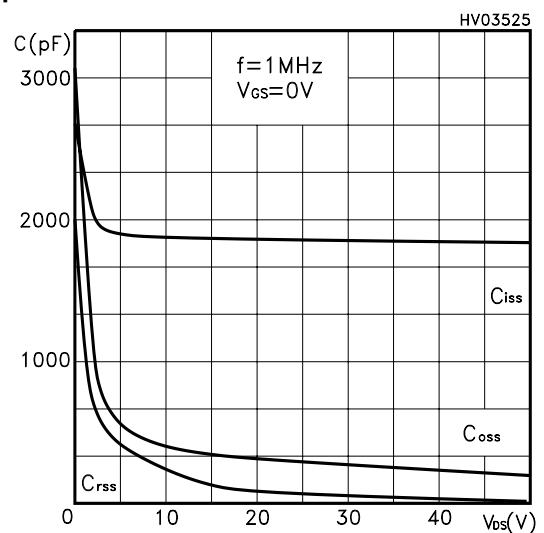
Static Drain-source On Resistance



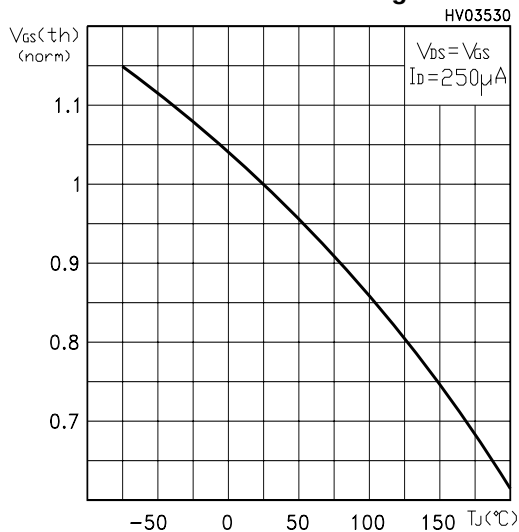
Gate Charge vs Gate-source Voltage



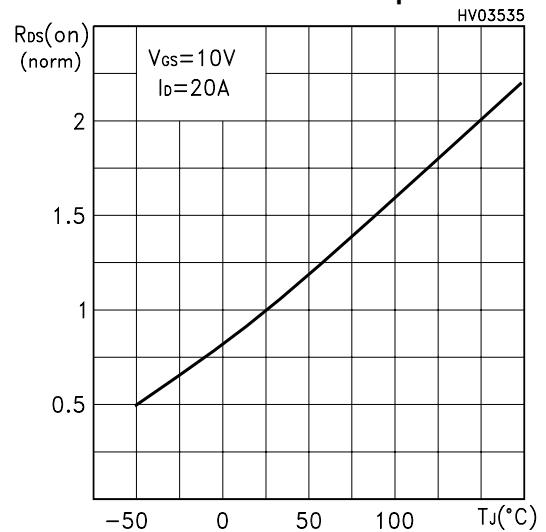
Capacitance Variations



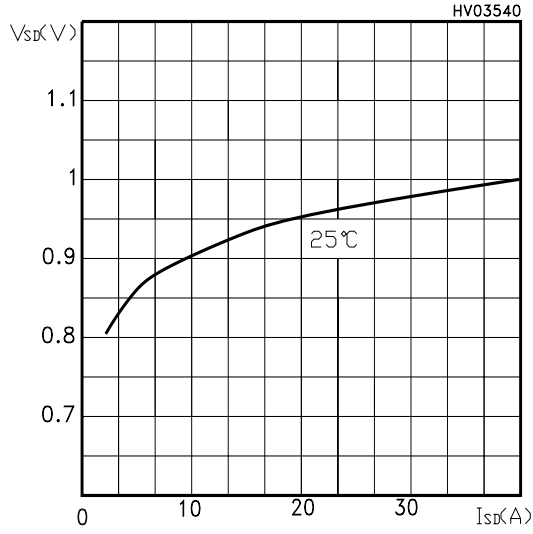
Normalized Gate Threshold Voltage vs Temp.



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics



Normalized Drain-Source Breakdown vs Temp.

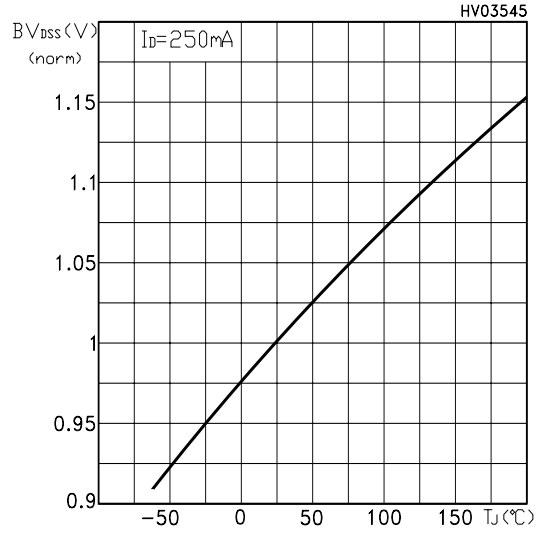


Fig. 1: Unclamped Inductive Load Test Circuit

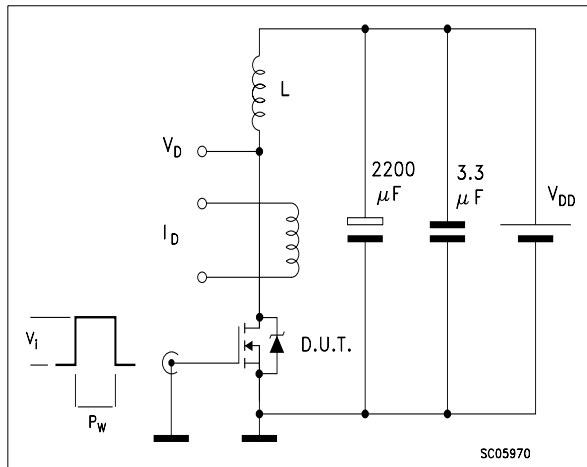


Fig. 2: Unclamped Inductive Waveform

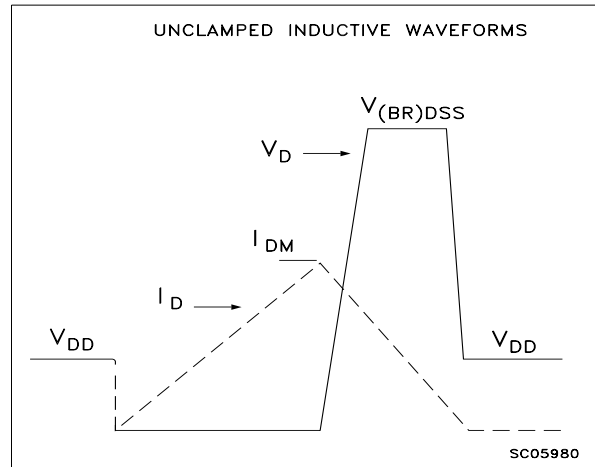


Fig. 3: Switching Times Test Circuit For Resistive Load

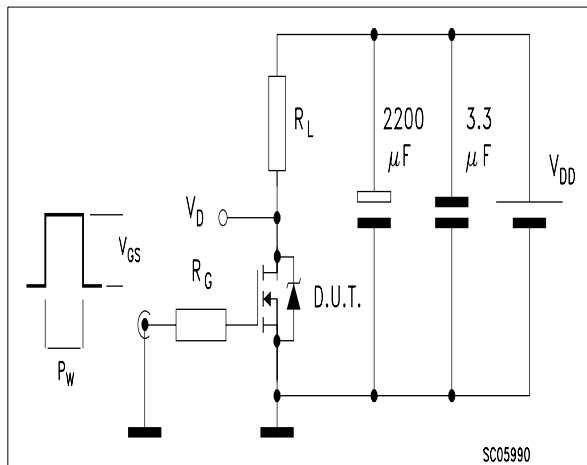


Fig. 4: Gate Charge test Circuit

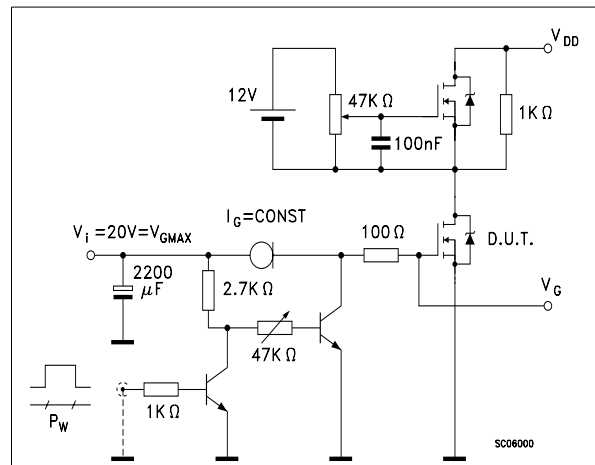
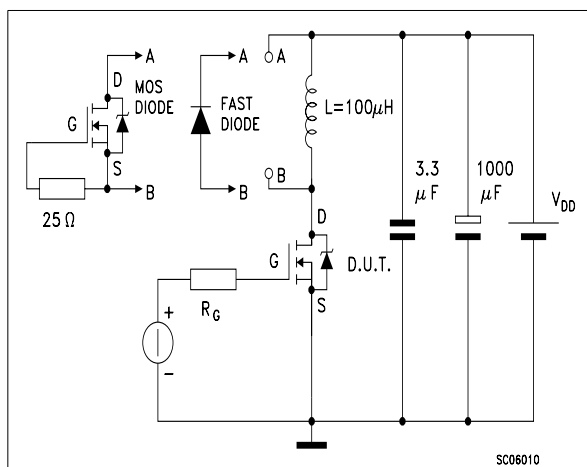
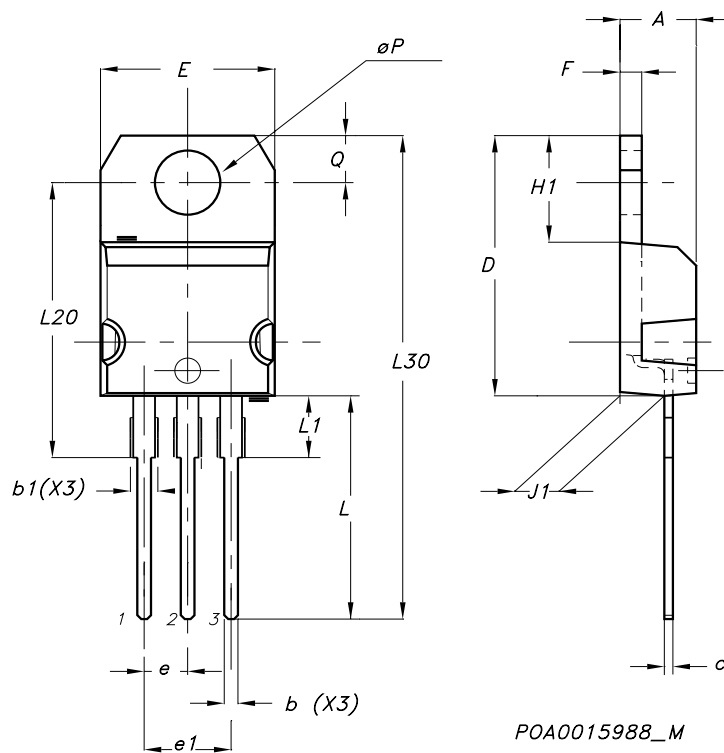


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



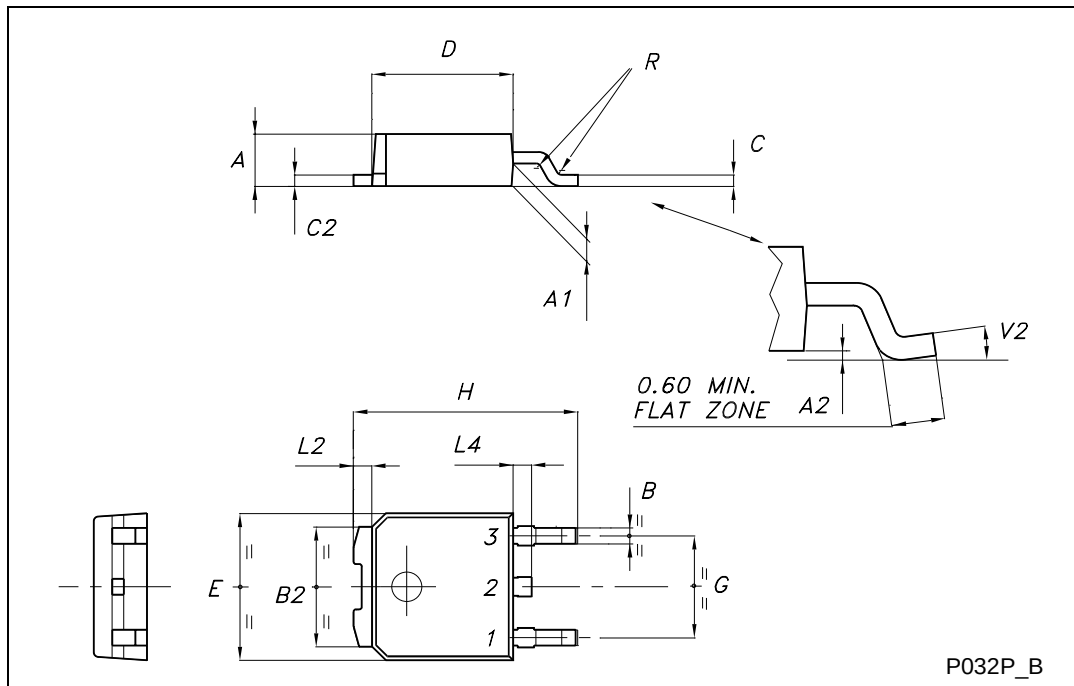
TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



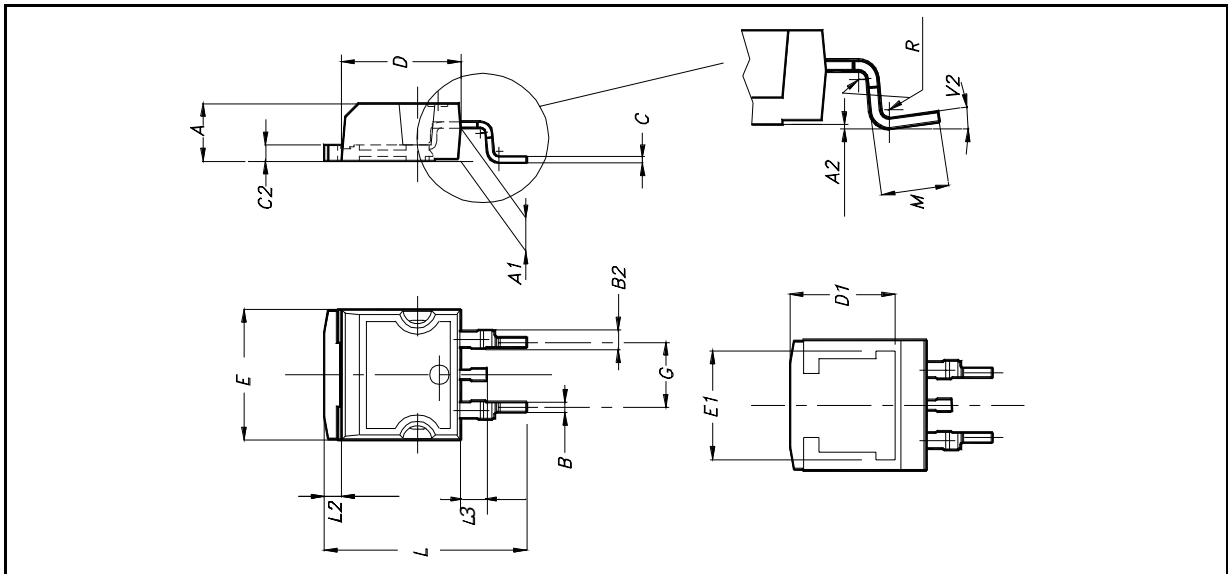
TO-252 (DPAK) MECHANICAL DATA

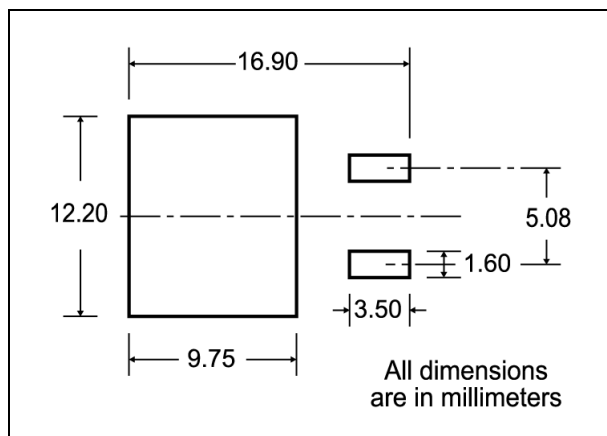
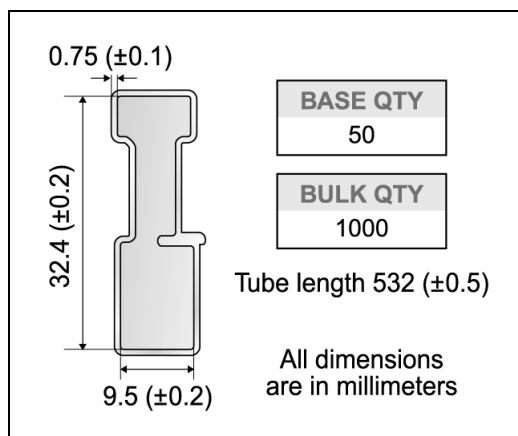
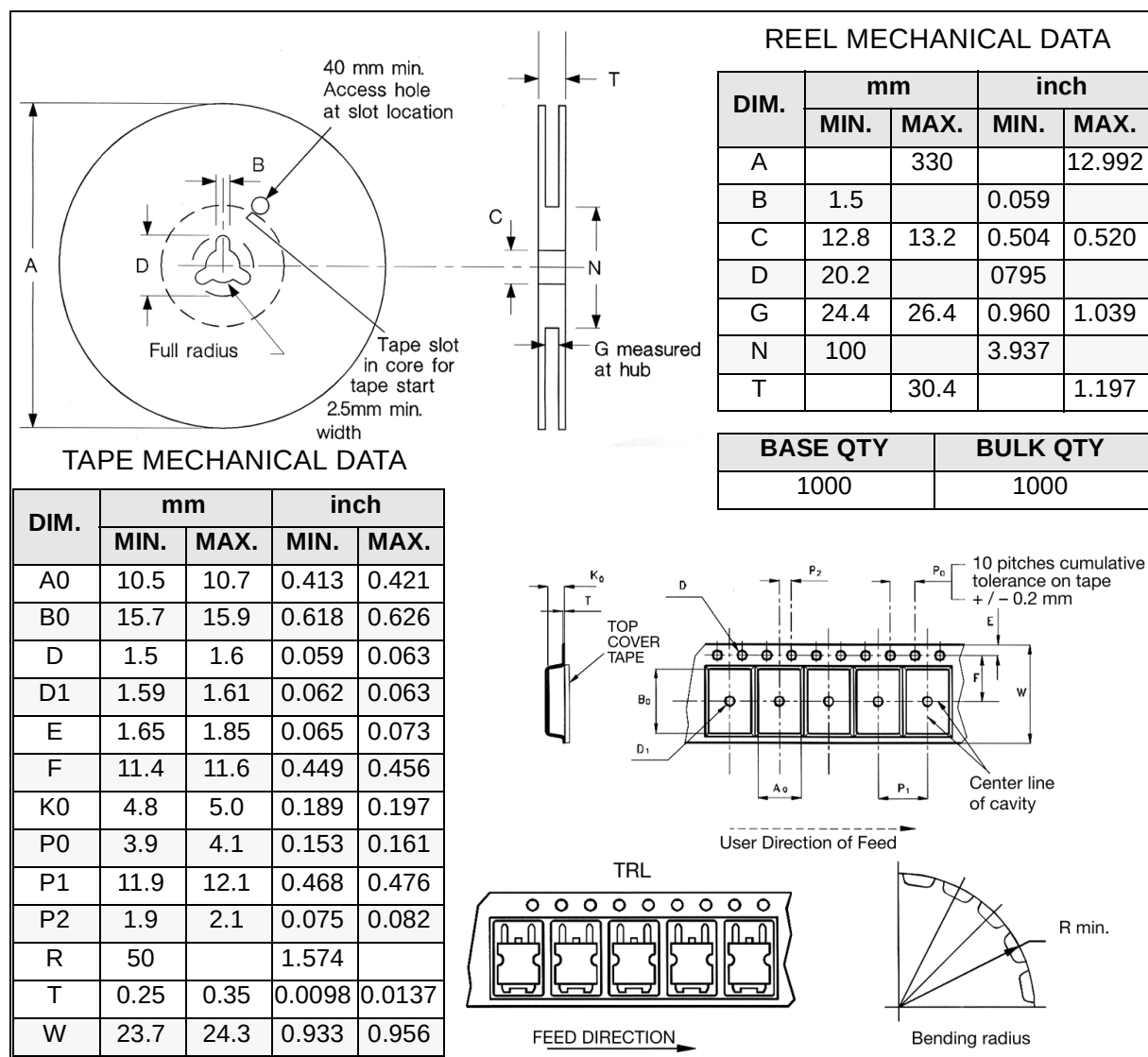
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.20		2.40	0.087		0.094
A1	0.90		1.10	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.90	0.025		0.035
B2	5.20		5.40	0.204		0.213
C	0.45		0.60	0.018		0.024
C2	0.48		0.60	0.019		0.024
D	6.00		6.20	0.236		0.244
E	6.40		6.60	0.252		0.260
G	4.40		4.60	0.173		0.181
H	9.35		10.10	0.368		0.398
L2		0.8			0.031	
L4	0.60		1.00	0.024		0.039
V2	0°		8°	0°		0°



D²PAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		8°			



D²PAK FOOTPRINT**TUBE SHIPMENT (no suffix)*****TAPE AND REEL SHIPMENT (suffix "T4")***

* on sales type

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